SEVENTH EDITION

Electronic Devices and Circuit Theory

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Contents

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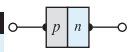


CHAPTER

1 Semiconductor Diodes

1.1 INTRODUCTION

It is now some 50 years since the first transistor was introduced on December 23, 1947. For those of us who experienced the change from glass envelope tubes to the solid-state era, it still seems like a few short years ago. The first edition of this text contained heavy coverage of tubes, with succeeding editions involving the important decision of how much coverage should be dedicated to tubes and how much to semiconductor devices. It no longer seems valid to mention tubes at all or to compare the advantages of one over the other—we are firmly in the solid-state era.

The miniaturization that has resulted leaves us to wonder about its limits. Complete systems now appear on wafers thousands of times smaller than the single element of earlier networks. New designs and systems surface weekly. The engineer becomes more and more limited in his or her knowledge of the broad range of advances—it is difficult enough simply to stay abreast of the changes in one area of research or development. We have also reached a point at which the primary purpose of the container is simply to provide some means of handling the device or system and to provide a mechanism for attachment to the remainder of the network. Miniaturization appears to be limited by three factors (each of which will be addressed in this text): the quality of the semiconductor material itself, the network design technique, and the limits of the manufacturing and processing equipment.

1.2 IDEAL DIODE

The first electronic device to be introduced is called the *diode*. It is the simplest of semiconductor devices but plays a very vital role in electronic systems, having characteristics that closely match those of a simple switch. It will appear in a range of applications, extending from the simple to the very complex. In addition to the details of its construction and characteristics, the very important data and graphs to be found on specification sheets will also be covered to ensure an understanding of the terminology employed and to demonstrate the wealth of information typically available from manufacturers.

The term *ideal* will be used frequently in this text as new devices are introduced. It refers to any device or system that has ideal characteristics—perfect in every way. It provides a basis for comparison, and it reveals where improvements can still be made. The *ideal diode* is a *two-terminal* device having the symbol and characteristics shown in Figs. 1.1a and b, respectively.

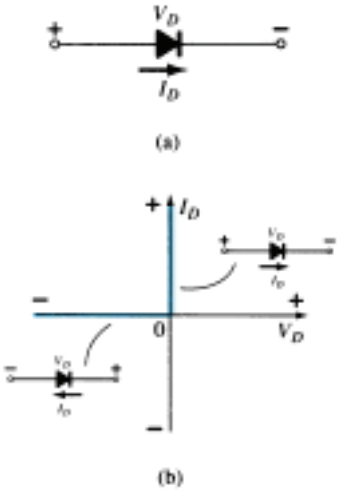
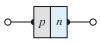


Figure 1.1 Ideal diode: (a) symbol; (b) characteristics.



Ideally, a diode will conduct current in the direction defined by the arrow in the symbol and act like an open circuit to any attempt to establish current in the opposite direction. In essence:

The characteristics of an ideal diode are those of a switch that can conduct current in only one direction.

In the description of the elements to follow, it is critical that the various *letter symbols, voltage polarities,* and *current directions* be defined. If the polarity of the applied voltage is consistent with that shown in Fig. 1.1a, the portion of the characteristics to be considered in Fig. 1.1b is to the right of the vertical axis. If a reverse voltage is applied, the characteristics to the left are pertinent. If the current through the diode has the direction indicated in Fig. 1.1a, the portion of the characteristics to be considered is above the horizontal axis, while a reversal in direction would require the use of the characteristics below the axis. For the majority of the device characteristics that appear in this book, the *ordinate* (or "y" axis) will be the *current* axis, while the *abscissa* (or "x" axis) will be the *voltage* axis.

One of the important parameters for the diode is the resistance at the point or region of operation. If we consider the conduction region defined by the direction of I_D and polarity of V_D in Fig. 1.1a (upper-right quadrant of Fig. 1.1b), we will find that the value of the forward resistance, R_F, as defined by Ohm's law is

$$R_F = \frac{V_F}{I_F} = \frac{0\ \text{V}}{2,\ 3,\ \text{mA},\ \ldots,\ \text{or any positive value}} = \mathbf{0\ \Omega} \quad \text{(short circuit)}$$

where V_F is the forward voltage across the diode and I_F is the forward current through the diode.

The ideal diode, therefore, is a short circuit for the region of conduction.

Consider the region of negatively applied potential (third quadrant) of Fig. 1.1b,

$$R_R = \frac{V_R}{I_R} = \frac{-5,\ -20,\ \text{or any reverse-bias potential}}{0\ \text{mA}} = \infty\ \mathbf{\Omega} \quad \text{(open-circuit)}$$

where V_R is reverse voltage across the diode and I_R is reverse current in the diode.

The ideal diode, therefore, is an open circuit in the region of nonconduction.

In review, the conditions depicted in Fig. 1.2 are applicable.

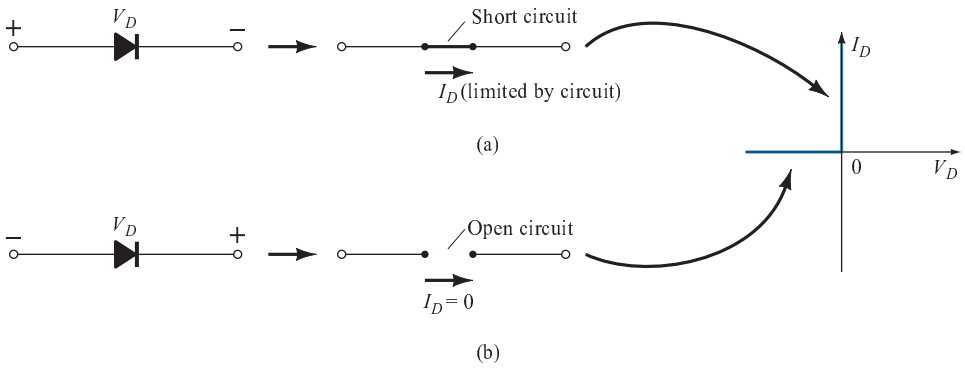


Figure 1.2 (a) Conduction and (b) nonconduction states of the ideal diode as determined by the applied bias.

In general, it is relatively simple to determine whether a diode is in the region of conduction or nonconduction simply by noting the direction of the current I_D established by an applied voltage. For conventional flow (opposite to that of electron flow), if the resultant diode current has the same direction as the arrowhead of the diode symbol, the diode is operating in the conducting region as depicted in Fig. 1.3a. If

the resulting current has the opposite direction, as shown in Fig. 1.3b, the open-circuit equivalent is appropriate.

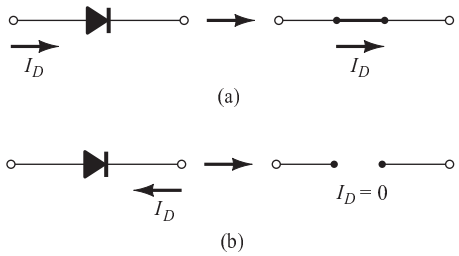


Figure 1.3 (a) Conduction and (b) nonconduction states of the ideal diode as determined by the direction of conventional current established by the network.

As indicated earlier, the primary purpose of this section is to introduce the characteristics of an ideal device for comparison with the characteristics of the commercial variety. As we progress through the next few sections, keep the following questions in mind:

How close will the forward or "on" resistance of a practical diode compare with the desired 0-Ω level?

Is the reverse-bias resistance sufficiently large to permit an open-circuit approximation?

1.3 SEMICONDUCTOR MATERIALS

The label *semiconductor* itself provides a hint as to its characteristics. The prefix *semi-* is normally applied to a range of levels midway between two limits.

The term conductor is applied to any material that will support a generous flow of charge when a voltage source of limited magnitude is applied across its terminals.

An insulator is a material that offers a very low level of conductivity under pressure from an applied voltage source.

A semiconductor, therefore, is a material that has a conductivity level somewhere between the extremes of an insulator and a conductor.

Inversely related to the conductivity of a material is its resistance to the flow of charge, or current. That is, the higher the conductivity level, the lower the resistance level. In tables, the term *resistivity* (ρ, Greek letter rho) is often used when comparing the resistance levels of materials. In metric units, the resistivity of a material is measured in Ω-cm or Ω-m. The units of Ω-cm are derived from the substitution of the units for each quantity of Fig. 1.4 into the following equation (derived from the basic resistance equation $R = \rho l/A$):

$$\rho = \frac{RA}{l} = \frac{(\Omega)(\text{cm}^2)}{\text{cm}} \Rightarrow \Omega\text{-cm} \tag{1.1}$$

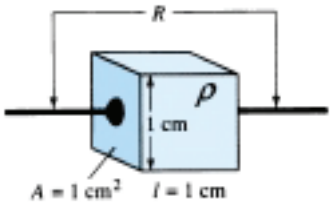


Figure 1.4 Defining the metric units of resistivity.

In fact, if the area of Fig. 1.4 is 1 cm^2 and the length 1 cm, the magnitude of the resistance of the cube of Fig. 1.4 is equal to the magnitude of the resistivity of the material as demonstrated below:

$$|R| = \rho \frac{l}{A} = \rho \frac{(1\text{ cm})}{(1\text{ cm}^2)} = |\rho| \text{ohms}$$

This fact will be helpful to remember as we compare resistivity levels in the discussions to follow.

In Table 1.1, typical resistivity values are provided for three broad categories of materials. Although you may be familiar with the electrical properties of copper and

TABLE 1.1 Typical Resistivity Values

Conductor	*Semiconductor*	*Insulator*
$\rho \cong 10^{-6}$ Ω-cm (copper)	$\rho \cong 50$ Ω-cm (germanium) $\rho \cong 50 \times 10^{3}$ Ω-cm (silicon)	$\rho \cong 10^{12}$ Ω-cm (mica)

mica from your past studies, the characteristics of the semiconductor materials of germanium (Ge) and silicon (Si) may be relatively new. As you will find in the chapters to follow, they are certainly not the only two semiconductor materials. They are, however, the two materials that have received the broadest range of interest in the development of semiconductor devices. In recent years the shift has been steadily toward silicon and away from germanium, but germanium is still in modest production.

Note in Table 1.1 the extreme range between the conductor and insulating materials for the 1-cm length (1-cm^2 area) of the material. Eighteen places separate the placement of the decimal point for one number from the other. Ge and Si have received the attention they have for a number of reasons. One very important consideration is the fact that they can be manufactured to a very high purity level. In fact, recent advances have reduced impurity levels in the pure material to 1 part in 10 billion (1 : 10,000,000,000). One might ask if these low impurity levels are really necessary. They certainly are if you consider that the addition of one part impurity (of the proper type) per million in a wafer of silicon material can change that material from a relatively poor conductor to a good conductor of electricity. We are obviously dealing with a whole new spectrum of comparison levels when we deal with the semiconductor medium. The ability to change the characteristics of the material significantly through this process, known as "doping," is yet another reason why Ge and Si have received such wide attention. Further reasons include the fact that their characteristics can be altered significantly through the application of heat or light—an important consideration in the development of heat- and light-sensitive devices.

Some of the unique qualities of Ge and Si noted above are due to their atomic structure. The atoms of both materials form a very definite pattern that is periodic in nature (i.e., continually repeats itself). One complete pattern is called a *crystal* and the periodic arrangement of the atoms a *lattice.* For Ge and Si the crystal has the three-dimensional diamond structure of Fig. 1.5. Any material composed solely of repeating crystal structures of the same kind is called a *single-crystal* structure. For semiconductor materials of practical application in the electronics field, this single-crystal feature exists, and, in addition, the periodicity of the structure does not change significantly with the addition of impurities in the doping process.

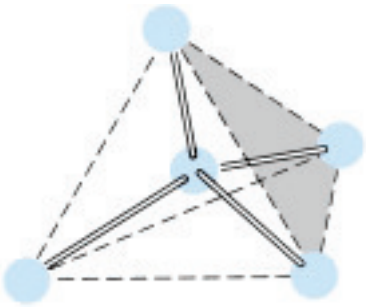


Figure 1.5 Ge and Si single-crystal structure.

Let us now examine the structure of the atom itself and note how it might affect the electrical characteristics of the material. As you are aware, the atom is composed of three basic particles: the *electron,* the *proton,* and the *neutron.* In the atomic lattice, the neutrons and protons form the *nucleus,* while the electrons revolve around the nucleus in a fixed *orbit.* The Bohr models of the two most commonly used semiconductors, *germanium* and *silicon,* are shown in Fig. 1.6.

As indicated by Fig. 1.6a, the germanium atom has 32 orbiting electrons, while silicon has 14 orbiting electrons. In each case, there are 4 electrons in the outermost (*valence*) shell. The potential (*ionization potential*) required to remove any one of these 4 valence electrons is lower than that required for any other electron in the structure. In a pure germanium or silicon crystal these 4 valence electrons are bonded to 4 adjoining atoms, as shown in Fig. 1.7 for silicon. Both Ge and Si are referred to as *tetravalent atoms* because they each have four valence electrons.

A bonding of atoms, strengthened by the sharing of electrons, is called covalent bonding.

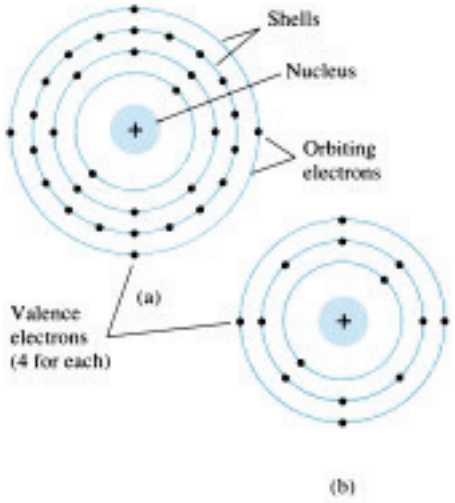


Figure 1.6 Atomic structure: (a) germanium; (b) silicon.

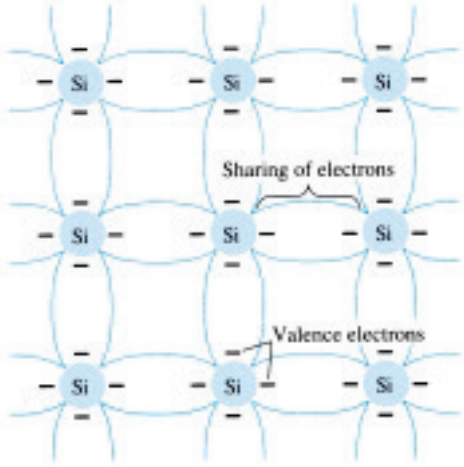


Figure 1.7 Covalent bonding of the silicon atom.

Although the covalent bond will result in a stronger bond between the valence electrons and their parent atom, it is still possible for the valence electrons to absorb sufficient kinetic energy from natural causes to break the covalent bond and assume the "free" state. The term *free* reveals that their motion is quite sensitive to applied electric fields such as established by voltage sources or any difference in potential. These natural causes include effects such as light energy in the form of photons and thermal energy from the surrounding medium. At room temperature there are approximately 1.5×10^{10} free carriers in a cubic centimeter of intrinsic silicon material.

Intrinsic materials are those semiconductors that have been carefully refined to reduce the impurities to a very low level—essentially as pure as can be made available through modern technology.

The free electrons in the material due only to natural causes are referred to as *intrinsic carriers*. At the same temperature, intrinsic germanium material will have approximately 2.5×10^{13} free carriers per cubic centimeter. The ratio of the number of carriers in germanium to that of silicon is greater than 10^3 and would indicate that germanium is a better conductor at room temperature. This may be true, but both are still considered poor conductors in the intrinsic state. Note in Table 1.1 that the resistivity also differs by a ratio of about 1000:1, with silicon having the larger value. This should be the case, of course, since resistivity and conductivity are inversely related.

An increase in temperature of a semiconductor can result in a substantial increase in the number of free electrons in the material.

As the temperature rises from absolute zero (0 K), an increasing number of valence electrons absorb sufficient thermal energy to break the covalent bond and contribute to the number of free carriers as described above. This increased number of carriers will increase the conductivity index and result in a lower resistance level.

Semiconductor materials such as Ge and Si that show a reduction in resistance with increase in temperature are said to have a negative temperature coefficient.

You will probably recall that the resistance of most conductors will increase with temperature. This is due to the fact that the numbers of carriers in a conductor will

not increase significantly with temperature, but their vibration pattern about a relatively fixed location will make it increasingly difficult for electrons to pass through. An increase in temperature therefore results in an increased resistance level and a *positive temperature coefficient*.

1.4 ENERGY LEVELS

In the isolated atomic structure there are discrete (individual) energy levels associated with each orbiting electron, as shown in Fig. 1.8a. Each material will, in fact, have its own set of permissible energy levels for the electrons in its atomic structure.

The more distant the electron from the nucleus, the higher the energy state, and any electron that has left its parent atom has a higher energy state than any electron in the atomic structure.

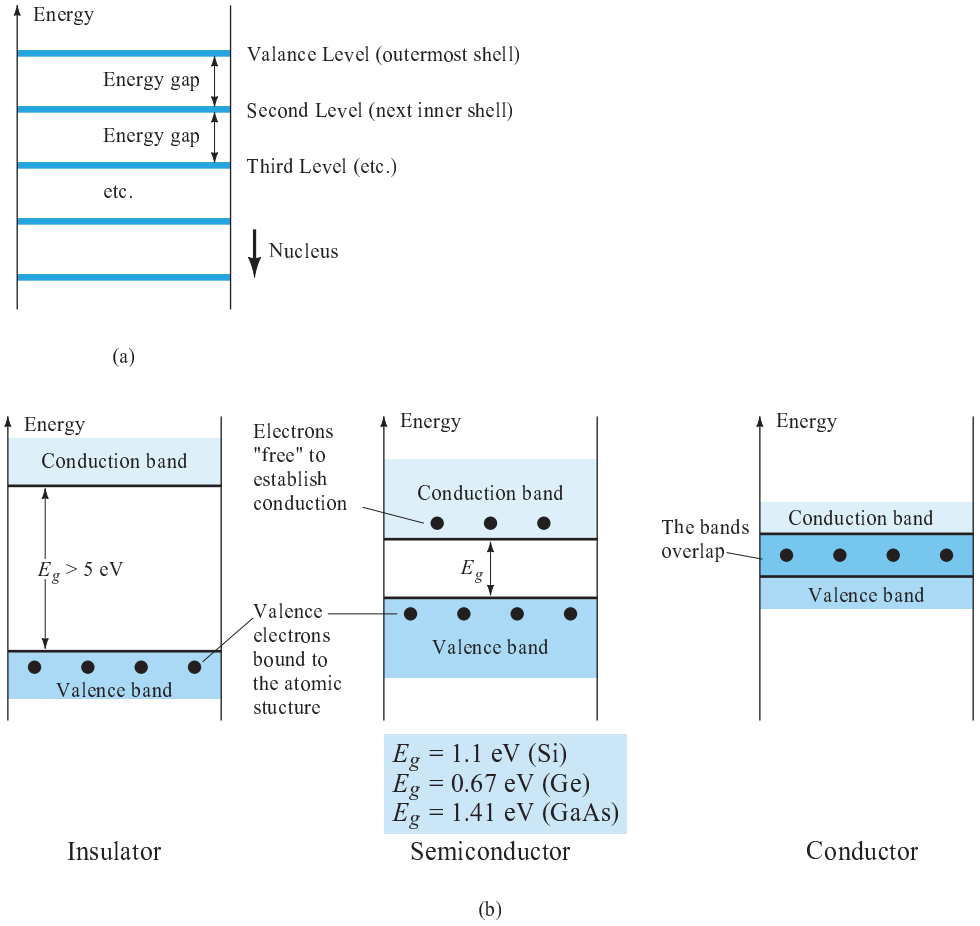


Figure 1.8 Energy levels: (a) discrete levels in isolated atomic structures; (b) conduction and valence bands of an insulator, semiconductor, and conductor.

Between the discrete energy levels are gaps in which no electrons in the isolated atomic structure can appear. As the atoms of a material are brought closer together to form the crystal lattice structure, there is an interaction between atoms that will result in the electrons in a particular orbit of one atom having slightly different energy levels from electrons in the same orbit of an adjoining atom. The net result is an expansion of the discrete levels of possible energy states for the valence electrons to that of bands as shown in Fig. 1.8b. Note that there are boundary levels and maximum energy states in which any electron in the atomic lattice can find itself, and there remains a *forbidden region* between the valence band and the ionization level. Recall

that ionization is the mechanism whereby an electron can absorb sufficient energy to break away from the atomic structure and enter the conduction band. You will note that the energy associated with each electron is measured in *electron volts* (eV). The unit of measure is appropriate, since

$$\boxed{W = QV} \quad \text{eV} \tag{1.2}$$

as derived from the defining equation for voltage $V = W/Q$. The charge Q is the charge associated with a single electron.

Substituting the charge of an electron and a potential difference of 1 volt into Eq. (1.2) will result in an energy level referred to as one *electron volt.* Since energy is also measured in joules and the charge of one electron $= 1.6 \times 10^{-19}$ coulomb,

$$W = QV = (1.6 \times 10^{-19}\ \text{C})(1\ \text{V})$$

and

$$\boxed{1\ \text{eV} = 1.6 \times 10^{-19}\ \text{J}} \tag{1.3}$$

At 0 K or absolute zero (−273.15°C), all the valence electrons of semiconductor materials find themselves locked in their outermost shell of the atom with energy levels associated with the valence band of Fig. 1.8b. However, at room temperature (300 K, 25°C) a large number of valence electrons have acquired sufficient energy to leave the valence band, cross the energy gap defined by E_g in Fig. 1.8b and enter the conduction band. For silicon E_g is 1.1 eV, for germanium 0.67 eV, and for gallium arsenide 1.41 eV. The obviously lower E_g for germanium accounts for the increased number of carriers in that material as compared to silicon at room temperature. Note for the insulator that the energy gap is typically 5 eV or more, which severely limits the number of electrons that can enter the conduction band at room temperature. The conductor has electrons in the conduction band even at 0 K. Quite obviously, therefore, at room temperature there are more than enough free carriers to sustain a heavy flow of charge, or current.

We will find in Section 1.5 that if certain impurities are added to the intrinsic semiconductor materials, energy states in the forbidden bands will occur which will cause a net reduction in E_g for both semiconductor materials—consequently, increased carrier density in the conduction band at room temperature!

1.5 EXTRINSIC MATERIALS—*n*- AND *p*-TYPE

The characteristics of semiconductor materials can be altered significantly by the addition of certain impurity atoms into the relatively pure semiconductor material. These impurities, although only added to perhaps 1 part in 10 million, can alter the band structure sufficiently to totally change the electrical properties of the material.

A semiconductor material that has been subjected to the doping process is called an extrinsic material.

There are two extrinsic materials of immeasurable importance to semiconductor device fabrication: *n*-type and *p*-type. Each will be described in some detail in the following paragraphs.

n-Type Material

Both the *n*- and *p*-type materials are formed by adding a predetermined number of impurity atoms into a germanium or silicon base. The *n*-type is created by introducing those impurity elements that have *five* valence electrons (*pentavalent*), such as *antimony, arsenic,* and *phosphorus*. The effect of such impurity elements is indicated in

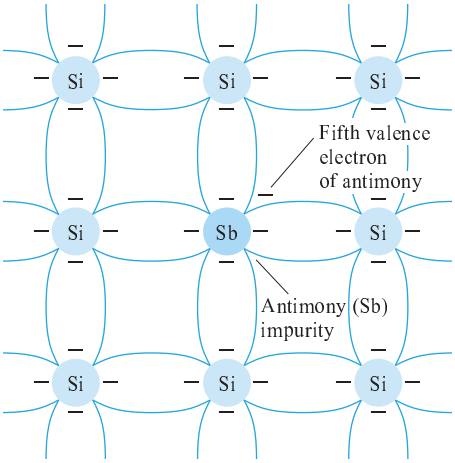


Figure 1.9 Antimony impurity in *n*-type material.

Fig. 1.9 (using antimony as the impurity in a silicon base). Note that the four covalent bonds are still present. There is, however, an additional fifth electron due to the impurity atom, which is *unassociated* with any particular covalent bond. This remaining electron, loosely bound to its parent (antimony) atom, is relatively free to move within the newly formed *n*-type material. Since the inserted impurity atom has donated a relatively "free" electron to the structure:

Diffused impurities with five valence electrons are called donor atoms.

It is important to realize that even though a large number of "free" carriers have been established in the *n*-type material, it is still electrically *neutral* since ideally the number of positively charged protons in the nuclei is still equal to the number of "free" and orbiting negatively charged electrons in the structure.

The effect of this doping process on the relative conductivity can best be described through the use of the energy-band diagram of Fig. 1.10. Note that a discrete energy level (called the *donor level*) appears in the forbidden band with an E_g significantly less than that of the intrinsic material. Those "free" electrons due to the added impurity sit at this energy level and have less difficulty absorbing a sufficient measure of thermal energy to move into the conduction band at room temperature. The result is that at room temperature, there are a large number of carriers (electrons) in the conduction level and the conductivity of the material increases significantly. At room temperature in an intrinsic Si material there is about one free electron for every 10^{12} atoms (1 to 10^9 for Ge). If our dosage level were 1 in 10 million (10^7), the ratio ($10^{12}/10^7 = 10^5$) would indicate that the carrier concentration has increased by a ratio of 100,000:1.

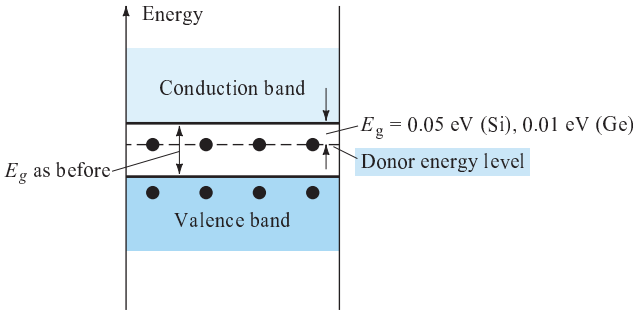


Figure 1.10 Effect of donor impurities on the energy band structure.

p-Type Material

The *p*-type material is formed by doping a pure germanium or silicon crystal with impurity atoms having *three* valence electrons. The elements most frequently used for this purpose are *boron, gallium,* and *indium.* The effect of one of these elements, boron, on a base of silicon is indicated in Fig. 1.11.

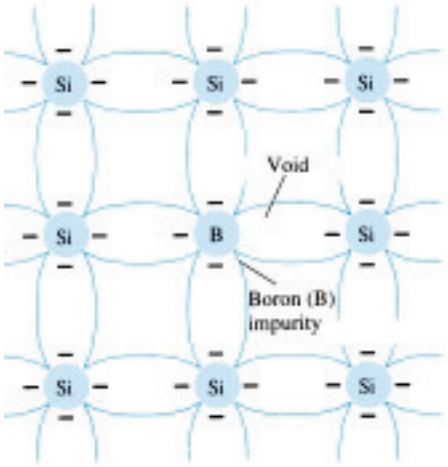


Figure 1.11 Boron impurity in *p*-type material.

Note that there is now an insufficient number of electrons to complete the covalent bonds of the newly formed lattice. The resulting vacancy is called a *hole* and is represented by a small circle or positive sign due to the absence of a negative charge. Since the resulting vacancy will readily *accept* a "free" electron:

The diffused impurities with three valence electrons are called acceptor atoms.

The resulting *p*-type material is electrically neutral, for the same reasons described for the *n*-type material.

Electron versus Hole Flow

The effect of the hole on conduction is shown in Fig. 1.12. If a valence electron acquires sufficient kinetic energy to break its covalent bond and fills the void created by a hole, then a vacancy, or hole, will be created in the covalent bond that released the electron. There is, therefore, a transfer of holes to the left and electrons to the right, as shown in Fig. 1.12. The direction to be used in this text is that of *conventional flow,* which is indicated by the direction of hole flow.

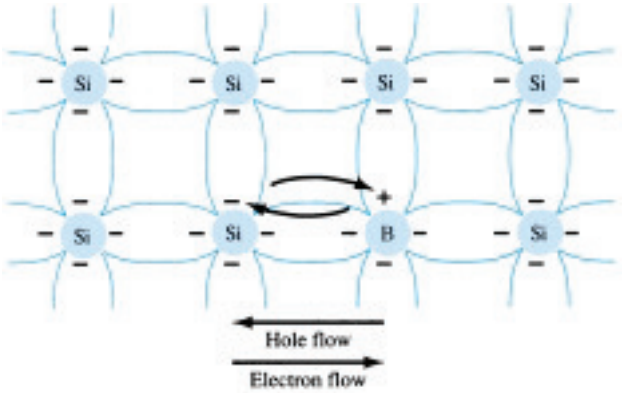


Figure 1.12 Electron versus hole flow.

Majority and Minority Carriers

In the intrinsic state, the number of free electrons in Ge or Si is due only to those few electrons in the valence band that have acquired sufficient energy from thermal or light sources to break the covalent bond or to the few impurities that could not be removed. The vacancies left behind in the covalent bonding structure represent our very limited supply of holes. In an *n*-type material, the number of holes has not changed significantly from this intrinsic level. The net result, therefore, is that the number of electrons far outweighs the number of holes. For this reason:

In an n-type material (Fig. 1.13a) the electron is called the majority carrier and the hole the minority carrier.

For the *p*-type material the number of holes far outweighs the number of electrons, as shown in Fig. 1.13b. Therefore:

In a p-type material the hole is the majority carrier and the electron is the minority carrier.

When the fifth electron of a donor atom leaves the parent atom, the atom remaining acquires a net positive charge: hence the positive sign in the donor-ion representation. For similar reasons, the negative sign appears in the acceptor ion.

The *n*- and *p*-type materials represent the basic building blocks of semiconductor devices. We will find in the next section that the "joining" of a single *n*-type material with a *p*-type material will result in a semiconductor element of considerable importance in electronic systems.

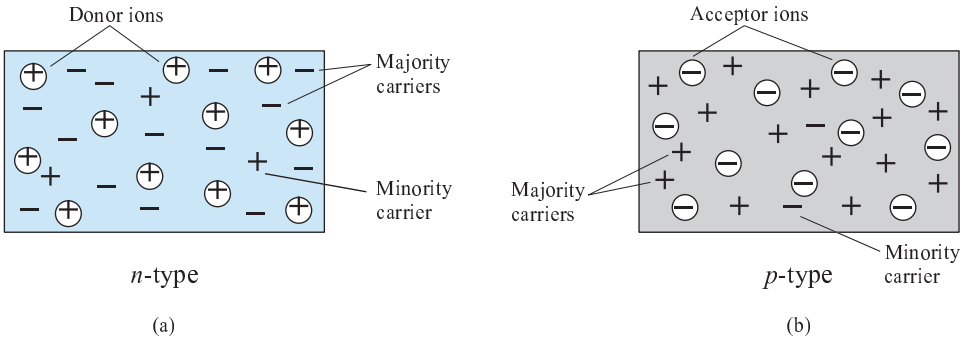


Figure 1.13 (a) *n*-type material; (b) *p*-type material.

1.6 SEMICONDUCTOR DIODE

In Section 1.5 both the *n*- and *p*-type materials were introduced. The semiconductor diode is formed by simply bringing these materials together (constructed from the same base—Ge or Si), as shown in Fig. 1.14, using techniques to be described in Chapter 20. At the instant the two materials are "joined" the electrons and holes in the region of the junction will combine, resulting in a lack of carriers in the region near the junction.

This region of uncovered positive and negative ions is called the depletion region due to the depletion of carriers in this region.

Since the diode is a two-terminal device, the application of a voltage across its terminals leaves three possibilities: *no bias* ($V_D = 0$ V), *forward bias* ($V_D > 0$ V), and *reverse bias* ($V_D < 0$ V). Each is a condition that will result in a response that the user must clearly understand if the device is to be applied effectively.

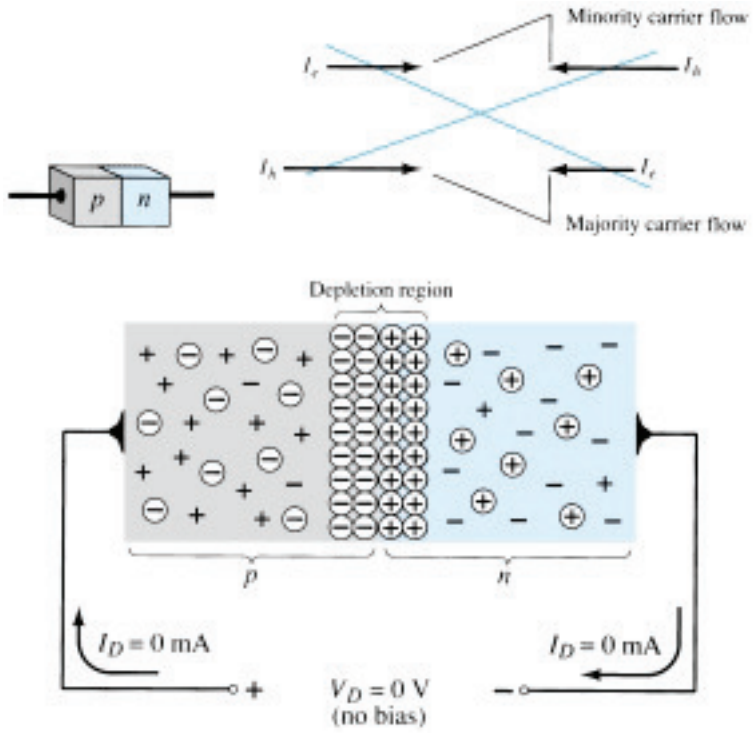


Figure 1.14 *p-n* junction with no external bias.

No Applied Bias ($V_D = 0$ V)

Under no-bias (no applied voltage) conditions, any minority carriers (holes) in the *n*-type material that find themselves within the depletion region will pass directly into the *p*-type material. The closer the minority carrier is to the junction, the greater the attraction for the layer of negative ions and the less the opposition of the positive ions in the depletion region of the *n*-type material. For the purposes of future discussions we shall assume that all the minority carriers of the *n*-type material that find themselves in the depletion region due to their random motion will pass directly into the *p*-type material. Similar discussion can be applied to the minority carriers (electrons) of the *p*-type material. This carrier flow has been indicated in Fig. 1.14 for the minority carriers of each material.

The majority carriers (electrons) of the *n*-type material must overcome the attractive forces of the layer of positive ions in the *n*-type material and the shield of negative ions in the *p*-type material to migrate into the area beyond the depletion region of the *p*-type material. However, the number of majority carriers is so large in the *n*-type material that there will invariably be a small number of majority carriers with sufficient kinetic energy to pass through the depletion region into the *p*-type material. Again, the same type of discussion can be applied to the majority carriers (holes) of the *p*-type material. The resulting flow due to the majority carriers is also shown in Fig. 1.14.

A close examination of Fig. 1.14 will reveal that the relative magnitudes of the flow vectors are such that the net flow in either direction is zero. This cancellation of vectors has been indicated by crossed lines. The length of the vector representing hole flow has been drawn longer than that for electron flow to demonstrate that the magnitude of each need not be the same for cancellation and that the doping levels for each material may result in an unequal carrier flow of holes and electrons. In summary, therefore:

In the absence of an applied bias voltage, the net flow of charge in any one direction for a semiconductor diode is zero.

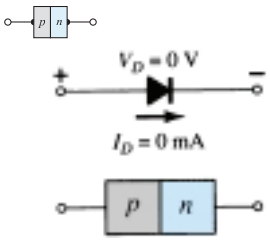


Figure 1.15 No-bias conditions for a semiconductor diode.

The symbol for a diode is repeated in Fig. 1.15 with the associated *n*- and *p*-type regions. Note that the arrow is associated with the *p*-type component and the bar with the *n*-type region. As indicated, for $V_D = 0$ V, the current in any direction is 0 mA.

Reverse-Bias Condition ($V_D < 0$ V)

If an external potential of *V* volts is applied across the *p*-*n* junction such that the positive terminal is connected to the *n*-type material and the negative terminal is connected to the *p*-type material as shown in Fig. 1.16, the number of uncovered positive ions in the depletion region of the *n*-type material will increase due to the large number of "free" electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the *p*-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero as shown in Fig. 1.16.

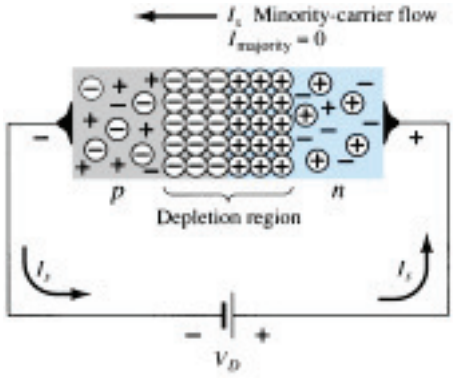


Figure 1.16 Reverse-biased *p*-*n* junction.

The number of minority carriers, however, that find themselves entering the depletion region will not change, resulting in minority-carrier flow vectors of the same magnitude indicated in Fig. 1.14 with no applied voltage.

The current that exists under reverse-bias conditions is called the reverse saturation current and is represented by I_s.

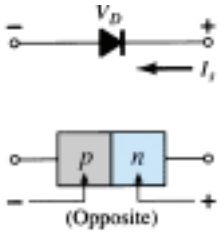


Figure 1.17 Reverse-bias conditions for a semiconductor diode.

The reverse saturation current is seldom more than a few microamperes except for high-power devices. In fact, in recent years its level is typically in the nanoampere range for silicon devices and in the low-microampere range for germanium. The term *saturation* comes from the fact that it reaches its maximum level quickly and does not change significantly with increase in the reverse-bias potential, as shown on the diode characteristics of Fig. 1.19 for $V_D < 0$ V. The reverse-biased conditions are depicted in Fig. 1.17 for the diode symbol and *p*-*n* junction. Note, in particular, that the direction of I_s is against the arrow of the symbol. Note also that the *n*egative potential is connected to the *p*-type material and the *p*ositive potential to the *n*-type material—the difference in underlined letters for each region revealing a reverse-bias condition.

Forward-Bias Condition ($V_D > 0$ V)

A *forward-bias* or "on" condition is established by applying the positive potential to the *p*-type material and the negative potential to the *n*-type material as shown in Fig. 1.18. For future reference, therefore:

A semiconductor diode is forward-biased when the association p*-type and positive and* n*-type and negative has been established.*

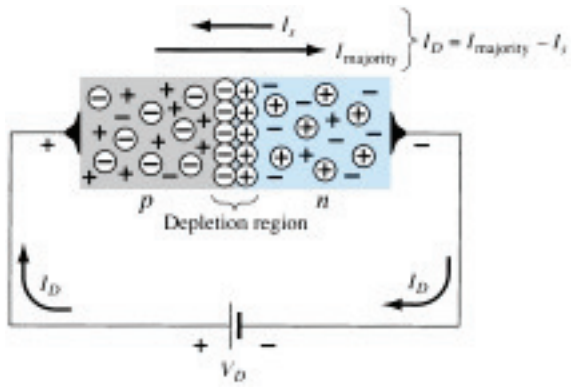


Figure 1.18 Forward-biased *p-n* junction.

The application of a forward-bias potential V_D will "pressure" electrons in the *n*-type material and holes in the *p*-type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in Fig. 1.18. The resulting minority-carrier flow of electrons from the *p*-type material to the *n*-type material (and of holes from the *n*-type material to the *p*-type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction. An electron of the *n*-type material now "sees" a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the *p*-type material. As the applied bias increases in magnitude the depletion region will continue to decrease in width until a flood of electrons can pass through the junction, re-

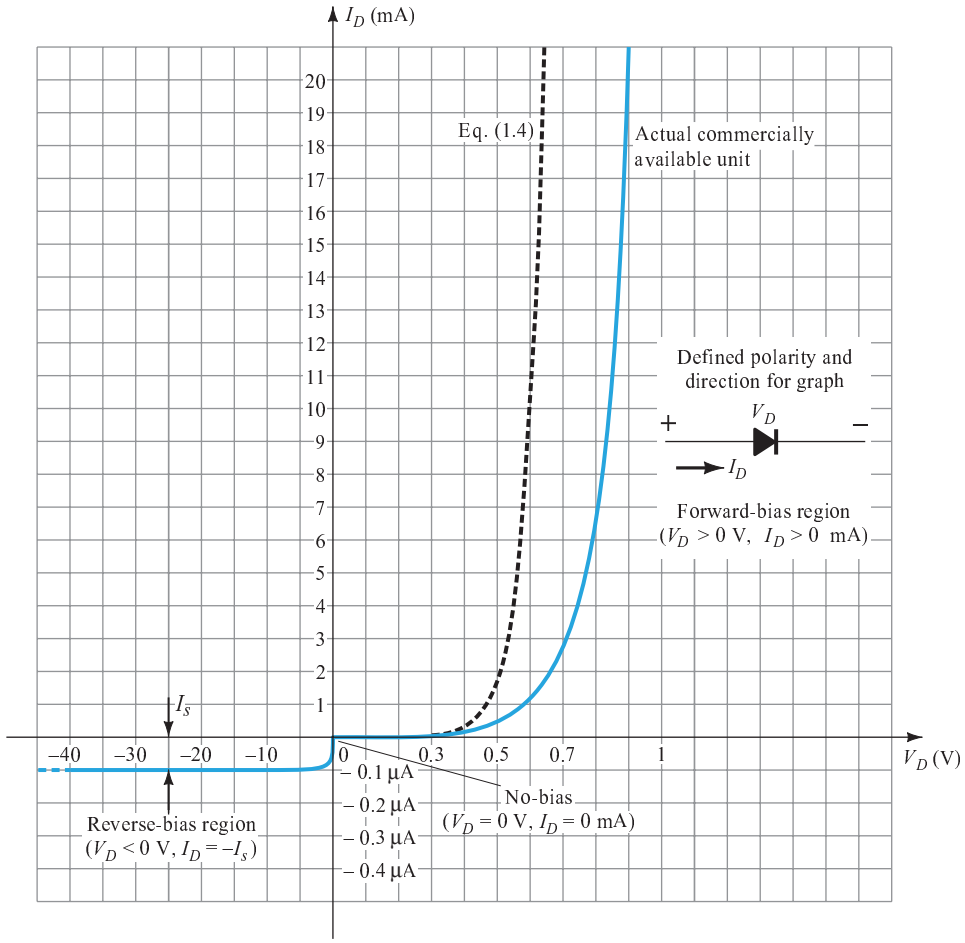


Figure 1.19 Silicon semiconductor diode characteristics.

sulting in an exponential rise in current as shown in the forward-bias region of the characteristics of Fig. 1.19. Note that the vertical scale of Fig. 1.19 is measured in milliamperes (although some semiconductor diodes will have a vertical scale measured in amperes) and the horizontal scale in the forward-bias region has a maximum of 1 V. Typically, therefore, the voltage across a forward-biased diode will be less than 1 V. Note also, how quickly the current rises beyond the knee of the curve.

It can be demonstrated through the use of solid-state physics that the general characteristics of a semiconductor diode can be defined by the following equation for the forward- and reverse-bias regions:

$$I_D = I_s(e^{kV_D/T_K} - 1) \tag{1.4}$$

where I_s = reverse saturation current

$k = 11{,}600/\eta$ with $\eta = 1$ for Ge and $\eta = 2$ for Si for relatively low levels of diode current (at or below the knee of the curve) and $\eta = 1$ for Ge and Si for higher levels of diode current (in the rapidly increasing section of the curve)

$T_K = T_C + 273°$

A plot of Eq. (1.4) is provided in Fig. 1.19. If we expand Eq. (1.4) into the following form, the contributing component for each region of Fig. 1.19 can easily be described:

$$I_D = I_s e^{kV_D/T_K} - I_s$$

For positive values of V_D the first term of the equation above will grow very quickly and overpower the effect of the second term. The result is that for positive values of V_D, I_D will be positive and grow as the function $y = e^x$ appearing in Fig. 1.20. At $V_D = 0$ V, Eq. (1.4) becomes $I_D = I_s(e^0 - 1) = I_s(1 - 1) = 0$ mA as appearing in Fig. 1.19. For negative values of V_D the first term will quickly drop off below I_s, resulting in $I_D = -I_s$, which is simply the horizontal line of Fig. 1.19. The break in the characteristics at $V_D = 0$ V is simply due to the dramatic change in scale from mA to μA.

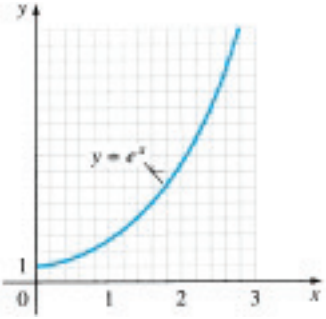


Figure 1.20 Plot of e^x.

Note in Fig. 1.19 that the commercially available unit has characteristics that are shifted to the right by a few tenths of a volt. This is due to the internal "body" resistance and external "contact" resistance of a diode. Each contributes to an additional voltage at the same current level as determined by Ohm's law ($V = IR$). In time, as production methods improve, this difference will decrease and the actual characteristics approach those of Eq. (1.4).

It is important to note the change in scale for the vertical and horizontal axes. For positive values of I_D the scale is in milliamperes and the current scale below the axis is in microamperes (or possibly nanoamperes). For V_D the scale for positive values is in tenths of volts and for negative values the scale is in tens of volts.

Initially, Eq. (1.4) does appear somewhat complex and may develop an unwarranted fear that it will be applied for all the diode applications to follow. Fortunately, however, a number of approximations will be made in a later section that will negate the need to apply Eq. (1.4) and provide a solution with a minimum of mathematical difficulty.

Before leaving the subject of the forward-bias state the conditions for conduction (the "on" state) are repeated in Fig. 1.21 with the required biasing polarities and the resulting direction of majority-carrier flow. Note in particular how the direction of conduction matches the arrow in the symbol (as revealed for the ideal diode).

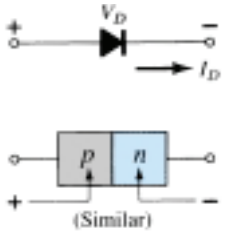


Figure 1.21 Forward-bias conditions for a semiconductor diode.

Zener Region

Even though the scale of Fig. 1.19 is in tens of volts in the negative region, there is a point where the application of too negative a voltage will result in a sharp change

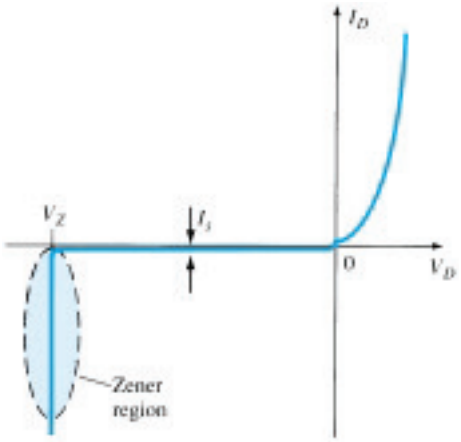


Figure 1.22 Zener region.

in the characteristics, as shown in Fig. 1.22. The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse-bias potential that results in this dramatic change in characteristics is called the *Zener potential* and is given the symbol V_Z.

As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current I_s will also increase. Eventually, their velocity and associated kinetic energy ($W_K = \frac{1}{2}mv^2$) will be sufficient to release additional carriers through collisions with otherwise stable atomic structures. That is, an *ionization* process will result whereby valence electrons absorb sufficient energy to leave the parent atom. These additional carriers can then aid the ionization process to the point where a high *avalanche* current is established and the *avalanche breakdown* region determined.

The avalanche region (V_Z) can be brought closer to the vertical axis by increasing the doping levels in the *p*- and *n*-type materials. However, as V_Z decreases to very low levels, such as -5 V, another mechanism, called *Zener breakdown,* will contribute to the sharp change in the characteristic. It occurs because there is a strong electric field in the region of the junction that can disrupt the bonding forces within the atom and "generate" carriers. Although the Zener breakdown mechanism is a significant contributor only at lower levels of V_Z, this sharp change in the characteristic at any level is called the *Zener region* and diodes employing this unique portion of the characteristic of a *p-n* junction are called *Zener diodes*. They are described in detail in Section 1.14.

The Zener region of the semiconductor diode described must be avoided if the response of a system is not to be completely altered by the sharp change in characteristics in this reverse-voltage region.

The maximum reverse-bias potential that can be applied before entering the Zener region is called the peak inverse voltage (referred to simply as the PIV rating) or the peak reverse voltage (denoted by PRV rating).

If an application requires a PIV rating greater than that of a single unit, a number of diodes of the same characteristics can be connected in series. Diodes are also connected in parallel to increase the current-carrying capacity.

Silicon versus Germanium

Silicon diodes have, in general, higher PIV and current rating and wider temperature ranges than germanium diodes. PIV ratings for silicon can be in the neighborhood of 1000 V, whereas the maximum value for germanium is closer to 400 V. Silicon can be used for applications in which the temperature may rise to about 200°C (400°F), whereas germanium has a much lower maximum rating (100°C). The disadvantage of silicon, however, as compared to germanium, as indicated in Fig. 1.23, is the higher

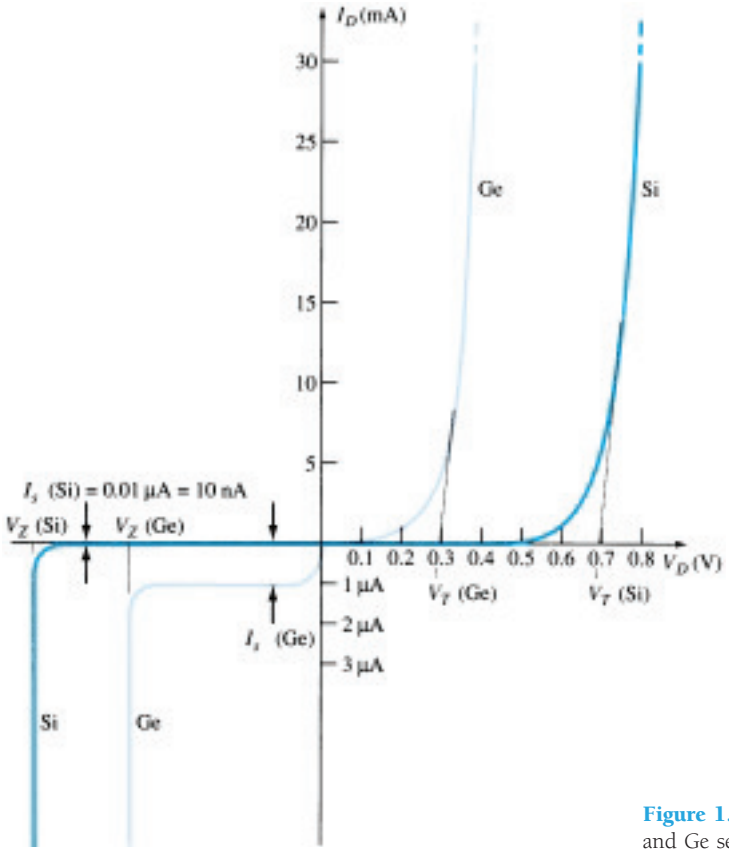


Figure 1.23 Comparison of Si and Ge semiconductor diodes.

forward-bias voltage required to reach the region of upward swing. It is typically of the order of magnitude of 0.7 V for *commercially* available silicon diodes and 0.3 V for germanium diodes when rounded off to the nearest tenths. The increased offset for silicon is due primarily to the factor η in Eq. (1.4). This factor plays a part in determining the shape of the curve only at very low current levels. Once the curve starts its vertical rise, the factor η drops to 1 (the continuous value for germanium). This is evidenced by the similarities in the curves once the offset potential is reached. The potential at which this rise occurs is commonly referred to as the *offset, threshold,* or *firing potential*. Frequently, the first letter of a term that describes a particular quantity is used in the notation for that quantity. However, to ensure a minimum of confusion with other terms, such as output voltage (V_o) and forward voltage (V_F), the notation V_T has been adopted for this book, from the word "threshold."

In review:

$$V_T = 0.7 \text{ (Si)}$$
$$V_T = 0.3 \text{ (Ge)}$$

Obviously, the closer the upward swing is to the vertical axis, the more "ideal" the device. However, the other characteristics of silicon as compared to germanium still make it the choice in the majority of commercially available units.

Temperature Effects

Temperature can have a marked effect on the characteristics of a silicon semiconductor diode as witnessed by a typical silicon diode in Fig. 1.24. It has been found experimentally that:

The reverse saturation current I_s will just about double in magnitude for every 10°C increase in temperature.

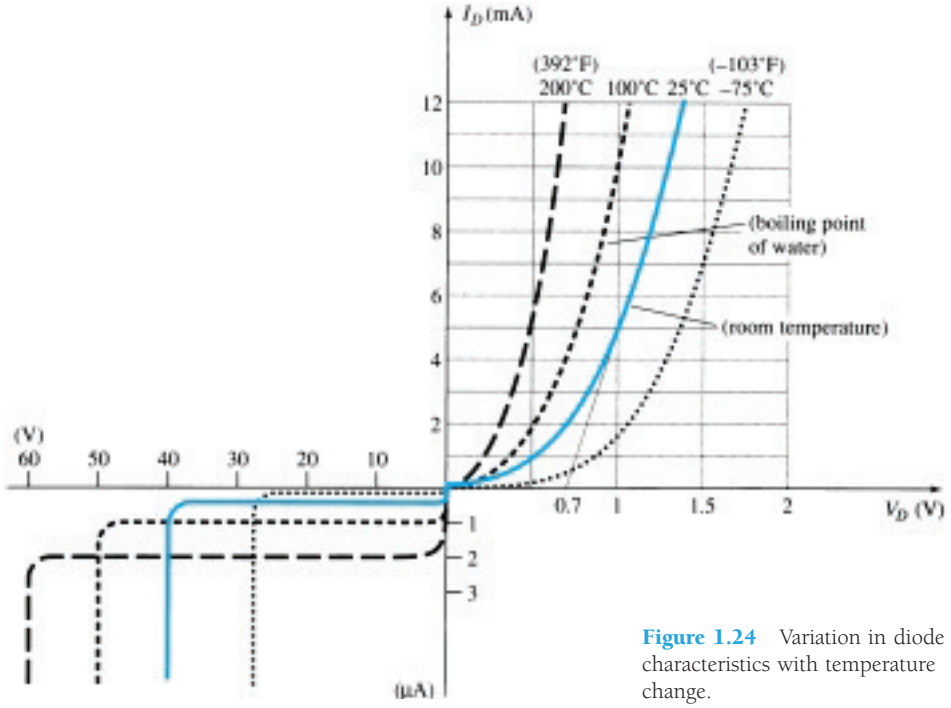


Figure 1.24 Variation in diode characteristics with temperature change.

It is not uncommon for a germanium diode with an I_s in the order of 1 or 2 μA at 25°C to have a leakage current of 100 μA = 0.1 mA at a temperature of 100°C. Current levels of this magnitude in the reverse-bias region would certainly question our desired open-circuit condition in the reverse-bias region. Typical values of I_s for silicon are much lower than that of germanium for similar power and current levels as shown in Fig. 1.23. The result is that even at high temperatures the levels of I_s for silicon diodes do not reach the same high levels obtained for germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design. Fundamentally, the open-circuit equivalent in the reverse-bias region is better realized at any temperature with silicon than with germanium.

The increasing levels of I_s with temperature account for the lower levels of threshold voltage, as shown in Fig. 1.24. Simply increase the level of I_s in Eq. (1.4) and note the earlier rise in diode current. Of course, the level of T_K also will be increasing in the same equation, but the increasing level of I_s will overpower the smaller percent change in T_K. As the temperature increases the forward characteristics are actually becoming more "ideal," but we will find when we review the specifications sheets that temperatures beyond the normal operating range can have a very detrimental effect on the diode's maximum power and current levels. In the reverse-bias region the breakdown voltage is increasing with temperature, but note the undesirable increase in reverse saturation current.

1.7 RESISTANCE LEVELS

As the operating point of a diode moves from one region to another the resistance of the diode will also change due to the nonlinear shape of the characteristic curve. It will be demonstrated in the next few paragraphs that the type of applied voltage or signal will define the resistance level of interest. Three different levels will be introduced in this section that will appear again as we examine other devices. It is therefore paramount that their determination be clearly understood.

DC or Static Resistance

The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in Fig. 1.25 and applying the following equation:

$$R_D = \frac{V_D}{I_D} \tag{1.5}$$

The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few milliamperes).

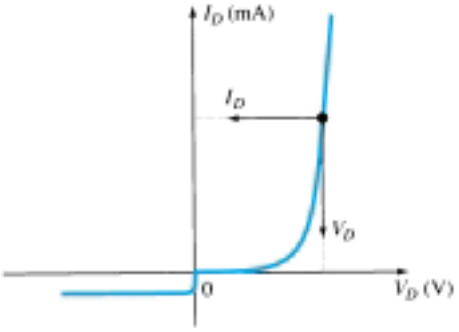


Figure 1.25 Determining the dc resistance of a diode at a particular operating point.

In general, therefore, the lower the current through a diode the higher the dc resistance level.

EXAMPLE 1.1

Determine the dc resistance levels for the diode of Fig. 1.26 at
(a) $I_D = 2$ mA
(b) $I_D = 20$ mA
(c) $V_D = -10$ V

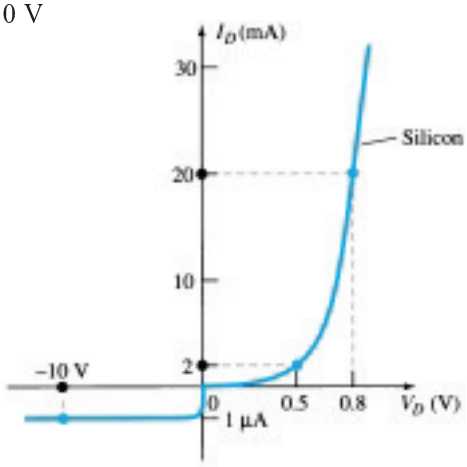


Figure 1.26 Example 1.1

Solution

(a) At $I_D = 2$ mA, $V_D = 0.5$ V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.5 \text{ V}}{2 \text{ mA}} = \mathbf{250\ \Omega}$$

(b) At $I_D = 20$ mA, $V_D = 0.8$ V (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{0.8\text{ V}}{20\text{ mA}} = \mathbf{40\ \Omega}$$

(c) At $V_D = -10$ V, $I_D = -I_s = -1\ \mu$A (from the curve) and

$$R_D = \frac{V_D}{I_D} = \frac{10\text{ V}}{1\ \mu\text{A}} = \mathbf{10\ M\Omega}$$

clearly supporting some of the earlier comments regarding the dc resistance levels of a diode.

AC or Dynamic Resistance

It is obvious from Eq. 1.5 and Example 1.1 that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.27. With no applied varying signal, the point of operation would be the *Q*-point appearing on Fig. 1.27 determined by the applied dc levels. The designation *Q-point* is derived from the word *quiescent,* which means "still or unvarying."

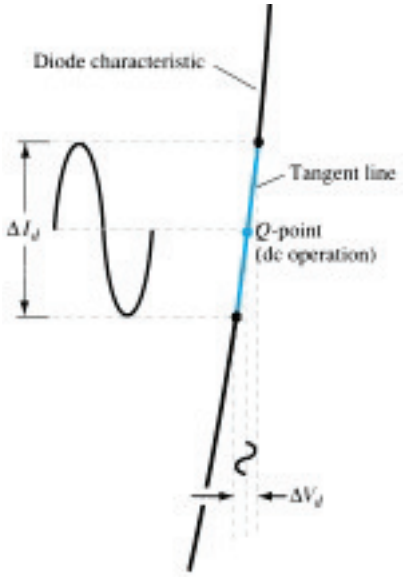


Figure 1.27 Defining the dynamic or ac resistance.

A straight line drawn tangent to the curve through the *Q*-point as shown in Fig. 1.28 will define a particular change in voltage and current that can be used to determine the *ac* or *dynamic* resistance for this region of the diode characteristics. An effort should be made to keep the change in voltage and current as small as possible and equidistant to either side of the *Q*-point. In equation form,

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$ where Δ signifies a finite change in the quantity. (1.6)

The steeper the slope, the less the value of ΔV_d for the same change in ΔI_d and the less the resistance. The ac resistance in the vertical-rise region of the characteristic is therefore quite small, while the ac resistance is much higher at low current levels.

In general, therefore, the lower the Q-point of operation (smaller current or lower voltage) the higher the ac resistance.

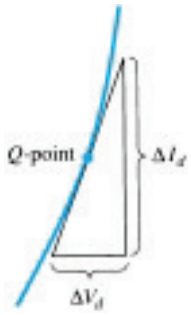


Figure 1.28 Determining the ac resistance at a *Q*-point.

EXAMPLE 1.2

For the characteristics of Fig. 1.29:

(a) Determine the ac resistance at $I_D = 2$ mA.

(b) Determine the ac resistance at $I_D = 25$ mA.

(c) Compare the results of parts (a) and (b) to the dc resistances at each current level.

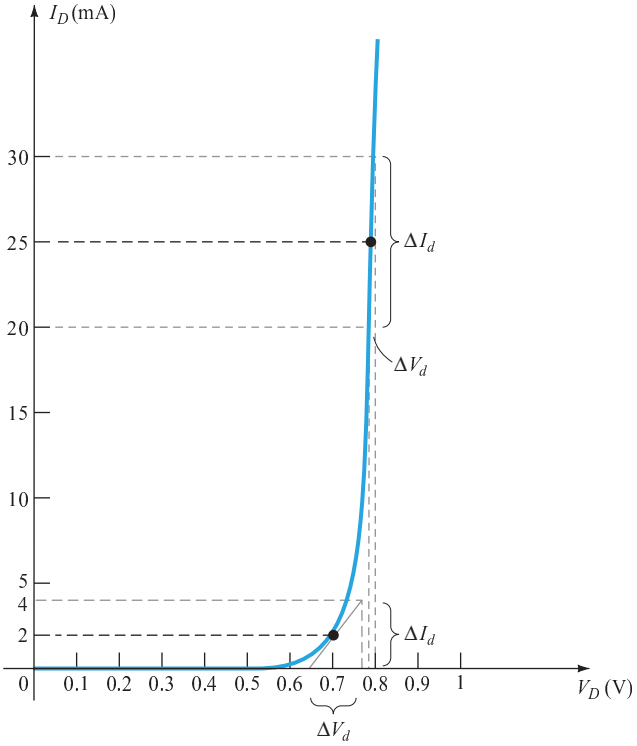


Figure 1.29 Example 1.2

Solution

(a) For $I_D = 2$ mA; the tangent line at $I_D = 2$ mA was drawn as shown in the figure and a swing of 2 mA above and below the specified diode current was chosen. At $I_D = 4$ mA, $V_D = 0.76$ V, and at $I_D = 0$ mA, $V_D = 0.65$ V. The resulting changes in current and voltage are

$$\Delta I_d = 4 \text{ mA} - 0 \text{ mA} = 4 \text{ mA}$$

and

$$\Delta V_d = 0.76 \text{ V} - 0.65 \text{ V} = 0.11 \text{ V}$$

and the ac resistance:

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.11 \text{ V}}{4 \text{ mA}} = \mathbf{27.5\ \Omega}$$

(b) For $I_D = 25$ mA, the tangent line at $I_D = 25$ mA was drawn as shown on the figure and a swing of 5 mA above and below the specified diode current was chosen. At $I_D = 30$ mA, $V_D = 0.8$ V, and at $I_D = 20$ mA, $V_D = 0.78$ V. The resulting changes in current and voltage are

$$\Delta I_d = 30 \text{ mA} - 20 \text{ mA} = 10 \text{ mA}$$

and

$$\Delta V_d = 0.8 \text{ V} - 0.78 \text{ V} = 0.02 \text{ V}$$

and the ac resistance is

$$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{0.02 \text{ V}}{10 \text{ mA}} = \mathbf{2\ \Omega}$$

(c) For $I_D = 2$ mA, $V_D = 0.7$ V and

$$R_D = \frac{V_D}{I_D} = \frac{0.7 \text{ V}}{2 \text{ mA}} = \mathbf{350\ \Omega}$$

which far exceeds the r_d of 27.5 Ω.

For $I_D = 25$ mA, $V_D = 0.79$ V and

$$R_D = \frac{V_D}{I_D} = \frac{0.79 \text{ V}}{25 \text{ mA}} = \mathbf{31.62\ \Omega}$$

which far exceeds the r_d of 2 Ω.

We have found the dynamic resistance graphically, but there is a basic definition in differential calculus which states:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

Equation (1.6), as defined by Fig. 1.28, is, therefore, essentially finding the derivative of the function at the Q-point of operation. If we find the derivative of the general equation (1.4) for the semiconductor diode with respect to the applied forward bias and then invert the result, we will have an equation for the dynamic or ac resistance in that region. That is, taking the derivative of Eq. (1.4) with respect to the applied bias will result in

$$\frac{d}{dV_D}(I_D) = \frac{d}{dV}[I_s(e^{kV_D/T_K} - 1)]$$

and

$$\frac{dI_D}{dV_D} = \frac{k}{T_K}(I_D + I_s)$$

following a few basic maneuvers of differential calculus. In general, $I_D \gg I_s$ in the vertical slope section of the characteristics and

$$\frac{dI_D}{dV_D} \cong \frac{k}{T_K} I_D$$

Substituting $\eta = 1$ for Ge and Si in the vertical-rise section of the characteristics, we obtain

$$k = \frac{11{,}600}{\eta} = \frac{11{,}600}{1} = 11{,}600$$

and at room temperature,

$$T_K = T_C + 273° = 25° + 273° = 298°$$

so that

$$\frac{k}{T_K} = \frac{11{,}600}{298} \cong 38.93$$

and

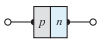
$$\frac{dI_D}{dV_D} = 38.93 I_D$$

Flipping the result to define a resistance ratio ($R = V/I$) gives us

$$\frac{dV_D}{dI_D} \cong \frac{0.026}{I_D}$$

or

$$\boxed{r_d = \frac{26 \text{ mV}}{I_D}}_{\text{Ge,Si}} \qquad (1.7)$$



The significance of Eq. (1.7) must be clearly understood. It implies that the dynamic resistance can be found simply by substituting the quiescent value of the diode current into the equation. There is no need to have the characteristics available or to worry about sketching tangent lines as defined by Eq. (1.6). It is important to keep in mind, however, that Eq. (1.7) is accurate only for values of I_D in the vertical-rise section of the curve. For lesser values of I_D, $\eta = 2$ (silicon) and the value of r_d obtained must be multiplied by a factor of 2. For small values of I_D below the knee of the curve, Eq. (1.7) becomes inappropriate.

All the resistance levels determined thus far have been defined by the *p-n* junction and do not include the resistance of the semiconductor material itself (called *body* resistance) and the resistance introduced by the connection between the semiconductor material and the external metallic conductor (called *contact* resistance). These additional resistance levels can be included in Eq. (1.7) by adding resistance denoted by r_B as appearing in Eq. (1.8). The resistance r'_d, therefore, includes the dynamic resistance defined by Eq. 1.7 and the resistance r_B just introduced.

$$r'_d = \frac{26 \text{ mV}}{I_D} + r_B \quad \text{ohms} \tag{1.8}$$

The factor r_B can range from typically 0.1 Ω for high-power devices to 2 Ω for some low-power, general-purpose diodes. For Example 1.2 the ac resistance at 25 mA was calculated to be 2 Ω. Using Eq. (1.7), we have

$$r_d = \frac{26 \text{ mV}}{I_D} = \frac{26 \text{ mV}}{25 \text{ mA}} = \mathbf{1.04\ \Omega}$$

The difference of about 1 Ω could be treated as the contribution of r_B.

For Example 1.2 the ac resistance at 2 mA was calculated to be 27.5 Ω. Using Eq. (1.7) but multiplying by a factor of 2 for this region (in the knee of the curve $\eta = 2$),

$$r_d = 2\left(\frac{26 \text{ mV}}{I_D}\right) = 2\left(\frac{26 \text{ mV}}{2 \text{ mA}}\right) = 2(13\ \Omega) = \mathbf{26\ \Omega}$$

The difference of 1.5 Ω could be treated as the contribution due to r_B.

In reality, determining r_d to a high degree of accuracy from a characteristic curve using Eq. (1.6) is a difficult process at best and the results have to be treated with a grain of salt. At low levels of diode current the factor r_B is normally small enough compared to r_d to permit ignoring its impact on the ac diode resistance. At high levels of current the level of r_B may approach that of r_d, but since there will frequently be other resistive elements of a much larger magnitude in series with the diode we will assume in this book that the ac resistance is determined solely by r_d and the impact of r_B will be ignored unless otherwise noted. Technological improvements of recent years suggest that the level of r_B will continue to decrease in magnitude and eventually become a factor that can certainly be ignored in comparison to r_d.

The discussion above has centered solely on the forward-bias region. In the reverse-bias region we will assume that the change in current along the I_s line is nil from 0 V to the Zener region and the resulting ac resistance using Eq. (1.6) is sufficiently high to permit the open-circuit approximation.

Average AC Resistance

If the input signal is sufficiently large to produce a broad swing such as indicated in Fig. 1.30, the resistance associated with the device for this region is called the *average ac resistance*. The average ac resistance is, by definition, the resistance deter-

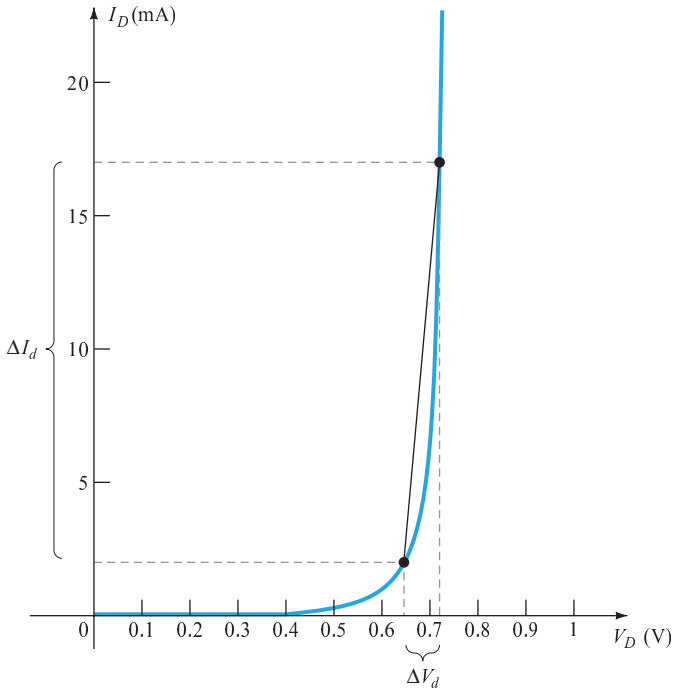


Figure 1.30 Determining the average ac resistance between indicated limits.

mined by a straight line drawn between the two intersections established by the maximum and minimum values of input voltage. In equation form (note Fig. 1.30),

$$r_{\text{av}} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}} \tag{1.9}$$

For the situation indicated by Fig. 1.30,

$$\Delta I_d = 17\ \text{mA} - 2\ \text{mA} = 15\ \text{mA}$$

and

$$\Delta V_d = 0.725\ \text{V} - 0.65\ \text{V} = 0.075\ \text{V}$$

with

$$r_{\text{av}} = \frac{\Delta V_d}{\Delta I_d} = \frac{0.075\,\text{V}}{15\ \text{mA}} = \mathbf{5\ \Omega}$$

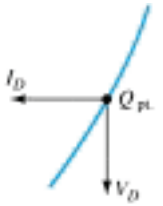
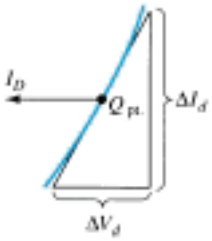
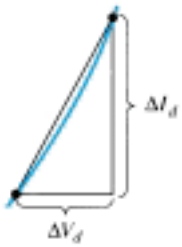
If the ac resistance (r_d) were determined at $I_D = 2$ mA its value would be more than 5 Ω, and if determined at 17 mA it would be less. In between the ac resistance would make the transition from the high value at 2 mA to the lower value at 17 mA. Equation (1.9) has defined a value that is considered the average of the ac values from 2 to 17 mA. The fact that one resistance level can be used for such a wide range of the characteristics will prove quite useful in the definition of equivalent circuits for a diode in a later section.

As with the dc and ac resistance levels, the lower the level of currents used to determine the average resistance the higher the resistance level.

Summary Table

Table 1.2 was developed to reinforce the important conclusions of the last few pages and to emphasize the differences among the various resistance levels. As indicated earlier, the content of this section is the foundation for a number of resistance calculations to be performed in later sections and chapters.

TABLE 1.2 Resistance Levels

Type	*Equation*	*Special Characteristics*	*Graphical Determination*
DC or static	$R_D = \frac{V_D}{I_D}$	Defined as a *point* on the characteristics	
AC or dynamic	$r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{26\text{ mV}}{I_D}$	Defined by a tangent line at the Q-point	
Average ac	$r_{av} = \frac{\Delta V_d}{\Delta I_d}\Big\vert_{\text{pt. to pt.}}$	Defined by a straight line between limits of operation	

1.8 DIODE EQUIVALENT CIRCUITS

An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region.

In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behavior of the system. The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments, as shown in Fig. 1.31. The resulting equivalent circuit is naturally called the *piecewise-linear equivalent circuit.* It should be obvious from Fig. 1.31 that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region. However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behavior of the device. For the sloping section of the equivalence the average ac resistance as introduced in Section 1.7 is the resistance level appearing in the equivalent circuit of Fig. 1.32 next to the actual device. In essence, it defines the resistance level of the device when it is in the "on" state. The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will re-

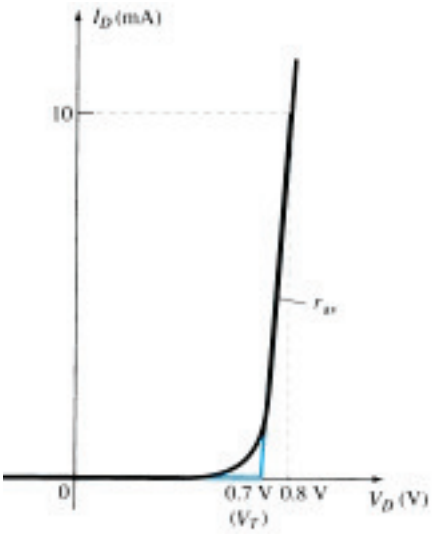


Figure 1.31 Defining the piecewise-linear equivalent circuit using straight-line segments to approximate the characteristic curve.

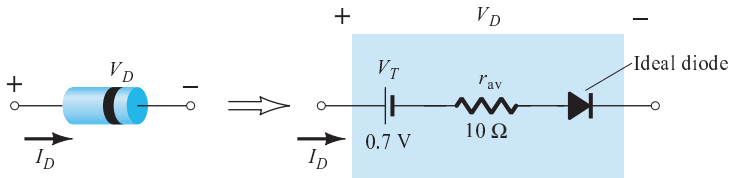


Figure 1.32 Components of the piecewise-linear equivalent circuit.

sult in the open-circuit state for the device. Since a silicon semiconductor diode does not reach the conduction state until V_D reaches 0.7 V with a forward bias (as shown in Fig. 1.31), a battery V_T opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.32. The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established. When conduction is established the resistance of the diode will be the specified value of r_{av}.

Keep in mind, however, that V_T in the equivalent circuit is not an independent voltage source. If a voltmeter is placed across an isolated diode on the top of a lab bench, a reading of 0.7 V will not be obtained. The battery simply represents the horizontal offset of the characteristics that must be exceeded to establish conduction.

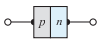
The approximate level of r_{av} can usually be determined from a specified operating point on the specification sheet (to be discussed in Section 1.9). For instance, for a silicon semiconductor diode, if $I_F = 10$ mA (a forward conduction current for the diode) at $V_D = 0.8$ V, we know for silicon that a shift of 0.7 V is required before the characteristics rise and

$$r_{av} = \left.\frac{\Delta V_d}{\Delta I_d}\right|_{\text{pt. to pt.}} = \frac{0.8\text{ V} - 0.7\text{ V}}{10\text{ mA} - 0\text{ mA}} = \frac{0.1\text{ V}}{10\text{ mA}} = \mathbf{10\ \Omega}$$

as obtained for Fig. 1.30.

Simplified Equivalent Circuit

For most applications, the resistance r_{av} is sufficiently small to be ignored in comparison to the other elements of the network. The removal of r_{av} from the equivalent



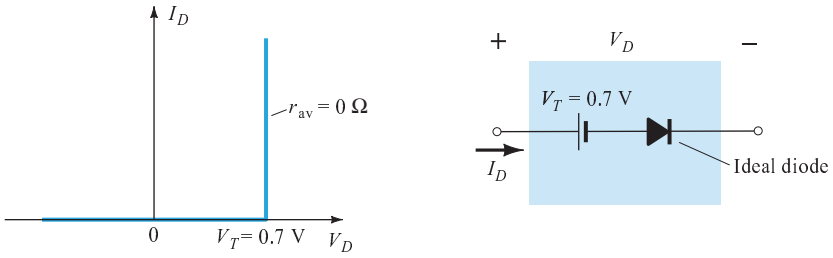


Figure 1.33 Simplified equivalent circuit for the silicon semiconductor diode.

circuit is the same as implying that the characteristics of the diode appear as shown in Fig. 1.33. Indeed, this approximation is frequently employed in semiconductor circuit analysis as demonstrated in Chapter 2. The reduced equivalent circuit appears in the same figure. It states that a forward-biased silicon diode in an electronic system under dc conditions has a drop of 0.7 V across it in the conduction state at any level of diode current (within rated values, of course).

Ideal Equivalent Circuit

Now that r_{av} has been removed from the equivalent circuit let us take it a step further and establish that a 0.7-V level can often be ignored in comparison to the applied voltage level. In this case the equivalent circuit will be reduced to that of an ideal diode as shown in Fig. 1.34 with its characteristics. In Chapter 2 we will see that this approximation is often made without a serious loss in accuracy.

In industry a popular substitution for the phrase "diode equivalent circuit" is diode *model*—a model by definition being a representation of an existing device, object, system, and so on. In fact, this substitute terminology will be used almost exclusively in the chapters to follow.

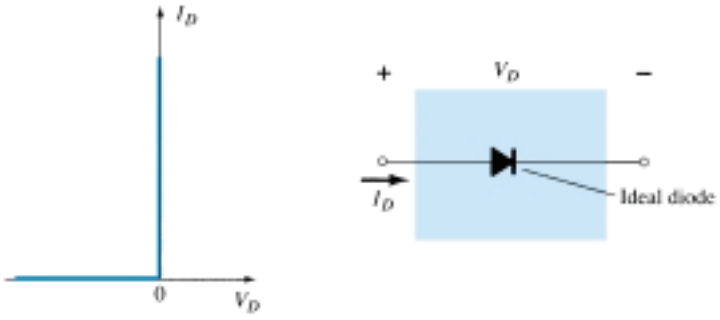
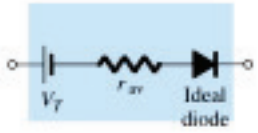
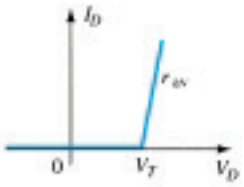
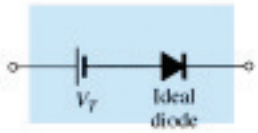
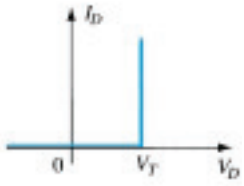
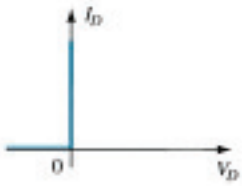


Figure 1.34 Ideal diode and its characteristics.

Summary Table

For clarity, the diode models employed for the range of circuit parameters and applications are provided in Table 1.3 with their piecewise-linear characteristics. Each will be investigated in greater detail in Chapter 2. There are always exceptions to the general rule, but it is fairly safe to say that the simplified equivalent model will be employed most frequently in the analysis of electronic systems while the ideal diode is frequently applied in the analysis of power supply systems where larger voltages are encountered.

TABLE 1.3 Diode Equivalent Circuits (Models)

Type	*Conditions*	*Model*	*Characteristics*
Piecewise-linear model			
Simplified model	$R_{network} \gg r_{av}$		
Ideal device	$R_{network} \gg r_{av}$ $E_{network} \gg V_T$		

1.9 DIODE SPECIFICATION SHEETS

Data on specific semiconductor devices are normally provided by the manufacturer in one of two forms. Most frequently, it is a very brief description limited to perhaps one page. Otherwise, it is a thorough examination of the characteristics using graphs, artwork, tables, and so on. In either case, there are specific pieces of data that must be included for proper utilization of the device. They include:

1. The forward voltage V_F (at a specified current and temperature)
2. The maximum forward current I_F (at a specified temperature)
3. The reverse saturation current I_R (at a specified voltage and temperature)
4. The reverse-voltage rating [PIV or PRV or V(BR), where BR comes from the term "breakdown" (at a specified temperature)]
5. The maximum power dissipation level at a particular temperature
6. Capacitance levels (as defined in Section 1.10)
7. Reverse recovery time t_{rr} (as defined in Section 1.11)
8. Operating temperature range

Depending on the type of diode being considered, additional data may also be provided, such as frequency range, noise level, switching time, thermal resistance levels, and peak repetitive values. For the application in mind, the significance of the data will usually be self-apparent. If the maximum power or dissipation rating is also provided, it is understood to be equal to the following product:

$$P_{D\max} = V_D I_D \tag{1.10}$$

where I_D and V_D are the diode current and voltage at a particular point of operation.

If we apply the simplified model for a particular application (a common occurrence), we can substitute $V_D = V_T = 0.7$ V for a silicon diode in Eq. (1.10) and determine the resulting power dissipation for comparison against the maximum power rating. That is,

$$P_{\text{dissipated}} \cong (0.7 \text{ V})I_D \tag{1.11}$$

DIFFUSED SILICON PLANAR

A — • BV . . . 125 V (MIN) @ 100 µA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperatures

Storage Temperature Range	−65°C to +200°C
B — Maximum Junction Operating Temperature	+175°C
Lead Temperature	+260°C

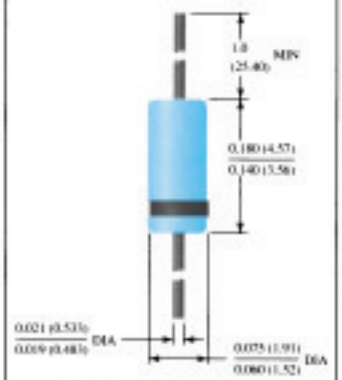
Power Dissipation (Note 2)

C — Maximum Total Power Dissipation at 25°C Ambient	500 mW
Linear Power Derating Factor (from 25°C)	3.33 mW/°C

Maximum Voltage and Currents

WIV	Working Inverse Voltage	100 V
I_O	Average Rectified Current	200 mA
D — I_F	Continuous Forward Current	500 mA
i_f	Peak Repetitive Forward Current	600 mA
$i_{f(surge)}$	Peak Forward Surge Current	
	Pulse Width = 1 s	1.0 A
	Pulse Width = 1 µs	4.0 A

DO-35 OUTLINE



NOTES:
Copper clad steel leads, tin plated
Gold plated leads available
Hermetically sealed glass package
Package weight is 0.14 gram

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
E — V_F	Forward Voltage	0.85	1.00	V	I_F = 200 mA
		0.81	0.94	V	I_F = 100 mA
		0.78	0.88	V	I_F = 50 mA
		0.69	0.80	V	I_F = 10 mA
		0.67	0.75	V	I_F = 5.0 mA
F		0.60	0.68	V	I_F = 1.0 mA
				V	I_F = 0.1 mA
G — I_R	Reverse Current		500	nA	V_R = 20 V, T_A = 125°C
			5.0	nA	V_R = 100 V
			1.0	µA	V_R = 100 V, T_A = 125°C
				nA	V_R = 180 V
				µA	V_R = 180 V, T_A = 100°C
BV	Breakdown Voltage	125		V	I_R = 100 µA
H — C	Capacitance		8.0	pF	V_R = 0, f = 1.0 MHz
I — t_{rr}	Reverse Recovery Time		3.0	µs	I_F = 10 mA, V_R = 35 V, R_L = 1.0 to 100 kΩ, C_L = 10 pF

NOTES
1 These ratings are limiting values above which the serviceability of the diode may be impaired.
2 These are steady state limits. The factory should be consulted on applications involving pulses or low duty-cycle operation.

Figure 1.35 Electrical characteristics of a high-voltage, low-leakage diode.

An exact copy of the data provided for a high-voltage/low-leakage diode appears in Figs. 1.35 and 1.36. This example would represent the expanded list of data and characteristics. The term *rectifier* is applied to a diode when it is frequently used in a *rectification* process to be described in Chapter 2.

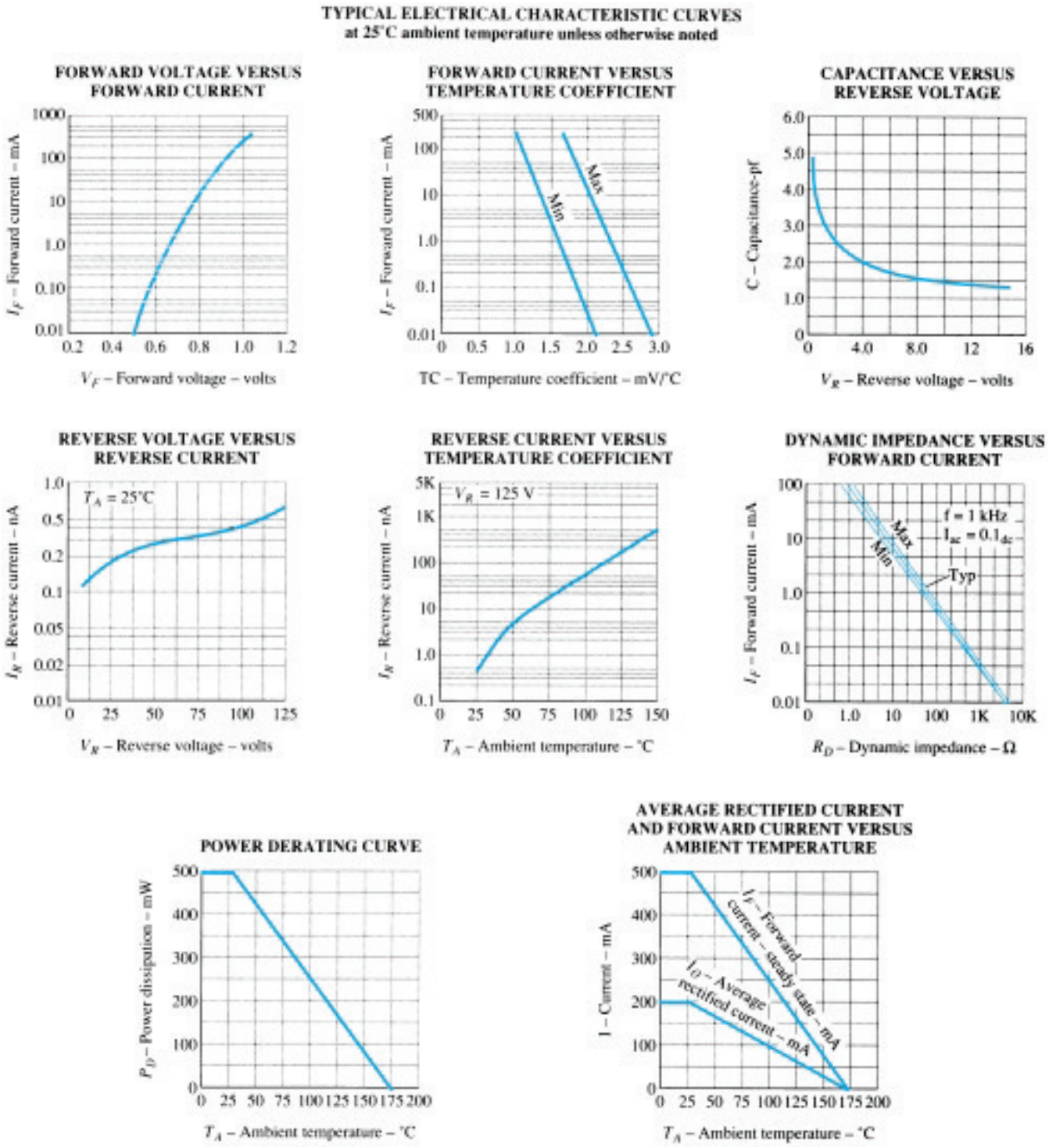
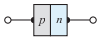


Figure 1.36 Terminal characteristics of a high-voltage diode.



Specific areas of the specification sheet have been highlighted in blue with a letter identification corresponding with the following description:

A: The *minimum* reverse-bias voltage (PIVs) for a diode at a specified reverse saturation current.

B: Temperature characteristics as indicated. Note the use of the Celsius scale and the wide range of utilization [recall that 32°F = 0°C = freezing (H_2O) and 212°F = 100°C = boiling (H_2O)].

C: Maximum power dissipation level $P_D = V_D I_D = 500$ mW. The maximum power rating decreases at a rate of 3.33 mW per degree increase in temperature above room temperature (25°C), as clearly indicated by the *power derating curve* of Fig. 1.36.

D: Maximum continuous forward current $I_{F_{max}} = 500$ mA (note I_F versus temperature in Fig. 1.36).

E: Range of values of V_F at $I_F = 200$ mA. Note that it exceeds $V_T = 0.7$ V for both devices.

F: Range of values of V_F at $I_F = 1.0$ mA. Note in this case how the upper limits surround 0.7 V.

G: At $V_R = 20$ V and a typical operating temperature $I_R = 500$ nA $= 0.5$ μA, while at a higher reverse voltage I_R drops to 5 nA $= 0.005$ μA.

H: The capacitance level between terminals is about 8 pF for the diode at $V_R = V_D = 0$ V (no-bias) and an applied frequency of 1 MHz.

I: The reverse recovery time is 3 μs for the list of operating conditions.

A number of the curves of Fig. 1.36 employ a log scale. A brief investigation of Section 11.2 should help with the reading of the graphs. Note in the top left figure how V_F increased from about 0.5 V to over 1 V as I_F increased from 10 μA to over 100 mA. In the figure below we find that the reverse saturation current does change slightly with increasing levels of V_R but remains at less than 1 nA at room temperature up to $V_R = 125$ V. As noted in the adjoining figure, however, note how quickly the reverse saturation current increases with increase in temperature (as forecasted earlier).

In the top right figure note how the capacitance decreases with increase in reverse-bias voltage, and in the figure below note that the ac resistance (r_d) is only about 1 Ω at 100 mA and increases to 100 Ω at currents less than 1 mA (as expected from the discussion of earlier sections).

The average rectified current, peak repetitive forward current, and peak forward surge current as they appear on the specification sheet are defined as follows:

1. *Average rectified current.* A half-wave-rectified signal (described in Section 2.8) has an average value defined by $I_{av} = 0.318 I_{peak}$. The average current rating is lower than the continuous or peak repetitive forward currents because a half-wave current waveform will have instantaneous values much higher than the average value.
2. *Peak repetitive forward current.* This is the maximum instantaneous value of repetitive forward current. Note that since it is at this level for a brief period of time, its level can be higher than the continuous level.
3. *Peak forward surge current.* On occasion during turn-on, malfunctions, and so on, there will be very high currents through the device for very brief intervals of time (that are not repetitive). This rating defines the maximum value and the time interval for such surges in current level.

The more one is exposed to specification sheets, the "friendlier" they will become, especially when the impact of each parameter is clearly understood for the application under investigation.

1.10 TRANSITION AND DIFFUSION CAPACITANCE

Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects that can be ignored at lower frequencies because the reactance $X_C = 1/2\pi fC$ is very large (open-circuit equivalent). This, however, cannot be ignored at very high frequencies. X_C will become sufficiently small due to the high value of f to introduce a low-reactance "shorting" path. In the *p-n* semiconductor diode, there are two capacitive effects to be considered. Both types of capacitance are present in the forward- and reverse-bias regions, but one so outweighs the other in each region that we consider the effects of only one in each region.

In the reverse-bias region we have the transition- or depletion-region capacitance (C_T), while in the forward-bias region we have the diffusion (C_D) or storage capacitance.

Recall that the basic equation for the capacitance of a parallel-plate capacitor is defined by $C = \epsilon A/d$, where ϵ is the permittivity of the dielectric (insulator) between the plates of area A separated by a distance d. In the reverse-bias region there is a depletion region (free of carriers) that behaves essentially like an insulator between the layers of opposite charge. Since the depletion width (d) will increase with increased reverse-bias potential, the resulting transition capacitance will decrease, as shown in Fig. 1.37. The fact that the capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems. In fact, in Chapter 20 a diode will be introduced whose operation is wholly dependent on this phenomenon.

Although the effect described above will also be present in the forward-bias region, it is overshadowed by a capacitance effect directly dependent on the rate at which charge is injected into the regions just outside the depletion region. The result is that increased levels of current will result in increased levels of diffusion capacitance. However, increased levels of current result in reduced levels of associated resistance (to be demonstrated shortly), and the resulting time constant ($\tau = RC$), which is very important in high-speed applications, does not become excessive.

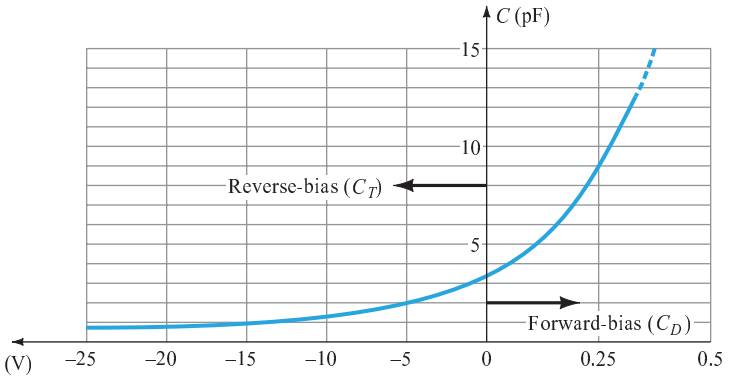


Figure 1.37 Transition and diffusion capacitance versus applied bias for a silicon diode.

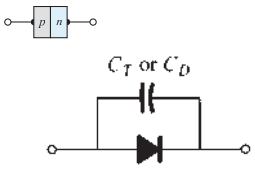


Figure 1.38 Including the effect of the transition or diffusion capacitance on the semiconductor diode.

The capacitive effects described above are represented by a capacitor in parallel with the ideal diode, as shown in Fig. 1.38. For low- or mid-frequency applications (except in the power area), however, the capacitor is normally not included in the diode symbol.

1.11 REVERSE RECOVERY TIME

There are certain pieces of data that are normally provided on diode specification sheets provided by manufacturers. One such quantity that has not been considered yet is the reverse recovery time, denoted by t_{rr}. In the forward-bias state it was shown earlier that there are a large number of electrons from the *n*-type material progressing through the *p*-type material and a large number of holes in the *n*-type—a requirement for conduction. The electrons in the *p*-type and holes progressing through the *n*-type material establish a large number of minority carriers in each material. If the applied voltage should be reversed to establish a reverse-bias situation, we would ideally like to see the diode change instantaneously from the conduction state to the nonconduction state. However, because of the large number of minority carriers in each material, the diode current will simply reverse as shown in Fig. 1.39 and stay at this measurable level for the period of time t_s (storage time) required for the minority carriers to return to their majority-carrier state in the opposite material. In essence, the diode will remain in the short-circuit state with a current I_{reverse} determined by the network parameters. Eventually, when this storage phase has passed, the current will reduce in level to that associated with the nonconduction state. This second period of time is denoted by t_t (transition interval). The reverse recovery time is the sum of these two intervals: $t_{rr} = t_s + t_t$. Naturally, it is an important consideration in high-speed switching applications. Most commercially available switching diodes have a t_{rr} in the range of a few nanoseconds to 1 μs. Units are available, however, with a t_{rr} of only a few hundred picoseconds (10^{-12}).

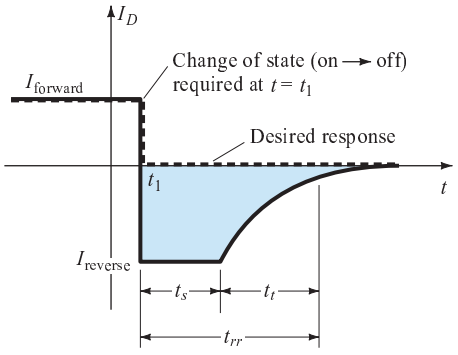


Figure 1.39 Defining the reverse recovery time.

1.12 SEMICONDUCTOR DIODE NOTATION

The notation most frequently used for semiconductor diodes is provided in Fig. 1.40. For most diodes any marking such as a dot or band, as shown in Fig. 1.40, appears at the cathode end. The terminology anode and cathode is a carryover from vacuum-tube notation. The anode refers to the higher or positive potential, and the cathode refers to the lower or negative terminal. This combination of bias levels will result in a forward-bias or "on" condition for the diode. A number of commercially available semiconductor diodes appear in Fig. 1.41. Some details of the actual construction of devices such as those appearing in Fig. 1.41 are provided in Chapters 12 and 20.

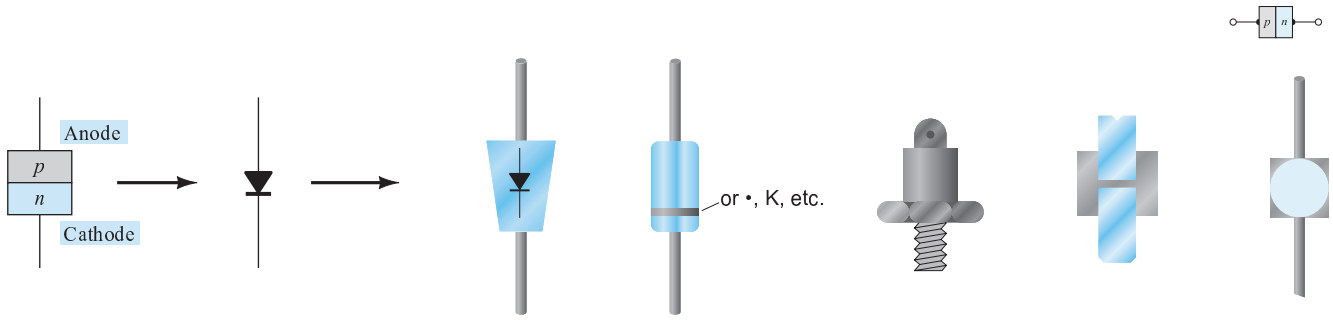


Figure 1.40 Semiconductor diode notation.

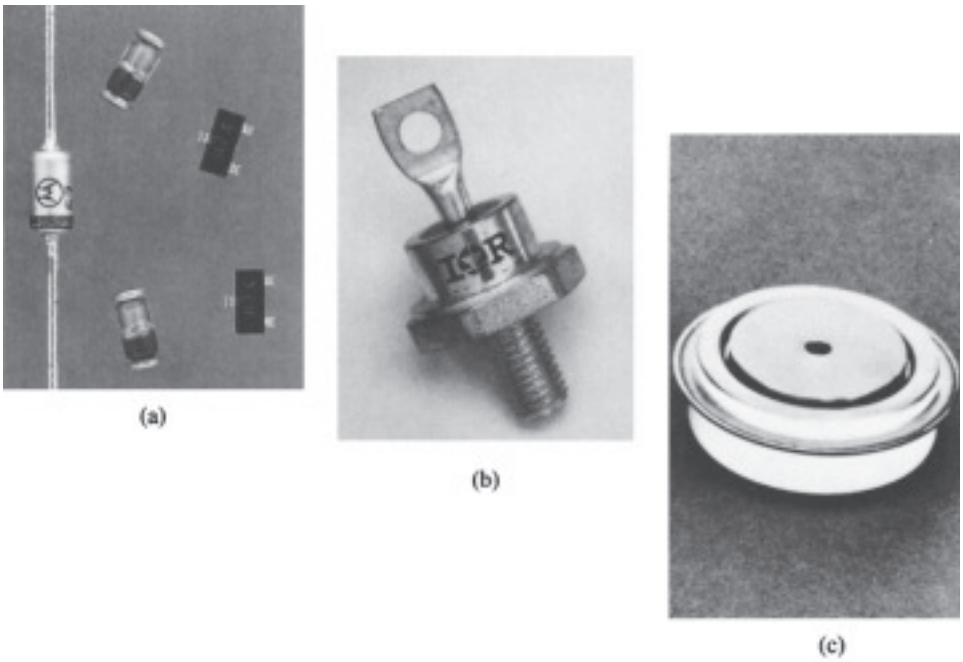


Figure 1.41 Various types of junction diodes. [(a) Courtesy of Motorola Inc.; and (b) and (c) Courtesy International Rectifier Corporation.]

1.13 DIODE TESTING

The condition of a semiconductor diode can be determined quickly using (1) a digital display meter (DDM) with a *diode checking function,* (2) the *ohmmeter section* of a multimeter, or (3) a *curve tracer.*

Diode Checking Function

A digital display meter with a diode checking capability appears in Fig. 1.42. Note the small diode symbol as the bottom option of the rotating dial. When set in this position and hooked up as shown in Fig. 1.43a, the diode should be in the "on" state and the display will provide an indication of the forward-bias voltage such as 0.67 V (for Si). The meter has an internal constant current source (about 2 mA) that will define the voltage level as indicated in Fig. 1.43b. An OL indication with the hookup of Fig. 1.43a reveals an open (defective) diode. If the leads are reversed, an OL indication should result due to the expected open-circuit equivalence for the diode. In general, therefore, an OL indication in both directions is an indication of an open or defective diode.

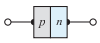


Figure 1.42 Digital display meter with diode checking capability. (Courtesy Computronics Technology, Inc.)

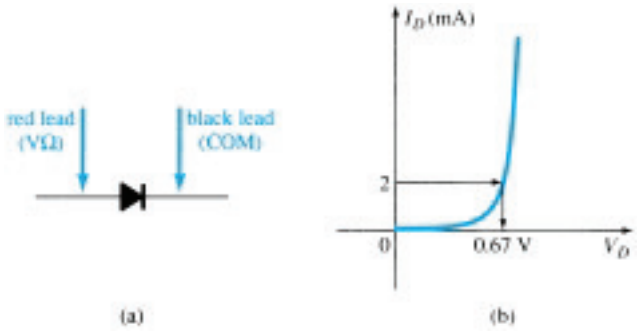


Figure 1.43 Checking a diode in the forward-bias state.

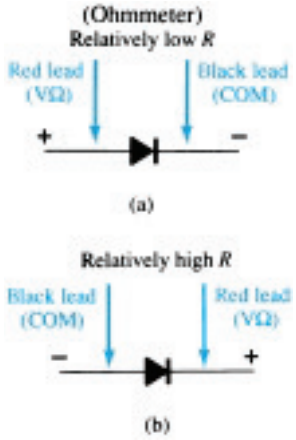


Figure 1.44 Checking a diode with an ohmmeter.

Ohmmeter Testing

In Section 1.7 we found that the forward-bias resistance of a semiconductor diode is quite low compared to the reverse-bias level. Therefore, if we measure the resistance of a diode using the connections indicated in Fig. 1.44a, we can expect a relatively low level. The resulting ohmmeter indication will be a function of the current established through the diode by the internal battery (often 1.5 V) of the ohmmeter circuit. The higher the current, the less the resistance level. For the reverse-bias situation the reading should be quite high, requiring a high resistance scale on the meter, as indicated in Fig. 1.44b. A high resistance reading in both directions obviously indicates an open (defective device) condition, while a very low resistance reading in both directions will probably indicate a shorted device.

Curve Tracer

The curve tracer of Fig. 1.45 can display the characteristics of a host of devices, including the semiconductor diode. By properly connecting the diode to the test panel at the bottom center of the unit and adjusting the controls, the display of Fig. 1.46

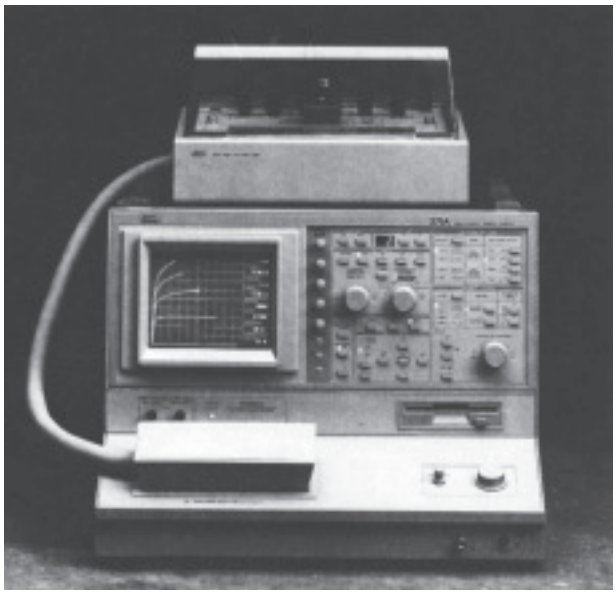


Figure 1.45 Curve tracer. (Courtesy of Tektronix, Inc.)

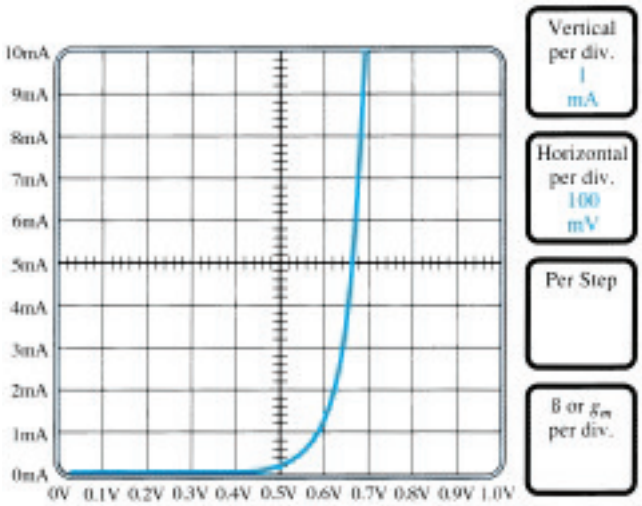


Figure 1.46 Curve tracer response to 1N4007 silicon diode.

can be obtained. Note that the vertical scaling is 1 mA/div, resulting in the levels indicated. For the horizontal axis the scaling is 100 mV/div, resulting in the voltage levels indicated. For a 2-mA level as defined for a DDM, the resulting voltage would be about 625 mV = 0.625 V. Although the instrument initially appears quite complex, the instruction manual and a few moments of exposure will reveal that the desired results can usually be obtained without an excessive amount of effort and time. The same instrument will appear on more than one occasion in the chapters to follow as we investigate the characteristics of the variety of devices.

1.14 ZENER DIODES

The Zener region of Fig. 1.47 was discussed in some detail in Section 1.6. The characteristic drops in an almost vertical manner at a reverse-bias potential denoted V_Z. The fact that the curve drops down and away from the horizontal axis rather than up and away for the positive V_D region reveals that the current in the Zener region has a direction opposite to that of a forward-biased diode.

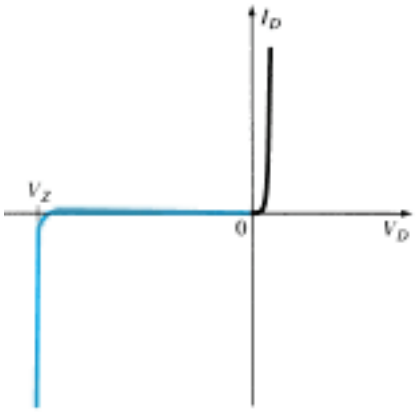


Figure 1.47 Reviewing the Zener region.

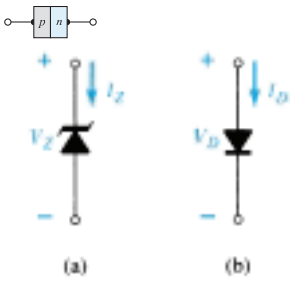


Figure 1.48 Conduction direction: (a) Zener diode; (b) semiconductor diode.

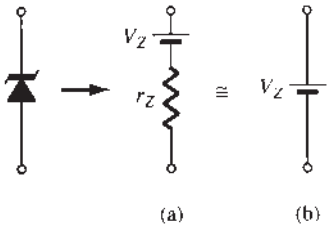


Figure 1.49 Zener equivalent circuit: (a) complete; (b) approximate.

This region of unique characteristics is employed in the design of *Zener diodes,* which have the graphic symbol appearing in Fig. 1.48a. Both the semiconductor diode and zener diode are presented side by side in Fig. 1.48 to ensure that the direction of conduction of each is clearly understood together with the required polarity of the applied voltage. For the semiconductor diode the "on" state will support a current in the direction of the arrow in the symbol. For the Zener diode the direction of conduction is opposite to that of the arrow in the symbol as pointed out in the introduction to this section. Note also that the polarity of V_D and V_Z are the same as would be obtained if each were a resistive element.

The location of the Zener region can be controlled by varying the doping levels. An increase in doping, producing an increase in the number of added impurities, will decrease the Zener potential. Zener diodes are available having Zener potentials of 1.8 to 200 V with power ratings from $\frac{1}{4}$ to 50 W. Because of its higher temperature and current capability, silicon is usually preferred in the manufacture of Zener diodes.

The complete equivalent circuit of the Zener diode in the Zener region includes a small dynamic resistance and dc battery equal to the Zener potential, as shown in Fig. 1.49. For all applications to follow, however, we shall assume as a first approximation that the external resistors are much larger in magnitude than the Zener-equivalent resistor and that the equivalent circuit is simply the one indicated in Fig. 1.49b.

A larger drawing of the Zener region is provided in Fig. 1.50 to permit a description of the Zener nameplate data appearing in Table 1.4 for a 10-V, 500-mW, 20% diode. The term *nominal* associated with V_Z indicates that it is a typical average value. Since this is a 20% diode, the Zener potential can be expected to vary as 10 V ± 20%

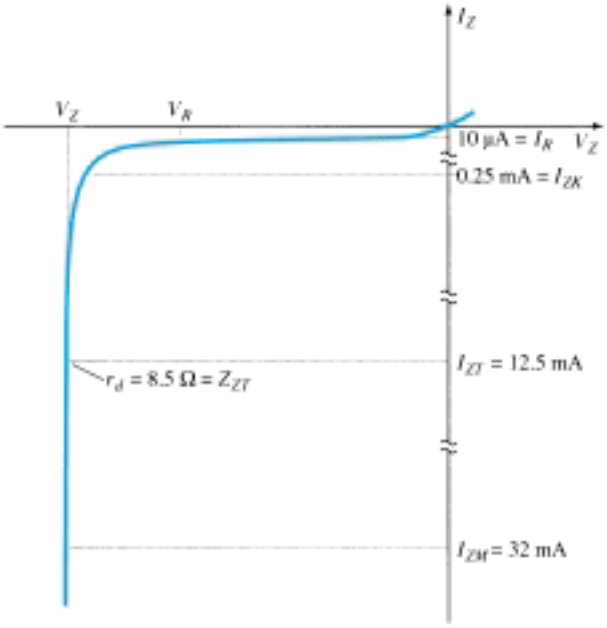


Figure 1.50 Zener test characteristics.

TABLE 1.4 Electrical Characteristics (25°C Ambient Temperature Unless Otherwise Noted)

Zener Voltage Nominal, V_Z *(V)*	*Test Current,* I_{ZT} *(mA)*	*Max Dynamic Impedance,* Z_{ZT} *at* I_{ZT} *(Ω)*	*Maximum Knee Impedance,* Z_{ZK} *at* I_{ZK} *(Ω)*	*(mA)*	*Maximum Reverse Current,* I_R *at* V_R *(μA)*	*Test Voltage,* V_R *(V)*	*Maximum Regulator Current,* I_{ZM} *(mA)*	*Typical Temperature Coefficient (%/°C)*
10	12.5	8.5	700	0.25	10	7.2	32	+0.072

or from 8 to 12 V in its range of application. Also available are 10% and 5% diodes with the same specifications. The test current I_{ZT} is the current defined by the $\frac{1}{4}$ power level, and Z_{ZT} is the dynamic impedance at this current level. The maximum knee impedance occurs at the knee current of I_{ZK}. The reverse saturation current is provided at a particular potential level, and I_{ZM} is the maximum current for the 20% unit.

The temperature coefficient reflects the percent change in V_Z with temperature. It is defined by the equation

$$T_C = \frac{\Delta V_Z}{V_Z(T_1 - T_0)} \times 100\% \qquad \%/^\circ\text{C} \tag{1.12}$$

where ΔV_Z is the resulting change in Zener potential due to the temperature variation. Note in Fig. 1.51a that the temperature coefficient can be positive, negative, or even zero for different Zener levels. A positive value would reflect an increase in V_Z with an increase in temperature, while a negative value would result in a decrease in value with increase in temperature. The 24-V, 6.8-V, and 3.6-V levels refer to three Zener diodes having these nominal values within the same family of Zeners. The curve for the 10-V Zener would naturally lie between the curves of the 6.8-V and 24-V devices. Returning to Eq. (1.12), T_0 is the temperature at which V_Z is provided (normally room temperature—25°C), and T_1 is the new level. Example 1.3 will demonstrate the use of Eq. (1.12).

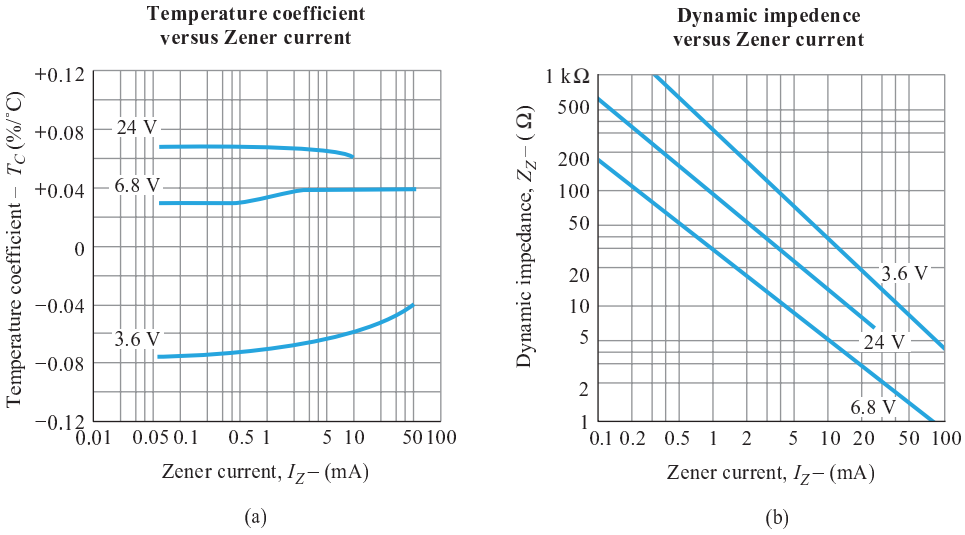


Figure 1.51 Electrical characteristics for a 10-V, 500-mW Zener diode.

EXAMPLE 1.3

Determine the nominal voltage for the Zener diode of Table 1.4 at a temperature of 100°C.

Solution

From Eq. 1.12,

$$\Delta V_Z = \frac{T_C V_Z}{100}(T_1 - T_0)$$

Substitution values from Table 1.4 yield

$$\Delta V_Z = \frac{(0.072)(10\text{ V})}{100}(100°\text{C} - 25°\text{C})$$
$$= (0.0072)(75)$$
$$= 0.54\text{ V}$$

and because of the positive temperature coefficient, the new Zener potential, defined by V_Z', is

$$V_Z' = V_Z + 0.54\text{ V}$$
$$\mathbf{= 10.54\text{ V}}$$

The variation in dynamic impedance (fundamentally, its series resistance) with current appears in Fig. 1.51b. Again, the 10-V Zener appears between the 6.8-V and 24-V Zeners. Note that the heavier the current (or the farther up the vertical rise you are in Fig. 1.47), the less the resistance value. Also note that as you drop below the knee of the curve, the resistance increases to significant levels.

The terminal identification and the casing for a variety of Zener diodes appear in Fig. 1.52. Figure 1.53 is an actual photograph of a variety of Zener devices. Note that their appearance is very similar to the semiconductor diode. A few areas of application for the Zener diode will be examined in Chapter 2.

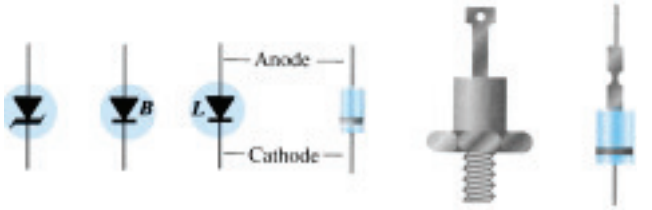


Figure 1.52 Zener terminal identification and symbols.

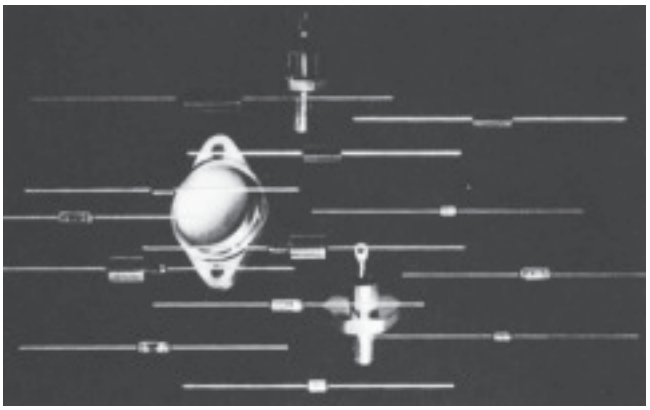


Figure 1.53 Zener diodes. (Courtesy Siemens Corporation.)

1.15 LIGHT-EMITTING DIODES

The increasing use of digital displays in calculators, watches, and all forms of instrumentation has contributed to the current extensive interest in structures that will emit light when properly biased. The two types in common use today to perform this function are the *light-emitting diode* (LED) and the *liquid-crystal display* (LCD). Since the LED falls within the family of *p-n* junction devices and will appear in some of

the networks in the next few chapters, it will be introduced in this chapter. The LCD display is described in Chapter 20.

As the name implies, the light-emitting diode (LED) is a diode that will give off visible light when it is energized. In any forward-biased *p-n* junction there is, within the structure and primarily close to the junction, a recombination of holes and electrons. This recombination requires that the energy possessed by the unbound free electron be transferred to another state. In all semiconductor *p-n* junctions some of this energy will be given off as heat and some in the form of photons. In silicon and germanium the greater percentage is given up in the form of heat and the emitted light is insignificant. In other materials, such as gallium arsenide phosphide (GaAsP) or gallium phosphide (GaP), the number of photons of light energy emitted is sufficient to create a very visible light source.

The process of giving off light by applying an electrical source of energy is called electroluminescence.

As shown in Fig. 1.54 with its graphic symbol, the conducting surface connected to the *p*-material is much smaller, to permit the emergence of the maximum number of photons of light energy. Note in the figure that the recombination of the injected carriers due to the forward-biased junction results in emitted light at the site of recombination. There may, of course, be some absorption of the packages of photon energy in the structure itself, but a very large percentage are able to leave, as shown in the figure.

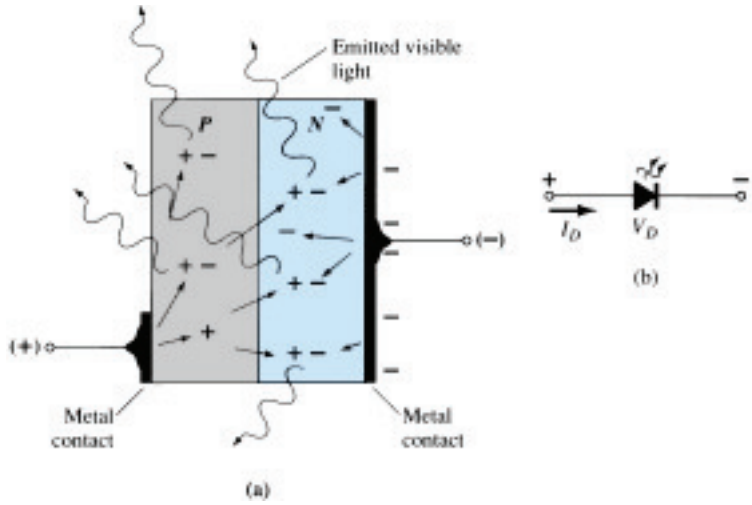


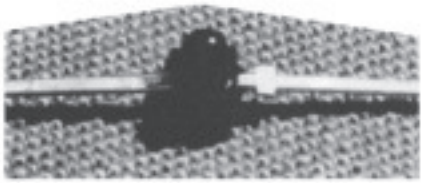
Figure 1.54 (a) Process of electroluminescence in the LED; (b) graphic symbol.

The appearance and characteristics of a subminiature high-efficiency solid-state lamp manufactured by Hewlett-Packard appears in Fig. 1.55. Note in Fig. 1.55b that the peak forward current is 60 mA, with 20 mA the typical average forward current. The test conditions listed in Fig. 1.55c, however, are for a forward current of 10 mA. The level of V_D under forward-bias conditions is listed as V_F and extends from 2.2 to 3 V. In other words, one can expect a typical operating current of about 10 mA at 2.5 V for good light emission.

Two quantities yet undefined appear under the heading Electrical/Optical Characteristics at $T_A = 25°C$. They are the *axial luminous intensity* (I_V) and the *luminous efficacy* (η_v). Light intensity is measured in *candela*. One candela emits a light flux of 4π lumens and establishes an illumination of 1 footcandle on a 1-ft^2 area 1 ft from the light source. Even though this description may not provide a clear understanding of the candela as a unit of measure, its level can certainly be compared between similar devices. The term *efficacy* is, by definition, a measure of the ability of a device to produce a desired effect. For the LED this is the ratio of the number of lumens generated per applied watt of electrical energy. The relative efficiency is defined by

the luminous intensity per unit current, as shown in Fig. 1.55g. The relative intensity of each color versus wavelength appears in Fig. 1.55d.

Since the LED is a *p-n* junction device, it will have a forward-biased characteristic (Fig. 1.55e) similar to the diode response curves. Note the almost linear increase in relative luminous intensity with forward current (Fig. 1.55f). Figure 1.55h reveals that the longer the pulse duration at a particular frequency, the lower the permitted peak current (after you pass the break value of t_p). Figure 1.55i simply reveals that the intensity is greater at 0° (or head on) and the least at 90° (when you view the device from the side).



(a)

Absolute Maximum Ratings at T_A = 25°C

Parameter	*High Eff. Red 4160*	*Units*
Power dissipation	120	mW
Average forward current	20[1]	mA
Peak forward current	60	mA
Operating and storage temperature range	–55°C to 100°C	
Lead soldering temperature [1.6 mm (0.063 in.) from body]	230°C for 3 seconds	

[1] Derate from 50°C at 0.2 mA/°C.

(b)

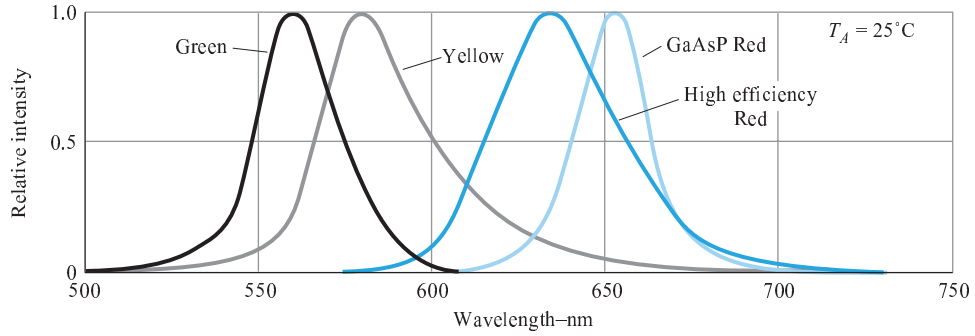
Electrical/Optical Characteristics at T_A = 25°C

Symbol	*Description*	*High Eff. Red 4160* *Min.*	*Typ.*	*Max.*	*Units*	*Test Conditions*
						I_F = 10 mA
I_V	Axial luminous intensity	1.0	3.0		mcd	
$2\theta_{1/2}$	Included angle between half luminous intensity points		80		deg.	Note 1
λ_{peak}	Peak wavelength		635		nm	Measurement at peak
λ_d	Dominant wavelength		628		nm	Note 2
τ_s	Speed of response		90		ns	
C	Capacitance		11		pF	V_F = 0; f = 1 Mhz
θ_{JC}	Thermal resistance		120		°C/W	Junction to cathode lead at 0.79 mm (.031 in) from body
V_F	Forward voltage		2.2	3.0	V	I_F = 10 mA
BV_R	Reverse breakdown voltage	5.0			V	I_R = 100 µA
η_v	Luminous efficacy		147		lm/W	Note 3

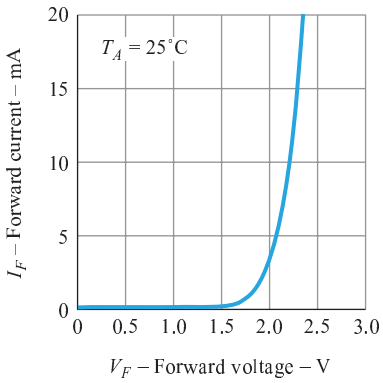
NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength that defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

(c)

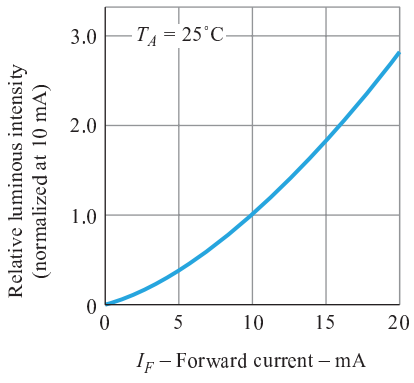
Figure 1.55 Hewlett-Packard subminiature high-efficiency red solid-state lamp: (a) appearance; (b) absolute maximum ratings; (c) electrical/optical characteristics; (d) relative intensity versus wavelength; (e) forward current versus forward voltage; (f) relative luminous intensity versus forward current; (g) relative efficiency versus peak current; (h) maximum peak current versus pulse duration; (i) relative luminous intensity versus angular displacement. (Courtesy Hewlett-Packard Corporation.)



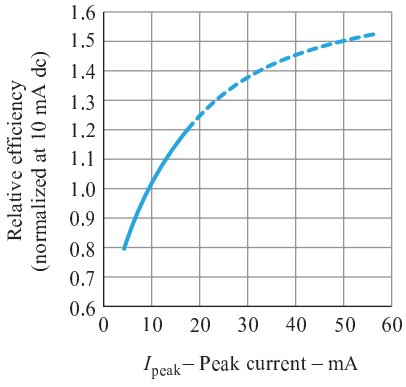
(d)



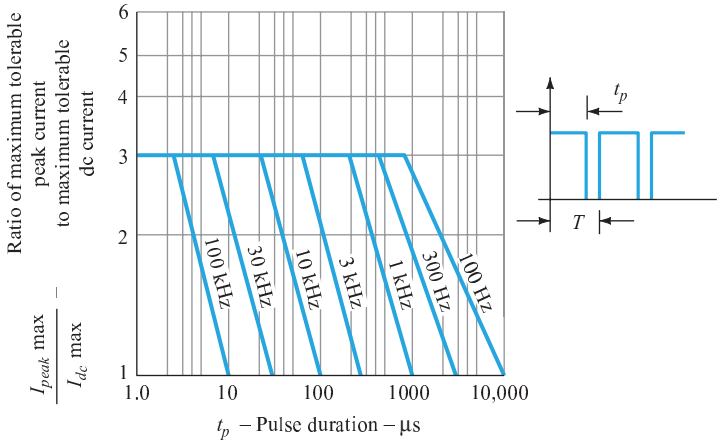
(e)



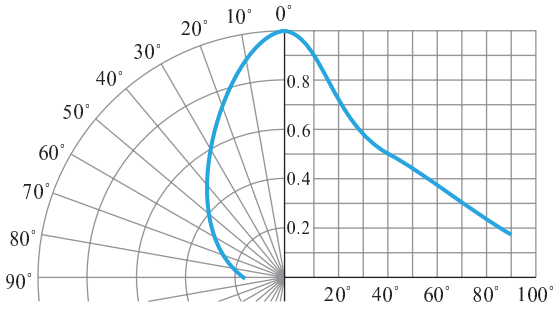
(f)



(g)



(h)



(i)

Figure 1.55 Continued.

LED displays are available today in many different sizes and shapes. The light-emitting region is available in lengths from 0.1 to 1 in. Numbers can be created by segments such as shown in Fig. 1.56. By applying a forward bias to the proper *p*-type material segment, any number from 0 to 9 can be displayed.

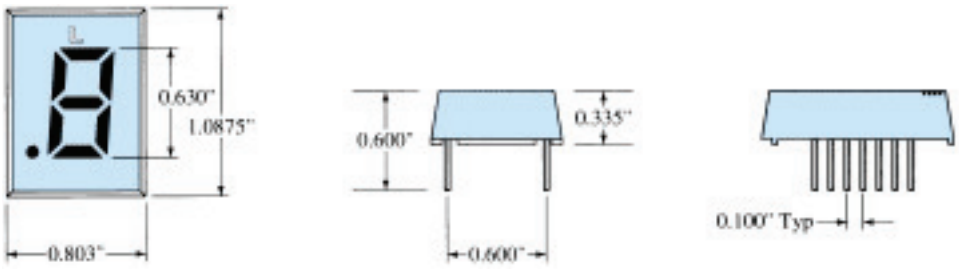


Figure 1.56 Litronix segment display.

There are also two-lead LED lamps that contain two LEDs, so that a reversal in biasing will change the color from green to red, or vice versa. LEDs are presently available in red, green, yellow, orange, and white, and white with blue soon to be commercially available. In general, LEDs operate at voltage levels from 1.7 to 3.3 V, which makes them completely compatible with solid-state circuits. They have a fast response time (nanoseconds) and offer good contrast ratios for visibility. The power requirement is typically from 10 to 150 mW with a lifetime of 100,000+ hours. Their semiconductor construction adds a significant ruggedness factor.

1.16 DIODE ARRAYS—INTEGRATED CIRCUITS

The unique characteristics of integrated circuits will be introduced in Chapter 12. However, we have reached a plateau in our introduction to electronic circuits that permits at least a surface examination of diode arrays in the integrated-circuit package. You will find that the integrated circuit is not a unique device with characteristics totally different from those we examine in these introductory chapters. It is simply a packaging technique that permits a significant reduction in the size of electronic systems. In other words, internal to the integrated circuit are systems and discrete devices that were available long before the integrated circuit as we know it today became a reality.

One possible array appears in Fig. 1.57. Note that eight diodes are internal to the diode array. That is, in the container shown in Fig. 1.58 there are diodes set in a single silicon wafer that have all the anodes connected to pin 1 and the cathodes of each to pins 2 through 9. Note in the same figure that pin 1 can be determined as being to the left of the small projection in the case if we look from the bottom toward the case. The other numbers then follow in sequence. If only one diode is to be used, then only pins 1 and 2 (or any number from 3 to 9) would be used. The remaining diodes would be left hanging and not affect the network to which pins 1 and 2 are connected.

Another diode array appears in Fig. 1.59 (see page 44). In this case the package is different but the numbering sequence appears in the outline. Pin 1 is the pin directly above the small indentation as you look down on the device.

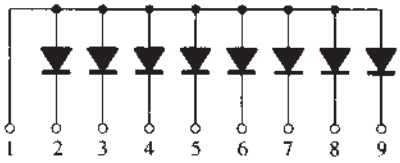
PLANAR AIR–ISOLATED MONOLITHIC DIODE ARRAY

- C . . . 5.0 pF (MAX)
- ΔV_F . . . 15 mv (MAX) @ 10 mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperatures	
Storage Temperature Range	–55°C to +200°C
Maximum Junction Operating Temperature	+150°C
Lead Temperature	+260°C
Power Dissipation (Note 2)	
Maximum Dissipation per Junction at 25°C Ambient	400 mW
per Package at 25°C Ambient	600 mW
Linear Derating Factor (from 25°C) Junction	3.2 mW/°C
Package	4.8 mW/°C
Maximum Voltage and Currents	
WIV Working Inverse Voltage	55 V
I_F Continuous Forward Current	350 mA
$i_{f(surge)}$ Peak Forward Surge Current	
Pulse Width = 1.0 s	1.0 A
Pulse Width = 1.0 μs	2.0 A

CONNECTION DIAGRAM



See Package Outline TO-96

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
B_V	Breakdown Voltage	60		V	I_R = 10 μA
V_F	Forward Voltage (Note 3)		1.5 1.1 1.0	V V V	I_F = 500 mA I_F = 200 mA I_F = 100 mA
I_R	Reverse Current Reverse Current (T_A = 150°C)		100 100	nA μA	V_R = 40 V V_R = 40 V
C	Capacitance		5.0	pF	V_R = 0, f = 1 MHz
V_{FM}	Peak Forward Voltage		4.0	V	I_f = 500 mA, t_r < 10 ns
t_{fr}	Forward Recovery Time		40	ns	I_f = 500 mA, t_r < 10 ns
t_{rr}	Reverse Recovery Time		10 50	ns ns	$I_f = I_r$ = 10 – 200 mA R_L = 100Ω, Rec. to 0.1 I_r I_f = 500 mA, I_r = 50 mA R_L = 100Ω, Rec. to 5 mA
ΔV_F	Forward Voltage Match		15	mV	I_F = 10 mA

NOTES
1. These ratings are limiting values above which life or satisfactory performance may be impaired.
2. These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operation.
3. V_F is measured using an 8 ms pulse.

Figure 1.57 Monolithic diode array.

1.17 PSPICE WINDOWS

The computer has now become such an integral part of the electronics industry that the capabilities of this working "tool" must be introduced at the earliest possible opportunity. For those students with no prior computer experience there is a common initial fear of this seemingly complicated powerful system. With this in mind the computer analysis of this book was designed to make the computer system more "friendly" by revealing the relative ease with which it can be applied to perform some very help-

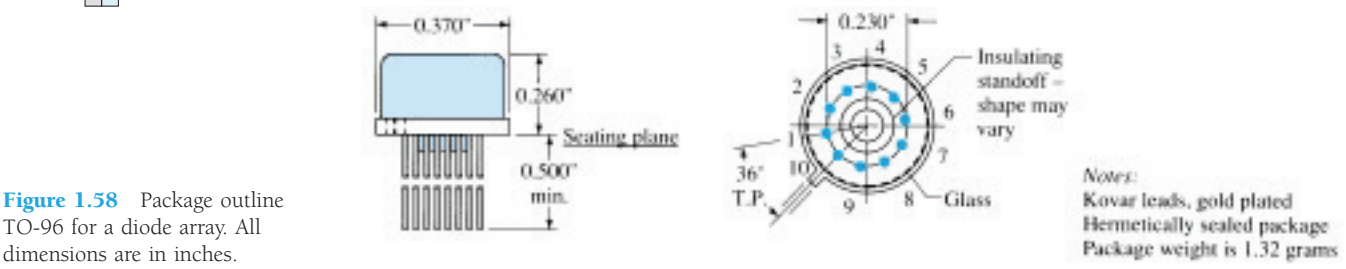


Figure 1.58 Package outline TO-96 for a diode array. All dimensions are in inches.

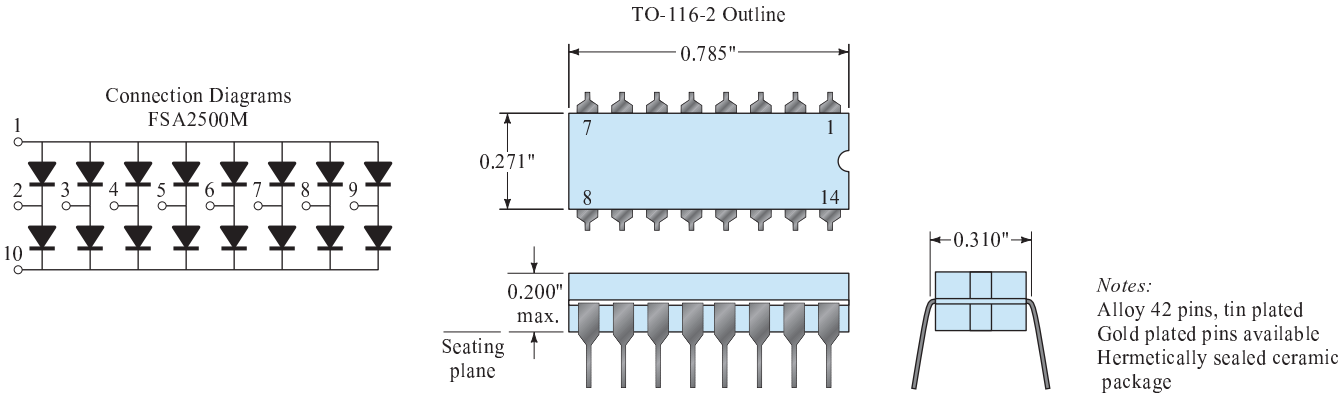


Figure 1.59 Monolithic diode array. All dimensions are in inches.

ful and special tasks in a minimum amount of time with a high degree of accuracy. The content was written with the assumption that the reader has no prior computer experience or exposure to the terminology to be applied. There is also no suggestion that the content of this book is sufficient to permit a complete understanding of the "hows" and "whys" that will surface. The purpose here is solely to introduce some of the terminology, discuss a few of its capabilities, reveal the possibilities available, touch on some of its limitations, and demonstrate its versatility with a number of carefully chosen examples.

In general, the computer analysis of electronic systems can take one of two approaches: using a *language* such as BASIC, Fortran, Pascal, or C; or utilizing a *software package* such as PSpice, MicroCap II, Breadboard, or Circuit Master, to name a few. A language, through its symbolic notation, forms a bridge between the user and the computer that permits a dialogue between the two for establishing the operations to be performed.

In earlier editions of this text, the chosen language was BASIC, primarily because it uses a number of familiar words and phrases from the English language that in themselves reveal the operation to be performed. When a language is employed to analyze a system, a *program* is developed that sequentially defines the operations to be performed—in much the same order in which we perform the same analysis in longhand. As with the longhand approach, one wrong step and the result obtained can be completely meaningless. Programs typically develop with time and application as more efficient paths toward a solution become obvious. Once established in its "best" form it can be cataloged for future use. The important advantage of the language approach is that a program can be tailored to meet all the special needs of the user. It permits innovative "moves" by the user that can result in printouts of data in an informative and interesting manner.

The alternative approach referred to above utilizes a software package to perform the desired investigation. A software package is a program written and tested over a

period of time designed to perform a particular type of analysis or synthesis in an efficient manner with a high level of accuracy.

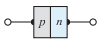
The package itself cannot be altered by the user, and its application is limited to the operations built into the system. A user must adjust his or her desire for output information to the range of possibilities offered by the package. In addition, the user must input information exactly as requested by the package or the data may be misinterpreted. The software package chosen for this book is PSpice.* PSpice currently is available in two forms: DOS and Windows. Although DOS format was the first introduced, the Windows version is the most popular today. The Windows version employed in this text is 8.0, the latest available. A photograph of a complete Design Center package appears in Fig. 1.60 with the 8.0 CD-ROM version. It is also available in 3.5″ diskettes. A more sophisticated version referred to simply as SPICE is finding widespread application in industry.

Figure 1.60 PSpice Design package. (Courtesy of the OrCAD-MicroSim Corporation.)

In total, therefore, a software package is "packaged" to perform a specific series of calculations and operations and to provide the results in a defined format. A language permits an expanded level of flexibility but also fails to benefit from the extensive testing and research normally devoted to the development of a "trusted" package. The user must define which approach best fits the needs of the moment. Obviously, if a package exists for the desired analysis or synthesis, it should be considered before turning to the many hours required to develop a reliable, efficient program. In addition, one may acquire the data needed for a particular analysis from a software package and then turn to a language to define the format of the output. In many ways, the two approaches go hand in hand. If one is to depend on computer analysis on a continuing basis, knowledge of the use and limits of both languages and software packages is a necessity. The choice of which language or software package to become familiar with is primarily a function of the area of investigation. Fortunately, however, a fluent knowledge of one language or a particular software package will usually help the user become familiar with other languages and software packages. There is a similarity in purpose and procedures that ease the transition from one approach to another.

When using PSpice Windows, the network is first drawn on the screen followed by an analysis dictated by the needs of the user. This text will be using **Version 8.0,** though the differences between this and earlier Windows versions are so few and relatively minor for this level of application that one should not be concerned if using an earlier edition. The first step, of course, is to install PSpice into the hard-disk

*PSpice is a registered trademark of the OrCAD-MicroSim Corporation.



memory of your computer following the directions provided by MicroSim. Next, the **Schematics** screen must be obtained using a control mechanism such as **Windows 95.** Once established, the elements for the network must be obtained and placed on the screen to build the network. In this text, the procedure for each element will be described following the discussion of the characteristics and analysis of each device.

Since we have just finished covering the diode in detail, the procedure for finding the diodes stored in the library will be introduced along with the method for placing them on the screen. The next chapter will introduce the procedure for analyzing a complete network with diodes using PSpice. There are several ways to proceed, but the most direct path is to click on the picture symbol with the binoculars on the top right of the schematics screen. As you bring the marker close to the box using the mouse, a message **Get New Part** will be displayed. Left click on the symbol and a **Part Browser Basic** dialog box will appear. By choosing **Libraries,** a **Library Browser** dialog box will appear and the **EVAL.slb** library should be chosen. When selected, all available parts in this library will appear in the **Part** listing. Next, scroll the **Part** list and choose the **D1N4148** diode. The result is that the **Part Name** will appear above and the **Description** will indicate it is a diode. Once set, click **OK** and the **Part Browser Basic** dialog box will reappear with the full review of the chosen element. To place the device on the screen and close the dialog box, simply click on the **Place & Close** option. The result is that the diode will appear on the screen and can be put in place with a left click of the mouse. Once located, two labels will appear—one indicating how any diodes have been placed (**D1, D2, D3,** and so on) and the other the name of the chosen diode (**D1N4148**). The same diode can be placed in other places on the same screen by simply moving the pointer and left clicking the mouse. The process can be ended by a single right click of the mouse. Any of the diodes can be removed by simply clicking on them to make them red and pressing the **Delete** key. If preferred, the **Edit** choice of the menu bar at the top of the screen also can be chosen, followed by using the **Delete** command.

Another path for obtaining an element is to choose **Draw** on the menu bar, followed by **Get New Part.** Once chosen, the **Part Browser Basic** dialog box will appear as before and the same procedure can be followed. Now that we know the D1N4148 diode exists, it can be obtained directly once the **Part Browser Basic** dialog box appears. Simply type D1N4148 in the **Part Name** box, followed by **Place & Close,** and the **diode** will appear on the screen.

If a diode has to be moved, simply left click on it once, until it turns red. Then, click on it again and hold the clicker down on the mouse. At the same time, move the diode to any location you prefer and, when set, lift up on the clicker. Remember that anything in red can be operated on. To remove the red status, simply remove the pointer from the element and click it once. The diode will turn green and blue, indicating that its location and associated information is set in memory. For all the above and for the chapters to follow, if you happen to have a monochromatic (black-and-white) screen, you will simply have to remember whether the device is in the active state.

If the label or parameters of the diode are to be changed, simply click on the element once (to make it red) and choose **Edit,** followed by **Model.** An **Edit Model** dialog box will appear with a choice of changing the **model reference** (D1N4148), the **text** associated with each parameter, or the **parameters** that define the characteristics of the diode.

As mentioned above, additional comments regarding use of the diode will be made in the chapters to follow. For the moment, we are at least aware of how to find and place an element on the screen. If time permits, review the other elements available within the various libraries to prepare yourself for the work to follow.

§ 1.2 Ideal Diode

1. Describe in your own words the meaning of the word *ideal* as applied to a device or system.
2. Describe in your own words the characteristics of the *ideal* diode and how they determine the on and off states of the device. That is, describe why the short-circuit and open-circuit equivalents are appropriate.
3. What is the one important difference between the characteristics of a simple switch and those of an ideal diode?

§ 1.3 Semiconductor Materials

4. In your own words, define *semiconductor, resistivity, bulk resistance,* and *ohmic contact resistance.*
5. (a) Using Table 1.1, determine the resistance of a silicon sample having an area of 1 cm^2 and a length of 3 cm.
   (b) Repeat part (a) if the length is 1 cm and the area 4 cm^2.
   (c) Repeat part (a) if the length is 8 cm and the area 0.5 cm^2.
   (d) Repeat part (a) for copper and compare the results.
6. Sketch the atomic structure of copper and discuss why it is a good conductor and how its structure is different from germanium and silicon.
7. In your own words, define an intrinsic material, a negative temperature coefficient, and covalent bonding.
8. Consult your reference library and list three materials that have a negative temperature coefficient and three that have a positive temperature coefficient.

§ 1.4 Energy Levels

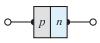
9. How much energy in joules is required to move a charge of 6 C through a difference in potential of 3 V?
10. If 48 eV of energy is required to move a charge through a potential difference of 12 V, determine the charge involved.
11. Consult your reference library and determine the level of E_g for GaP and ZnS, two semiconductor materials of practical value. In addition, determine the written name for each material.

§ 1.5 Extrinsic Materials—*n*- and *p*-Type

12. Describe the difference between *n*-type and *p*-type semiconductor materials.
13. Describe the difference between donor and acceptor impurities.
14. Describe the difference between majority and minority carriers.
15. Sketch the atomic structure of silicon and insert an impurity of arsenic as demonstrated for silicon in Fig. 1.9.
16. Repeat Problem 15 but insert an impurity of indium.
17. Consult your reference library and find another explanation of hole versus electron flow. Using both descriptions, describe in your own words the process of hole conduction.

§ 1.6 Semiconductor Diode

18. Describe in your own words the conditions established by forward- and reverse-bias conditions on a *p*-*n* junction diode and how the resulting current is affected.
19. Describe how you will remember the forward- and reverse-bias states of the *p*-*n* junction diode. That is, how you will remember which potential (positive or negative) is applied to which terminal?
20. Using Eq. (1.4), determine the diode current at 20°C for a silicon diode with $I_s = 50$ nA and an applied forward bias of 0.6 V.



21. Repeat Problem 20 for $T = 100°C$ (boiling point of water). Assume that I_s has increased to 5.0 μA.

22. (a) Using Eq. (1.4), determine the diode current at 20°C for a silicon diode with $I_s = 0.1$ μA at a reverse-bias potential of -10 V.

(b) Is the result expected? Why?

23. (a) Plot the function $y = e^x$ for x from 0 to 5.

(b) What is the value of $y = e^x$ at $x = 0$?

(c) Based on the results of part (b), why is the factor -1 important in Eq. (1.4)?

24. In the reverse-bias region the saturation current of a silicon diode is about 0.1 μA ($T = 20°C$). Determine its approximate value if the temperature is increased 40°C.

25. Compare the characteristics of a silicon and a germanium diode and determine which you would prefer to use for most practical applications. Give some details. Refer to a manufacturer's listing and compare the characteristics of a germanium and a silicon diode of similar maximum ratings.

26. Determine the forward voltage drop across the diode whose characteristics appear in Fig. 1.24 at temperatures of $-75°C$, 25°C, 100°C, and 200°C and a current of 10 mA. For each temperature, determine the level of saturation current. Compare the extremes of each and comment on the ratio of the two.

§ 1.7 Resistance Levels

27. Determine the static or dc resistance of the commercially available diode of Fig. 1.19 at a forward current of 2 mA.

28. Repeat Problem 26 at a forward current of 15 mA and compare results.

29. Determine the static or dc resistance of the commercially available diode of Fig. 1.19 at a reverse voltage of -10 V. How does it compare to the value determined at a reverse voltage of -30 V?

30. (a) Determine the dynamic (ac) resistance of the diode of Fig. 1.29 at a forward current of 10 mA using Eq. (1.6).

(b) Determine the dynamic (ac) resistance of the diode of Fig. 1.29 at a forward current of 10 mA using Eq. (1.7).

(c) Compare solutions of parts (a) and (b).

31. Calculate the dc and ac resistance for the diode of Fig. 1.29 at a forward current of 10 mA and compare their magnitudes.

32. Using Eq. (1.6), determine the ac resistance at a current of 1 mA and 15 mA for the diode of Fig. 1.29. Compare the solutions and develop a general conclusion regarding the ac resistance and increasing levels of diode current.

33. Using Eq. (1.7), determine the ac resistance at a current of 1 mA and 15 mA for the diode of Fig. 1.19. Modify the equation as necessary for low levels of diode current. Compare to the solutions obtained in Problem 32.

34. Determine the average ac resistance for the diode of Fig. 1.19 for the region between 0.6 and 0.9 V.

35. Determine the ac resistance for the diode of Fig. 1.19 at 0.75 V and compare to the average ac resistance obtained in Problem 34.

§ 1.8 Diode Equivalent Circuits

36. Find the piecewise-linear equivalent circuit for the diode of Fig. 1.19. Use a straight line segment that intersects the horizontal axis at 0.7 V and best approximates the curve for the region greater than 0.7 V.

37. Repeat Problem 36 for the diode of Fig. 1.29.

§ 1.9 Diode Specification Sheets

*38. Plot I_F versus V_F using linear scales for the diode of Fig. 1.36. Note that the provided graph employs a log scale for the vertical axis (log scales are covered in sections 11.2 and 11.3).

39. Comment on the change in capacitance level with increase in reverse-bias potential for the diode of Fig. 1.36.

40. Does the reverse saturation current of the diode of Fig. 1.36 change significantly in magnitude for reverse-bias potentials in the range -25 to -100 V?

*41. For the diode of Fig. 1.36 determine the level of I_R at room temperature (25°C) and the boiling point of water (100°C). Is the change significant? Does the level just about double for every 10°C increase in temperature?

42. For the diode of Fig. 1.36 determine the maximum ac (dynamic) resistance at a forward current of 0.1, 1.5, and 20 mA. Compare levels and comment on whether the results support conclusions derived in earlier sections of this chapter.

43. Using the characteristics of Fig. 1.36, determine the maximum power dissipation levels for the diode at room temperature (25°C) and 100°C. Assuming that V_F remains fixed at 0.7 V, how has the maximum level of I_F changed between the two temperature levels?

44. Using the characteristics of Fig. 1.36, determine the temperature at which the diode current will be 50% of its value at room temperature (25°C).

§ 1.10 Transition and Diffusion Capacitance

*45. (a) Referring to Fig. 1.37, determine the transition capacitance at reverse-bias potentials of -25 and -10 V. What is the ratio of the change in capacitance to the change in voltage?

(b) Repeat part (a) for reverse-bias potentials of -10 and -1 V. Determine the ratio of the change in capacitance to the change in voltage.

(c) How do the ratios determined in parts (a) and (b) compare? What does it tell you about which range may have more areas of practical application?

46. Referring to Fig. 1.37, determine the diffusion capacitance at 0 and 0.25 V.

47. Describe in your own words how diffusion and transition capacitances differ.

48. Determine the reactance offered by a diode described by the characteristics of Fig. 1.37 at a forward potential of 0.2 V and a reverse potential of -20 V if the applied frequency is 6 MHz.

§ 1.11 Reverse Recovery Time

49. Sketch the waveform for i of the network of Fig. 1.61 if $t_t = 2t_s$ and the total reverse recovery time is 9 ns.

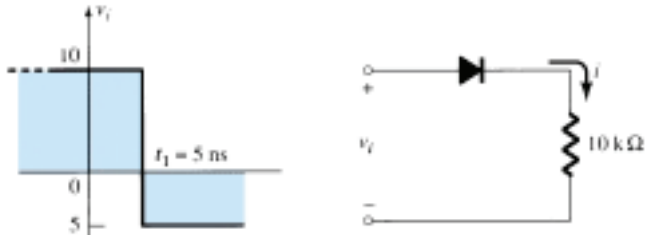
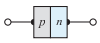


Figure 1.61 Problem 49

§ 1.14 Zener Diodes

50. The following characteristics are specified for a particular Zener diode: $V_Z = 29$ V, $V_R = 16.8$ V, $I_{ZT} = 10$ mA, $I_R = 20$ μA, and $I_{ZM} = 40$ mA. Sketch the characteristic curve in the manner displayed in Fig. 1.50.

* 51. At what temperature will the 10-V Zener diode of Fig. 1.50 have a nominal voltage of 10.75 V? (*Hint:* Note the data in Table 1.4.)



52. Determine the temperature coefficient of a 5-V Zener diode (rated 25°C value) if the nominal voltage drops to 4.8 V at a temperature of 100°C.

53. Using the curves of Fig. 1.51a, what level of temperature coefficient would you expect for a 20-V diode? Repeat for a 5-V diode. Assume a linear scale between nominal voltage levels and a current level of 0.1 mA.

54. Determine the dynamic impedance for the 24-V diode at $I_Z = 10$ mA for Fig. 1.51b. Note that it is a log scale.

***55.** Compare the levels of dynamic impedance for the 24-V diode of Fig. 1.51b at current levels of 0.2, 1, and 10 mA. How do the results relate to the shape of the characteristics in this region?

§ 1.15 Light-Emitting Diodes

56. Referring to Fig. 1.55e, what would appear to be an appropriate value of V_T for this device? How does it compare to the value of V_T for silicon and germanium?

57. Using the information provided in Fig. 1.55, determine the forward voltage across the diode if the relative luminous intensity is 1.5.

***58.** (a) What is the percent increase in relative efficiency of the device of Fig. 1.55 if the peak current is increased from 5 to 10 mA?

(b) Repeat part (a) for 30 to 35 mA (the same increase in current).

(c) Compare the percent increase from parts (a) and (b). At what point on the curve would you say there is little gained by further increasing the peak current?

***59.** (a) Referring to Fig. 1.55h, determine the maximum tolerable peak current if the period of the pulse duration is 1 ms, the frequency is 300 Hz, and the maximum tolerable dc current is 20 mA.

(b) Repeat part (a) for a frequency of 100 Hz.

60. (a) If the luminous intensity at 0° angular displacement is 3.0 mcd for the device of Fig. 1.55, at what angle will it be 0.75 mcd?

(b) At what angle does the loss of luminous intensity drop below the 50% level?

***61.** Sketch the current derating curve for the average forward current of the high-efficiency red LED of Fig. 1.55 as determined by temperature. (Note the absolute maximum ratings.)

*Please Note: Asterisks indicate more difficult problems.

CHAPTER

2 Diode Applications

2.1 INTRODUCTION

The construction, characteristics, and models of semiconductor diodes were introduced in Chapter 1. The primary goal of this chapter is to develop a working knowledge of the diode in a variety of configurations using models appropriate for the area of application. By chapter's end, the fundamental behavior pattern of diodes in dc and ac networks should be clearly understood. The concepts learned in this chapter will have significant carryover in the chapters to follow. For instance, diodes are frequently employed in the description of the basic construction of transistors and in the analysis of transistor networks in the dc and ac domains.

The content of this chapter will reveal an interesting and very positive side of the study of a field such as electronic devices and systems—once the basic behavior of a device is understood, its function and response in an infinite variety of configurations can be determined. The range of applications is endless, yet the characteristics and models remain the same. The analysis will proceed from one that employs the actual diode characteristic to one that utilizes the approximate models almost exclusively. It is important that the role and response of various elements of an electronic system be understood without continually having to resort to lengthy mathematical procedures. This is usually accomplished through the approximation process, which can develop into an art itself. Although the results obtained using the actual characteristics may be slightly different from those obtained using a series of approximations, keep in mind that the characteristics obtained from a specification sheet may in themselves be slightly different from the device in actual use. In other words, the characteristics of a 1N4001 semiconductor diode may vary from one element to the next in the same lot. The variation may be slight, but it will often be sufficient to validate the approximations employed in the analysis. Also consider the other elements of the network: Is the resistor labeled 100 Ω exactly 100 Ω? Is the applied voltage exactly 10 V or perhaps 10.08 V? All these tolerances contribute to the general belief that a response determined through an appropriate set of approximations can often be "as accurate" as one that employs the full characteristics. In this book the emphasis is toward developing a working knowledge of a device through the use of appropriate approximations, thereby avoiding an unnecessary level of mathematical complexity. Sufficient detail will normally be provided, however, to permit a detailed mathematical analysis if desired.

2.2 LOAD-LINE ANALYSIS

The applied load will normally have an important impact on the point or region of operation of a device. If the analysis is performed in a graphical manner, a line can be drawn on the characteristics of the device that represents the applied load. The intersection of the load line with the characteristics will determine the point of operation of the system. Such an analysis is, for obvious reasons, called *load-line analysis*. Although the majority of the diode networks analyzed in this chapter do not employ the load-line approach, the technique is one used quite frequently in subsequent chapters, and this introduction offers the simplest application of the method. It also permits a validation of the approximate technique described throughout the remainder of this chapter.

Consider the network of Fig. 2.1a employing a diode having the characteristics of Fig. 2.1b. Note in Fig. 2.1a that the "pressure" established by the battery is to establish a current through the series circuit in the clockwise direction. The fact that this current and the defined direction of conduction of the diode are a "match" reveals that the diode is in the "on" state and conduction has been established. The resulting polarity across the diode will be as shown and the first quadrant (V_D and I_D positive) of Fig. 2.1b will be the region of interest—the forward-bias region.

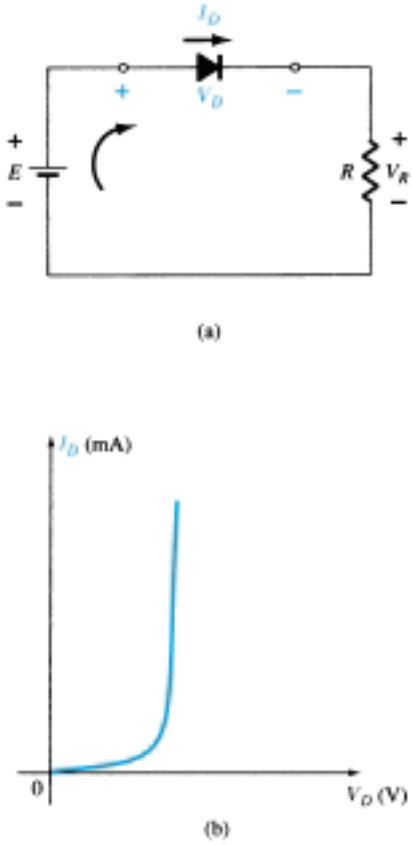


Figure 2.1 Series diode configuration: (a) circuit; (b) characteristics.

Applying Kirchhoff's voltage law to the series circuit of Fig. 2.1a will result in

$$E - V_D - V_R = 0$$

or

$$\boxed{E = V_D + I_D R} \tag{2.1}$$

The two variables of Eq. (2.1) (V_D and I_D) are the same as the diode axis variables of Fig. 2.1b. This similarity permits a plotting of Eq. (2.1) on the same characteristics of Fig. 2.1b.

The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis $I_D = 0$ A and anywhere on the vertical axis $V_D = 0$ V.

If we *set* $V_D = 0$ V in Eq. (2.1) and solve for I_D, we have the magnitude of I_D *on* the vertical axis. Therefore, with $V_D = 0$ V, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= 0\ \text{V} + I_D R \end{aligned}$$

and

$$\boxed{I_D = \left.\frac{E}{R}\right|_{V_D = 0\ \text{V}}} \tag{2.2}$$

as shown in Fig. 2.2. If we *set* $I_D = 0$ A in Eq. (2.1) and solve for V_D, we have the magnitude of V_D *on* the horizontal axis. Therefore, with $I_D = 0$ A, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= V_D + (0\ \text{A})R \end{aligned}$$

and

$$\boxed{V_D = E|_{I_D = 0\ A}} \tag{2.3}$$

as shown in Fig. 2.2. A straight line drawn between the two points will define the load line as depicted in Fig. 2.2. Change the level of R (the load) and the intersection on the vertical axis will change. The result will be a change in the slope of the load line and a different point of intersection between the load line and the device characteristics.

We now have a load line defined by the network and a characteristic curve defined by the device. The point of intersection between the two is the point of opera-

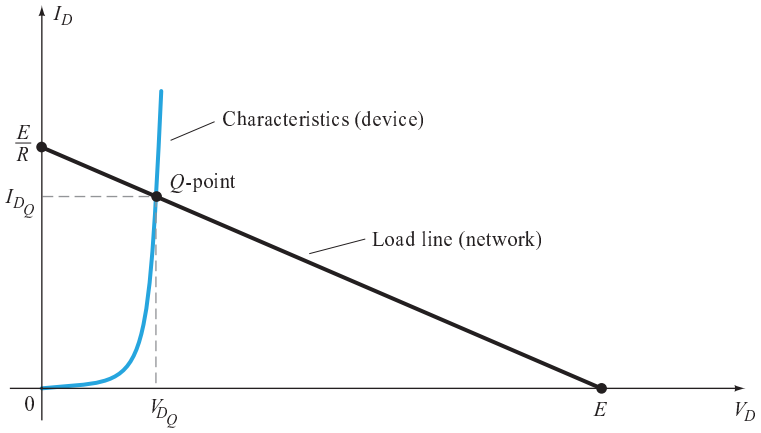


Figure 2.2 Drawing the load line and finding the point of operation.

tion for this circuit. By simply drawing a line down to the horizontal axis the diode voltage V_{D_Q} can be determined, whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{D_Q}. The current I_D is actually the current through the entire series configuration of Fig. 2.1a. The point of operation is usually called the *quiescent point* (abbreviated "Q-pt.") to reflect its "still, unmoving" qualities as defined by a dc network.

The solution obtained at the intersection of the two curves is the same that would be obtained by a simultaneous mathematical solution of Eqs. (2.1) and (1.4) [$I_D = I_s(e^{kV_D/T_K} - 1)$]. Since the curve for a diode has nonlinear characteristics the mathematics involved would require the use of nonlinear techniques that are beyond the needs and scope of this book. The load-line analysis described above provides a solution with a minimum of effort and a "pictorial" description of why the levels of solution for V_{D_Q} and I_{D_Q} were obtained. The next two examples will demonstrate the techniques introduced above and reveal the relative ease with which the load line can be drawn using Eqs. (2.2) and (2.3).

EXAMPLE 2.1

For the series diode configuration of Fig. 2.3a employing the diode characteristics of Fig. 2.3b determine:
(a) V_{D_Q} and I_{D_Q}.
(b) V_R.

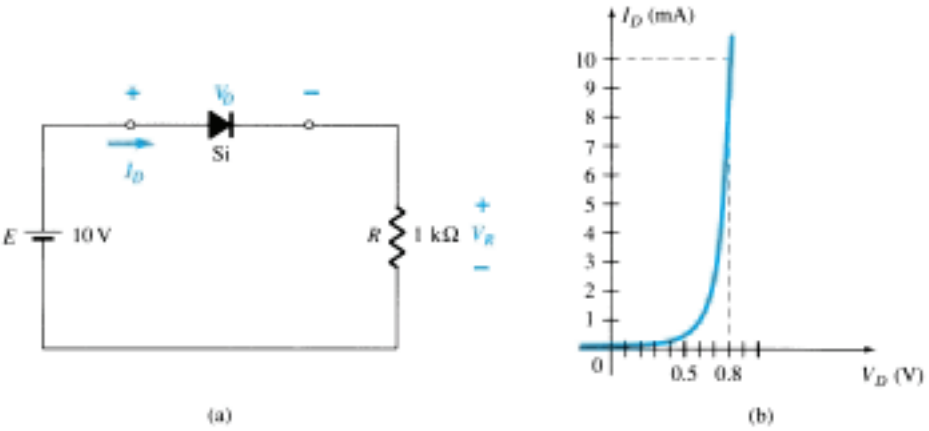


Figure 2.3 (a) Circuit; (b) characteristics.

Solution

(a) Eq. (2.2): $I_D = \left.\frac{E}{R}\right|_{V_D=0\text{ V}} = \frac{10\text{ V}}{2\text{ k}\Omega} = 10\text{ mA}$

Eq. (2.3): $V_D = E|_{I_D=0\text{ A}} = 10\text{ V}$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the Q-point as

$$V_{D_Q} \cong \mathbf{0.78\text{ V}}$$

$$I_{D_Q} \cong \mathbf{9.25\text{ mA}}$$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

(b) $V_R = I_R R = I_{D_Q} R = (9.25\text{ mA})(1\text{ k}\Omega) = \mathbf{9.25\text{ V}}$

or $V_R = E - V_D = 10\text{ V} - 0.78\text{ V} = \mathbf{9.22\text{ V}}$

The difference in results is due to the accuracy with which the graph can be read. Ideally, the results obtained either way should be the same.

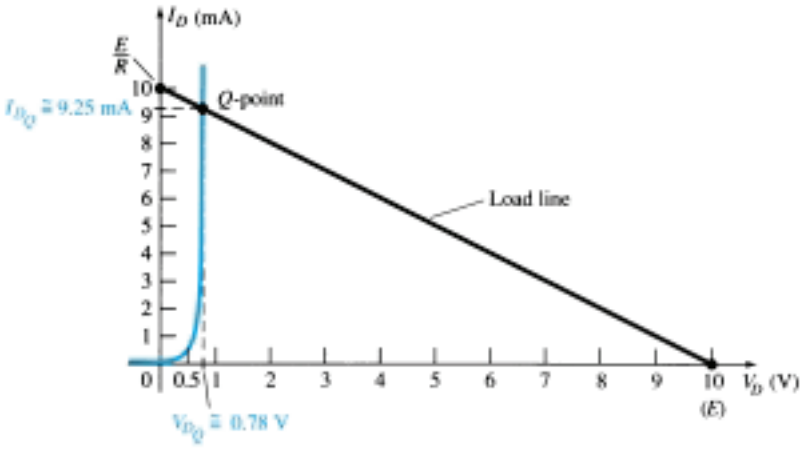


Figure 2.4 Solution to Example 2.1.

EXAMPLE 2.2

Repeat the analysis of Example 2.1 with $R = 2\text{ k}\Omega$.

Solution

(a) Eq. (2.2): $I_D = \left.\frac{E}{R}\right|_{V_D=0\text{ V}} = \frac{10\text{ V}}{2\text{ k}\Omega} = 5\text{ mA}$

Eq. (2.3): $V_D = E|_{I_D=0\text{ A}} = 10\text{ V}$

The resulting load line appears in Fig. 2.5. Note the reduced slope and levels of diode current for increasing loads. The resulting Q-point is defined by

$$V_{D_Q} \cong \mathbf{0.7\text{ V}}$$

$$I_{D_Q} \cong \mathbf{4.6\text{ mA}}$$

(b) $V_R = I_R R = I_{D_Q} R = (4.6\text{ mA})(2\text{ k}\Omega) = \mathbf{9.2\text{ V}}$

with $V_R = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$

The difference in levels is again due to the accuracy with which the graph can be read. Certainly, however, the results provide an expected magnitude for the voltage V_R.

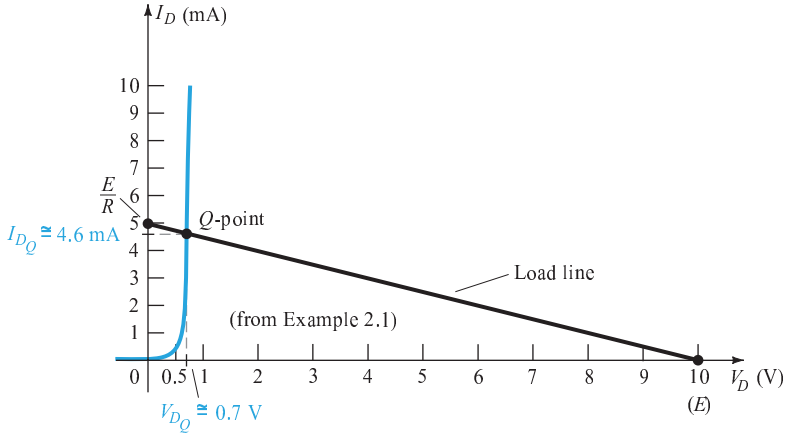


Figure 2.5 Solution to Example 2.2.

As noted in the examples above, the load line is determined solely by the applied network while the characteristics are defined by the chosen device. If we turn to our approximate model for the diode and do not disturb the network, the load line will be exactly the same as obtained in the examples above. In fact, the next two examples repeat the analysis of Examples 2.1 and 2.2 using the approximate model to permit a comparison of the results.

EXAMPLE 2.3

Repeat Example 2.1 using the approximate equivalent model for the silicon semiconductor diode.

Solution

The load line is redrawn as shown in Fig. 2.6 with the same intersections as defined in Example 2.1. The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting *Q*-point:

$$V_{D_Q} = \mathbf{0.7\ V}$$

$$I_{D_Q} = \mathbf{9.25\ mA}$$

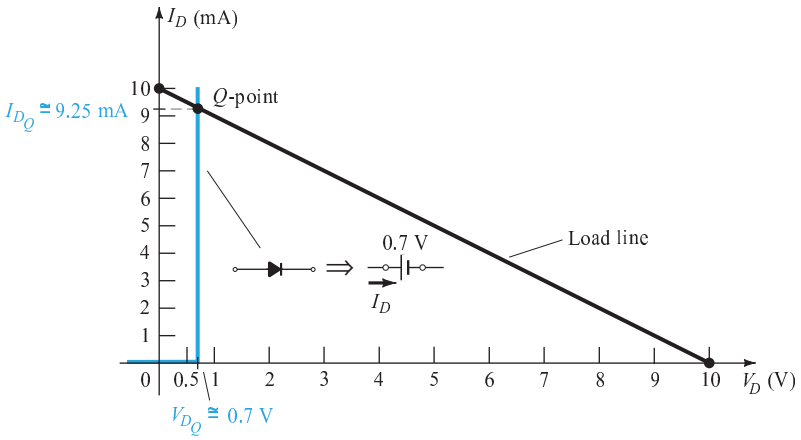


Figure 2.6 Solution to Example 2.1 using the diode approximate model.

The results obtained in Example 2.3 are quite interesting. The level of I_{D_Q} is exactly the same as obtained in Example 2.1 using a characteristic curve that is a great deal easier to draw than that appearing in Fig. 2.4. The level of $V_D = 0.7$ V versus 0.78 V from Example 2.1 is of a different magnitude to the hundredths place, but they are certainly in the same neighborhood if we compare their magnitudes to the magnitudes of the other voltages of the network.

EXAMPLE 2.4

Repeat Example 2.2 using the approximate equivalent model for the silicon semiconductor diode.

Solution

The load line is redrawn as shown in Fig. 2.7 with the same intersections defined in Example 2.2. The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting Q-point:

$$V_{D_Q} = \mathbf{0.7\ V}$$

$$I_{D_Q} = \mathbf{4.6\ mA}$$

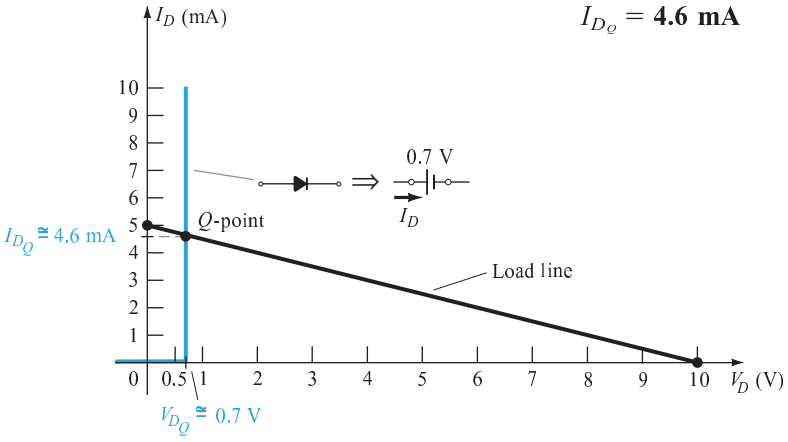


Figure 2.7 Solution to Example 2.2 using the diode approximate model.

In Example 2.4 the results obtained for both V_{D_Q} and I_{D_Q} are the same as those obtained using the full characteristics in Example 2.2. The examples above have demonstrated that the current and voltage levels obtained using the approximate model have been very close to those obtained using the full characteristics. It suggests, as will be applied in the sections to follow, that the use of appropriate approximations can result in solutions that are very close to the actual response with a reduced level of concern about properly reproducing the characteristics and choosing a large-enough scale. In the next example we go a step further and substitute the ideal model. The results will reveal the conditions that must be satisfied to apply the ideal equivalent properly.

EXAMPLE 2.4

Repeat Example 2.1 using the ideal diode model.

Solution

As shown in Fig. 2.8 the load line continues to be the same, but the ideal characteristics now intersect the load line on the vertical axis. The Q-point is therefore defined by

$$V_{D_Q} = \mathbf{0\ V}$$

$$I_{D_Q} = \mathbf{10\ mA}$$

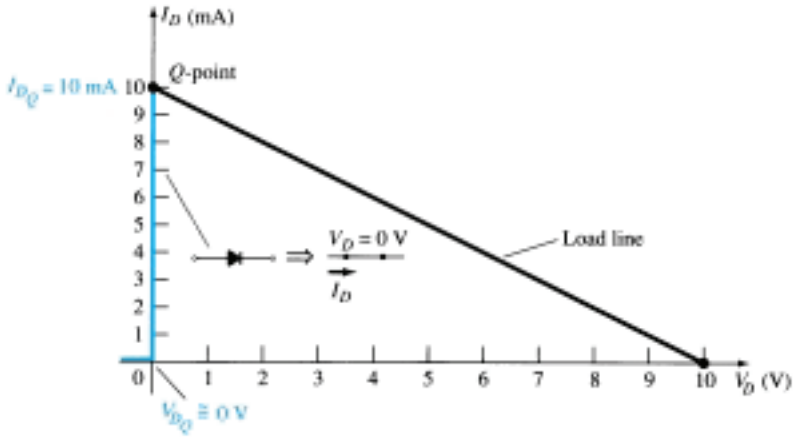


Figure 2.8 Solution to Example 2.1 using the ideal diode model.

The results are sufficiently different from the solutions of Example 2.1 to cause some concern about their accuracy. Certainly, they do provide some indication of the level of voltage and current to be expected relative to the other voltage levels of the network, but the additional effort of simply including the 0.7-V offset suggests that the approach of Example 2.3 is more appropriate.

Use of the ideal diode model therefore should be reserved for those occasions when the role of a diode is more important than voltage levels that differ by tenths of a volt and in those situations where the applied voltages are considerably larger than the threshold voltage V_T. In the next few sections the approximate model will be employed exclusively since the voltage levels obtained will be sensitive to variations that approach V_T. In later sections the ideal model will be employed more frequently since the applied voltages will frequently be quite a bit larger than V_T and the authors want to ensure that the role of the diode is correctly and clearly understood.

2.3 DIODE APPROXIMATIONS

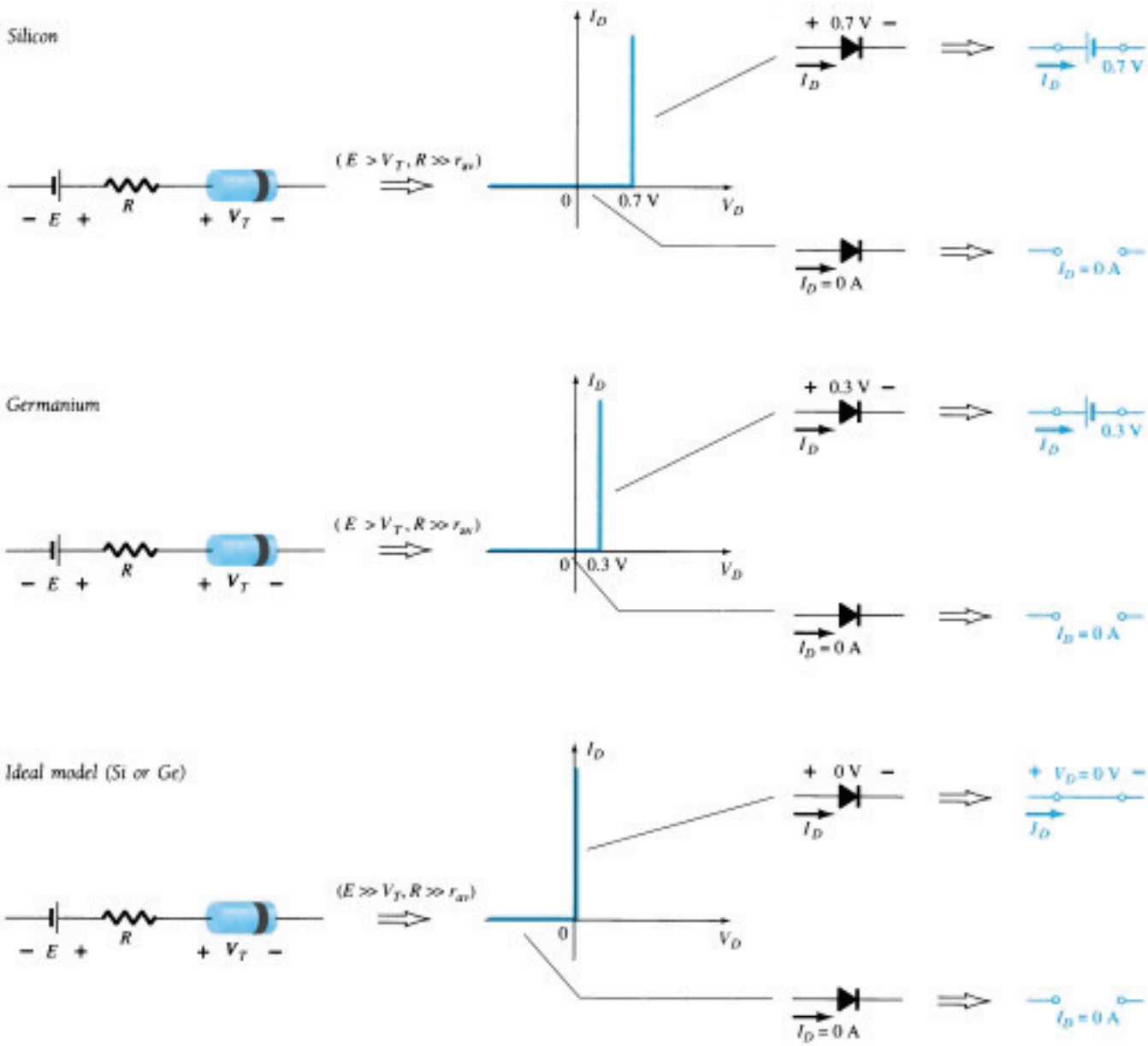
In Section 2.2 we revealed that the results obtained using the approximate piecewise-linear equivalent model were quite close, if not equal, to the response obtained using the full characteristics. In fact, if one considers all the variations possible due to tolerances, temperature, and so on, one could certainly consider one solution to be "as accurate" as the other. Since the use of the approximate model normally results in a reduced expenditure of time and effort to obtain the desired results, it is the approach that will be employed in this book unless otherwise specified. Recall the following:

The primary purpose of this book is to develop a general knowledge of the behavior, capabilities, and possible areas of application of a device in a manner that will minimize the need for extensive mathematical developments.

The complete piecewise-linear equivalent model introduced in Chapter 1 was not employed in the load-line analysis because r_{av} is typically much less than the other series elements of the network. If r_{av} should be close in magnitude to the other series elements of the network, the complete equivalent model can be applied in much the same manner as described in Section 2.2.

In preparation for the analysis to follow, Table 2.1 was developed to review the important characteristics, models, and conditions of application for the approximate and ideal diode models. Although the silicon diode is used almost exclusively due to

TABLE 2.1 Approximate and Ideal Semiconductor Diode Models



its temperature characteristics, the germanium diode is still employed and is therefore included in Table 2.1. As with the silicon diode, a germanium diode is approximated by an open-circuit equivalent for voltages less than V_T. It will enter the "on" state when $V_D \geq V_T = 0.3$ V.

Keep in mind that the 0.7 and 0.3 V in the equivalent circuits are not *independent* sources of energy but are there simply to remind us that there is a "price to pay" to turn on a diode. An isolated diode on a laboratory table will not indicate 0.7 or 0.3 V if a voltmeter is placed across its terminals. The supplies specify the voltage drop across each when the device is "on" and specify that the diode voltage must be at least the indicated level before conduction can be established.

In the next few sections we demonstrate the impact of the models of Table 2.1 on the analysis of diode configurations. For those situations where the approximate equivalent circuit will be employed, the diode symbol will appear as shown in Fig. 2.9a for the silicon and germanium diodes. If conditions are such that the ideal diode model can be employed, the diode symbol will appear as shown in Fig. 2.9b.

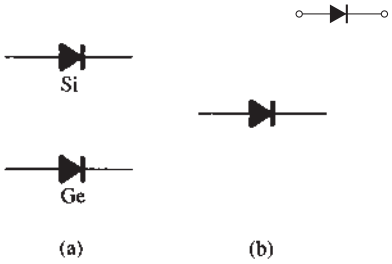


Figure 2.9 (a) Approximate model notation; (b) ideal diode notation.

2.4 SERIES DIODE CONFIGURATIONS WITH DC INPUTS

In this section the approximate model is utilized to investigate a number of series diode configurations with dc inputs. The content will establish a foundation in diode analysis that will carry over into the sections and chapters to follow. The procedure described can, in fact, be applied to networks with any number of diodes in a variety of configurations.

For each configuration the state of each diode must first be determined. Which diodes are "on" and which are "off"? Once determined, the appropriate equivalent as defined in Section 2.3 can be substituted and the remaining parameters of the network determined.

In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D \geq 0.7$ V for silicon and $V_D \geq 0.3$ V for germanium.

For each configuration, *mentally* replace the diodes with resistive elements and note the resulting current direction as established by the applied voltages ("pressure"). If the resulting direction is a "match" with the arrow in the diode symbol, conduction through the diode will occur and the device is in the "on" state. The description above is, of course, contingent on the supply having a voltage greater than the "turn-on" voltage (V_T) of each diode.

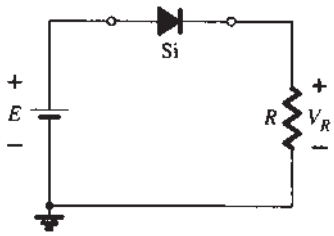


Figure 2.10 Series diode configuration.

If a diode is in the "on" state, one can either place a 0.7-V drop across the element, or the network can be redrawn with the V_T equivalent circuit as defined in Table 2.1. In time the preference will probably simply be to include the 0.7-V drop across each "on" diode and draw a line through each diode in the "off" or open state. Initially, however, the substitution method will be utilized to ensure that the proper voltage and current levels are determined.

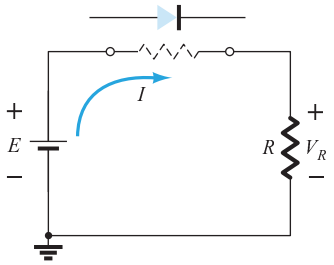


Figure 2.11 Determining the state of the diode of Fig. 2.10.

The series circuit of Fig. 2.10 described in some detail in Section 2.2 will be used to demonstrate the approach described in the paragraphs above. The state of the diode is first determined by mentally replacing the diode with a resistive element as shown in Fig. 2.11. The resulting direction of I is a match with the arrow in the diode symbol, and since $E > V_T$ the diode is in the "on" state. The network is then redrawn as shown in Fig. 2.12 with the appropriate equivalent model for the forward-biased silicon diode. Note for future reference that the polarity of V_D is the same as would result if in fact the diode were a resistive element. The resulting voltage and current levels are the following:

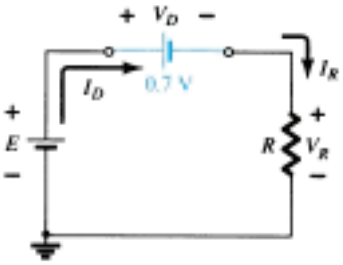


Figure 2.12 Substituting the equivalent model for the "on" diode of Fig. 2.10.

$$V_D = V_T \tag{2.4}$$

$$V_R = E - V_T \tag{2.5}$$

$$I_D = I_R = \frac{V_R}{R} \tag{2.6}$$

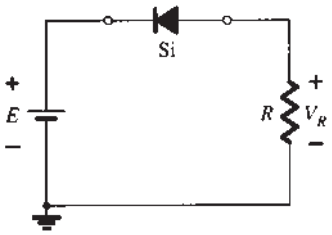


Figure 2.13 Reversing the diode of Fig. 2.10.

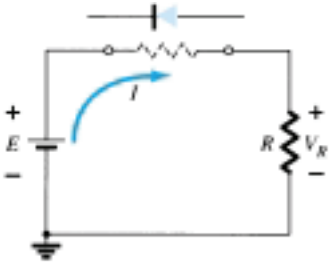


Figure 2.14 Determining the state of the diode of Fig. 2.13.

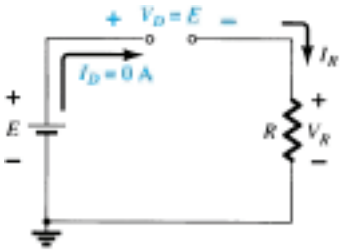


Figure 2.15 Substituting the equivalent model for the "off" diode of Figure 2.13.

In Fig. 2.13 the diode of Fig. 2.10 has been reversed. Mentally replacing the diode with a resistive element as shown in Fig. 2.14 will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.15. Due to the open circuit, the diode current is 0 A and the voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = (0\text{ A})R = \mathbf{0\text{ V}}$$

The fact that $V_R = 0$ V will establish E volts across the open circuit as defined by Kirchhoff's voltage law. Always keep in mind that under any circumstances—dc, ac instantaneous values, pulses, and so on—Kirchhoff's voltage law must be satisfied!

EXAMPLE 2.6

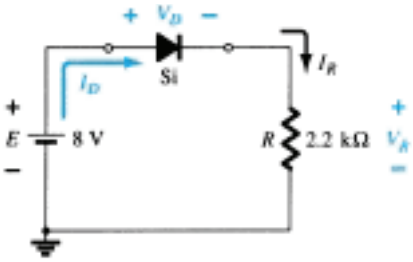


Figure 2.16 Circuit for Example 2.6.

For the series diode configuration of Fig. 2.16, determine V_D, V_R, and I_D.

Solution

Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = \mathbf{0.7\text{ V}}$$

$$V_R = E - V_D = 8\text{ V} - 0.7\text{ V} = \mathbf{7.3\text{ V}}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{3.32\text{ mA}}$$

EXAMPLE 2.7

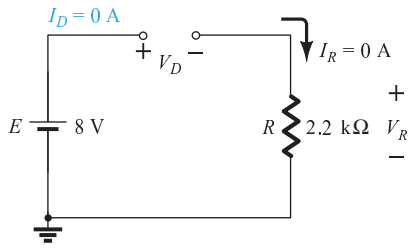


Figure 2.17 Determining the unknown quantities for Example 2.7.

Repeat Example 2.6 with the diode reversed.

Solution

Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of Fig. 2.17, where $I_D = \mathbf{0\text{ A}}$ due to the open circuit. Since $V_R = I_R R$, $V_R = (0)R = 0$ V. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$

and

$$V_D = E - V_R = E - 0 = E = \mathbf{8\text{ V}}$$

In particular, note in Example 2.7 the high voltage across the diode even though it is an "off" state. The current is zero, but the voltage is significant. For review purposes, keep the following in mind for the analysis to follow:

1. An open circuit can have any voltage across its terminals, but the current is always 0 A.
2. A short circuit has a 0-V drop across its terminals, but the current is limited only by the surrounding network.

In the next example the notation of Fig. 2.18 will be employed for the applied voltage. It is a common industry notation and one with which the reader should become very familiar. Such notation and other defined voltage levels are treated further in Chapter 4.

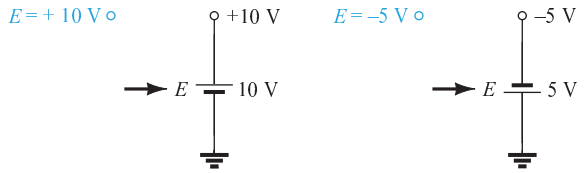


Figure 2.18 Source notation.

EXAMPLE 2.8

For the series diode configuration of Fig. 2.19, determine V_D, V_R, and I_D.

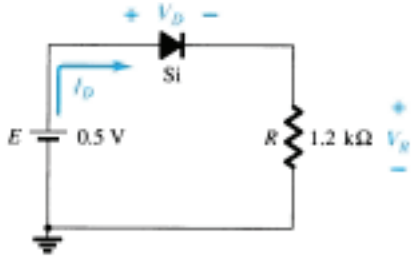


Figure 2.19 Series diode circuit for Example 2.8.

Solution

Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.20, establishing the open-circuit equivalent as the appropriate approximation. The resulting voltage and current levels are therefore the following:

$$I_D = \mathbf{0\ A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})1.2\ \text{k}\Omega = \mathbf{0\ V}$$

and

$$V_D = E = \mathbf{0.5\ V}$$

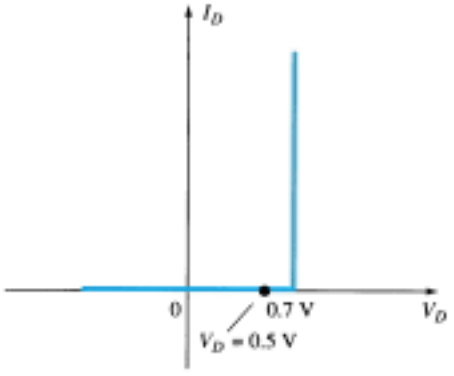


Figure 2.20 Operating point with $E = 0.5$ V.

EXAMPLE 2.9

Determine V_o and I_D for the series circuit of Fig. 2.21.

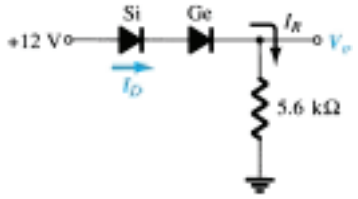


Figure 2.21 Circuit for Example 2.9.

Solution

An attack similar to that applied in Example 2.6 will reveal that the resulting current has the same direction as the arrowheads of the symbols of both diodes, and the network of Fig. 2.22 results because $E = 12\text{ V} > (0.7\text{ V} + 0.3\text{ V}) = 1\text{ V}$. Note the redrawn supply of 12 V and the polarity of V_o across the 5.6-kΩ resistor. The resulting voltage

$$V_o = E - V_{T_1} - V_{T_2} = 12\text{ V} - 0.7\text{ V} - 0.3\text{ V} = \mathbf{11\text{ V}}$$

and

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{11\text{ V}}{5.6\text{ k}\Omega} \cong \mathbf{1.96\text{ mA}}$$

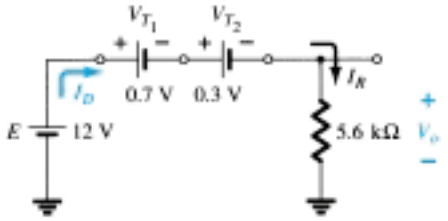


Figure 2.22 Determining the unknown quantities for Example 2.9.

EXAMPLE 2.10

Determine I_D, V_{D_2}, and V_o for the circuit of Fig. 2.23.

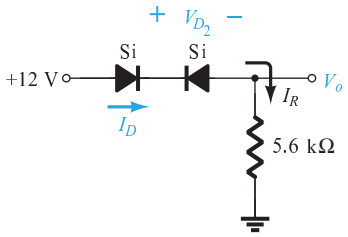


Figure 2.23 Circuit for Example 2.10.

Solution

Removing the diodes and determining the direction of the resulting current I will result in the circuit of Fig. 2.24. There is a match in current direction for the silicon diode but not for the germanium diode. The combination of a short circuit in series with an open circuit always results in an open circuit and $I_D = \mathbf{0\text{ A}}$, as shown in Fig. 2.25.

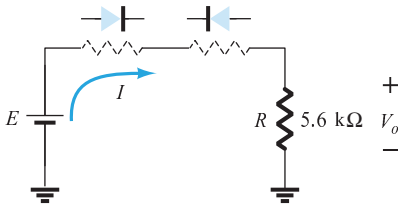


Figure 2.24 Determining the state of the diodes of Figure 2.23.

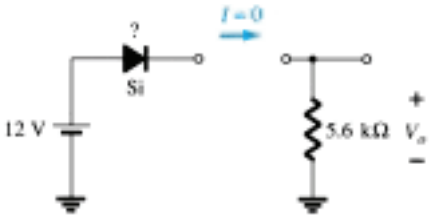


Figure 2.25 Substituting the equivalent state for the open diode.

The question remains as to what to substitute for the silicon diode. For the analysis to follow in this and succeeding chapters, simply recall for the actual practical diode that when $I_D = 0$ A, $V_D = 0$ V (and vice versa), as described for the no-bias situation in Chapter 1. The conditions described by $I_D = 0$ A and $V_{D_1} = 0$ V are indicated in Fig. 2.26.

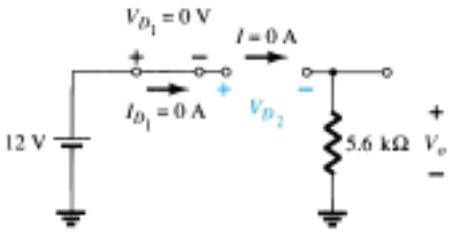


Figure 2.26 Determining the unknown quantities for the circuit of Example 2.10.

$$V_o = I_R R = I_D R = (0 \text{ A})R = 0 \text{ V}$$

and
$$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{12\ V}$$

Applying Kirchhoff's voltage law in a clockwise direction gives us

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

and
$$V_{D_2} = E - V_{D_1} - V_o = 12 \text{ V} - 0 - 0$$
$$= \mathbf{12\ V}$$

with
$$V_o = \mathbf{0\ V}$$

Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.27. *EXAMPLE 2.11*

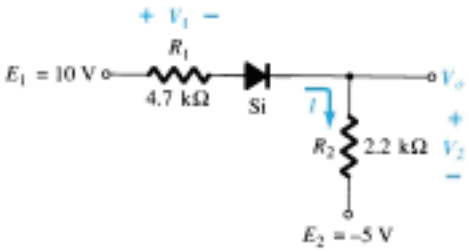


Figure 2.27 Circuit for Example 2.11.

Solution

The sources are drawn and the current direction indicated as shown in Fig. 2.28. The diode is in the "on" state and the notation appearing in Fig. 2.29 is included to indicate this state. Note that the "on" state is noted simply by the additional $V_D = 0.7$ V

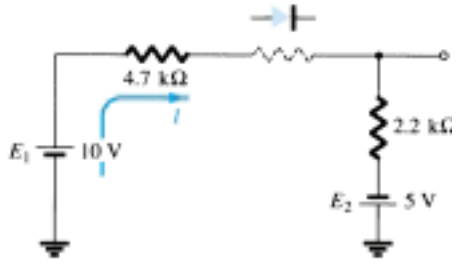


Figure 2.28 Determining the state of the diode for the network of Fig. 2.27.

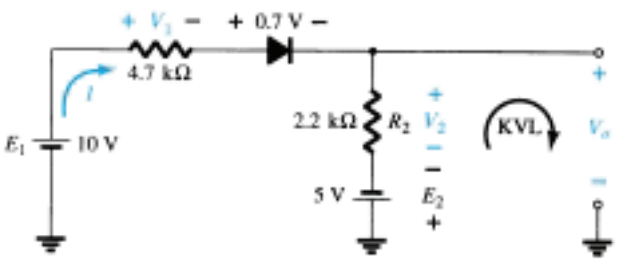


Figure 2.29 Determining the unknown quantities for the network of Fig. 2.27.

on the figure. This eliminates the need to redraw the network and avoids any confusion that may result from the appearance of another source. As indicated in the introduction to this section, this is probably the path and notation that one will take when a level of confidence has been established in the analysis of diode configurations. In time the entire analysis will be performed simply by referring to the original network. Recall that a reverse-biased diode can simply be indicated by a line through the device.

The resulting current through the circuit is,

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\text{ V} + 5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{14.3\text{ V}}{6.9\text{ k}\Omega}$$

$$\cong \mathbf{2.072\ mA}$$

and the voltages are

$$V_1 = IR_1 = (2.072\text{ mA})(4.7\text{ k}\Omega) = \mathbf{9.74\ V}$$

$$V_2 = IR_2 = (2.072\text{ mA})(2.2\text{ k}\Omega) = \mathbf{4.56\ V}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction will result in

$$-E_2 + V_2 - V_o = 0$$

and

$$V_o = V_2 - E_2 = 4.56\text{ V} - 5\text{ V} = \mathbf{-0.44\ V}$$

The minus sign indicates that V_o has a polarity opposite to that appearing in Fig. 2.27.

2.5 PARALLEL AND SERIES–PARALLEL CONFIGURATIONS

The methods applied in Section 2.4 can be extended to the analysis of parallel and series–parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

EXAMPLE 2.12

Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration of Fig. 2.30.

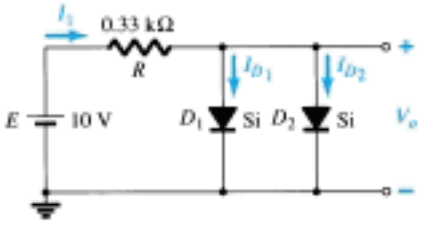


Figure 2.30 Network for Example 2.12.

Solution

For the applied voltage the "pressure" of the source is to establish a current through each diode in the same direction as shown in Fig. 2.31. Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always the same and

$$V_o = \mathbf{0.7\ V}$$

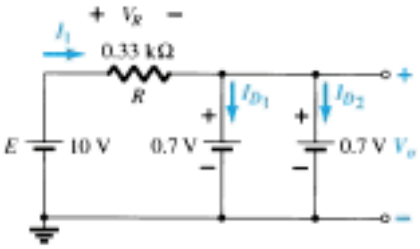


Figure 2.31 Determining the unknown quantities for the network of Example 2.12.

The current

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = \mathbf{28.18\text{ mA}}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = \mathbf{14.09\text{ mA}}$$

Example 2.12 demonstrated one reason for placing diodes in parallel. If the current rating of the diodes of Fig. 2.30 is only 20 mA, a current of 28.18 mA would damage the device if it appeared alone in Fig. 2.30. By placing two in parallel, the current is limited to a safe value of 14.09 mA with the same terminal voltage.

EXAMPLE 2.13

Determine the current I for the network of Fig. 2.32.

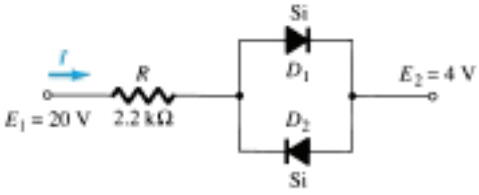


Figure 2.32 Network for Example 2.13.

Solution

Redrawing the network as shown in Fig. 2.33 reveals that the resulting current direction is such as to turn on diode D_1 and turn off diode D_2. The resulting current I is then

$$I = \frac{E_1 - E_2 - V_D}{R} = \frac{20\text{ V} - 4\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{6.95\text{ mA}}$$

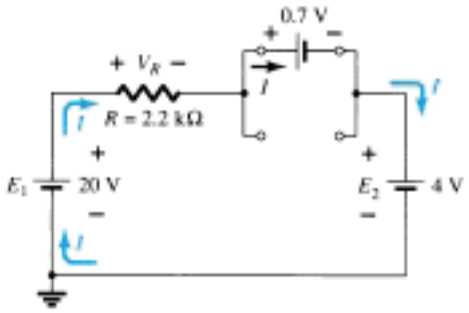


Figure 2.33 Determining the unknown quantities for the network of Example 2.13.

EXAMPLE 2.14

Determine the voltage V_o for the network of Fig. 2.34.

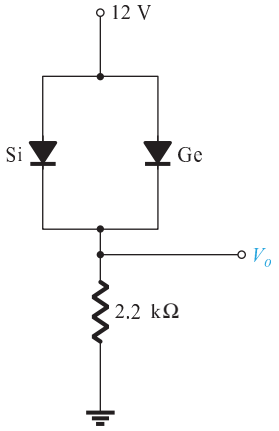


Figure 2.34 Network for Example 2.14.

Solution

Initially, it would appear that the applied voltage will turn both diodes "on." However, if both were "on," the 0.7-V drop across the silicon diode would not match the 0.3 V across the germanium diode as required by the fact that the voltage across parallel elements must be the same. The resulting action can be explained simply by realizing that when the supply is turned on it will increase from 0 to 12 V over a period of time—although probably measurable in milliseconds. At the instant during the rise that 0.3 V is established across the germanium diode it will turn "on" and maintain a level of 0.3 V. The silicon diode will never have the opportunity to capture its required 0.7 V and therefore remains in its open-circuit state as shown in Fig. 2.35. The result:

$$V_o = 12\text{ V} - 0.3\text{ V} = \mathbf{11.7\text{ V}}$$

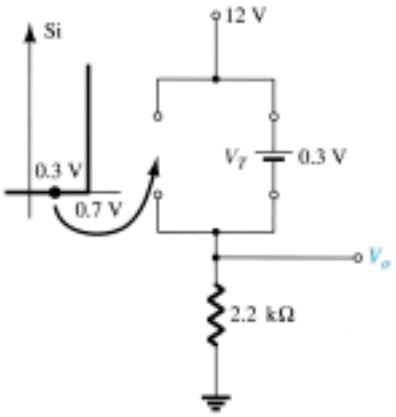


Figure 2.35 Determining V_o for the network of Fig. 2.34.

EXAMPLE 2.15

Determine the currents I_1, I_2, and I_{D_2} for the network of Fig. 2.36.

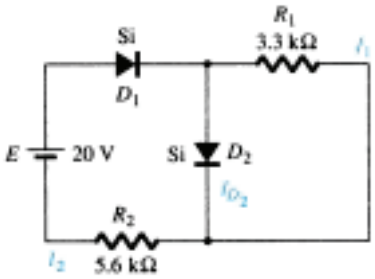


Figure 2.36 Network for Example 2.15.

Solution

The applied voltage (pressure) is such as to turn both diodes on, as noted by the resulting current directions in the network of Fig. 2.37. Note the use of the abbreviated notation for "on" diodes and that the solution is obtained through an application of techniques applied to dc series—parallel networks.

$$I_1 = \frac{V_{T_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

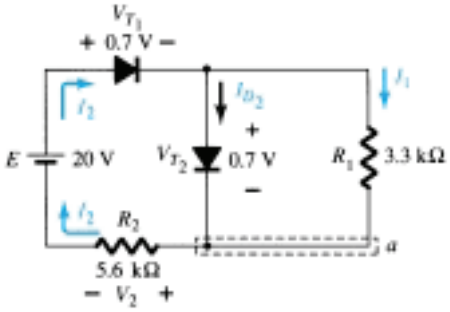


Figure 2.37 Determining the unknown quantities for Example 2.15.

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{T_1} - V_{T_2} = 0$$

and

$$V_2 = E - V_{T_1} - V_{T_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = 18.6\text{ V}$$

with

$$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

At the bottom node (a),

$$I_{D_2} + I_1 = I_2$$

and

$$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} = \mathbf{3.108\text{ mA}}$$

2.6 AND/OR GATES

The tools of analysis are now at our disposal, and the opportunity to investigate a computer configuration is one that will demonstrate the range of applications of this relatively simple device. Our analysis will be limited to determining the voltage levels and will not include a detailed discussion of Boolean algebra or positive and negative logic.

The network to be analyzed in Example 2.16 is an OR gate for positive logic. That is, the 10-V level of Fig. 2.38 is assigned a "1" for Boolean algebra while the 0-V input is assigned a "0." An OR gate is such that the output voltage level will be a 1 if either *or* both inputs is a 1. The output is a 0 if both inputs are at the 0 level.

The analysis of AND/OR gates is made measurably easier by using the approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7 V positive for the silicon diode (0.3 V for Ge) to switch to the "on" state.

In general, the best approach is simply to establish a "gut" feeling for the state of the diodes by noting the direction and the "pressure" established by the applied potentials. The analysis will then verify or negate your initial assumptions.

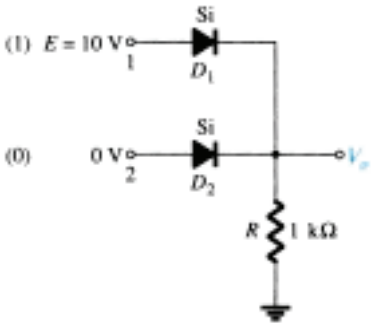


Figure 2.38 Positive logic OR gate.

EXAMPLE 2.16

Determine V_o for the network of Fig. 2.38.

Solution

First note that there is only one applied potential; 10 V at terminal 1. Terminal 2 with a 0-V input is essentially at ground potential, as shown in the redrawn network of Fig. 2.39. Figure 2.39 "suggests" that D_1 is probably in the "on" state due to the applied 10 V while D_2 with its "positive" side at 0 V is probably "off." Assuming these states will result in the configuration of Fig. 2.40.

The next step is simply to check that there is no contradiction to our assumptions. That is, note that the polarity across D_1 is such as to turn it on and the polarity across D_2 is such as to turn it off. For D_1 the "on" state establishes V_o at $V_o = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$. With 9.3 V at the cathode (−) side of D_2 and 0 V at the anode (+) side, D_2 is definitely in the "off" state. The current direction and the resulting continuous path for conduction further confirm our assumption that D_1 is conducting. Our assumptions seem confirmed by the resulting voltages and current, and our initial analysis can be assumed to be correct. The output voltage level is not 10 V as defined for an input of 1, but the 9.3 V is sufficiently large to be considered a 1 level. The output is therefore at a 1 level with only one input, which suggests that

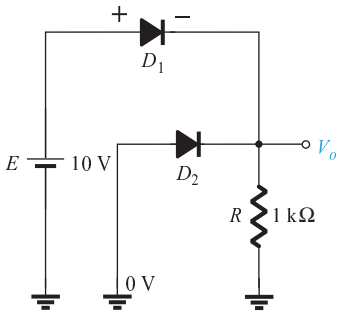


Figure 2.39 Redrawn network of Fig. 2.38.

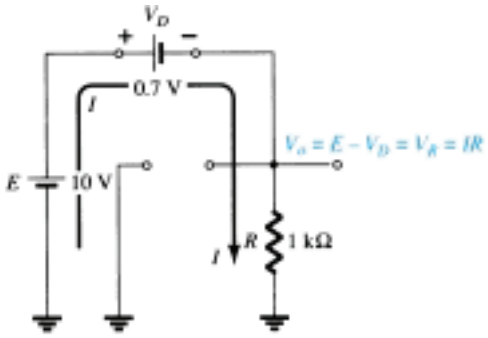


Figure 2.40 Assumed diode states for Fig. 2.38.

the gate is an OR gate. An analysis of the same network with two 10-V inputs will result in both diodes being in the "on" state and an output of 9.3 V. A 0-V input at both inputs will not provide the 0.7 V required to turn the diodes on, and the output will be a 0 due to the 0-V output level. For the network of Fig. 2.40 the current level is determined by

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

EXAMPLE 2.17

Determine the output level for the positive logic AND gate of Fig. 2.41.

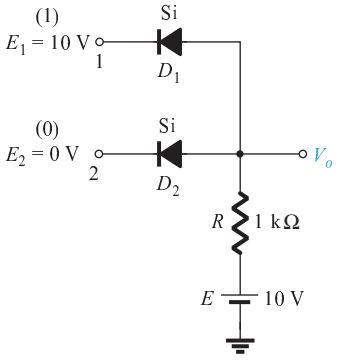


Figure 2.41 Positive logic AND gate.

Solution

Note in this case that an independent source appears in the grounded leg of the network. For reasons soon to become obvious it is chosen at the same level as the input logic level. The network is redrawn in Fig. 2.42 with our initial assumptions regarding the state of the diodes. With 10 V at the cathode side of D_1 it is assumed that D_1 is in the "off" state even though there is a 10-V source connected to the anode of D_1 through the resistor. However, recall that we mentioned in the introduction to this section that the use of the approximate model will be an aid to the analysis. For D_1, where will the 0.7 V come from if the input and source voltages are at the same level and creating opposing "pressures"? D_2 is assumed to be in the "on" state due to the low voltage at the cathode side and the availability of the 10-V source through the 1-kΩ resistor.

For the network of Fig. 2.42 the voltage at V_o is 0.7 V due to the forward-biased diode D_2. With 0.7 V at the anode of D_1 and 10 V at the cathode, D_1 is definitely in the "off" state. The current I will have the direction indicated in Fig. 2.42 and a magnitude equal to

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

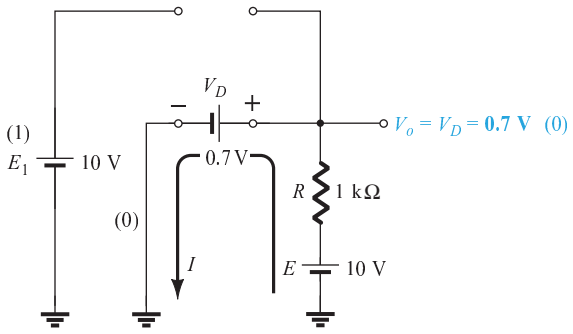


Figure 2.42 Substituting the assumed states for the diodes of Fig. 2.41.

The state of the diodes is therefore confirmed and our earlier analysis was correct. Although not 0 V as earlier defined for the 0 level, the output voltage is sufficiently small to be considered a 0 level. For the AND gate, therefore, a single input will result in a 0-level output. The remaining states of the diodes for the possibilities of two inputs and no inputs will be examined in the problems at the end of the chapter.

2.7 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. There is no question that the degree of difficulty will increase, but once a few fundamental maneuvers are understood, the analysis will be fairly direct and follow a common thread.

The simplest of networks to examine with a time-varying signal appears in Fig. 2.43. For the moment we will use the ideal model (note the absence of the Si or Ge label to denote ideal diode) to ensure that the approach is not clouded by additional mathematical complexity.

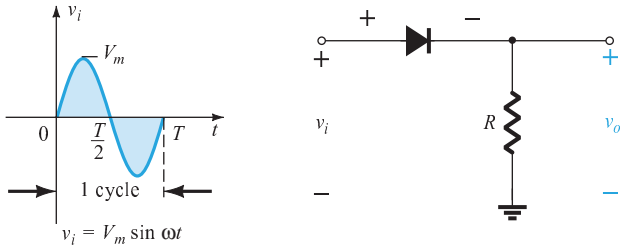


Figure 2.43 Half-wave rectifier.

Over one full cycle, defined by the period T of Fig. 2.43, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Fig. 2.43, called a *half-wave rectifier,* will generate a waveform v_o that will have an average value of particular, use in the ac-to-dc conversion process. When employed in the rectification process, a diode is typically referred to as a *rectifier.* Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems.

During the interval $t = 0 \rightarrow T/2$ in Fig. 2.43 the polarity of the applied voltage v_i is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.44, where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode.

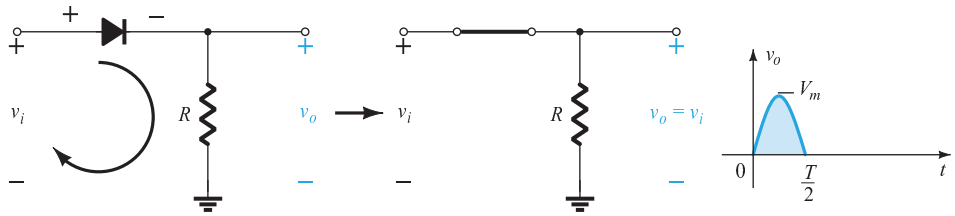


Figure 2.44 Conduction region ($0 \rightarrow T/2$).

For the period $T/2 \rightarrow T$, the polarity of the input v_i is as shown in Fig. 2.45 and the resulting polarity across the ideal diode produces an "off" state with an open-circuit equivalent. The result is the absence of a path for charge to flow and $v_o = iR = (0)R = 0$ V for the period $T/2 \rightarrow T$. The input v_i and the output v_o were sketched together in Fig. 2.46 for comparison purposes. The output signal v_o now has a net positive area above the axis over a full period and an average value determined by

$$V_{dc} = 0.318V_m \quad \text{half-wave} \tag{2.7}$$

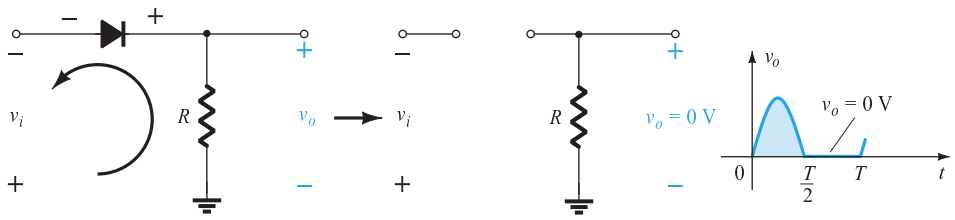


Figure 2.45 Nonconduction region ($T/2 \rightarrow T$).

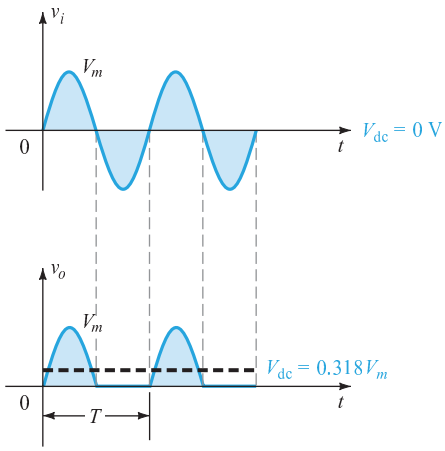


Figure 2.46 Half-wave rectified signal.

The process of removing one-half the input signal to establish a dc level is aptly called *half-wave rectification.*

The effect of using a silicon diode with $V_T = 0.7$ V is demonstrated in Fig. 2.47 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7 V, the diode is still in an open-circuit state and $v_o = 0$ V as shown in the same figure. When conducting, the difference between v_o and v_i is a fixed level of $V_T = 0.7$ V and $v_o = v_i - V_T$, as shown in the figure. The net effect is a reduction in area above the axis, which naturally reduces

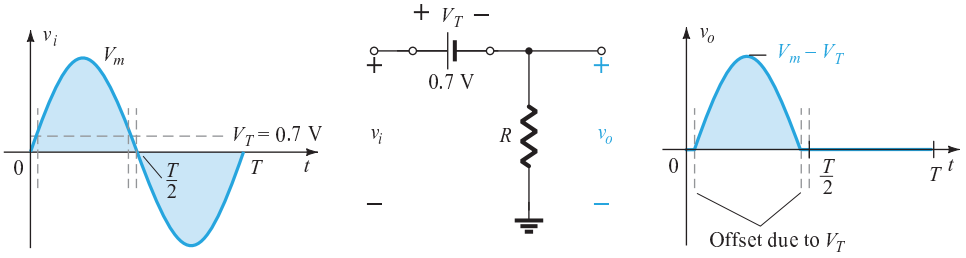


Figure 2.47 Effect of V_T on half-wave rectified signal.

the resulting dc voltage level. For situations where $V_m \gg V_T$, Eq. 2.8 can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_T) \tag{2.8}$$

In fact, if V_m is sufficiently greater than V_T, Eq. 2.7 is often applied as a first approximation for V_{dc}.

EXAMPLE 2.18

(a) Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.48.
(b) Repeat part (a) if the ideal diode is replaced by a silicon diode.
(c) Repeat parts (a) and (b) if V_m is increased to 200 V and compare solutions using Eqs. (2.7) and (2.8).

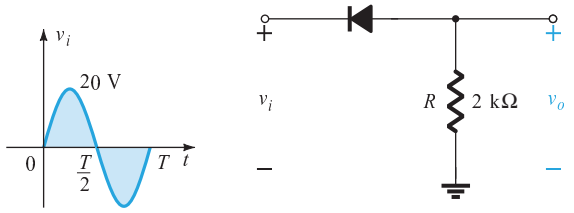


Figure 2.48 Network for Example 2.18.

Solution

(a) In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.49, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.48.

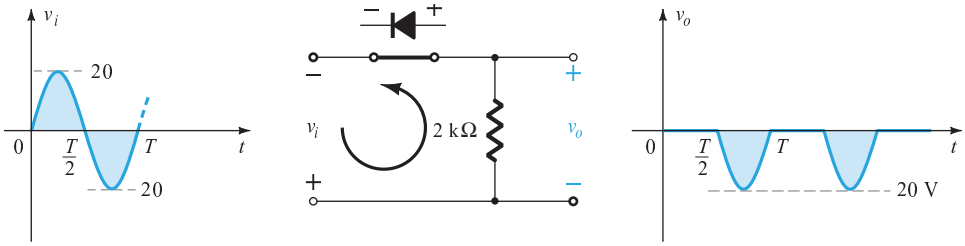


Figure 2.49 Resulting v_o for the circuit of Example 2.18.

(b) Using a silicon diode, the output has the appearance of Fig. 2.50 and

$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V or about 3.5%.

(c) Eq. (2.7): $V_{dc} = -0.318V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{dc} = -0.318(V_m - V_T) = -0.318(200\text{ V} - 0.7\text{ V})$

$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$

which is a difference that can certainly be ignored for most applications. For part c the offset and drop in amplitude due to V_T would not be discernible on a typical oscilloscope if the full pattern is displayed.

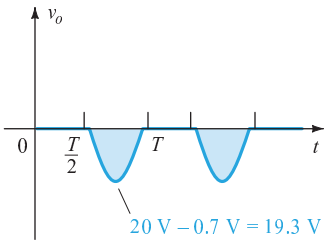


Figure 2.50 Effect of V_T on output of Fig. 2.49.

PIV (PRV)

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.51, which displays the reverse-biased diode of Fig. 2.43 with maximum applied voltage. Applying Kirchhoff's voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\text{PIV rating} \geqq V_m \quad \text{half-wave rectifier} \tag{2.9}$$

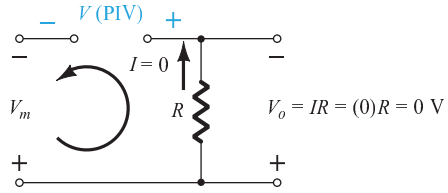


Figure 2.51 Determining the required PIV rating for the half-wave rectifier.

2.8 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Fig. 2.52 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.53. The resulting polarities across the ideal diodes are also shown in Fig. 2.53 to reveal that D_2 and D_3 are conducting while D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.54, with its indicated current and polarity across R. Since the diodes are ideal the load voltage is $v_o = v_i$, as shown in the same figure.

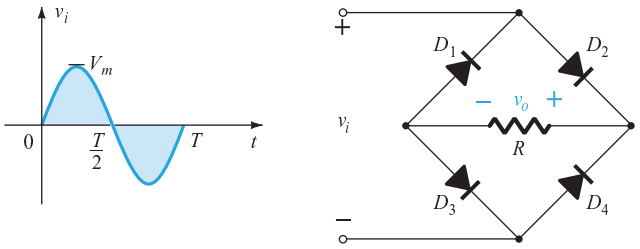


Figure 2.52 Full-wave bridge rectifier.

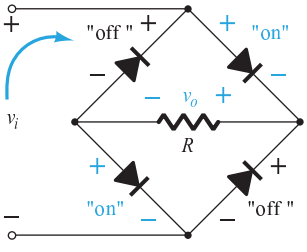


Figure 2.53 Network of Fig. 2.52 for the period $0 \rightarrow T/2$ of the input voltage v_i.

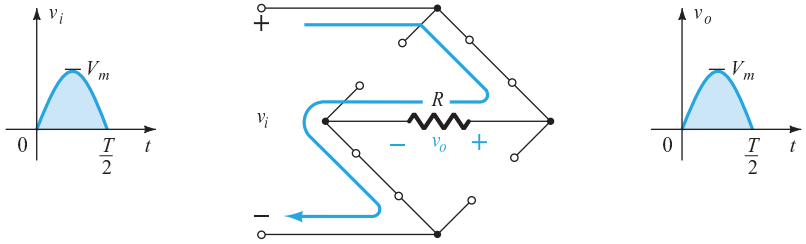


Figure 2.54 Conduction path for the positive region of v_i.

For the negative region of the input the conducting diodes are D_1 and D_4, resulting in the configuration of Fig. 2.55. The important result is that the polarity across the load resistor R is the same as in Fig. 2.53, establishing a second positive pulse, as shown in Fig. 2.55. Over one full cycle the input and output voltages will appear as shown in Fig. 2.56.

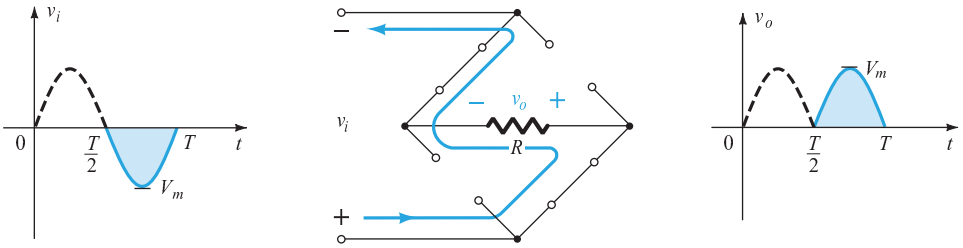


Figure 2.55 Conduction path for the negative region of v_i.

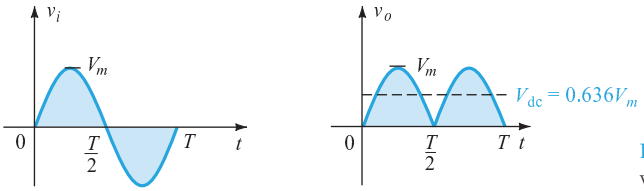


Figure 2.56 Input and output waveforms for a full-wave rectifier.

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2(\text{Eq. } 2.7) = 2(0.318V_m)$$

or

$$\boxed{V_{dc} = 0.636V_m} \quad \text{full-wave} \tag{2.10}$$

If silicon rather than ideal diodes are employed as shown in Fig. 2.57, an application of Kirchhoff's voltage law around the conduction path would result in

$$v_i - V_T - v_o - V_T = 0$$

and

$$v_o = v_i - 2V_T$$

The peak value of the output voltage v_o is therefore

$$V_{o_{max}} = V_m - 2V_T$$

For situations where $V_m \gg 2V_T$, Eq. (2.11) can be applied for the average value with a relatively high level of accuracy.

$$\boxed{V_{dc} \cong 0.636(V_m - 2V_T)} \tag{2.11}$$

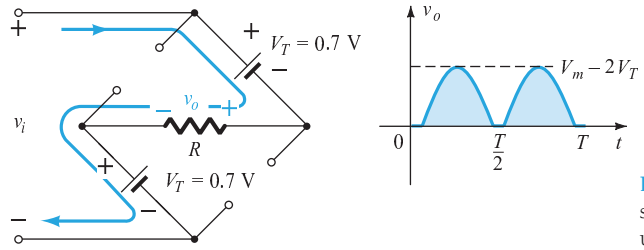


Figure 2.57 Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.

Then again, if V_m is sufficiently greater than $2V_T$, then Eq. (2.10) is often applied as a first approximation for V_{dc}.

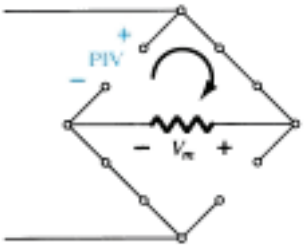


Figure 2.58 Determining the required PIV for the bridge configuration.

PIV

The required PIV of each diode (ideal) can be determined from Fig. 2.58 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V_m and the PIV rating is defined by

$$\text{PIV} \geqq V_m \quad \text{full-wave bridge rectifier} \tag{2.12}$$

Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.59 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in Fig. 2.60. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.60.

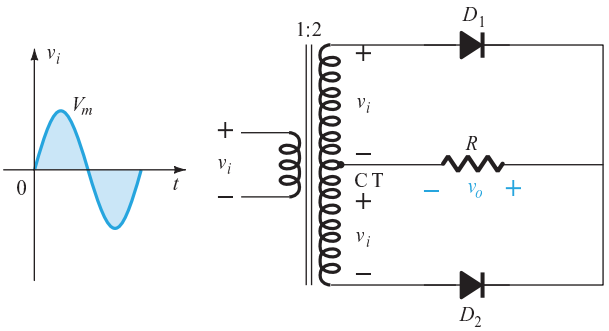


Figure 2.59 Center-tapped transformer full-wave rectifier.

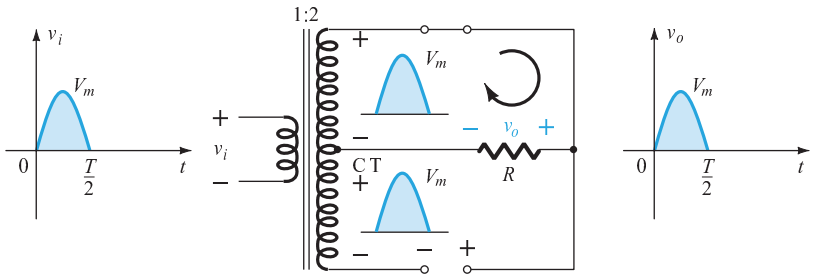


Figure 2.60 Network conditions for the positive region of v_i.

During the negative portion of the input the network appears as shown in Fig. 2.61, reversing the roles of the diodes but maintaining the same polarity for the volt-

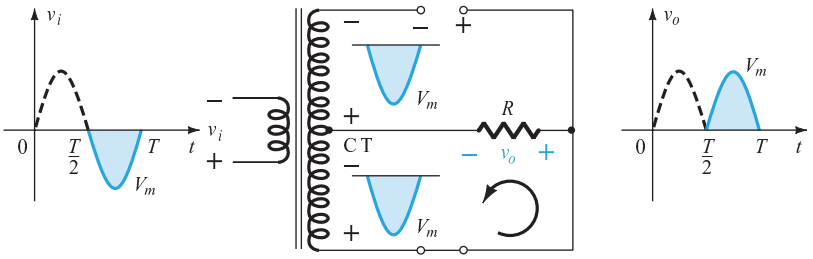


Figure 2.61 Network conditions for the negative region of v_i.

age across the load resistor R. The net effect is the same output as that appearing in Fig. 2.56 with the same dc levels.

PIV

The network of Fig. 2.62 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop will result in

$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

and

$$\boxed{\text{PIV} \geqq 2V_m} \quad \text{CT transformer, full-wave rectifier} \tag{2.13}$$

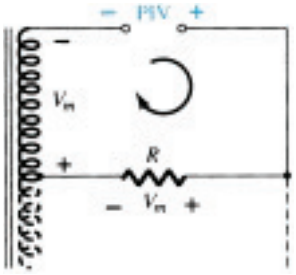


Figure 2.62 Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

EXAMPLE 2.19

Determine the output waveform for the network of Fig. 2.63 and calculate the output dc level and the required PIV of each diode.

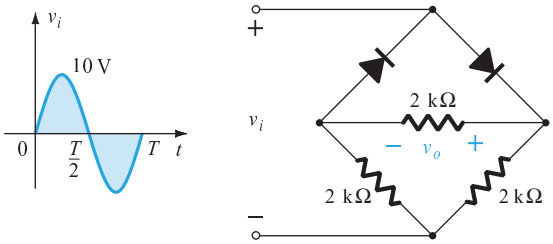


Figure 2.63 Bridge network for Example 2.19.

Solution

The network will appear as shown in Fig. 2.64 for the positive region of the input voltage. Redrawing the network will result in the configuration of Fig. 2.65, where $v_o = \frac{1}{2}v_i$ or $V_{o_{\max}} = \frac{1}{2}V_{i_{\max}} = \frac{1}{2}(10\text{ V}) = 5\text{ V}$, as shown in Fig. 2.65. For the negative part of the input the roles of the diodes will be interchanged and v_o will appear as shown in Fig. 2.66.

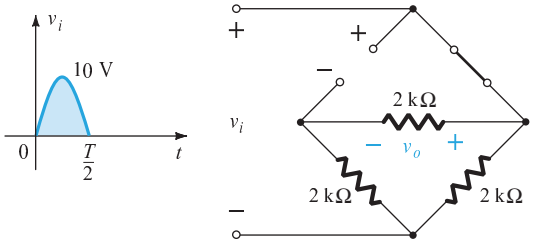


Figure 2.64 Network of Fig. 2.63 for the positive region of v_i.

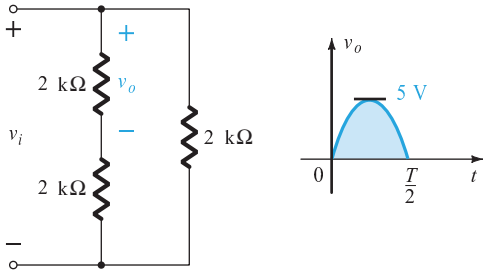


Figure 2.65 Redrawn network of Fig. 2.64.

The effect of removing two diodes from the bridge configuration was therefore to reduce the available dc level to the following:

$$V_{\text{dc}} = 0.636(5\text{ V}) = \mathbf{3.18\text{ V}}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.58 is equal to the maximum voltage across R, which is 5 V or half of that required for a half-wave rectifier with the same input.

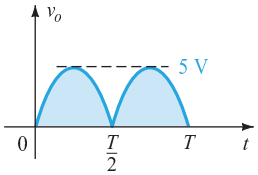


Figure 2.66 Resulting output for Example 2.19.

2.9 CLIPPERS

There are a variety of diode networks called *clippers* that have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform. The half-wave rectifier of Section 2.7 is an example of the simplest form of diode clipper—one resistor and diode. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

There are two general categories of clippers: *series* and *parallel*. The series configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in a branch parallel to the load.

Series

The response of the series configuration of Fig. 2.67a to a variety of alternating waveforms is provided in Fig. 2.67b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper. The addition of a dc supply such as shown in Fig. 2.68 can have a pronounced effect on the output of a clipper. Our initial discussion will be limited to ideal diodes, with the effect of V_T reserved for a concluding example.

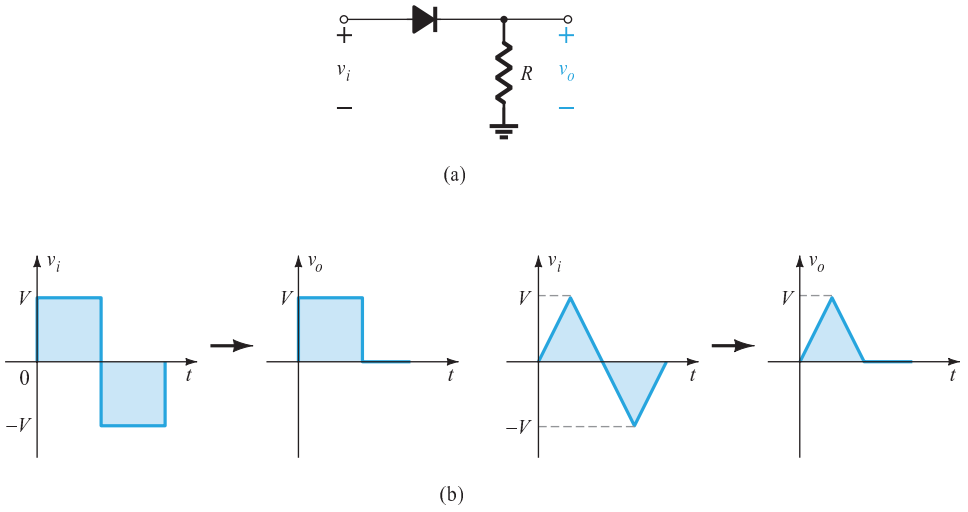


Figure 2.67 Series clipper.

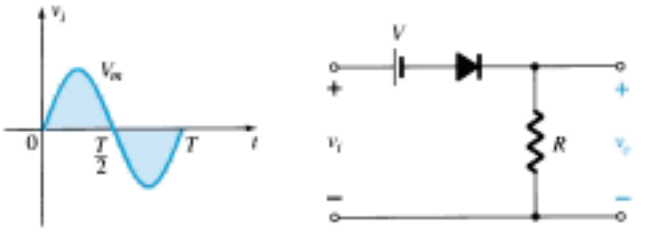


Figure 2.68 Series clipper with a dc supply.

There is no general procedure for analyzing networks such as the type in Fig. 2.68, but there are a few thoughts to keep in mind as you work toward a solution.

1. *Make a mental sketch of the response of the network based on the direction of the diode and the applied voltage levels.*

For the network of Fig. 2.68, the direction of the diode suggests that the signal v_i must be positive to turn it on. The dc supply further requires that the voltage v_i be greater than V volts to turn the diode on. The negative region of the input signal is

"pressuring" the diode into the "off" state, supported further by the dc supply. In general, therefore, we can be quite sure that the diode is an open circuit ("off" state) for the negative region of the input signal.

2. *Determine the applied voltage (transition voltage) that will cause a change in state for the diode.*

For the ideal diode the transition between states will occur at the point on the characteristics where $v_d = 0$ V and $i_d = 0$ A. Applying the condition $i_d = 0$ at $v_d = 0$ to the network of Fig. 2.68 will result in the configuration of Fig. 2.69, where it is recognized that the level of v_i that will cause a transition in state is

$$v_i = V \tag{2.14}$$

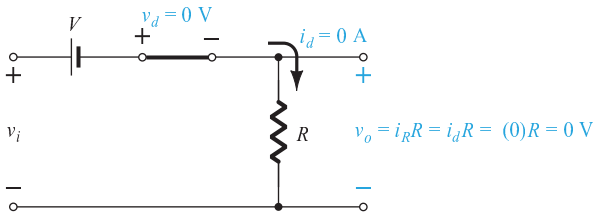


Figure 2.69 Determining the transition level for the circuit of Fig. 2.68.

For an input voltage greater than V volts the diode is in the short-circuit state, while for input voltages less than V volts it is in the open-circuit or "off" state.

3. *Be continually aware of the defined terminals and polarity of v_o.*

When the diode is in the short-circuit state, such as shown in Fig. 2.70, the output voltage v_o can be determined by applying Kirchhoff's voltage law in the clockwise direction:

$$v_i - V - v_o = 0 \text{ (CW direction)}$$

and

$$v_o = v_i - V \tag{2.15}$$

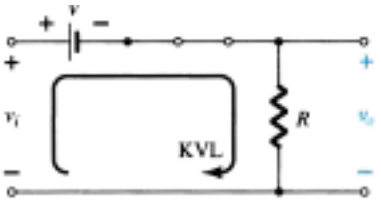


Figure 2.70 Determining v_o.

4. *It can be helpful to sketch the input signal above the output and determine the output at instantaneous values of the input.*

It is then possible that the output voltage can be sketched from the resulting data points of v_o as demonstrated in Fig. 2.71. Keep in mind that at an instantaneous value of v_i the input can be treated as a dc supply of that value and the corresponding dc value (the instantaneous value) of the output determined. For instance, at $v_i = V_m$ for the network of Fig. 2.68, the network to be analyzed appears in Fig. 2.72. For $V_m > V$ the diode is in the short-circuit state and $v_o = V_m - V$, as shown in Fig. 2.71.

At $v_i = V$ the diodes change state; at $v_i = -V_m$, $v_o = 0$ V; and the complete curve for v_o can be sketched as shown in Fig. 2.73.

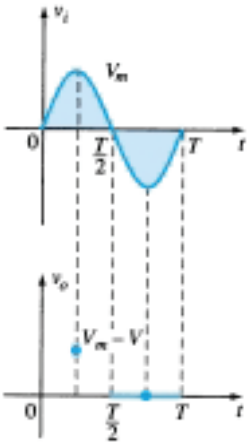


Figure 2.71 Determining levels of v_o.

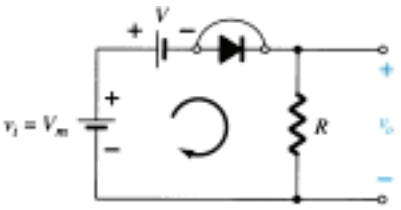


Figure 2.72 Determining v_o when $v_i = V_m$.

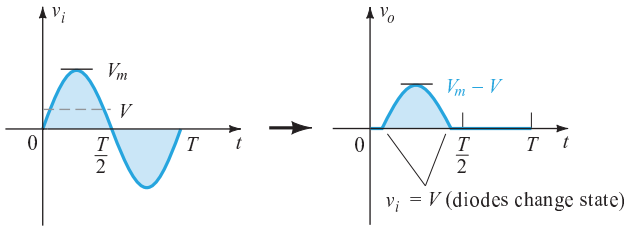


Figure 2.73 Sketching v_o.

EXAMPLE 2.20

Determine the output waveform for the network of Fig. 2.74.

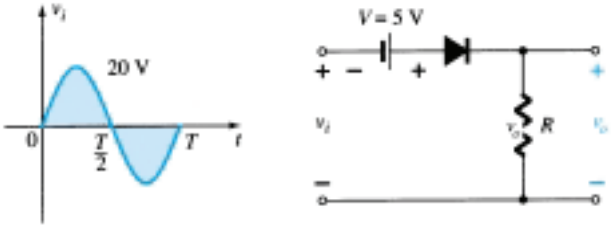


Figure 2.74 Series clipper for Example 2.20.

Solution

Past experience suggests that the diode will be in the "on" state for the positive region of v_i—especially when we note the aiding effect of $V = 5$ V. The network will then appear as shown in Fig. 2.75 and $v_o = v_i + 5$ V. Substituting $i_d = 0$ at $v_d = 0$ for the transition levels, we obtain the network of Fig. 2.76 and $v_i = -5$ V.

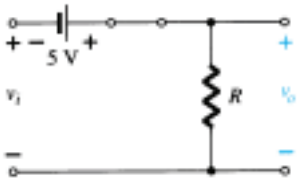


Figure 2.75 v_o with diode in the "on" state.

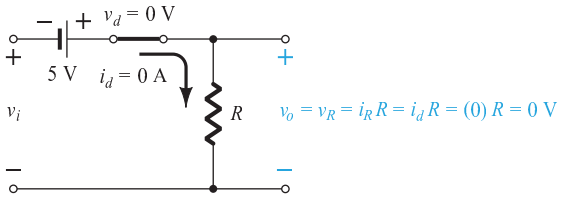


Figure 2.76 Determining the transition level for the clipper of Fig. 2.74.

For v_i more negative than -5 V the diode will enter its open-circuit state, while for voltages more positive than -5 V the diode is in the short-circuit state. The input and output voltages appear in Fig. 2.77.

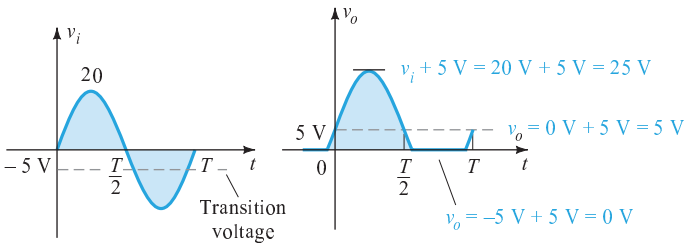


Figure 2.77 Sketching v_o for Example 2.20.

The analysis of clipper networks with square-wave inputs is actually easier to analyze than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting output v_o plotted in the proper time frame.

Repeat Example 2.20 for the square-wave input of Fig. 2.78.

EXAMPLE 2.21

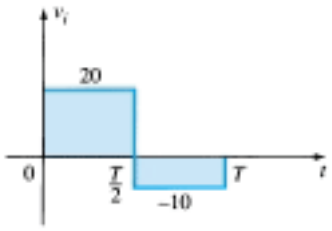


Figure 2.78 Applied signal for Example 2.21.

Solution

For $v_i = 20$ V $(0 \rightarrow T/2)$ the network of Fig. 2.79 will result. The diode is in the short-circuit state and $v_o = 20$ V + 5 V = 25 V. For $v_i = -10$ V the network of Fig. 2.80 will result, placing the diode in the "off" state and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.81.

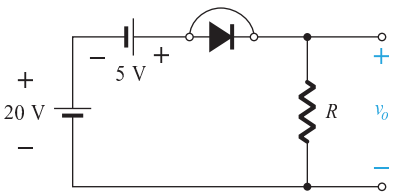


Figure 2.79 v_o at $v_i = +20$ V.

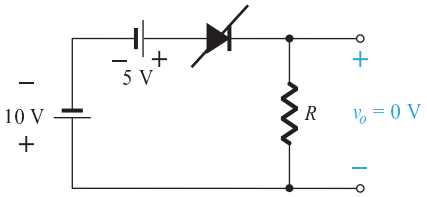


Figure 2.80 v_o at $v_i = -10$ V.

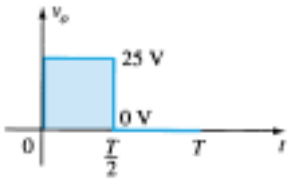


Figure 2.81 Sketching v_o for Example 2.21.

Note in Example 2.21 that the clipper not only clipped off 5 V from the total swing but raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.82 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.67. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

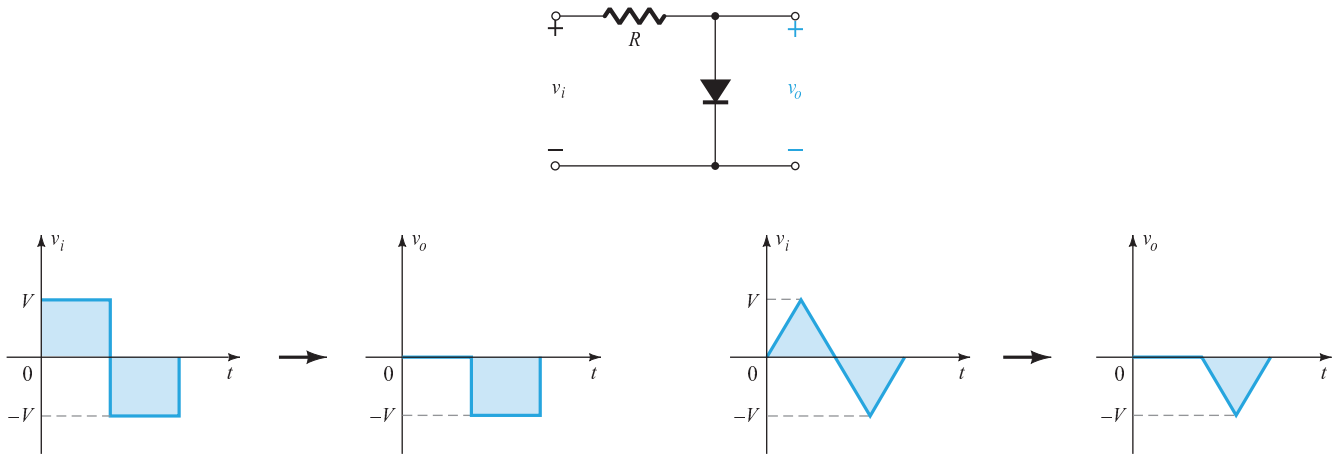


Figure 2.82 Response to a parallel clipper.

EXAMPLE 2.2

Determine v_o for the network of Fig. 2.83.

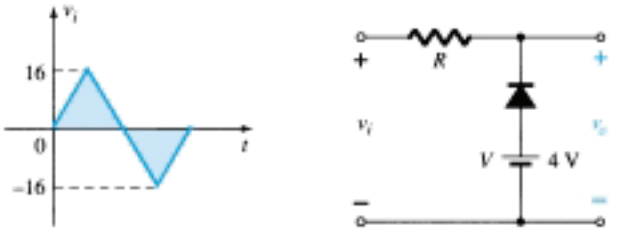


Figure 2.83 Example 2.22.

Solution

The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for the negative region of the input signal. For this region the network will appear as shown in Fig. 2.84, where the defined terminals for v_o require that $v_o = V = 4$ V.

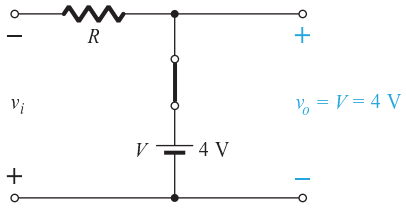


Figure 2.84 v_o for the negative region of v_i.

The transition state can be determined from Fig. 2.85, where the condition $i_d = 0$ A at $v_d = 0$ V has been imposed. The result is v_i (transition) $= V = 4$ V.

Since the dc supply is obviously "pressuring" the diode to stay in the short-circuit state, the input voltage must be greater than 4 V for the diode to be in the "off" state. Any input voltage less than 4 V will result in a short-circuited diode.

For the open-circuit state the network will appear as shown in Fig. 2.86, where $v_o = v_i$. Completing the sketch of v_o results in the waveform of Fig. 2.87.

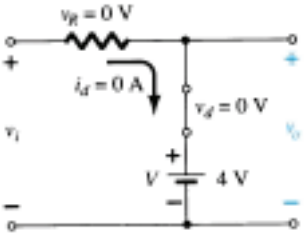


Figure 2.85 Determining the transition level for Example 2.22.

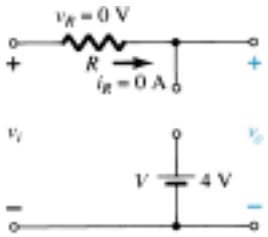


Figure 2.86 Determining v_o for the open state of the diode.

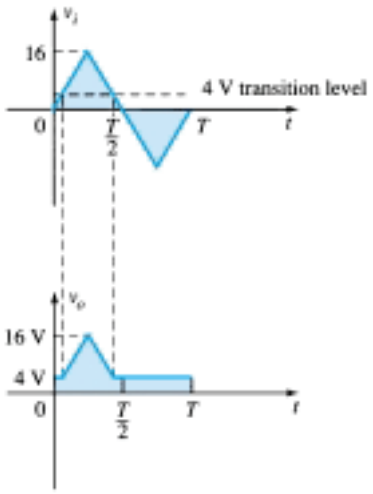


Figure 2.87 Sketching v_o for Example 2.22.

To examine the effects of V_T on the output voltage, the next example will specify a silicon diode rather than an ideal diode equivalent.

Repeat Example 2.22 using a silicon diode with $V_T = 0.7$ V. *EXAMPLE 2.23*

Solution

The transition voltage can first be determined by applying the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of Fig. 2.88. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_T - V = 0$$

and

$$v_i = V - V_T = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

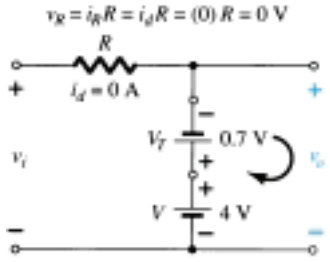


Figure 2.88 Determining the transition level for the network of Fig. 2.83.

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages of less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.89 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3\ V}$$

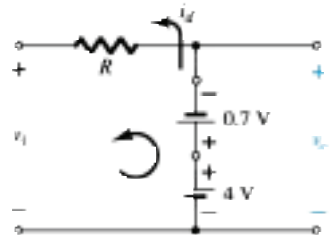


Figure 2.89 Determining v_o for the diode of Fig. 2.83 in the "on" state.

The resulting output waveform appears in Fig. 2.90. Note that the only effect of V_T was to drop the transition level to 3.3 from 4 V.

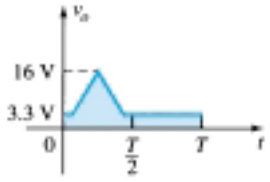


Figure 2.90 Sketching v_o for Example 2.23.

There is no question that including the effects of V_T will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_T, will not be that difficult.

Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.91. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

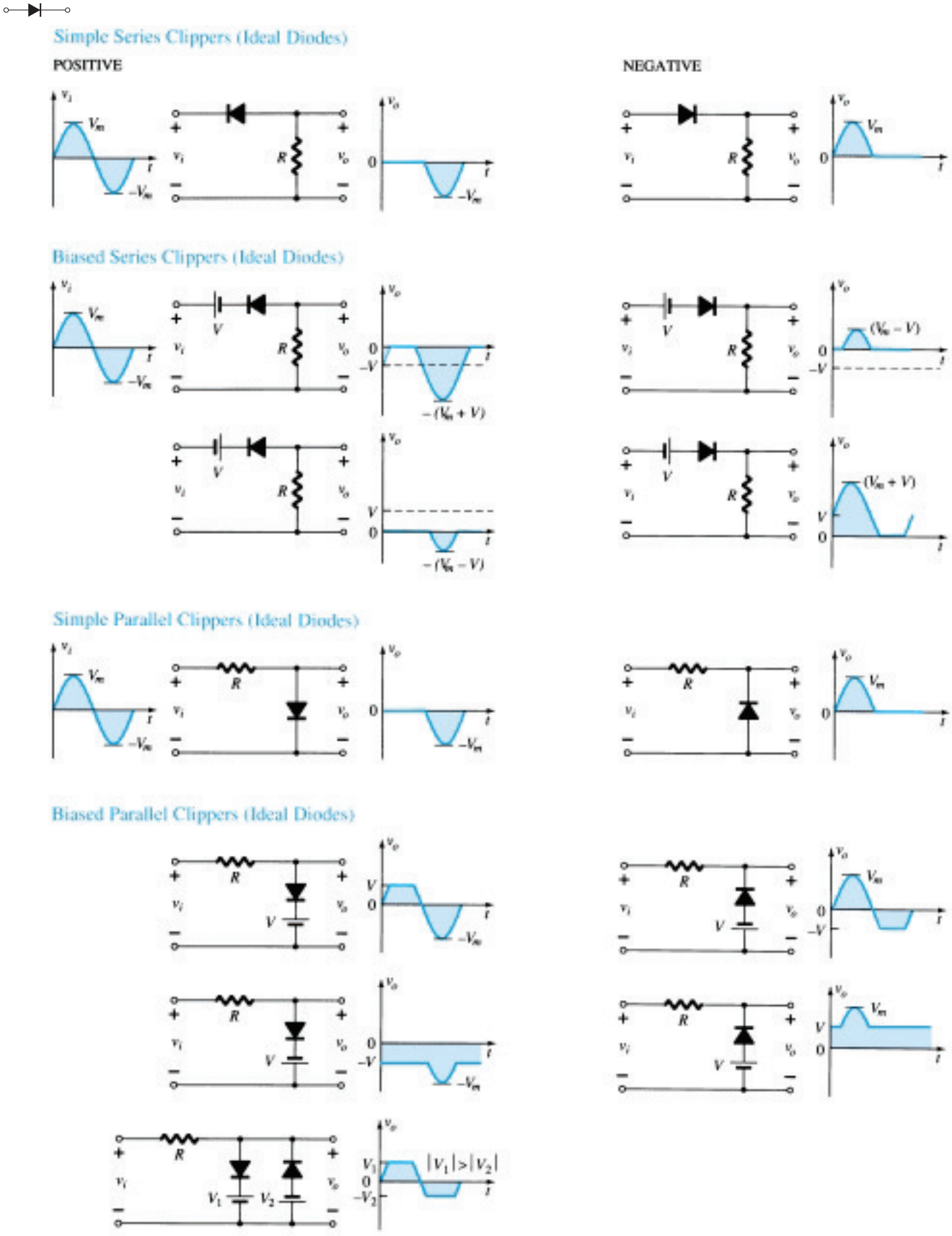


Figure 2.91 Clipping circuits.

2.10 CLAMPERS

The *clamping* network is one that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants.

The network of Fig. 2.92 will clamp the input signal to the zero level (for ideal diodes). The resistor R can be the load resistor or a parallel combination of the load resistor and a resistor designed to provide the desired level of R.

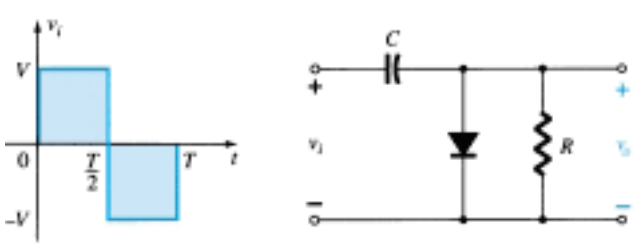


Figure 2.92 Clamper.

During the interval $0 \rightarrow T/2$ the network will appear as shown in Fig. 2.93, with the diode in the "on" state effectively "shorting out" the effect of the resistor R. The resulting RC time constant is so small (R determined by the inherent resistance of the network) that the capacitor will charge to V volts very quickly. During this interval the output voltage is directly across the short circuit and $v_o = 0$ V.

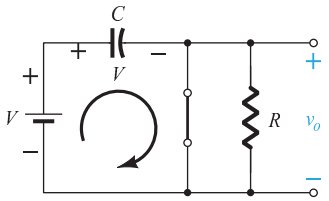


Figure 2.93 Diode "on" and the capacitor charging to V volts.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.94, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

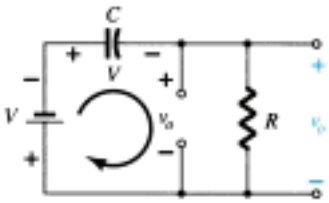


Figure 2.94 Determining v_o with the diode "off."

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.94. Applying Kirchhoff's voltage law around the input loop will result in

$$-V - V - v_o = 0$$

and

$$v_o = -2V$$

The negative sign resulting from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in Fig. 2.95 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

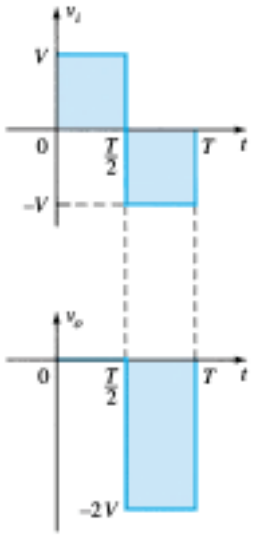


Figure 2.95 Sketching v_o for the network of Fig. 2.92.

For a clamping network:

The total swing of the output is equal to the total swing of the input signal.

This fact is an excellent checking tool for the result obtained.

In general, the following steps may be helpful when analyzing clamping networks:

1. *Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.*

The statement above may require skipping an interval of the input signal (as demonstrated in an example to follow), but the analysis will not be extended by an unnecessary measure of investigation.

2. *During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.*
3. *Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage level.*
4. *Throughout the analysis maintain a continual awareness of the location and reference polarity for v_o to ensure that the proper levels for v_o are obtained.*
5. *Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.*

EXAMPLE 2.24

Determine v_o for the network of Fig. 2.96 for the input indicated.

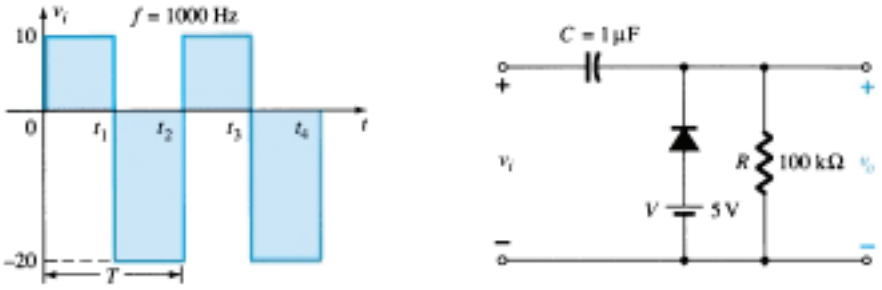


Figure 2.96 Applied signal and network for Example 2.24.

Solution

Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state as recommended by comment 1. For this interval the network will appear as shown in Fig. 2.97. The output is across R, but it is also directly across the 5-V battery if you follow the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop will result in

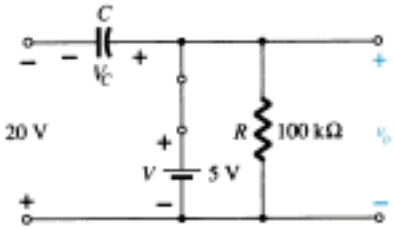


Figure 2.97 Determining v_o and V_C with the diode in the "on" state.

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V, as stated in comment 2. In this case the resistor R is not shorted out by the diode but a Thévenin equivalent circuit of that portion of the network which includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.98.

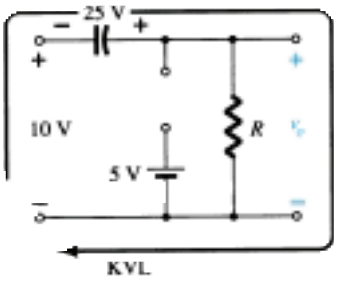


Figure 2.98 Determining v_o with the diode in the "off" state.

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network will result in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and

$$v_o = 35\text{ V}$$

The time constant of the discharging network of Fig. 2.98 is determined by the product RC and has the magnitude

$$\tau = RC = (100\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.01\ \text{s} = 10\ \text{ms}$$

The total discharge time is therefore $5\tau = 5(10\ \text{ms}) = 50\ \text{ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.99 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

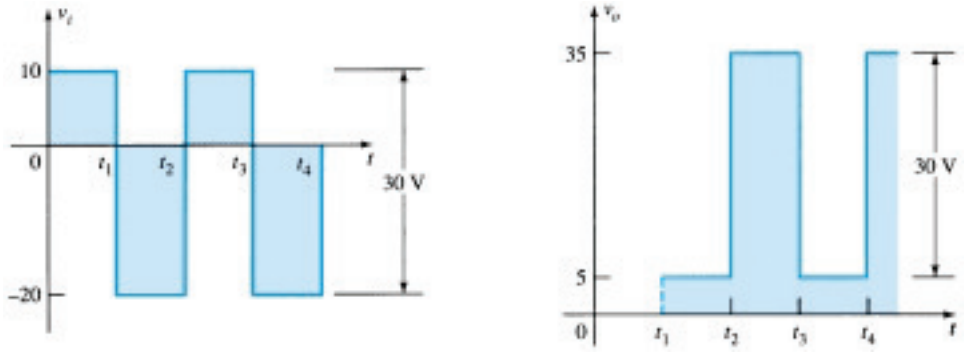


Figure 2.99 v_i and v_o for the clamper of Fig. 2.96.

EXAMPLE 2.25

Repeat Example 2.24 using a silicon diode with $V_T = 0.7$ V.

Solution

For the short-circuit state the network now takes on the appearance of Fig. 2.100 and v_o can be determined by Kirchhoff's voltage law in the output section.

$$+5\ \text{V} - 0.7\ \text{V} - v_o = 0$$

and

$$v_o = 5\ \text{V} - 0.7\ \text{V} = 4.3\ \text{V}$$

For the input section Kirchhoff's voltage law will result in

$$-20\ \text{V} + V_C + 0.7\ \text{V} - 5\ \text{V} = 0$$

and

$$V_C = 25\ \text{V} - 0.7\ \text{V} = 24.3\ \text{V}$$

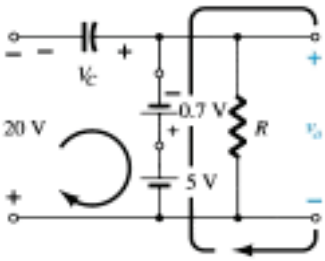


Figure 2.100 Determining v_o and V_C with the diode in the "on" state.

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.101, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\ \text{V} + 24.3\ \text{V} - v_o = 0$$

and

$$v_o = 34.3\ \text{V}$$

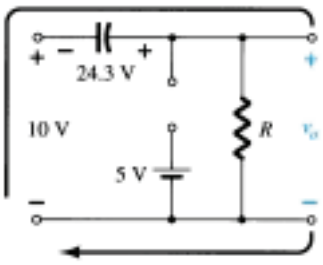


Figure 2.101 Determining v_o with the diode in the open state.

The resulting output appears in Fig. 2.102, verifying the statement that the input and output swings are the same.

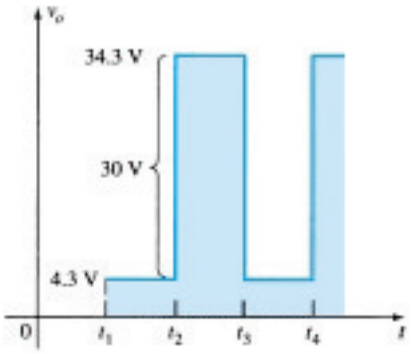


Figure 2.102 Sketching v_o for the clamper of Fig. 2.96 with a silicon diode.

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.103. Although all the waveforms appearing in Fig. 2.103 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.104 for a network appearing in the bottom right of Fig. 2.103.

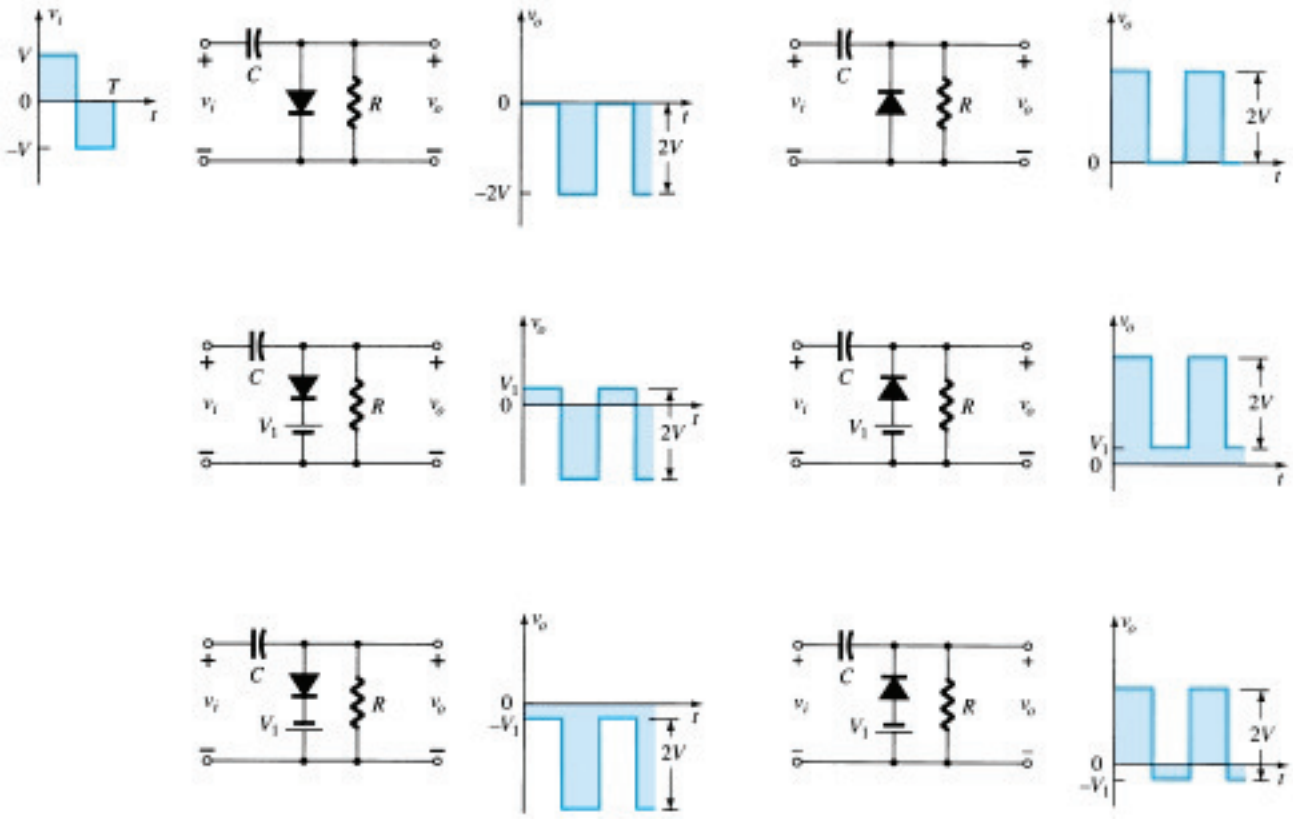


Figure 2.103 Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

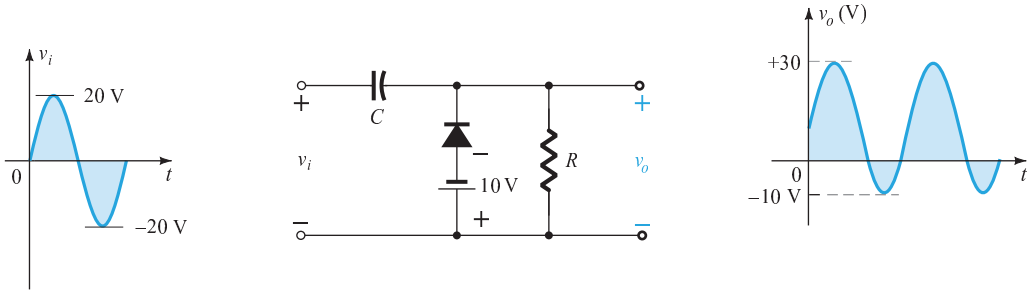


Figure 2.104 Clamping network with a sinusoidal input.

2.11 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to that applied to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Unless otherwise specified, the Zener model to be employed for the "on" state will be as shown in Fig. 2.105a. For the "off" state as defined by a voltage less than V_Z but greater than 0 V with the polarity indicated in Fig. 2.105b, the Zener equivalent is the open circuit that appears in the same figure.

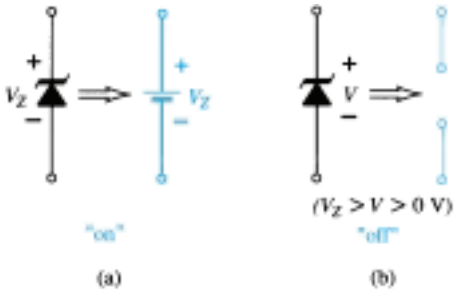


Figure 2.105 Zener diode equivalents for the (a) "on" and (b) "off" states.

V_i and R

The simplest of Zener diode networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. *Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.*

Applying step 1 to the network of Fig. 2.106 will result in the network of Fig. 2.107, where an application of the voltage divider rule will result in

$$V = V_L = \frac{R_L V_i}{R + R_L} \tag{2.16}$$

If $V \geq V_Z$, the Zener diode is "on" and the equivalent model of Fig. 2.105a can be substituted. If $V < V_Z$, the diode is "off" and the open-circuit equivalence of Fig. 2.105b is substituted.

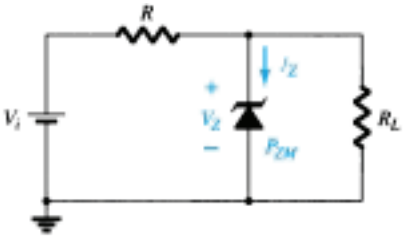


Figure 2.106 Basic Zener regulator.

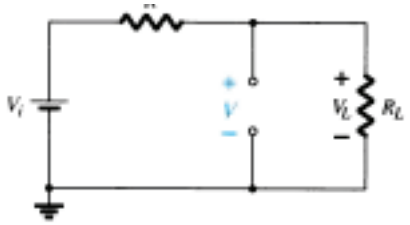


Figure 2.107 Determining the state of the Zener diode.

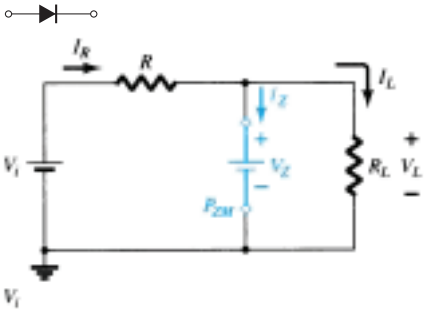


Figure 2.108 Substituting the Zener equivalent for the "on" situation.

2. Substitute the appropriate equivalent circuit and solve for the desired unknowns.

For the network of Fig. 2.106, the "on" state will result in the equivalent network of Fig. 2.108. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2.17}$$

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$I_Z = I_R - I_L \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \textit{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \tag{2.19}$$

which must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the *state of the Zener diode*. If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn "on" as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

Zener diodes are most frequently used in *regulator* networks or as a *reference* voltage. Figure 2.106 is a simple regulator designed to maintain a fixed voltage across the load R_L. For values of applied voltage greater than required to turn the Zener diode "on," the voltage across the load will be maintained at V_Z volts. If the Zener diode is employed as a reference voltage, it will provide a level for comparison against other voltages.

EXAMPLE 2.26

(a) For the Zener diode network of Fig. 2.109, determine V_L, V_R, I_Z, and P_Z.
(b) Repeat part (a) with $R_L = 3\ \text{k}\Omega$.

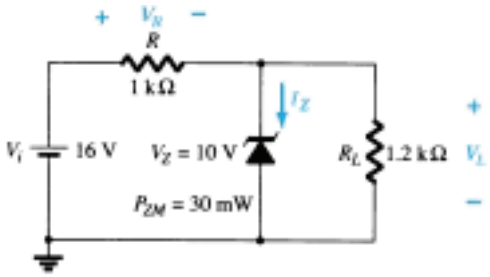


Figure 2.109 Zener diode regulator for Example 2.26.

Solution

(a) Following the suggested procedure the network is redrawn as shown in Fig. 2.110. Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 1.2\ \text{k}\Omega} = 8.73\ \text{V}$$

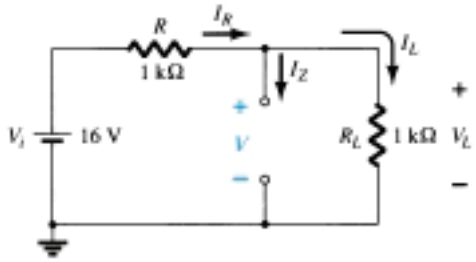


Figure 2.110 Determining V for the regulator of Fig. 2.109.

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state as shown on the characteristics of Fig. 2.111. Substituting the open-circuit equivalent will result in the same network as in Fig. 2.110, where we find that

$$V_L = V = \mathbf{8.73\ V}$$

$$V_R = V_i - V_L = 16\ V - 8.73\ \text{V} = \mathbf{7.27\ V}$$

$$I_Z = \mathbf{0\ A}$$

and

$$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = \mathbf{0\ W}$$

(b) Applying Eq. (2.16) will now result in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 3\ \text{k}\Omega} = 12\ \text{V}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the network of Fig. 2.112 will result. Applying Eq. (2.17) yields

$$V_L = V_Z = \mathbf{10\ V}$$

and

$$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$

with

$$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$

and

$$\text{I}_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$

so that

$$I_Z = I_R - I_L\ \text{[Eq. (2.18)]}$$

$$= 6\ \text{mA} - 3.33\ \text{mA}$$

$$= \mathbf{2.67\ mA}$$

The power dissipated,

$$P_Z = V_Z I_Z = (10\ \text{V})(2.67\ \text{mA}) = \mathbf{26.7\ mW}$$

which is less than the specified $P_{ZM} = 30$ mW.

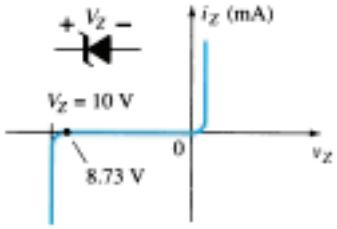


Figure 2.111 Resulting operating point for the network of Fig. 2.109.

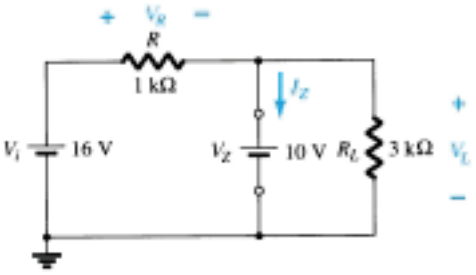


Figure 2.112 Network of Fig. 2.109 in the "on" state.

Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) which will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.106 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} \tag{2.20}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L but in turn specifies the maximum I_L as

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}} \tag{2.21}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z \tag{2.22}$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R} \tag{2.23}$$

The Zener current

$$I_Z = I_R - I_L \tag{2.24}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM} \tag{2.25}$$

and the maximum load resistance as

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} \tag{2.26}$$

EXAMPLE 2.27

(a) For the network of Fig. 2.113, determine the range of R_L and I_L that will result in V_{R_L} being maintained at 10 V.
(b) Determine the maximum wattage rating of the diode.

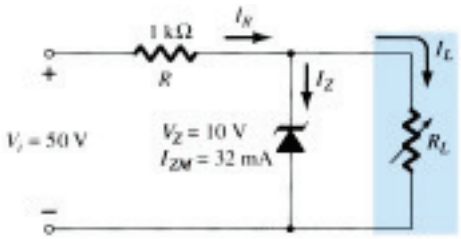


Figure 2.113 Voltage regulator for Example 2.27.

Solution

(a) To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\text{ k}\Omega)(10\text{ V})}{50\text{ V} - 10\text{ V}} = \frac{10\text{ k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\text{ V} - 10\text{ V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\text{ V}}{1\text{ k}\Omega} = \mathbf{40\ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{\min}} = I_R - I_{ZM} = 40\text{ mA} - 32\text{ mA} = \mathbf{8\ mA}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} = \frac{10\text{ V}}{8\text{ mA}} = \mathbf{1.25\ k\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.114a and for V_L versus I_L in Fig. 2.114b.

(b) $P_{\max} = V_Z I_{ZM}$
$= (10\text{ V})(32\text{ mA}) = \mathbf{320\ mW}$

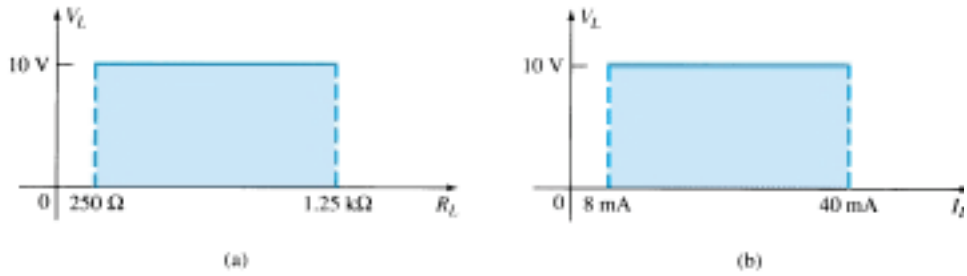


Figure 2.114 V_L versus R_L and I_L for the regulator of Fig. 2.113.

Fixed R_L, Variable V_i

For fixed values of R_L in Fig. 2.106, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$\boxed{V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L}} \tag{2.27}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$\boxed{I_{R_{max}} = I_{ZM} + I_L} \tag{2.28}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$\boxed{V_{i_{max}} = I_{R_{max}}R + V_Z} \tag{2.29}$$

EXAMPLE 2.28

Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.115 in the "on" state.

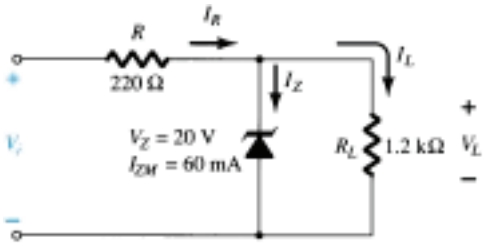


Figure 2.115 Regulator for Example 2.28.

Solution

$$\text{Eq. (2.27):}\quad V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\ \Omega + 220\ \Omega)(20\ \text{V})}{1200\ \Omega} = \mathbf{23.67\ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\ \text{V}}{1.2\ \text{k}\Omega} = 16.67\ \text{mA}$$

$$\text{Eq. (2.28):}\quad I_{R_{max}} = I_{ZM} + I_L = 60\ \text{mA} + 16.67\ \text{mA}$$

$$= 76.67\ \text{mA}$$

$$\text{Eq. (2.29):}\quad V_{i_{max}} = I_{R_{max}}R + V_Z$$

$$= (76.67\ \text{mA})(0.22\ \text{k}\Omega) + 20\ \text{V}$$

$$= 16.87\ \text{V} + 20\ \text{V}$$

$$= \mathbf{36.87\ V}$$

A plot of V_L versus V_i is provided in Fig. 2.116.

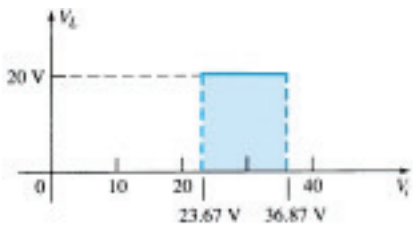


Figure 2.116 V_L versus V_i for the regulator of Fig. 2.115.

The results of Example 2.28 reveal that for the network of Fig. 2.115 with a fixed R_L, the output voltage will remain fixed at 20 V for a range of input voltage that extends from 23.67 to 36.87 V.

In fact, the input could appear as shown in Fig. 2.117 and the output would remain constant at 20 V, as shown in Fig. 2.116. The waveform appearing in Fig. 2.117 is obtained by *filtering* a half-wave- or full-wave-rectified output—a process described in detail in a later chapter. The net effect, however, is to establish a steady dc voltage (for a defined range of V_i) such as that shown in Fig. 2.116 from a sinusoidal source with 0 average value.

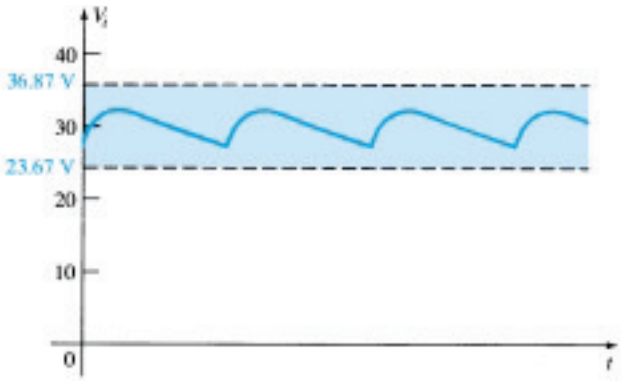


Figure 2.117 Waveform generated by a filtered rectified signal.

Two or more reference levels can be established by placing Zener diodes in series as shown in Fig. 2.118. As long as V_i is greater than the sum of V_{Z_1} and V_{Z_2}, both diodes will be in the "on" state and the three reference voltages will be available.

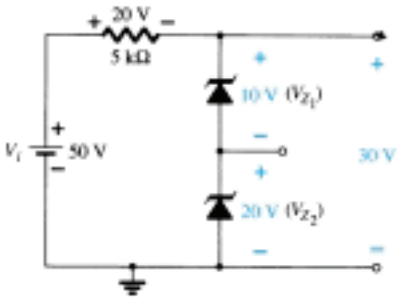


Figure 2.118 Establishing three reference voltage levels.

Two back-to-back Zeners can also be used as an ac regulator as shown in Fig. 2.119a. For the sinusoidal signal v_i the circuit will appear as shown in Fig. 2.119b at the instant $v_i = 10$ V. The region of operation for each diode is indicated in the adjoining figure. Note that Z_1 is in a low-impedance region, while the impedance of Z_2 is quite large, corresponding with the open-circuit representation. The result is that $v_o = v_i$ when $v_i = 10$ V. The input and output will continue to duplicate each other until v_i reaches 20 V. Z_2 will then "turn on" (as a Zener diode), while Z_1 will be in a

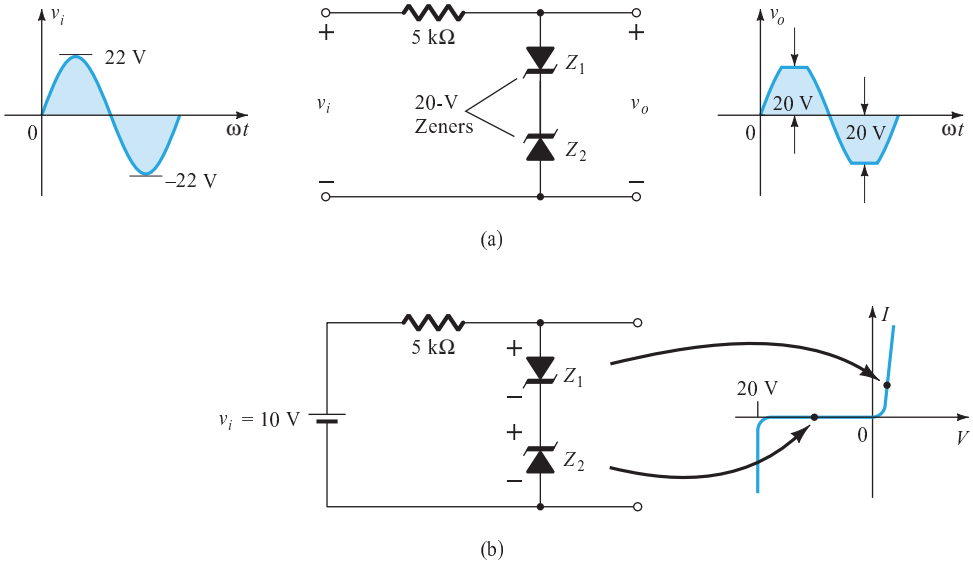


Figure 2.119 Sinusoidal ac regulation: (a) 40-V peak-to-peak sinusoidal ac regulator; (b) circuit operation at $v_i = 10$ V.

region of conduction with a resistance level sufficiently small compared to the series 5-kΩ resistor to be considered a short circuit. The resulting output for the full range of v_i is provided in Fig. 2.119(a). Note that the waveform is not purely sinusoidal, but its rms value is lower than that associated with a full 22-V peak signal. The network is effectively limiting the rms value of the available voltage. The network of Fig. 2.119a can be extended to that of a simple square-wave generator (due to the clipping action) if the signal v_i is increased to perhaps a 50-V peak with 10-V Zeners as shown in Fig. 2.120 with the resulting output waveform.

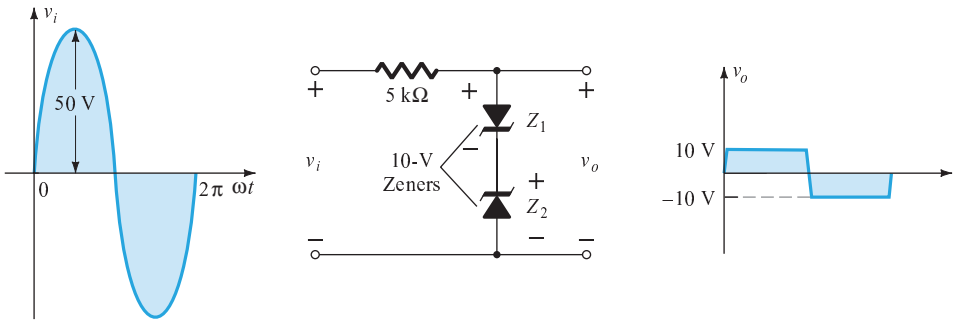


Figure 2.120 Simple square-wave generator.

2.12 VOLTAGE-MULTIPLIER CIRCUITS

Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

Voltage Doubler

The network of Figure 2.121 is a half-wave voltage doubler. During the positive voltage half-cycle across the transformer, secondary diode D_1 conducts (and diode D_2 is cut off), charging capacitor C_1 up to the peak rectified voltage (V_m). Diode D_1 is ideally a short during this half-cycle, and the input voltage charges capacitor C_1 to V_m with the polarity shown in Fig. 2.122a. During the negative half-cycle of the secondary voltage, diode D_1 is cut off and diode D_2 conducts charging capacitor C_2. Since diode D_2 acts as a short during the negative half-cycle (and diode D_1 is open), we can sum the voltages around the outside loop (see Fig. 2.122b):

$$-V_m - V_{C_1} + V_{C_2} = 0$$

$$-V_m - V_m + V_{C_2} = 0$$

from which

$$V_{C_2} = 2V_m$$

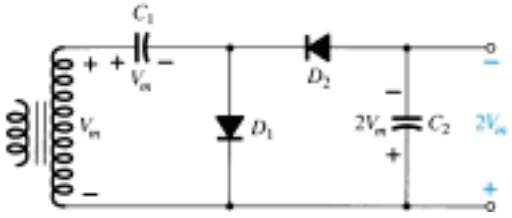


Figure 2.121 Half-wave voltage doubler.

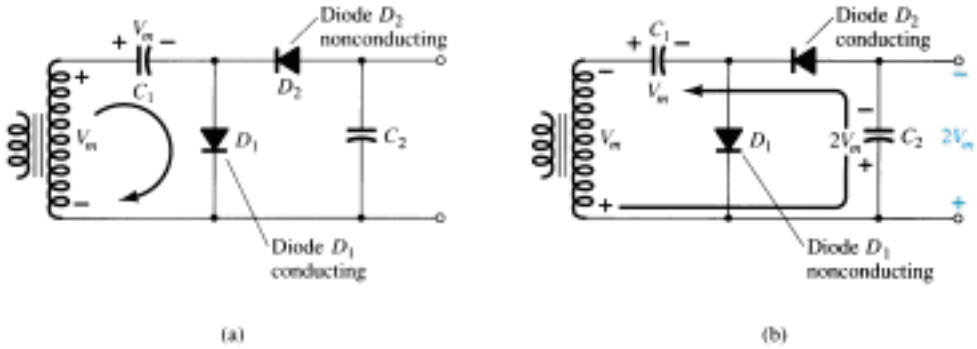


Figure 2.122 Double operation, showing each half-cycle of operation: (a) positive half-cycle; (b) negative half cycle.

On the next positive half-cycle, diode D_2 is nonconducting and capacitor C_2 will discharge through the load. If no load is connected across capacitor C_2, both capacitors stay charged—C_1 to V_m and C_2 to $2V_m$. If, as would be expected, there is a load connected to the output of the voltage doubler, the voltage across capacitor C_2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to $2V_m$ during the negative half-cycle. The output waveform across capacitor C_2 is that of a half-wave signal filtered by a capacitor filter. The peak inverse voltage across each diode is $2V_m$.

Another doubler circuit is the full-wave doubler of Fig. 2.123. During the positive half-cycle of transformer secondary voltage (see Fig. 2.124a) diode D_1 conducts charging capacitor C_1 to a peak voltage V_m. Diode D_2 is nonconducting at this time.

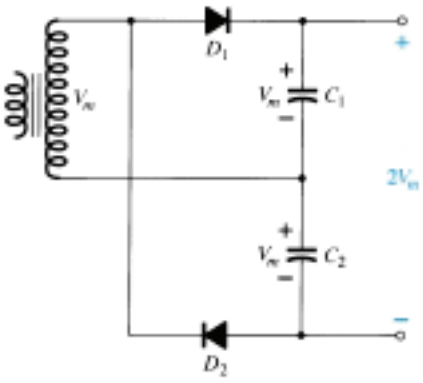


Figure 2.123 Full-wave voltage doubler.

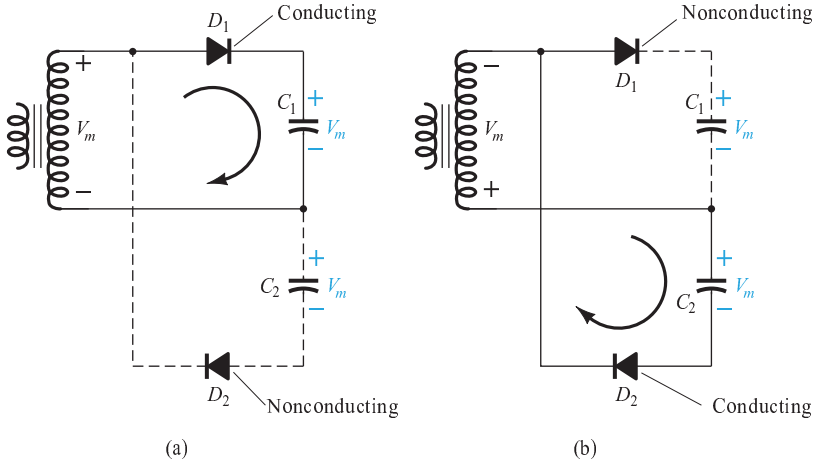


Figure 2.124 Alternate half-cycles of operation for full-wave voltage doubler.

During the negative half-cycle (see Fig. 2.124b) diode D_2 conducts charging capacitor C_2 while diode D_1 is nonconducting. If no load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is $2V_m$. If load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is the same as that across a capacitor fed by a full-wave rectifier circuit. One difference is that the effective capacitance is that of C_1 and C_2 in series, which is less than the capacitance of either C_1 or C_2 alone. The lower capacitor value will provide poorer filtering action than the single-capacitor filter circuit.

The peak inverse voltage across each diode is $2V_m$, as it is for the filter capacitor circuit. In summary, the half-wave or full-wave voltage-doubler circuits provide twice the peak voltage of the transformer secondary while requiring no center-tapped transformer and only $2V_m$ PIV rating for the diodes.

Voltage Tripler and Quadrupler

Figure 2.125 shows an extension of the half-wave voltage doubler, which develops three and four times the peak input voltage. It should be obvious from the pattern of the circuit connection how additional diodes and capacitors may be connected so that the output voltage may also be five, six, seven, and so on, times the basic peak voltage (V_m).

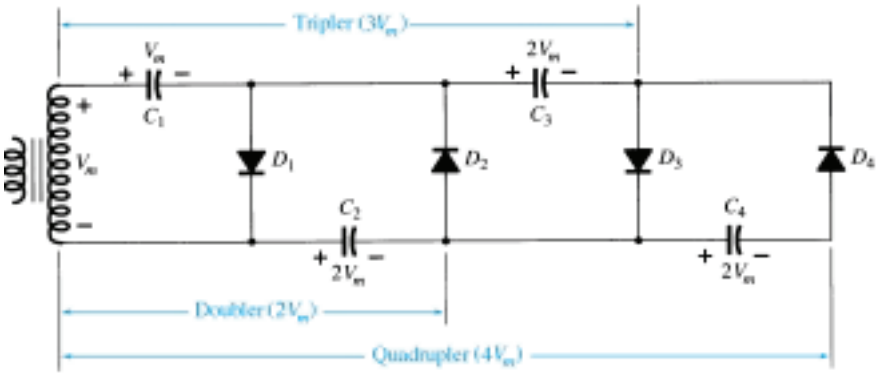


Figure 2.125 Voltage tripler and quadrupler.

In operation capacitor C_1 charges through diode D_1 to a peak voltage, V_m, during the positive half-cycle of the transformer secondary voltage. Capacitor C_2 charges to twice the peak voltage $2V_m$ developed by the sum of the voltages across capacitor C_1 and the transformer, during the negative half-cycle of the transformer secondary voltage.

During the positive half-cycle, diode D_3 conducts and the voltage across capacitor C_2 charges capacitor C_3 to the same $2V_m$ peak voltage. On the negative half-cycle, diodes D_2 and D_4 conduct with capacitor C_3, charging C_4 to $2V_m$.

The voltage across capacitor C_2 is $2V_m$, across C_1 and C_3 it is $3V_m$, and across C_2 and C_4 it is $4V_m$. If additional sections of diode and capacitor are used, each capacitor will be charged to $2V_m$. Measuring from the top of the transformer winding (Fig. 2.125) will provide odd multiples of V_m at the output, whereas measuring the output voltage from the bottom of the transformer will provide even multiples of the peak voltage, V_m.

The transformer rating is only V_m, maximum, and each diode in the circuit must be rated at $2V_m$ PIV. If the load is small and the capacitors have little leakage, extremely high dc voltages may be developed by this type of circuit, using many sections to step up the dc voltage.

2.13 PSPICE WINDOWS

Series Diode Configuration

PSpice Windows will now be applied to the network of Fig. 2.27 to permit a comparison with the hand-calculated solution. As briefly described in Chapter 1, the application of PSpice Windows requires that the network first be constructed on the schematics screen. The next few paragraphs will examine the basics of setting up the network on the screen, assuming no prior experience with the process. It might be helpful to reference the completed network of Fig. 2.126 as we progress through the discussion.

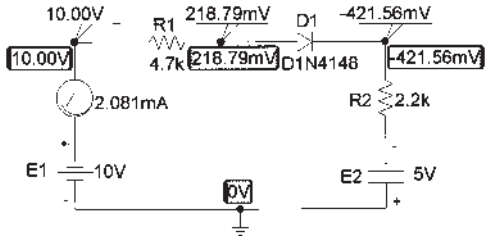


Figure 2.126 PSpice Windows analysis of a series diode configuration.

In general, it is easier to draw the network if the grid is on the screen and the stipulation is made that all elements be on the grid. This will ensure that all the connections are made between the elements. The screen can be set up by first choosing **Options** at the heading of the schematics screen, followed by **Display Options.** The **Display Options** dialog box will permit you to make all the choices necessary regarding the type of display desired. For our purposes, we will choose **Grid On, Stay on Grid,** and **Grid Spacing** of 0.1 in.

R

The resistor **R** will be the first to be positioned. By clicking on the **Get New Part** icon (the icon in the top right area with the binoculars) followed by **Libraries,** we can choose the **Analog.slb** library of basic elements. We can then scroll the **Part** list until we find **R.** Clicking on **R** followed by **OK** will result in the **Part Browser Basic** dialog box reflecting our choice of a resistive element. Choosing the **Place & Close** option will place the resistive element on the screen and close the dialog box. The resistor will appear horizontal, which is perfect for the R_1 of Fig. 2.27 (note Fig. 2.126). Move the resistor to a logical location, and click the left button of the mouse—the resistor R_1 is in place. Note that it snaps to the grid structure. The resistor R_2 must now be placed to the right of R_1. By simply moving the mouse to the right, the second resistor will appear, and R_2 can be placed in the proper location with a subsequent click of the mouse. Since the network only has two resistors, the depositing of resistors can be ended by a right click of the mouse. The resistor R_2 can be rotated by pressing the keys **Ctrl** and **R** simultaneously or by choosing **Edit** on the menu bar, followed by **Rotate.**

The result of the above is two resistors with the right labels but the wrong values. To change a value, double click on the value of the screen (first **R1**). A **Set Attribute Value** dialog box will appear. Type in the correct value, and send the value to the screen with **OK.** The 4.7kΩ will appear within a box that can be moved by simply clicking on the small box and, while holding the clicker down, moving the 4.7kΩ to the desired location. Release the clicker, and the 4.7kΩ label will remain where placed. Once located, an additional click anywhere on the screen will remove the boxes and end the process. If you want to move the 4.7kΩ in the future, simply click once on the value and the boxes will reappear. Repeat the above for the value of the resistor R_2.

To remove (clip) an element, simply click on it (to establish the red or active color), and then click the **scissors** icon or use the sequence **Edit-Delete.**

E

The voltage sources are set by going to the **source.slb** library of **Library Browser** and choosing **VDC.** Clicking **OK** results in the source symbol appearing on the schematic. This symbol can be placed as required. After clicking it in the appropriate place, a **V1** label will appear. To change the label to **E1** simply click the **V1** twice and an **Edit Reference Designator** dialog box will appear. Change the label to **E1** and click **OK,** and then **E1** will appear on the screen within a box. The box can be moved in the same manner as the labels for resistors. When you have the correct position, simply click the mouse once more and place $\mathbf{E_1}$ as desired.

To set the value of E_1, click the value twice and the **Set Attribute Value** will appear. Set the value to 10V and click **OK.** The new value will appear on the schematic. The value can also be set by clicking the battery symbol itself twice, after which a dialog box will appear labeled **E1 PartName:VDC.** By choosing **DC = 0V, DC** and **Value** will appear in the designated areas at the top of the dialog box. Using the mouse, bring the marker to the **Value** box and change it to 10V. Then click **Save Attr.** to be sure and save the new value, and an **OK** will result in E_1 being changed to 10V. E_1 can now be set, but be sure to turn it 180° with the appropriate operations.

DIODE

The diode is found in the **EVAL.slb** library of the **Library Browser** dialog box. Choosing the **D1N4148** diode followed by an **OK** and **Close & Place** will place the diode symbol on the screen. Move the diode to the correct position, click it in place with a left click, and end the operation with a right click of the mouse. The labels **D1** and **D1N4148** will appear near the diode. Clicking on either label will provide the boxes that permit movement of the labels.

Let us now take a look at the diode specs by clicking the diode symbol once, followed by the **Edit-Model-Edit Instance Model** sequence. For the moment, we will leave the parameters as listed. In particular, note that $I_s = 2.682\text{nA}$ and the terminal capacitance (important when the applied frequency becomes a factor) is 4pF.

IPROBE

One or more currents of a network can be displayed by inserting an **IPROBE** in the desired path. **IPROBE** is found in the **SPECIAL.slb** library and appears as a meter face on the screen. **IPROBE** will respond with a positive answer if the current (conventional) enters the symbol at the end with the arc representing the scale. Since we are looking for a positive answer in this investigation, **IPROBE** should be installed as shown in Fig. 2.126. When the symbol first appears, it is 180° out of phase with the desired current. Therefore, it is necessary to use the **Ctrl-R** sequence twice to rotate the symbol before finalizing its position. As with the elements described above, once it is in place a single click will place the meter and a right click will complete the insertion process.

LINE

The elements now need to be connected by choosing the icon with the thin line and pencil or by the sequence **Draw-Wire.** A pencil will appear that can draw the desired connections in the following manner: Move the pencil to the beginning of the line, and click the left side of the mouse. The pencil is now ready to draw. Draw the desired line (connection), and click the left side again when the connection is complete. The line will appear in red, waiting for another random click of the mouse or

the insertion of another line. It will then turn geen to indicate it is in memory. For additional lines, simply repeat the procedure. When done, simply click the right side of the mouse.

EGND

The system must have a ground to serve as a reference point for the nodal voltages. Earth ground **(EGND)** is part of the **PORT.slb** library and can be placed in the same manner as the elements described above.

VIEWPOINT

Nodal voltages can be displayed on the diagram after the simulation using **VIEWPOINTS,** which is found in the **SPECIAL.slb** library. Simply place the arrow of the **VIEWPOINT** symbol where you desire the voltage with respect to ground. A **VIEWPOINT** can be placed at every node of the network if necessary, although only three are placed in Fig. 2.126. The network is now complete, as shown in Fig 2.126.

ANALYSIS

The network is now ready to be analyzed. To expedite the process, click on **Analysis** and choose **Probe Setup.** By selecting **Do not auto-run Probe** you save intermediary steps that are inappropriate for this analysis; it is an option that will be discussed later in this chapter. After **OK,** go to **Analysis** and choose **Simulation**. If the network was installed properly, a **PSpiceAD** dialog box will appear and reveal that the bias (dc) points have been calculated. If we now exit the box by clicking on the small **x** in the top right corner, you will obtain the results appearing in Fig. 2.126. Note that the program has automatically provided four dc voltages of the network (in addition to the **VIEWPOINT** voltages). This occurred because an option under analysis was enabled. For future analysis we will want control over what is displayed so follow the path through **Analysis-Display Results on Schematic** and slide over to the adjoining **Enable** box. Clicking the **Enable** box will remove the check, and the dc voltages will not automatically appear. They will only appear where **VIEWPOINTS** have been inserted. A more direct path toward controlling the appearance of the dc voltages is to use the icon on the menu bar with the large capital **V.** By clicking it on and off, you can control whether the dc levels of the network will appear. The icon with the large capital **I** will permit all the dc currents of the network to be shown if desired. For practice, click it on and off and note the effect on the schematic. If you want to remove selected dc voltages on the schematic, simply click the nodal voltage of interest, then click the icon with the smaller capital **V** in the same grouping. Clicking it once will remove the selected dc voltage. The same can be done for selected currents with the remaining icon of the group. For the future, it should be noted that an analysis can also be initiated by simply clicking the **Simulation** icon having the yellow background and the two waveforms (square wave and sinusoidal).

Note also that the results are not an exact match with those obtained in Example 2.11. The **VIEWPOINT** voltage at the far right is -421.56 rather than the -454.2 mV obtained in Example 2.11. In addition, the current is 2.081 rather than the 2.066 mA obtained in the same example. Further, the voltage across the diode is 281.79 mV + 421.56 mV = 0.64 V rather than the 0.7 V assumed for all silicon diodes. This all results from our using a real diode with a long list of variables defining its operation. However, it is important to remember that the analysis of Example 2.11 was an approximate one and, therefore, it is expected that the results are only close to the actual response. On the other hand, the results obtained for the nodal voltage and current are quite close. If taken to the tenths place, the currents (2.1 mA) are an exact match.

The results obtained in Fig. 2.126 can be improved (in the sense that they will be a closer match to the hand-written solution) by clicking on the diode (to make it red)

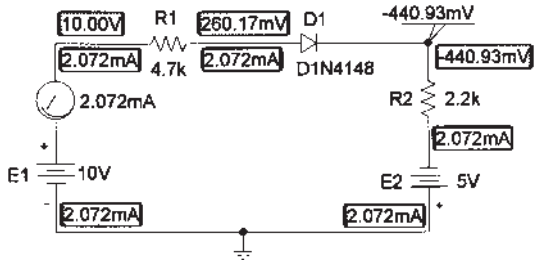


Figure 2.127 The circuit of Figure 2.126 reexamined with I_s set to 3.5E-15A.

and using the sequence **Edit-Model-Edit Instance Model (Text)** to obtain the **Model Editor** dialog box. Choose **Is = 3.5E-15A** (a value determined by trial and error), and delete all the other parameters for the device. Then, follow with **OK-Simulate** icon to obtain the results of Fig. 2.127. Note that the voltage across the diode now is 260.17 mV + 440.93 mV = 0.701 V, or almost exactly 0.7 V. The **VIEWPOINT** voltage is −440.93 V or, again, an almost perfect match with the hand-written solution of −0.44 V. In either case, the results obtained are very close to the expected values. One is more accurate as far as the actual device is concerned, while the other provides an almost exact match with the hand-written solution. One cannot expect a perfect match for every diode network by simply setting I_s to 3.5E-15A. As the current through the diode changes, the level of I_s must also change if an exact match with the hand-written solution is to be obtained. However, rather than worry about the current in each system, it is suggested that I_s = 3.5E-15A be used as the standard value if the PSpice solution is desired to be a close match with the hand-written solution. The results will not always be perfect, but in most cases they will be closer than if the parameters of the diode are left at their default values. For transistors in the chapters to follow, it will be set to 2E-15A to obtain a suitable match with the hand-written solution. Note also that the **Bias Current Display** was enabled to show that the current is indeed the same everywhere in the circuit.

The results can also be viewed in tabulated form by returning to **Analysis** and choosing **Examine Output.** The result is the long listing of Fig. 2.128. The **Schematics Netlist** describes the network in terms of numbered nodes. The 0 refers to ground level, with the 10V source from node 0 to 5. The source **E2** is from 0 to node 3. The resistor **R2** is connected from node 3 to 4, and so on. Scrolling down the output file, we find the **Diode MODEL PARAMETERS** clearly showing that I_s is set at 3.5E-15A and is the only parameter listed. Next is the **SMALL SIGNAL BIAS SOLUTION** or dc solution with the voltages at the various nodes. In addition, the current through the sources of the network is shown. The negative sign reveals that it is reflecting the direction of electron flow (into the positive terminal). The total power dissipation of the elements is 31.1 mW. Finally, the **OPERATING POINT INFORMATION** reveals that the current through the diode is 2.07 mA and the voltage across the diode 0.701 V.

The analysis is now complete for the diode circuit of interest. We have not touched on all the alternative paths available through PSpice Windows, but sufficient coverage has been provided to examine any of the networks covered in this chapter with a dc source. For practice, the other examples should be examined using the Windows approach since the results are provided for comparison. The same can be said for the odd-numbered exercises at the end of this chapter.

Diode Characteristics

The characteristics of the D1N4148 diode used in the above analysis will now be obtained using a few maneuvers somewhat more sophisticated than those employed previously. First, the network in Fig. 2.129 is constructed using the procedures described

```
 ****     CIRCUIT DESCRIPTION

******************************************************************************

* Schematics Netlist *

R_R1          $N_0002 $N_0001  4.7k
V_E2          0 $N_0003 5V
R_R2          $N_0003 $N_0004  2.2k
V_E1          $N_0005 0 10V
D_D1          $N_0001 $N_0004 D1N4148-X2
v_V3          $N_0005 $N_0002 0


****     Diode MODEL PARAMETERS

******************************************************************************

             D1N4148-X2
         IS    3.500000E-15


 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

($N_0001)     .2602                    ($N_0002)   10.0000

($N_0003)   -5.0000                    ($N_0004)    -.4409

($N_0005)   10.0000

    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_E2         -2.072E-03
    V_E1         -2.072E-03
    v_V3          2.072E-03

    TOTAL POWER DISSIPATION   3.11E-02  WATTS

 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

******************************************************************************

 **** DIODES

 NAME          D_D1
 MODEL         D1N4148-X2
 ID            2.07E-03
 VD            7.01E-01
 REQ           1.25E+01
 CAP           0.00E+00
```

Figure 2.128 Output file for PSpice Windows analysis of the circuit of Figure 2.127.

above. Note, however, the **Vd** appearing above the diode **D1.** A point in the network (representing the voltage from anode to ground for the diode) has been identified as a particular voltage by double-clicking on the wire above the device and typing Vd in the **Set Attribute Value** as the **LABEL.** The resulting voltage V_d is, in this case, the voltage across the diode.

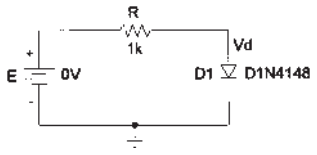


Figure 2.129 Network to obtain the characteristics of the D1N4148 diode.

Next, **Analysis Setup** is chosen by either clicking on the Analysis Setup icon (at the top left edge of the schematic with the horizontal blue bar and the two small squares and rectangles) or by using the sequence **Analysis-Setup.** Within the **Analysis-Setup** dialog box the **DC Sweep** is enabled (the only one necessary for this exercise), followed by a single click of the **DC Sweep** rectangle. The **DC Sweep** dialog box will appear with various inquiries. In this case, we plan to sweep the source voltage from 0 to 10 V in 0.01-V increments, so the **Swept Var. Type** is Voltage Source, the **Sweep Type** will be linear, the **Name** E, and the **Start Value** 0V, the **End Value** 10V, and the **Increment** 0.01V. Then, with an **OK** followed by a **Close** of the

Analysis Setup box, we are set to obtain the solution. The analysis to be performed will obtain a complete solution for the network for each value of E from 0 to 10 V in 0.01-V increments. In other words, the network will be analyzed 1000 times and the resulting data stored for the plot to be obtained. The analysis is performed by the sequence **Analysis-Run Probe,** followed by an immediate appearance of the **MicroSim Probe** graph showing only a horizontal axis of the source voltage E running from 0 to 10 V.

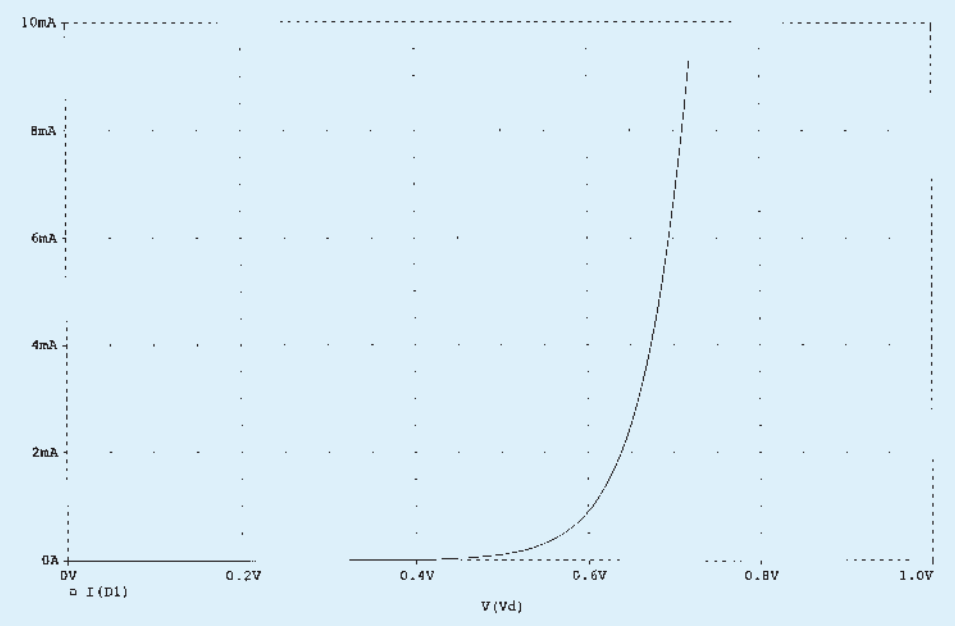
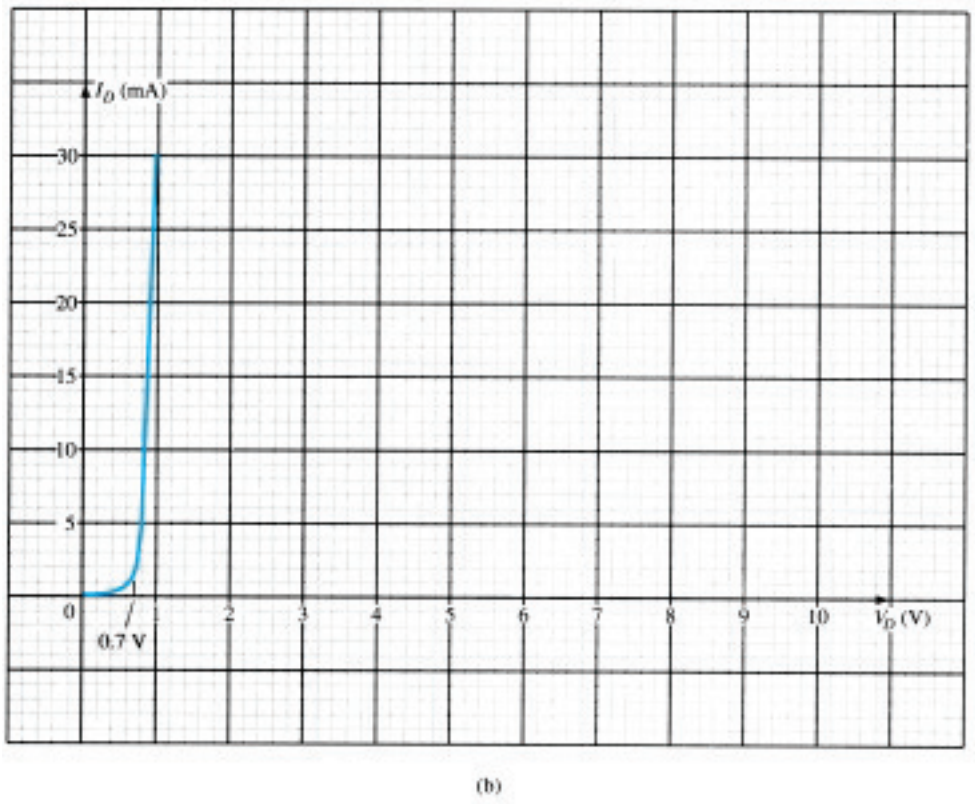


Figure 2.130 Characteristics of the D1N4148 diode.

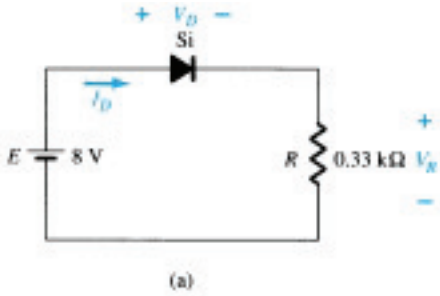
Since the plot we want is of I_D versus V_D, we have to change the horizontal (x-axis) to V_D. This is accomplished by selecting **Plot** and then **X-Axis Settings** to obtain the **X Axis Settings** dialog box. Next, we click **Axis Variable** and select **V(Vd)** from the listing. After **OK**, we return to the dialog box to set the horizontal scale. Choose **User Defined,** then enter 0V to 1V since this is the range of interest for Vd with a **Linear** scale. Click **OK** and you will find that the horizontal axis is now V(Vd) with a range of 0 to 1.0 V. The vertical axis must now be set to I_D by first choosing **Trace** (or the **Trace** icon, which is the red waveform with two sharp peaks and a set of axis) and then **Add** to obtain **Add Traces.** Choosing **I(D1)** and clicking **OK** will result in the plot of Fig. 2.130. In this case, the resulting plot extended from 0 to 10 mA. The range can be reduced or expanded by simply going to **Plot-Y-Axis Setting** and defining the range of interest.

In the previous analysis, the voltage across the diode was 0.64 V, corresponding to a current of about 2 mA on the graph (recall the solution of 2.07 mA for the current). If the resulting current had been closer to 6.5 mA, the voltage across the diode would have been about 0.7 V and the PSpice solution closer to the hand-written approach. If I_s had been set to 3.5E-15A and all other parameters removed from the diode listing, the curve would have shifted to the right and an intersection of 0.7 V and 2.07 mA would have obtained.

1. (a) Using the characteristics of Fig. 2.131b, determine I_D, V_D, and V_R for the circuit of Fig. 2.131a.
(b) Repeat part (a) using the approximate model for the diode and compare results.
(c) Repeat part (a) using the ideal model for the diode and compare results.



(b)



(a)

Figure 2.131 Problems 1, 2

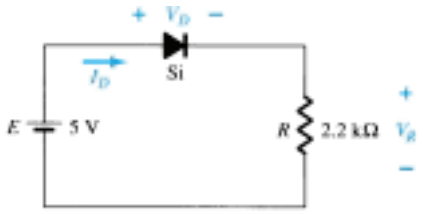


Figure 2.132 Problems 2, 3

2. (a) Using the characteristics of Fig. 2.131b, determine I_D and V_D for the circuit of Fig. 2.132.
(b) Repeat part (a) with $R = 0.47$ kΩ.
(c) Repeat part (a) with $R = 0.18$ kΩ.
(d) Is the level of V_D relatively close to 0.7 V in each case?

How do the resulting levels of I_D compare? Comment accordingly.

3. Determine the value of R for the circuit of Fig. 2.132 that will result in a diode current of 10 mA if $E = 7$ V. Use the characteristics of Fig. 2.131b for the diode.

4. (a) Using the approximate characteristics for the Si diode, determine the level of V_D, I_D, and V_R for the circuit of Fig. 2.133.
(b) Perform the same analysis as part (a) using the ideal model for the diode.
(c) Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?

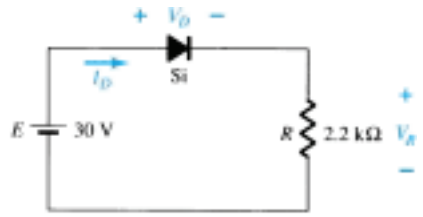


Figure 2.133 Problem 4

5. Determine the current I for each of the configurations of Fig. 2.134 using the approximate equivalent model for the diode.

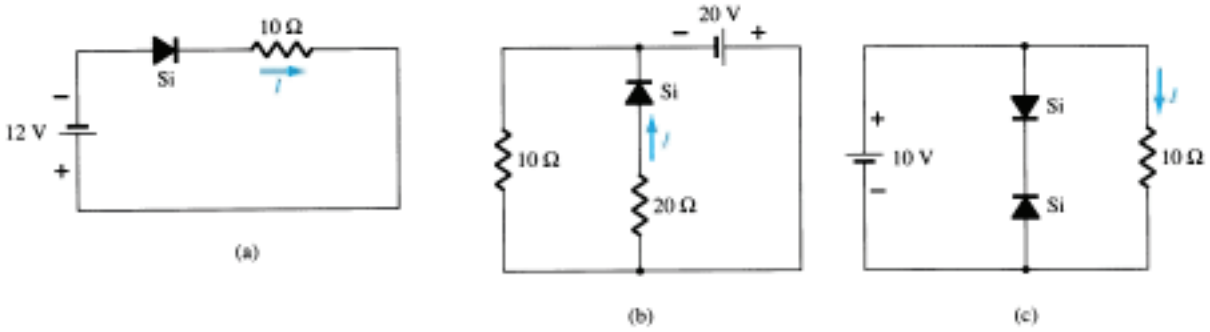


Figure 2.134 Problem 5

6. Determine V_o and I_D for the networks of Fig. 2.135.

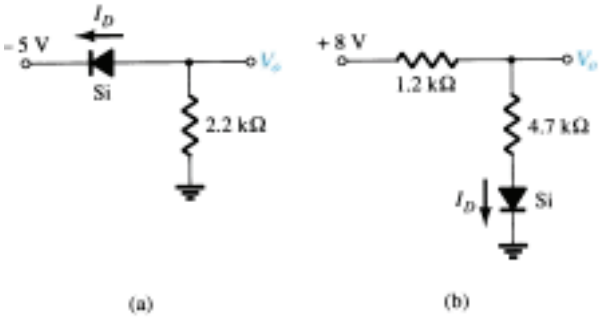


Figure 2.135 Problems 6, 49

* **7.** Determine the level of V_o for each network of Fig. 2.136.

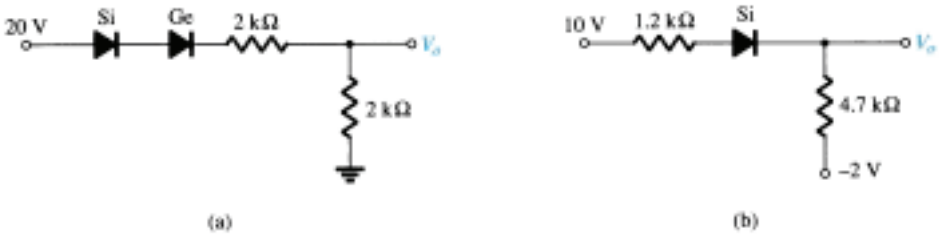


Figure 2.136 Problem 7

* **8.** Determine V_o and I_D for the networks of Fig. 2.137.

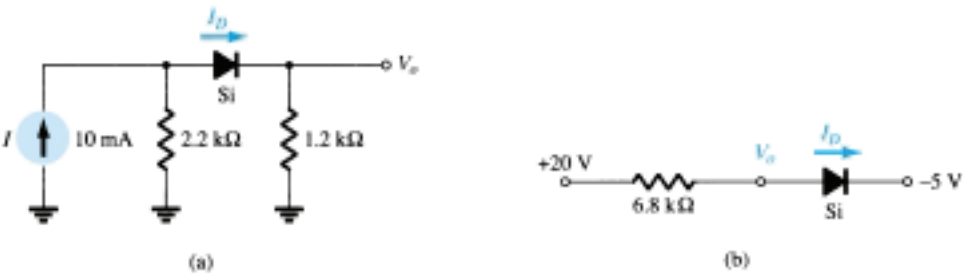


Figure 2.137 Problem 8

* **9.** Determine V_{o_1} and V_{o_2} for the networks of Fig. 2.138.

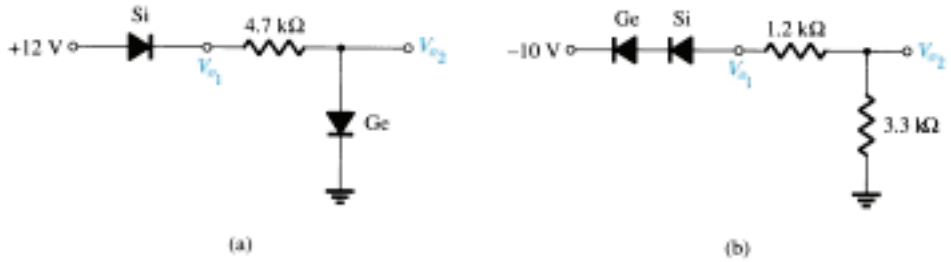


Figure 2.138 Problem 9

§ 2.5 Parallel and Series–Parallel Configurations

10. Determine V_o and I_D for the networks of Fig. 2.139.

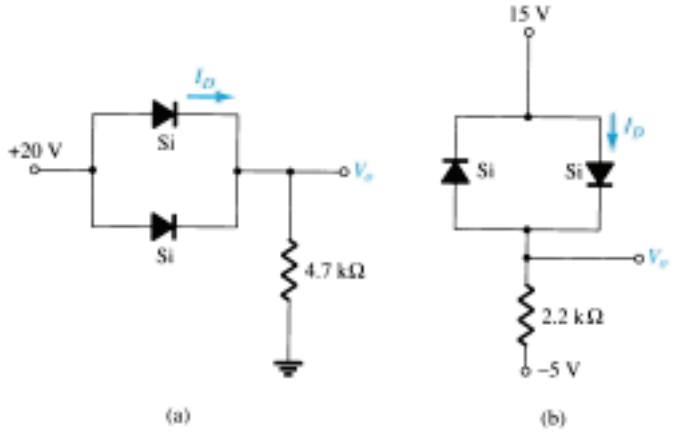


Figure 2.139 Problems 10, 50

* **11.** Determine V_o and I for the networks of Fig. 2.140.

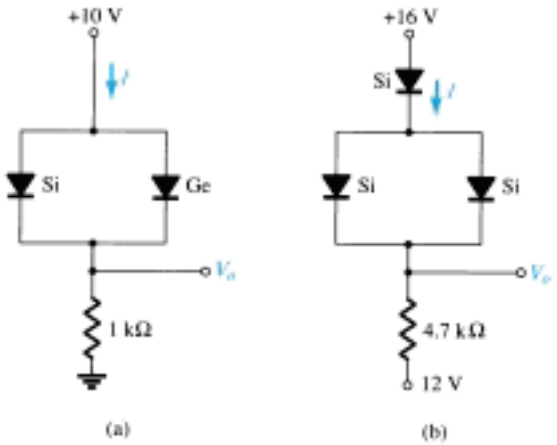


Figure 2.140 Problem 11

12. Determine V_{o_1}, V_{o_2}, and I for the network of Fig. 2.141.

* 13. Determine V_o and I_D for the network of Fig. 2.142.

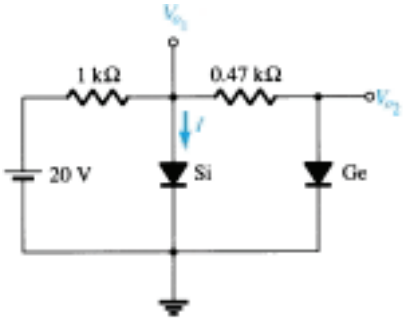


Figure 2.141 Problem 12

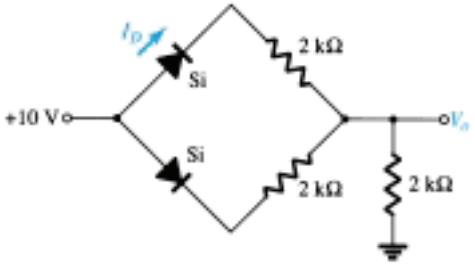


Figure 2.142 Problems 13, 51

§ 2.6 AND/OR Gates

14. Determine V_o for the network of Fig. 2.38 with 0 V on both inputs.
15. Determine V_o for the network of Fig. 2.38 with 10 V on both inputs.
16. Determine V_o for the network of Fig. 2.41 with 0 V on both inputs.
17. Determine V_o for the network of Fig. 2.41 with 10 V on both inputs.
18. Determine V_o for the negative logic OR gate of Fig. 2.143.
19. Determine V_o for the negative logic AND gate of Fig. 2.144.
20. Determine the level of V_o for the gate of Fig. 2.145.
21. Determine V_o for the configuration of Fig. 2.146.

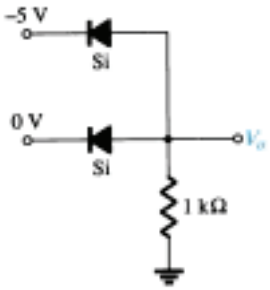


Figure 2.143 Problem 18

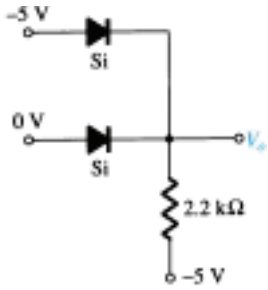


Figure 2.144 Problem 19

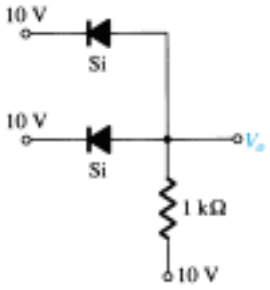


Figure 2.145 Problem 20

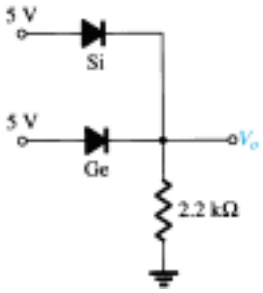


Figure 2.146 Problem 21

§ 2.7 Sinusoidal Inputs; Half-Wave Rectification

22. Assuming an ideal diode, sketch v_i, v_d, and i_d for the half-wave rectifier of Fig. 2.147. The input is a sinusoidal waveform with a frequency of 60 Hz

* 23. Repeat Problem 22 with a silicon diode ($V_T = 0.7$ V).

* 24. Repeat Problem 22 with a 6.8-kΩ load applied as shown in Fig. 2.148. Sketch v_L and i_L.

25. For the network of Fig. 2.149, sketch v_o and determine V_{dc}.

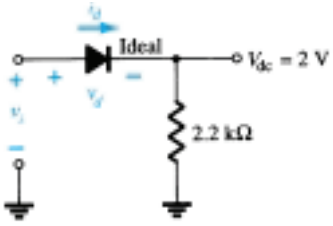


Figure 2.147 Problems 22, 23, 24

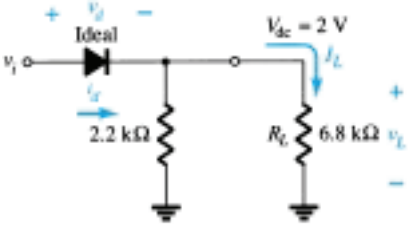


Figure 2.148 Problem 24

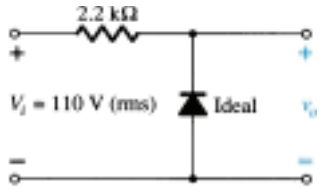


Figure 2.149 Problem 25

* **26.** For the network of Fig. 2.150, sketch v_o and i_R.

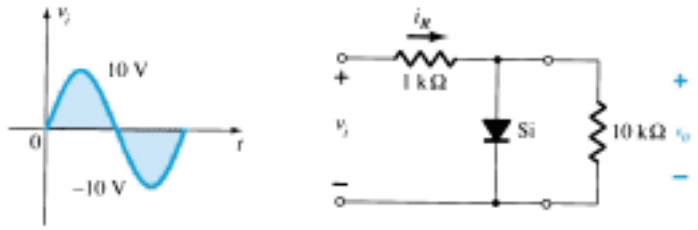


Figure 2.150 Problem 26

* **27.** (a) Given $P_{max} = 14$ mW for each diode of Fig. 2.151, determine the maximum current rating of each diode (using the approximate equivalent model).
(b) Determine I_{max} for $V_{i_{max}} = 160$ V.
(c) Determine the current through each diode at $V_{i_{max}}$ using the results of part (b).
(e) If only one diode were present, determine the diode current and compare it to the maximum rating.

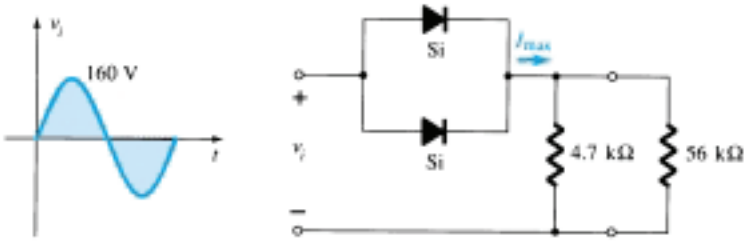


Figure 2.151 Problem 27

§ 2.8 Full-Wave Rectification

28. A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.
(a) If silicon diodes are employed, what is the dc voltage available at the load?
(b) Determine the required PIV rating of each diode.
(c) Find the maximum current through each diode during conduction.
(d) What is the required power rating of each diode?

29. Determine v_o and the required PIV rating of each diode for the configuration of Fig. 2.152.

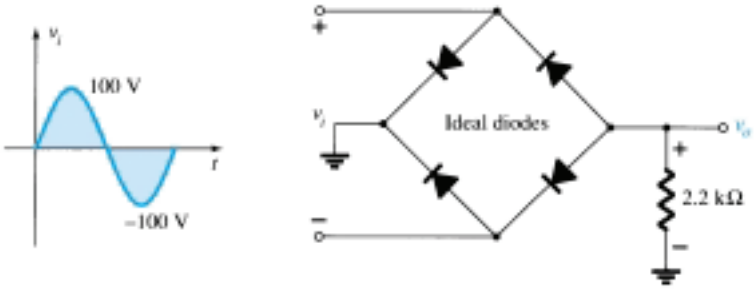


Figure 2.152 Problem 29

* **30.** Sketch v_o for the network of Fig. 2.153 and determine the dc voltage available.

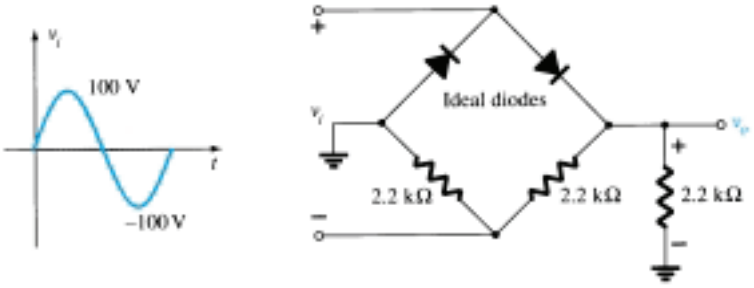


Figure 2.153 Problem 30

* **31.** Sketch v_o for the network of Fig. 2.154 and determine the dc voltage available.

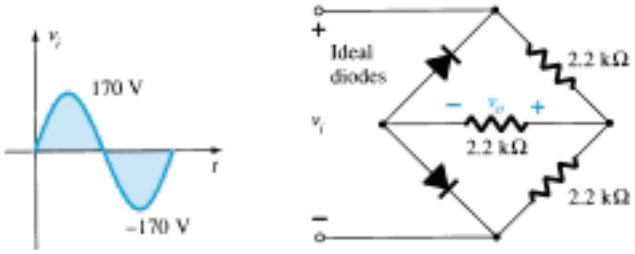


Figure 2.154 Problem 31

§ 2.9 Clippers

32. Determine v_o for each network of Fig. 2.155 for the input shown.

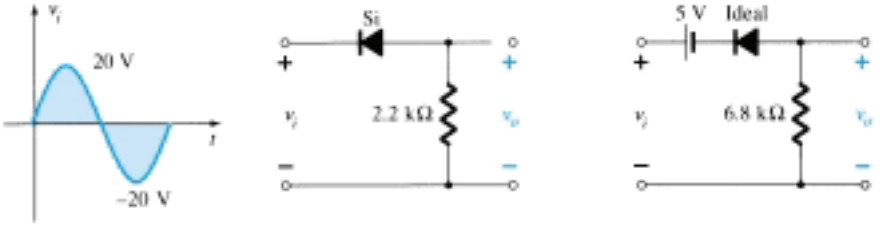


Figure 2.155 Problem 32

33. Determine v_o for each network of Fig. 2.156 for the input shown.

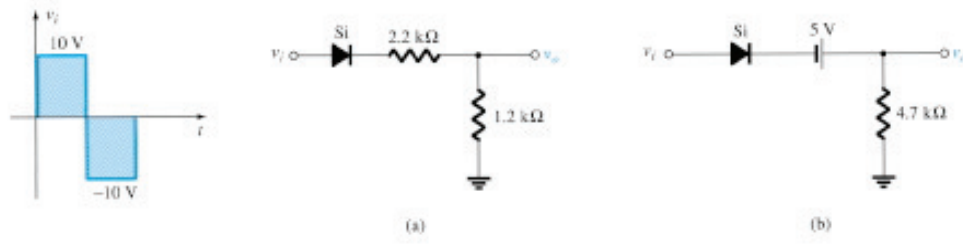


Figure 2.156 Problem 33

* **34.** Determine v_o for each network of Fig. 2.157 for the input shown.

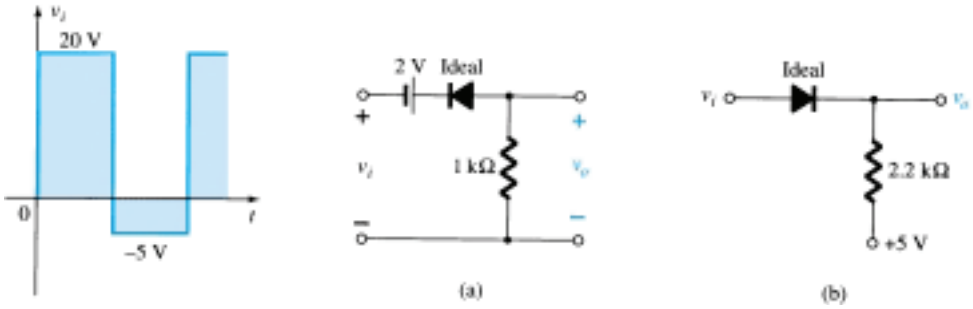


Figure 2.157 Problem 34

* **35.** Determine v_o for each network of Fig. 2.158 for the input shown.

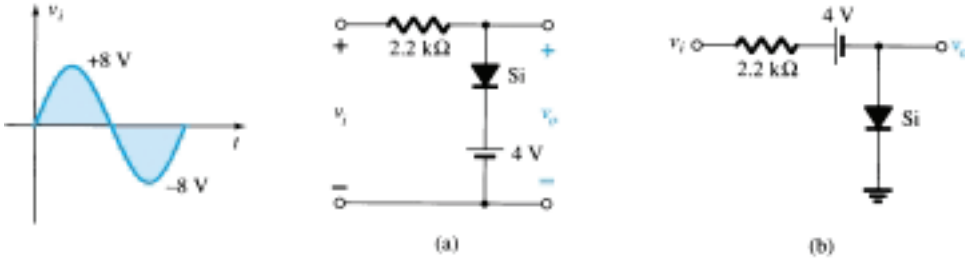


Figure 2.158 Problem 35

36. Sketch i_R and v_o for the network of Fig. 2.159 for the input shown.

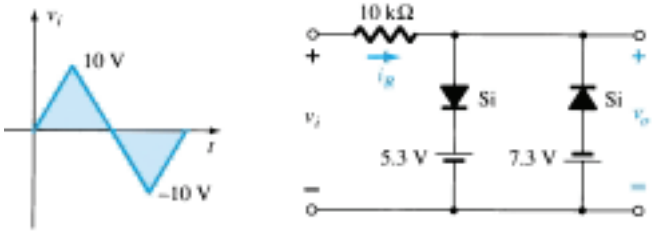


Figure 2.159 Problem 36

§ 2.10 Clampers

37. Sketch v_o for each network of Fig. 2.160 for the input shown.

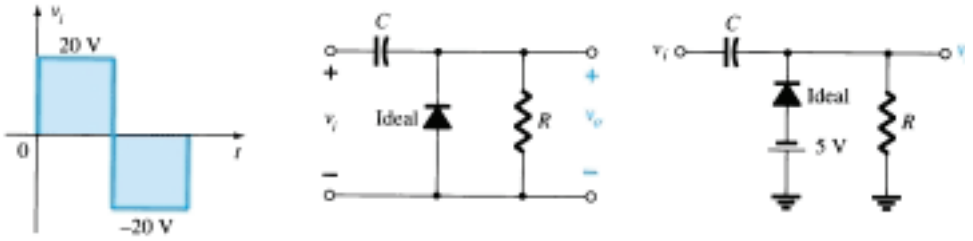


Figure 2.160 Problem 37

38. Sketch v_o for each network of Fig. 2.161 for the input shown. Would it be a good approximation to consider the diode to be ideal for both configurations? Why?

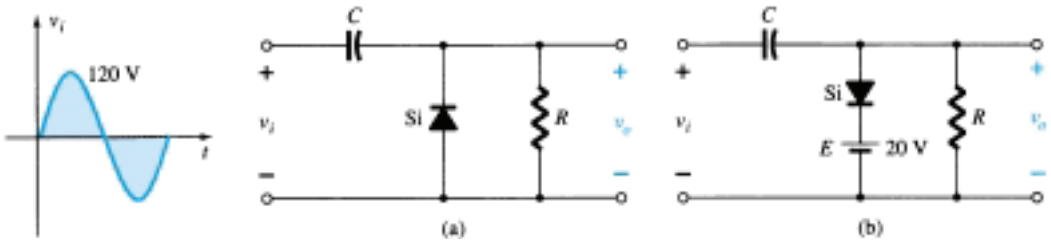


Figure 2.161 Problem 38

* **39.** For the network of Fig. 2.162:

(a) Calculate 5τ.

(b) Compare 5τ to half the period of the applied signal.

(c) Sketch v_o.

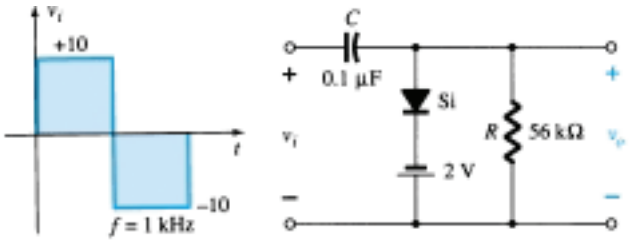


Figure 2.162 Problem 39

* **40.** Design a clamper to perform the function indicated in Fig. 2.163.

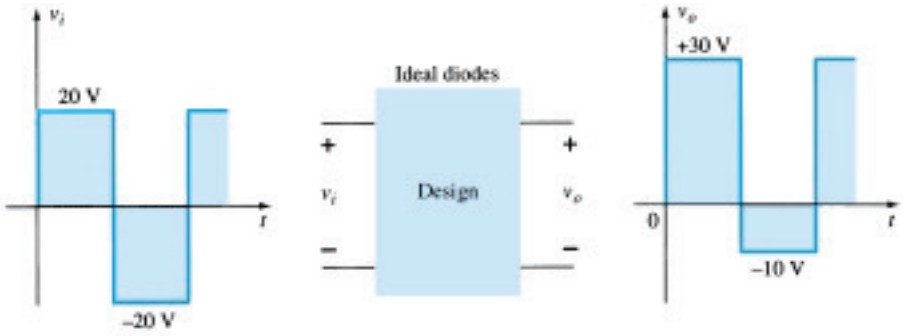


Figure 2.163 Problem 40

* **41.** Design a clamper to perform the function indicated in Fig. 2.164.

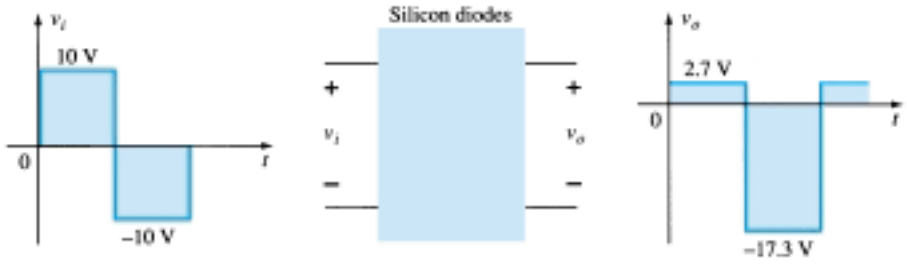


Figure 2.164 Problem 41

§ 2.11 Zener Diodes

* **42.** (a) Determine V_L, I_L, I_Z, and I_R for the network Fig. 2.165 if $R_L = 180\ \Omega$
(b) Repeat part (a) if $R_L = 470\ \Omega$.
(c) Determine the value of R_L that will establish maximum power conditions for the Zener diode.
(d) Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state.

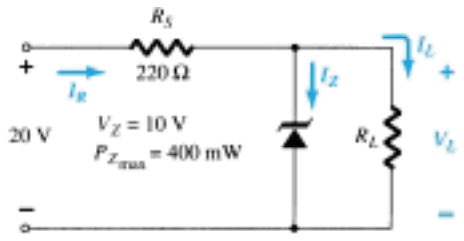


Figure 2.165 Problem 42

* **43.** (a) Design the network of Fig. 2.166 to maintain V_L at 12 V for a load variation (I_L) from 0 to 200 mA. That is, determine R_s and V_Z.
(b) Determine $P_{Z_{max}}$ for the Zener diode of part (a).

* **44.** For the network of Fig. 2.167, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the Zener diode.

45. Design a voltage regulator that will maintain an output voltage of 20 V across a 1-kΩ load with an input that will vary between 30 and 50 V. That is, determine the proper value of R_s and the maximum current I_{ZM}.

46. Sketch the output of the network of Fig. 2.120 if the input is a 50-V square wave. Repeat for a 5-V square wave.

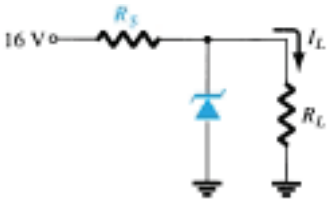


Figure 2.166 Problem 43

§ 2.12 Voltage-Multiplier Circuits

47. Determine the voltage available from the voltage doubler of Fig. 2.121 if the secondary voltage of the transformer is 120 V (rms).

48. Determine the required PIV ratings of the diodes of Fig. 2.121 in terms of the peak secondary voltage V_m.

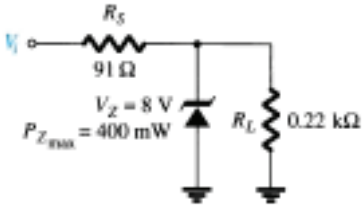


Figure 2.167 Problems 44, 52

§ 2.13 PSpice Windows

49. Perform an analysis of the network of Fig. 2.135 using PSpice Windows.

50. Perform an analysis of the network of Fig. 2.139 using PSpice Windows.

51. Perform an analysis of the network of Fig. 2.142 using PSpice Windows.

52. Perform a general analysis of the Zener network of Fig. 2.167 using PSpice Windows.

* Please Note: Asterisks indicate more difficult problems.

β

CHAPTER

3 Bipolar Junction Transistors

3.1 INTRODUCTION

During the period 1904–1947, the vacuum tube was undoubtedly the electronic device of interest and development. In 1904, the vacuum-tube diode was introduced by J. A. Fleming. Shortly thereafter, in 1906, Lee De Forest added a third element, called the *control grid,* to the vacuum diode, resulting in the first amplifier, the *triode.* In the following years, radio and television provided great stimulation to the tube industry. Production rose from about 1 million tubes in 1922 to about 100 million in 1937. In the early 1930s the four-element tetrode and five-element pentode gained prominence in the electron-tube industry. In the years to follow, the industry became one of primary importance and rapid advances were made in design, manufacturing techniques, high-power and high-frequency applications, and miniaturization.

On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Walter H. Brattain and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories. The original transistor (a point-contact transistor) is shown in Fig. 3.1. The advantages of this three-terminal solid-state device over the tube were immediately obvious: It was smaller

Co-inventors of the first transistor at Bell Laboratories: Dr. William Shockley (seated); Dr. John Bardeen (left); Dr. Walter H. Brattain. (Courtesy of AT&T Archives.)

Dr. Shockley Born: London, England, 1910
PhD Harvard, 1936

Dr. Bardeen Born: Madison, Wisconsin, 1908
PhD Princeton, 1936

Dr. Brattain Born: Amoy, China, 1902
PhD University of Minnesota, 1928

All shared the Nobel Prize in 1956 for this contribution.

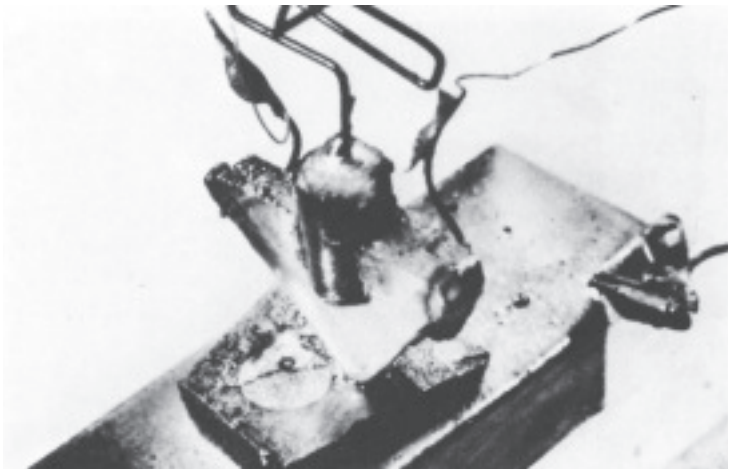


Figure 3.1 The first transistor. (Courtesy Bell Telephone Laboratories.)

and lightweight; had no heater requirement or heater loss; had rugged construction; and was more efficient since less power was absorbed by the device itself; it was instantly available for use, requiring no warm-up period; and lower operating voltages were possible. Note in the discussion above that this chapter is our first discussion of devices with three or more terminals. You will find that all amplifiers (devices that increase the voltage, current, or power level) will have at least three terminals with one controlling the flow between two other terminals.

3.2 TRANSISTOR CONSTRUCTION

The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material. The former is called an *npn transistor,* while the latter is called a *pnp transistor.* Both are shown in Fig. 3.2 with the proper dc biasing. We will find in Chapter 4 that the dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, the base lightly doped, and the collector only lightly doped. The outer layers have widths much greater than the sandwiched *p*- or *n*-type material. For the transistors shown in Fig. 3.2 the ratio of the total width to that of the center layer is 0.150/0.001 = 150:1. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10:1 or less). This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of "free" carriers.

For the biasing shown in Fig. 3.2 the terminals have been indicated by the capital letters *E* for *emitter, C* for *collector,* and *B* for *base.* An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor. The abbreviation BJT, from *bipolar junction transistor,* is often applied to this three-terminal device. The term *bipolar* reflects the fact that holes *and* electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a *unipolar* device. The Schottky diode of Chapter 20 is such a device.

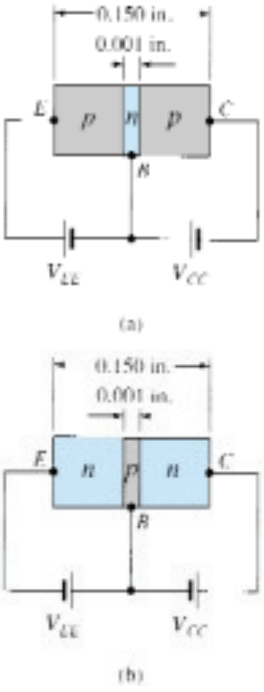


Figure 3.2 Types of transistors: (a) *pnp*; (b) *npn*.

3.3 TRANSISTOR OPERATION

The basic operation of the transistor will now be described using the *pnp* transistor of Fig. 3.2a. The operation of the *npn* transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 3.3 the *pnp* transistor has been redrawn without the base-to-collector bias. Note the similarities between this situation and that of the *forward-biased* diode in Chapter 1. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *p*- to the *n*-type material.

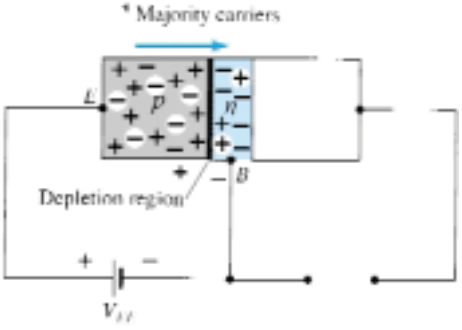


Figure 3.3 Forward-biased junction of a *pnp* transistor.

β

Let us now remove the base-to-emitter bias of the *pnp* transistor of Fig. 3.2a as shown in Fig. 3.4. Consider the similarities between this situation and that of the *reverse-biased* diode of Section 1.6. Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 3.4. In summary, therefore:

One p-n junction of a transistor is reverse biased, while the other is forward biased.

In Fig. 3.5 both biasing potentials have been applied to a *pnp* transistor, with the resulting majority- and minority-carrier flow indicated. Note in Fig. 3.5 the widths of the depletion regions, indicating clearly which junction is forward-biased and which is reverse-biased. As indicated in Fig. 3.5, a large number of majority carriers will diffuse across the forward-biased *p-n* junction into the *n*-type material. The question then is whether these carriers will contribute directly to the base current I_B or pass directly into the *p*-type material. Since the sandwiched *n*-type material is very thin and has a low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically on the order of microamperes as compared to milliamperes for the emitter and collector currents. The larger number of these majority carriers will diffuse across the reverse-biased junction into the *p*-type material connected to the collector terminal as indicated in Fig. 3.5. The reason for the relative ease with which the majority carriers can cross the reverse-biased junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the *n*-type material. In other words, there has been an *injection* of minority carriers into the *n*-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. 3.5.

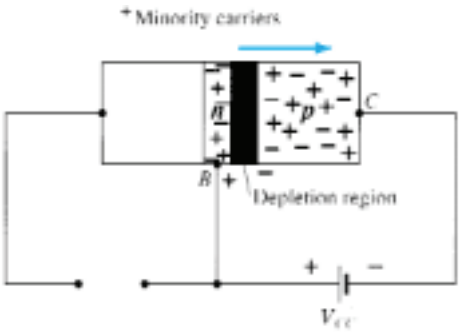


Figure 3.4 Reverse-biased junction of a *pnp* transistor.

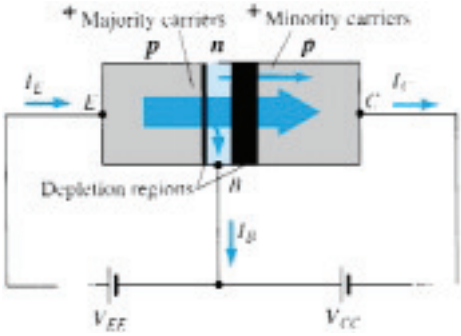


Figure 3.5 Majority and minority carrier flow of a *pnp* transistor.

Applying Kirchhoff's current law to the transistor of Fig. 3.5 as if it were a single node, we obtain

$$I_E = I_C + I_B \tag{3.1}$$

and find that the emitter current is the sum of the collector and base currents. The collector current, however, is comprised of two components—the majority and minority carriers as indicated in Fig. 3.5. The minority-current component is called the *leakage current* and is given the symbol I_{CO} (I_C current with emitter terminal *O*pen). The collector current, therefore, is determined in total by Eq. (3.2).

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}} \tag{3.2}$$

For general-purpose transistors, I_C is measured in milliamperes, while I_{CO} is measured in microamperes or nanoamperes. I_{CO}, like I_s for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of I_{CO}, to the point where its effect can often be ignored.

3.4 COMMON-BASE CONFIGURATION

The notation and symbols used in conjunction with the transistor in the majority of texts and manuals published today are indicated in Fig. 3.6 for the common-base configuration with *pnp* and *npn* transistors. The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential. Throughout this book all current directions will refer to conventional (hole) flow rather than electron flow. This choice was based primarily on the fact that the vast amount of literature available at educational and industrial institutions employs conventional flow and the arrows in all electronic symbols have a direction defined by this convention. Recall that the arrow in the diode symbol defined the direction of conduction for conventional current. For the transistor:

The arrow in the graphic symbol defines the direction of emitter current (conventional flow) through the device.

All the current directions appearing in Fig. 3.6 are the actual directions as defined by the choice of conventional flow. Note in each case that $I_E = I_C + I_B$. Note also that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch. That is, compare the direction of I_E to the polarity or V_{EE} for each configuration and the direction of I_C to the polarity of V_{CC}.

To fully describe the behavior of a three-terminal device such as the common-base amplifiers of Fig. 3.6 requires two sets of characteristics—one for the *driving point* or *input* parameters and the other for the *output* side. The input set for the common-base amplifier as shown in Fig. 3.7 will relate an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

The output set will relate an output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E) as shown in Fig. 3.8. The output or *collector* set of characteristics has three basic regions of interest, as indicated in Fig. 3.8: the *active,*

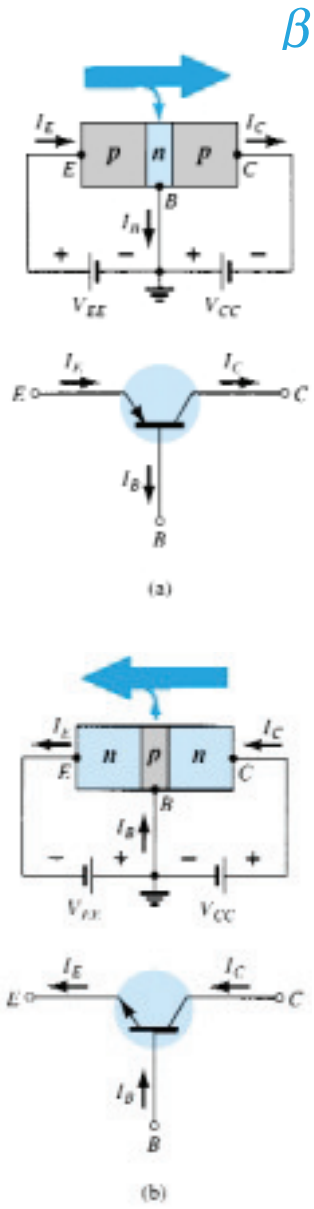


Figure 3.6 Notation and symbols used with the common-base configuration: (a) *pnp* transistor; (b) *npn* transistor.

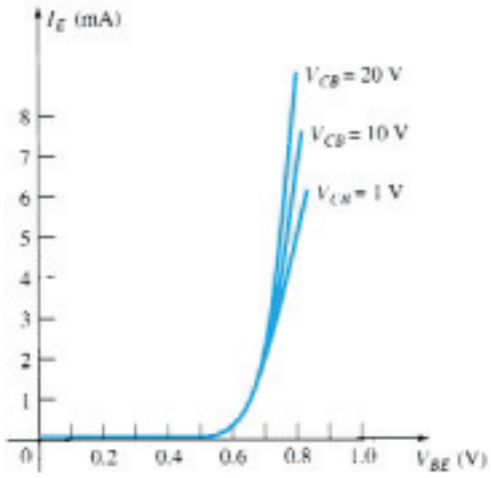


Figure 3.7 Input or driving point characteristics for a common-base silicon transistor amplifier.

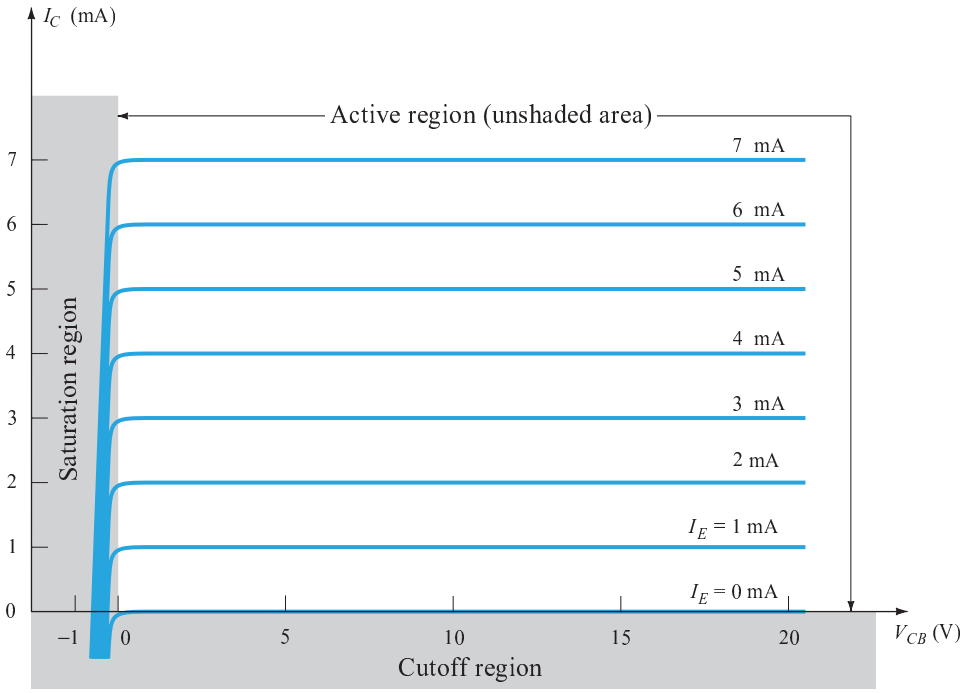


Figure 3.8 Output or collector characteristics for a common-base transistor amplifier.

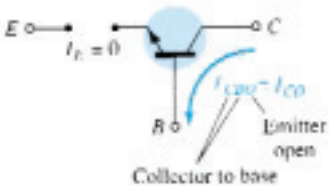


Figure 3.9 Reverse saturation current.

cutoff, and *saturation* regions. The active region is the region normally employed for linear (undistorted) amplifiers. In particular:

In the active region the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.

The active region is defined by the biasing arrangements of Fig. 3.6. At the lower end of the active region the emitter current (I_E) is zero, the collector current is simply that due to the reverse saturation current I_{CO}, as indicated in Fig. 3.8. The current I_{CO} is so small (microamperes) in magnitude compared to the vertical scale of I_C (milliamperes) that it appears on virtually the same horizontal line as $I_C = 0$. The circuit conditions that exist when $I_E = 0$ for the common-base configuration are shown in Fig. 3.9. The notation most frequently used for I_{CO} on data and specification sheets is, as indicated in Fig. 3.9, I_{CBO}. Because of improved construction techniques, the level of I_{CBO} for general-purpose transistors (especially silicon) in the low- and mid-power ranges is usually so low that its effect can be ignored. However, for higher power units I_{CBO} will still appear in the microampere range. In addition, keep in mind that I_{CBO}, like I_s, for the diode (both reverse leakage currents) is temperature sensitive. At higher temperatures the effect of I_{CBO} may become an important factor since it increases so rapidly with temperature.

Note in Fig. 3.8 that as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor-current relations. Note also the almost negligible effect of V_{CB} on the collector current for the active region. The curves clearly indicate that *a first approximation to the relationship between I_E and I_C in the active region is given by*

$$I_C \cong I_E \tag{3.3}$$

As inferred by its name, the cutoff region is defined as that region where the collector current is 0 A, as revealed on Fig. 3.8. In addition:

In the cutoff region the collector-base and base-emitter junctions of a transistor are both reverse-biased.

The saturation region is defined as that region of the characteristics to the left of $V_{CB} = 0$ V. The horizontal scale in this region was expanded to clearly show the dramatic change in characteristics in this region. Note the exponential increase in collector current as the voltage V_{CB} increases toward 0 V.

In the saturation region the collector-base and base-emitter junctions are forward-biased.

The input characteristics of Fig. 3.7 reveal that for fixed values of collector voltage (V_{CB}), as the base-to-emitter voltage increases, the emitter current increases in a manner that closely resembles the diode characteristics. In fact, increasing levels of V_{CB} have such a small effect on the characteristics that as a first approximation the change due to changes in V_{CB} can be ignored and the characteristics drawn as shown in Fig. 3.10a. If we then apply the piecewise-linear approach, the characteristics of Fig. 3.10b will result. Taking it a step further and ignoring the slope of the curve and therefore the resistance associated with the forward-biased junction will result in the characteristics of Fig. 3.10c. For the analysis to follow in this book the equivalent model of Fig. 3.10c will be employed for all dc analysis of transistor networks. That is, once a transistor is in the "on" state, the base-to-emitter voltage will be assumed to be the following:

$$V_{BE} = 0.7 \text{ V} \tag{3.4}$$

In other words, the effect of variations due to V_{CB} and the slope of the input characteristics will be ignored as we strive to analyze transistor networks in a manner that will provide a good approximation to the actual response without getting too involved with parameter variations of less importance.

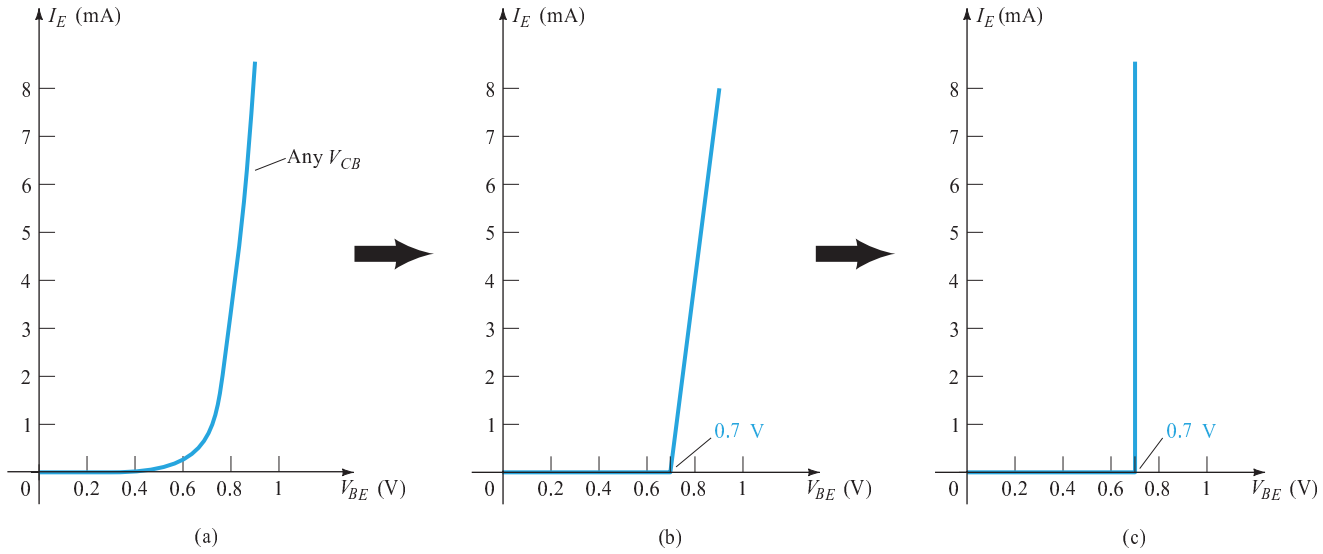


Figure 3.10 Developing the equivalent model to be employed for the base-to-emitter region of an amplifier in the dc mode.

It is important to fully appreciate the statement made by the characteristics of Fig. 3.10c. They specify that with the transistor in the "on" or active state the voltage from base to emitter will be 0.7 V at *any* level of emitter current as controlled by the external network. In fact, at the first encounter of any transistor configuration in the dc mode, one can now immediately specify that the voltage from base to emitter is 0.7 V if the device is in the active region—a very important conclusion for the dc analysis to follow.

EXAMPLE 3.1

(a) Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 3$ mA and $V_{CB} = 10$ V.
(b) Using the characteristics of Fig. 3.8, determine the resulting collector current if I_E remains at 3 mA but V_{CB} is reduced to 2 V.
(c) Using the characteristics of Figs. 3.7 and 3.8, determine V_{BE} if $I_C = 4$ mA and $V_{CB} = 20$ V.
(d) Repeat part (c) using the characteristics of Figs. 3.8 and 3.10c.

Solution

(a) The characteristics clearly indicate that $I_C \cong I_E = \mathbf{3\ mA}$.
(b) The effect of changing V_{CB} is negligible and I_C continues to be **3 mA.**
(c) From Fig. 3.8, $I_E \cong I_C = 4$ mA. On Fig. 3.7 the resulting level of V_{BE} is about **0.74 V.**
(d) Again from Fig. 3.8, $I_E \cong I_C = 4$ mA. However, on Fig. 3.10c, V_{BE} is **0.7 V** for any level of emitter current.

Alpha (α)

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

$$\alpha_{dc} = \frac{I_C}{I_E} \tag{3.5}$$

where I_C and I_E are the levels of current at the point of operation. Even though the characteristics of Fig. 3.8 would suggest that $\alpha = 1$, for practical devices the level of alpha typically extends from 0.90 to 0.998, with most approaching the high end of the range. Since alpha is defined solely for the majority carriers, Eq. (3.2) becomes

$$I_C = \alpha I_E + I_{CBO} \tag{3.6}$$

For the characteristics of Fig. 3.8 when $I_E = 0$ mA, I_C is therefore equal to I_{CBO}, but as mentioned earlier, the level of I_{CBO} is usually so small that it is virtually undetectable on the graph of Fig. 3.8. In other words, when $I_E = 0$ mA on Fig. 3.8, I_C also appears to be 0 mA for the range of V_{CB} values.

For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{constant}} \tag{3.7}$$

The ac alpha is formally called the *common-base, short-circuit, amplification factor,* for reasons that will be more obvious when we examine transistor equivalent circuits in Chapter 7. For the moment, recognize that Eq. (3.7) specifies that a relatively small change in collector current is divided by the corresponding change in I_E with the collector-to-base voltage held constant. For most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for the other. The use of an equation such as (3.7) will be demonstrated in Section 3.6.

Biasing

The proper biasing of the common-base configuration in the active region can be determined quickly using the approximation $I_C \cong I_E$ and assuming for the moment that

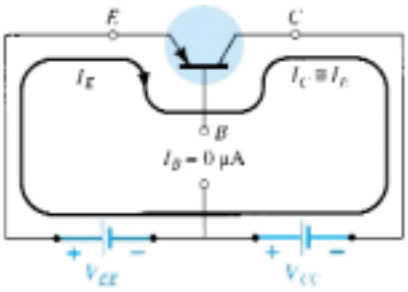


Figure 3.11 Establishing the proper biasing management for a common-base *pnp* transistor in the active region.

$I_B \cong 0\ \mu A$. The result is the configuration of Fig. 3.11 for the *pnp* transistor. The arrow of the symbol defines the direction of conventional flow for $I_E \cong I_C$. The dc supplies are then inserted with a polarity that will support the resulting current direction. For the *npn* transistor the polarities will be reversed.

Some students feel that they can remember whether the arrow of the device symbol in pointing in or out by matching the letters of the transistor type with the appropriate letters of the phrases "pointing in" or "not pointing in." For instance, there is a match between the letters *npn* and the italic letters of *n*ot *p*ointing i*n* and the letters *pnp* with *p*ointing i*n*.

3.5 TRANSISTOR AMPLIFYING ACTION

Now that the relationship between I_C and I_E has been established in Section 3.4, the basic amplifying action of the transistor can be introduced on a surface level using the network of Fig. 3.12. The dc biasing does not appear in the figure since our interest will be limited to the ac response. For the common-base configuration the ac input resistance determined by the characteristics of Fig. 3.7 is quite small and typically varies from 10 to 100 Ω. The output resistance as determined by the curves of Fig. 3.8 is quite high (the more horizontal the curves the higher the resistance) and typically varies from 50 kΩ to 1 MΩ (100 kΩ for the transistor of Fig. 3.12). The difference in resistance is due to the forward-biased junction at the input (base to emitter) and the reverse-biased junction at the output (base to collector). Using a common value of 20 Ω for the input resistance, we find that

$$I_i = \frac{V_i}{R_i} = \frac{200\ \text{mV}}{20\ \Omega} = \mathbf{10\ mA}$$

If we assume for the moment that $\alpha_{ac} = 1$ ($I_c = I_e$),

$$I_L = I_i = 10\ \text{mA}$$

and

$$V_L = I_L R$$
$$= (10\ \text{mA})(5\ \text{k}\Omega)$$
$$= \mathbf{50\ V}$$

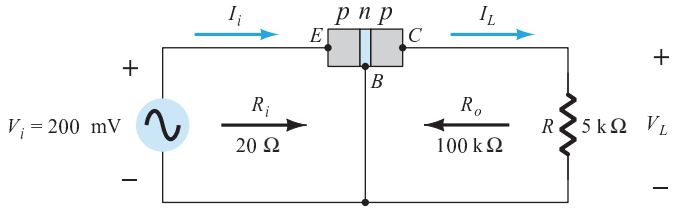


Figure 3.12 Basic voltage amplification action of the common-base configuration.

β

The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50\text{ V}}{200\text{ mV}} = \mathbf{250}$$

Typical values of voltage amplification for the common-base configuration vary from 50 to 300. The current amplification (I_C/I_E) is always less than 1 for the common-base configuration. This latter characteristic should be obvious since $I_C = \alpha I_E$ and α is always less than 1.

The basic amplifying action was produced by transferring a current I from a low- to a high-*resistance* circuit. The combination of the two terms in italics results in the label *transistor;* that is,

$$\textit{trans}\text{fer} + \text{re}\textit{sistor} \rightarrow \textit{transistor}$$

3.6 COMMON-EMITTER CONFIGURATION

The most frequently encountered transistor configuration appears in Fig. 3.13 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* since the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the *input* or *base-emitter* circuit and one for the *output* or *collector-emitter* circuit. Both are shown in Fig. 3.14.

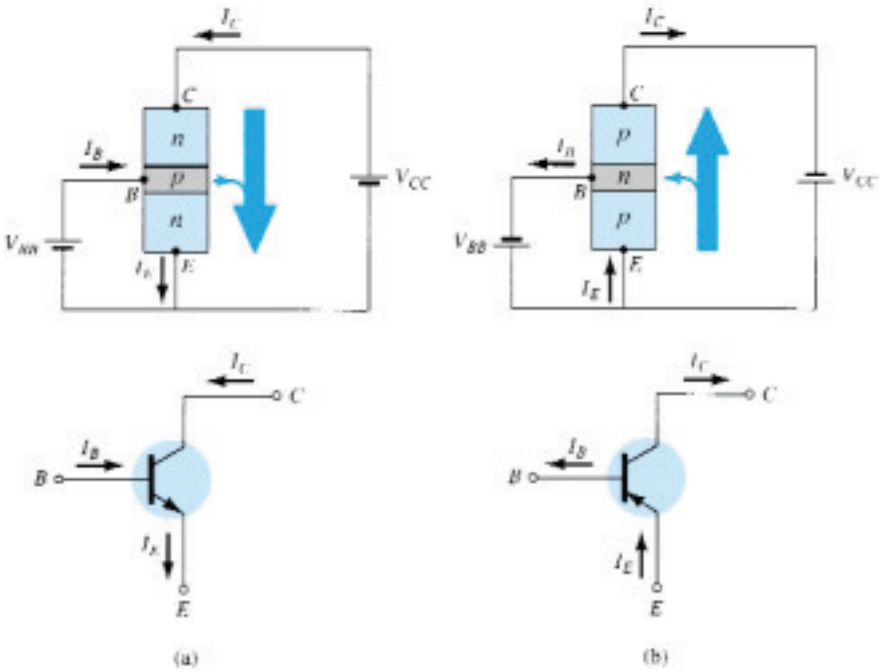


Figure 3.13 Notation and symbols used with the common-emitter configuration: (a) *npn* transistor; (b) *pnp* transistor.

The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. That is, $I_E = I_C + I_B$ and $I_C = \alpha I_E$.

For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

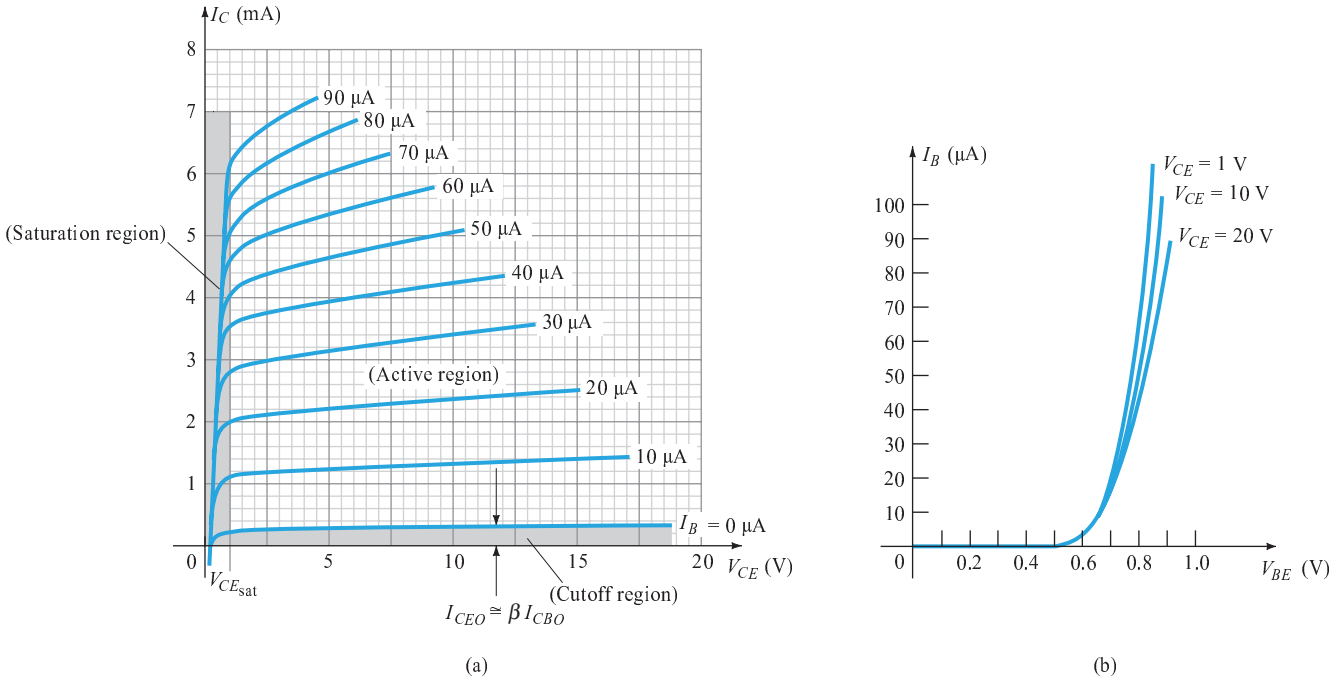


Figure 3.14 Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

Note that on the characteristics of Fig. 3.14 the magnitude of I_B is in microamperes, compared to milliamperes of I_C. Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common-base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for I_B are nearly straight and equally spaced. In Fig. 3.14a this region exists to the right of the vertical dashed line at $V_{CE_{sat}}$ and above the curve for I_B equal to zero. The region to the left of $V_{CE_{sat}}$ is called the saturation region.

In the active region of a common-emitter amplifier the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.

You will recall that these were the same conditions that existed in the active region of the common-base configuration. The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.

The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration. Note on the collector characteristics of Fig. 3.14 that I_C is not equal to zero when I_B is zero. For the common-base configuration, when the input current I_E was equal to zero, the collector current was equal only to the reverse saturation current I_{CO}, so that the curve $I_E = 0$ and the voltage axis were, for all practical purposes, one.

The reason for this difference in collector characteristics can be derived through the proper manipulation of Eqs. (3.3) and (3.6). That is,

$$\text{Eq. (3.6):} \quad I_C = \alpha I_E + I_{CBO}$$

Substitution gives $$\text{Eq. (3.3):} \quad I_C = \alpha(I_C + I_B) + I_{CBO}$$

Rearranging yields

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha} \tag{3.8}$$

If we consider the case discussed above, where $I_B = 0$ A, and substitute a typical value of α such as 0.996, the resulting collector current is the following:

$$I_C = \frac{\alpha(0\text{ A})}{1-\alpha} + \frac{I_{CBO}}{1-0.996}$$

$$= \frac{I_{CBO}}{0.004} = 250I_{CBO}$$

If I_{CBO} were 1 μA, the resulting collector current with $I_B = 0$ A would be 250(1 μA) = 0.25 mA, as reflected in the characteristics of Fig. 3.14.

For future reference, the collector current defined by the condition $I_B = 0$ μA will be assigned the notation indicated by Eq. (3.9).

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha}\bigg|_{I_B = 0\ \mu A} \tag{3.9}$$

In Fig. 3.15 the conditions surrounding this newly defined current are demonstrated with its assigned reference direction.

For linear (least distortion) amplification purposes, cutoff for the common-emitter configuration will be defined by $I_C = I_{CEO}$.

In other words, the region below $I_B = 0$ μA is to be avoided if an undistorted output signal is required.

When employed as a switch in the logic circuitry of a computer, a transistor will have two points of operation of interest: one in the cutoff and one in the saturation region. The cutoff condition should ideally be $I_C = 0$ mA for the chosen V_{CE} voltage. Since I_{CEO} is typically low in magnitude for silicon materials, *cutoff will exist for switching purposes when $I_B = 0$ μA or $I_C = I_{CEO}$ for silicon transistors only. For germanium transistors, however, cutoff for switching purposes will be defined as those conditions that exist when $I_C = I_{CBO}$*. This condition can normally be obtained for germanium transistors by reverse-biasing the base-to-emitter junction a few tenths of a volt.

Recall for the common-base configuration that the input set of characteristics was approximated by a straight-line equivalent that resulted in $V_{BE} = 0.7$ V for any level of I_E greater than 0 mA. For the common-emitter configuration the same approach can be taken, resulting in the approximate equivalent of Fig. 3.16. The result supports our earlier conclusion that for a transistor in the "on" or active region the base-to-emitter voltage is 0.7 V. In this case the voltage is fixed for any level of base current.

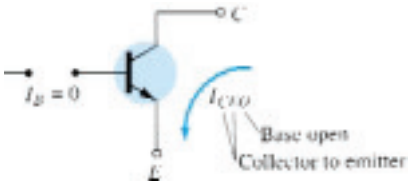


Figure 3.15 Circuit conditions related to I_{CEO}.

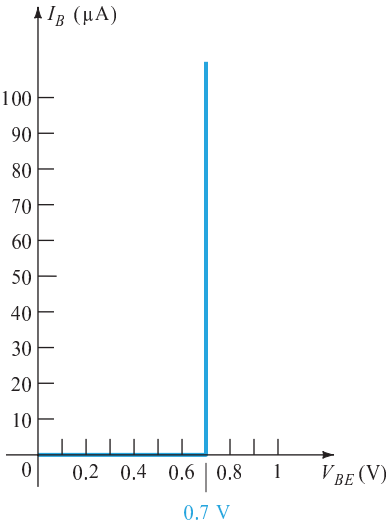


Figure 3.16 Piecewise-linear equivalent for the diode characteristics of Fig. 3.14b.

EXAMPLE 3.2

(a) Using the characteristics of Fig. 3.14, determine I_C at $I_B = 30\ \mu A$ and $V_{CE} = 10$ V.
(b) Using the characteristics of Fig. 3.14, determine I_C at $V_{BE} = 0.7$ V and $V_{CE} = 15$ V.

Solution

(a) At the intersection of $I_B = 30\ \mu A$ and $V_{CE} = 10$ V, $I_C = \mathbf{3.4\ mA}$.
(b) Using Fig. 3.14b, $I_B = 20\ \mu A$ at $V_{BE} = 0.7$ V. From Fig. 3.14a we find that $I_C = \mathbf{2.5\ mA}$ at the intersection of $I_B = 20\ \mu A$ and $V_{CE} = 15$ V.

Beta (β)

In the dc mode the levels of I_C and I_B are related by a quantity called *beta* and defined by the following equation:

$$\beta_{dc} = \frac{I_C}{I_B} \tag{3.10}$$

where I_C and I_B are determined at a particular operating point on the characteristics. For practical devices the level of β typically ranges from about 50 to over 400, with most in the midrange. As for α, β certainly reveals the relative magnitude of one current to the other. For a device with a β of 200, the collector current is 200 times the magnitude of the base current.

On specification sheets β_{dc} is usually included as h_{FE} with the h derived from an ac *h*ybrid equivalent circuit to be introduced in Chapter 7. The subscripts *FE* are derived from *f*orward-current amplification and common-*e*mitter configuration, respectively.

For ac situations an ac beta has been defined as follows:

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} \tag{3.11}$$

The formal name for β_{ac} is *common-emitter, forward-current, amplification factor.* Since the collector current is usually the output current for a common-emitter configuration and the base current the input current, the term *amplification* is included in the nomenclature above.

Equation (3.11) is similar in format to the equation for α_{ac} in Section 3.4. The procedure for obtaining α_{ac} from the characteristic curves was not described because of the difficulty of actually measuring changes of I_C and I_E on the characteristics. Equation (3.11), however, is one that can be described with some clarity, and in fact, the result can be used to find α_{ac} using an equation to be derived shortly.

On specification sheets β_{ac} is normally referred to as h_{fe}. Note that the only difference between the notation used for the dc beta, specifically, $\beta_{dc} = h_{FE}$, is the type of lettering for each subscript quantity. The lowercase letter h continues to refer to the hybrid equivalent circuit to be described in Chapter 7 and the *fe* to the *f*orward current gain in the common-*e*mitter configuration.

The use of Eq. (3.11) is best described by a numerical example using an actual set of characteristics such as appearing in Fig. 3.14a and repeated in Fig. 3.17. Let us determine β_{ac} for a region of the characteristics defined by an operating point of $I_B = 25\ \mu A$ and $V_{CE} = 7.5$ V as indicated on Fig. 3.17. The restriction of $V_{CE} =$ constant requires that a vertical line be drawn through the operating point at $V_{CE} = 7.5$ V. At any location on this vertical line the voltage V_{CE} is 7.5 V, a constant. The change

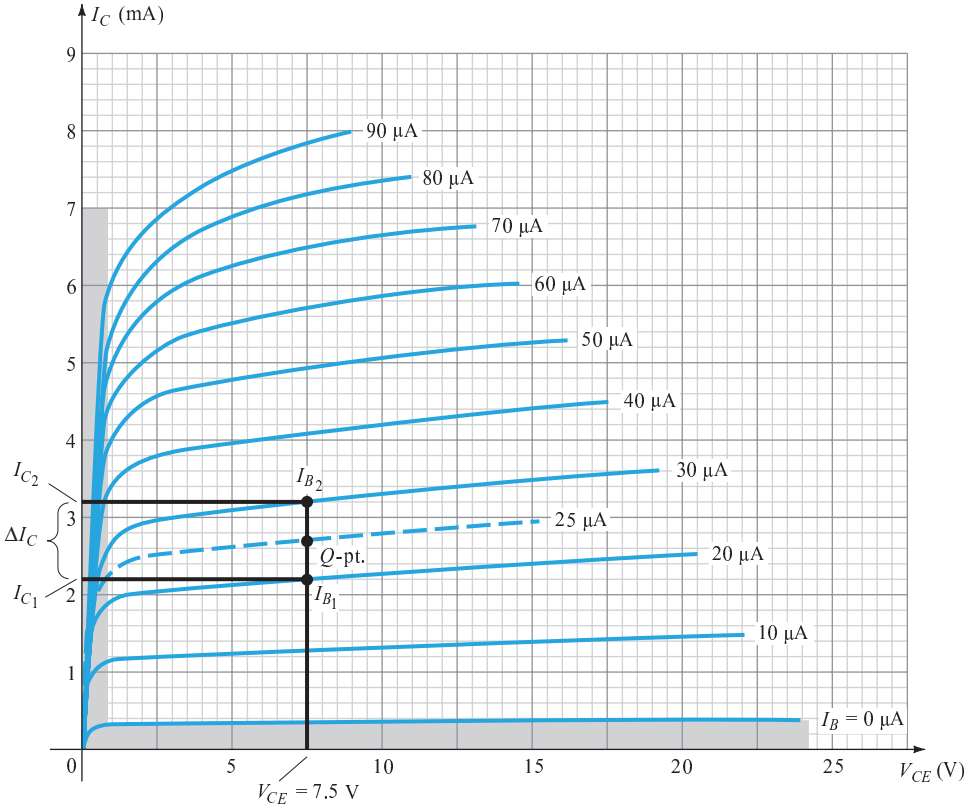


Figure 3.17 Determining β_{ac} and β_{dc} from the collector characteristics.

in I_B (ΔI_B) as appearing in Eq. (3.11) is then defined by choosing two points on either side of the Q-point along the vertical axis of about equal distances to either side of the Q-point. For this situation the $I_B = 20\ \mu A$ and $30\ \mu A$ curves meet the requirement without extending too far from the Q-point. They also define levels of I_B that are easily defined rather than have to interpolate the level of I_B between the curves. It should be mentioned that the best determination is usually made by keeping the chosen ΔI_B as small as possible. At the two intersections of I_B and the vertical axis, the two levels of I_C can be determined by drawing a horizontal line over to the vertical axis and reading the resulting values of I_C. The resulting β_{ac} for the region can then be determined by

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}$$

$$= \frac{3.2\ \text{mA} - 2.2\ \text{mA}}{30\ \mu\text{A} - 20\ \mu\text{A}} = \frac{1\ \text{mA}}{10\ \mu\text{A}}$$

$$= \mathbf{100}$$

The solution above reveals that for an ac input at the base, the collector current will be about 100 times the magnitude of the base current.

If we determine the dc beta at the Q-point:

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{2.7\ \text{mA}}{25\ \mu\text{A}} = \mathbf{108}$$

Although not exactly equal, the levels of β_{ac} and β_{dc} are usually reasonably close and are often used interchangeably. That is, if β_{ac} is known, it is assumed to be about the same magnitude as β_{dc}, and vice versa. Keep in mind that in the same lot, the value of β_{ac} will vary somewhat from one transistor to the next even though each transistor has the same number code. The variation may not be significant but for the majority of applications, it is certainly sufficient to validate the approximate approach above. Generally, the smaller the level of I_{CEO}, the closer the magnitude of the two betas. Since the trend is toward lower and lower levels of I_{CEO}, the validity of the foregoing approximation is further substantiated.

If the characteristics had the appearance of those appearing in Fig. 3.18, the level of β_{ac} would be the same in every region of the characteristics. Note that the step in I_B is fixed at 10 μA and the vertical spacing between curves is the same at every point in the characteristics—namely, 2 mA. Calculating the β_{ac} at the Q-point indicated will result in

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{9\ \text{mA} - 7\ \text{mA}}{45\ \mu\text{A} - 35\ \mu\text{A}} = \frac{2\ \text{mA}}{10\ \mu\text{A}} = \mathbf{200}$$

Determining the dc beta at the same Q-point will result in

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{8\ \text{mA}}{40\ \mu\text{A}} = \mathbf{200}$$

revealing that if the characteristics have the appearance of Fig. 3.18, the magnitude of β_{ac} and β_{dc} *will be the same* at every point on the characteristics. In particular, note that $I_{CEO} = 0\ \mu$A.

Although a true set of transistor characteristics will never have the exact appearance of Fig. 3.18, it does provide a set of characteristics for comparison with those obtained from a curve tracer (to be described shortly).

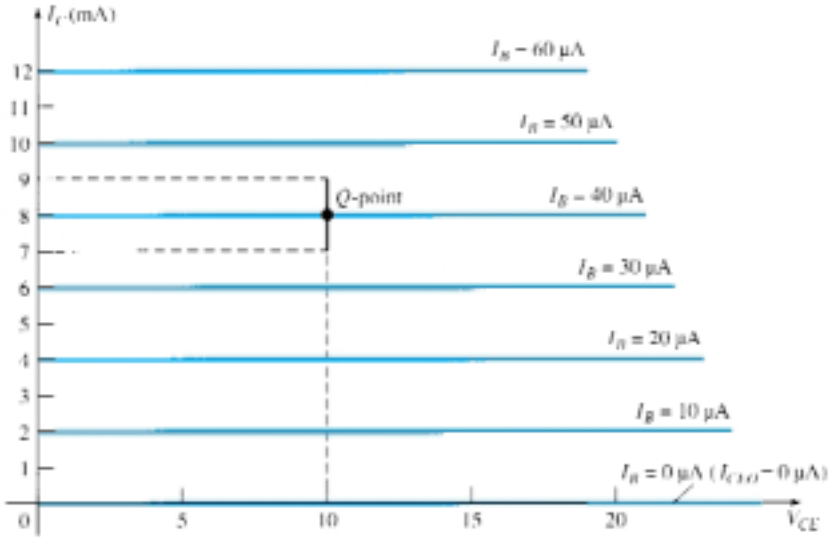


Figure 3.18 Characteristics in which β_{ac} is the same everywhere and $\beta_{ac} = \beta_{dc}$.

For the analysis to follow the subscript dc or ac will not be included with β to avoid cluttering the expressions with unnecessary labels. For dc situations it will simply be recognized as β_{dc} and for any ac analysis as β_{ac}. If a value of β is specified for a particular transistor configuration, it will normally be used for both the dc and ac calculations.

A relationship can be developed between β and α using the basic relationships introduced thus far. Using $\beta = I_C/I_B$ we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$ we have $I_E = I_C/\alpha$. Substituting into

$$I_E = I_C + I_B$$

we have

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

and dividing both sides of the equation by I_C will result in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\boxed{\alpha = \frac{\beta}{\beta + 1}} \tag{3.12a}$$

or

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \tag{3.12b}$$

In addition, recall that

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

but using an equivalence of

$$\frac{1}{1 - \alpha} = \beta + 1$$

derived from the above, we find that

$$I_{CEO} = (\beta + 1)I_{CBO}$$

or

$$\boxed{I_{CEO} \cong \beta I_{CBO}} \tag{3.13}$$

as indicated on Fig. 3.14a. Beta is a particularly important parameter because it provides a direct link between current levels of the input and output circuits for a common-emitter configuration. That is,

$$\boxed{I_C = \beta I_B} \tag{31.4}$$

and since

$$I_E = I_C + I_B$$
$$= \beta I_B + I_B$$

we have

$$\boxed{I_E = (\beta + 1)I_B} \tag{3.15}$$

Both of the equations above play a major role in the analysis in Chapter 4.

Biasing

The proper biasing of a common-emitter amplifier can be determined in a manner similar to that introduced for the common-base configuration. Let us assume that we are presented with an *npn* transistor such as shown in Fig. 3.19a and asked to apply the proper biasing to place the device in the active region.

The first step is to indicate the direction of I_E as established by the arrow in the transistor symbol as shown in Fig. 3.19b. Next, the other currents are introduced as

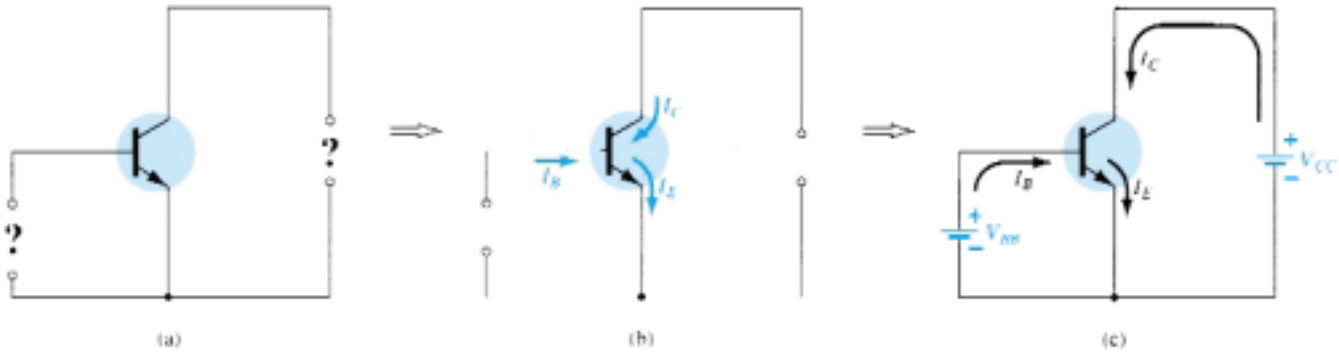


Figure 3.19 Determining the proper biasing arrangement for a common-emitter *npn* transistor configuration.

shown, keeping in mind the Kirchhoff's current law relationship: $I_C + I_B = I_E$. Finally, the supplies are introduced with polarities that will support the resulting directions of I_B and I_C as shown in Fig. 3.19c to complete the picture. The same approach can be applied to *pnp* transistors. If the transistor of Fig. 3.19 was a *pnp* transistor, all the currents and polarities of Fig. 3.19c would be reversed.

3.7 COMMON-COLLECTOR CONFIGURATION

The third and final transistor configuration is the *common-collector configuration,* shown in Fig. 3.20 with the proper current directions and voltage notation. The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

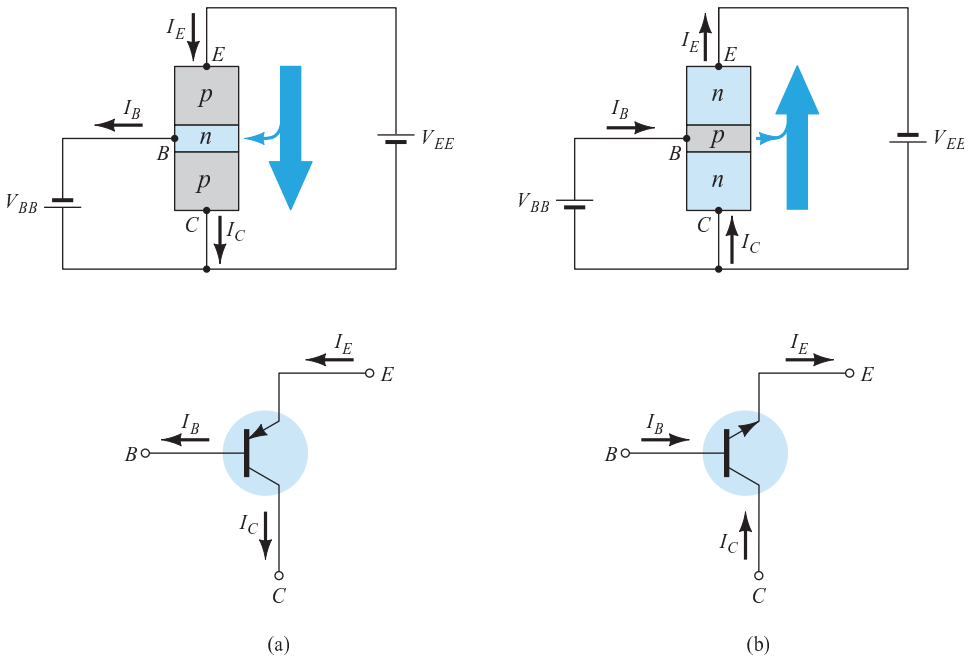


Figure 3.20 Notation and symbols used with the common-collector configuration: (a) *pnp* transistor; (b) *npn* transistor.

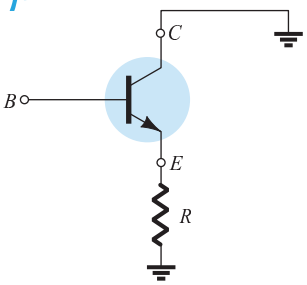


Figure 3.21 Common-collector configuration used for impedance-matching purposes.

A common-collector circuit configuration is provided in Fig. 3.21 with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration. From a design viewpoint, there is no need for a set of common-collector characteristics to choose the parameters of the circuit of Fig. 3.21. It can be designed using the common-emitter characteristics of Section 3.6. For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{EC} for a range of values of I_B. The input current, therefore, is the same for both the common-emitter and common-collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since $\alpha \cong 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

3.8 LIMITS OF OPERATION

For each transistor there is a region of operation on the characteristics which will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion. Such a region has been defined for the transistor characteristics of Fig. 3.22. All of the limits of operation are defined on a typical transistor specification sheet described in Section 3.9.

Some of the limits of operation are self-explanatory, such as maximum collector current (normally referred to on the specification sheet as *continuous* collector current) and maximum collector-to-emitter voltage (often abbreviated as V_{CEO} or $V_{(BR)CEO}$ on the specification sheet). For the transistor of Fig. 3.22, $I_{C_{max}}$ was specified as 50 mA and V_{CEO} as 20 V. The vertical line on the characteristics defined as $V_{CE_{sat}}$ specifies

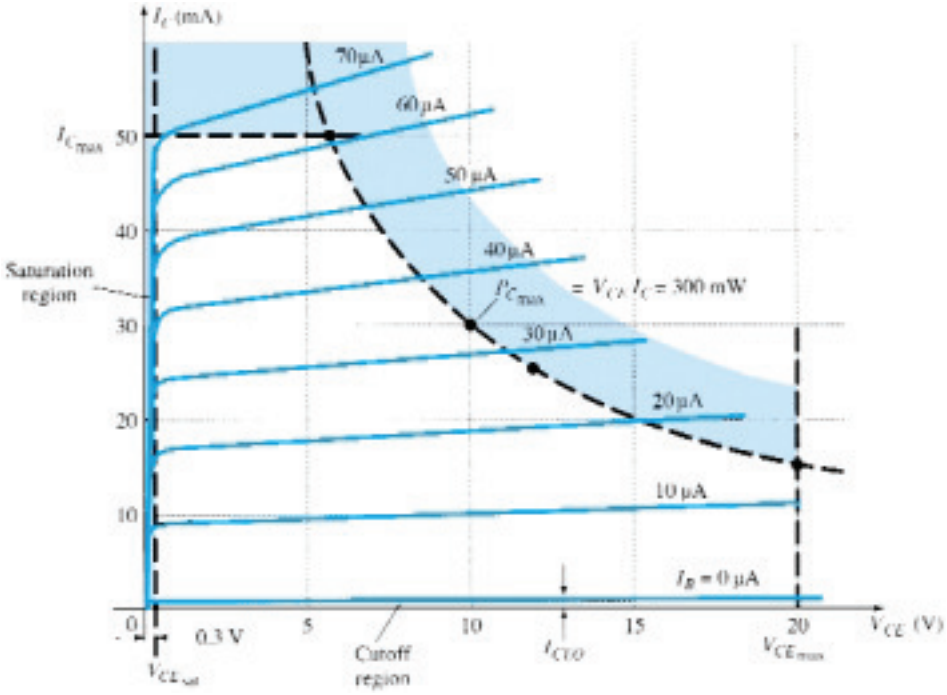


Figure 3.22 Defining the linear (undistorted) region of operation for a transistor.

the minimum V_{CE} that can be applied without falling into the nonlinear region labeled the *saturation* region. The level of $V_{CE_{sat}}$ is typically in the neighborhood of the 0.3 V specified for this transistor.

The maximum dissipation level is defined by the following equation:

$$P_{C_{max}} = V_{CE}I_C \tag{3.16}$$

For the device of Fig. 3.22, the collector power dissipation was specified as 300 mW. The question then arises of how to plot the collector power dissipation curve specified by the fact that

$$P_{C_{max}} = V_{CE}I_C = 300 \text{ mW}$$

or

$$V_{CE}I_C = 300 \text{ mW}$$

At any point on the characteristics the product of V_{CE} and I_C must be equal to 300 mW. If we choose I_C to be the maximum value of 50 mA and substitute into the relationship above, we obtain

$$V_{CE}I_C = 300 \text{ mW}$$

$$V_{CE}(50 \text{ mA}) = 300 \text{ mW}$$

$$V_{CE} = \frac{300 \text{ mW}}{50 \text{ mA}} = \mathbf{6\ V}$$

As a result we find that if $I_C = 50$ mA, then $V_{CE} = 6$ V on the power dissipation curve as indicated in Fig. 3.22. If we now choose V_{CE} to be its maximum value of 20 V, the level of I_C is the following:

$$(20 \text{ V})I_C = 300 \text{ mW}$$

$$I_C = \frac{300 \text{ mW}}{20 \text{ V}} = \mathbf{15\ mA}$$

defining a second point on the power curve.

If we now choose a level of I_C in the midrange such as 25 mA, and solve for the resulting level of V_{CE}, we obtain

$$V_{CE}(25 \text{ mA}) = 300 \text{ mW}$$

and

$$V_{CE} = \frac{300 \text{ mW}}{25 \text{ mA}} = \mathbf{12\ V}$$

as also indicated on Fig. 3.22.

A rough estimate of the actual curve can usually be drawn using the three points defined above. Of course, the more points you have, the more accurate the curve, but a rough estimate is normally all that is required.

The *cutoff* region is defined as that region below $I_C = I_{CEO}$. This region must also be avoided if the output signal is to have minimum distortion. On some specification sheets only I_{CBO} is provided. One must then use the equation $I_{CEO} = \beta I_{CBO}$ to establish some idea of the cutoff level if the characteristic curves are unavailable. Operation in the resulting region of Fig. 3.22 will ensure minimum distortion of the output signal and current and voltage levels that will not damage the device.

If the characteristic curves are unavailable or do not appear on the specification sheet (as is often the case), one must simply be sure that I_C, V_{CE}, and their product $V_{CE}I_C$ fall into the range appearing in Eq. (3.17).

β

$$I_{CEO} \leqq \boldsymbol{I_C} \leqq I_{C_{max}}$$
$$V_{CE_{sat}} \leqq \boldsymbol{V_{CE}} \leqq V_{CE_{max}} \tag{3.17}$$
$$\boldsymbol{V_{CE}I_C} \leqq P_{C_{max}}$$

For the common-base characteristics the maximum power curve is defined by the following product of output quantities:

$$P_{C_{max}} = V_{CB}I_C \tag{3.18}$$

3.9 TRANSISTOR SPECIFICATION SHEET

Since the specification sheet is the communication link between the manufacturer and user, it is particularly important that the information provided be recognized and correctly understood. Although all the parameters have not been introduced, a broad number will now be familiar. The remaining parameters will be introduced in the chapters that follow. Reference will then be made to this specification sheet to review the manner in which the parameter is presented.

The information provided as Fig. 3.23 is taken directly from the *Small-Signal Transistors, FETs, and Diodes* publication prepared by Motorola Inc. The 2N4123 is a general-purpose *npn* transistor with the casing and terminal identification appearing in the top-right corner of Fig. 3.23a. Most specification sheets are broken down into *maximum ratings, thermal characteristics, and electrical characteristics.* The electrical characteristics are further broken down into "on," "off," and small-signal characteristics. The "on" and "off" characteristics refer to dc limits, while the small-signal characteristics include the parameters of importance to ac operation.

Note in the maximum rating list that $V_{CE_{max}} = V_{CEO} = 30$ V with $I_{C_{max}} = 200$ mA. The maximum collector dissipation $P_{C_{max}} = P_D = 625$ mW. The derating factor under the maximum rating specifies that the maximum rating must be decreased 5 mW for every 1° rise in temperature above 25°C. In the "off" characteristics I_{CBO} is specified as 50 nA and in the "on" characteristics $V_{CE_{sat}} = 0.3$ V. The level of h_{FE} has a range of 50 to 150 at $I_C = 2$ mA and $V_{CE} = 1$ V and a minimum value of 25 at a higher current of 50 mA at the same voltage.

The limits of operation have now been defined for the device and are repeated below in the format of Eq. (3.17) using $h_{FE} = 150$ (the upper limit) and $I_{CEO} \cong \beta I_{CBO} = (150)(50\text{ nA}) = 7.5\ \mu\text{A}$. Certainly, for many applications the 7.5 μA = 0.0075 mA can be considered to be 0 mA on an approximate basis.

Limits of Operation

$$7.5\ m\text{A} \leqq \boldsymbol{I_C} \leqq 200\text{ mA}$$
$$0.3\text{ V} \leqq \boldsymbol{V_{CE}} \leqq 30\text{ V}$$
$$\boldsymbol{V_{CE}I_C} \leqq 650\text{ mW}$$

In the small-signal characteristics the level of h_{fe} (β_{ac}) is provided along with a plot of how it varies with collector current in Fig. 3.23f. In Fig. 3.23j the effect of temperature and collector current on the level of h_{FE} (β_{ac}) is demonstrated. At room temperature (25°C), note that h_{FE} (β_{dc}) is a maximum value of 1 in the neighborhood of about 8 mA. As I_C increased beyond this level, h_{FE} drops off to one-half the value with I_C equal to 50 mA. It also drops to this level if I_C decreases to the low level of 0.15 mA. Since this is a *normalized* curve, if we have a transistor with $\beta_{dc} = h_{FE} = 50$ at room temperature, the maximum value at 8 mA is 50. At $I_C = 50$ mA it has dropped to 50/2 = 25. In other words, normalizing reveals that the actual level of h_{FE}

at any level of I_C has been divided by the maximum value of h_{FE} at that temperature and $I_C = 8$ mA. Note also that the horizontal scale of Fig. 3.23j is a log scale. Log scales are examined in depth in Chapter 11. You may want to look back at the plots of this section when you find time to review the first few sections of Chapter 11.

MAXIMUM RATINGS

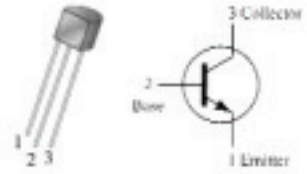
Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

2N4123

CASE 29-04, STYLE 1
TO-92 (TO-226AA)



GENERAL PURPOSE TRANSISTOR
NPN SILICON

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage ($I_C = 10$ µAdc, $I_E = 0$)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage ($I_E = 10$ µAdc, $I_C = 0$)	$V_{(BR)EBO}$	5.0		Vdc
Collector Cutoff Current ($V_{CB} = 20$ Vdc, $I_E = 0$)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current ($V_{EB} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) ($I_C = 2.0$ mAdc, $V_{CE} = 1.0$ Vdc) ($I_C = 50$ mAdc, $V_{CE} = 1.0$ Vdc)	h_{FE}	50 25	150 –	–
Collector-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{BE(sat)}$		0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, $f = 100$ MHz)	f_T	250		MHz
Output Capacitance ($V_{CB} = 5.0$ Vdc, $I_E = 0$, $f = 100$ MHz)	C_{obo}		4.0	pF
Input Capacitance ($V_{EB} = 0.5$ Vdc, $I_C = 0$, $f = 100$ kHz)	C_{ibo}		8.0	pF
Collector Base Capacitance ($I_E = 0$, $V_{CB} = 5.0$ V, $f = 100$ kHz)	C_{cb}	–	4.0	pF
Small-Signal Current Gain ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	h_{fe}	50	200	–
Current Gain – High Frequency ($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, $f = 100$ MHz) ($I_C = 2.0$ mAdc, $V_{CE} = 10$ V, $f = 1.0$ kHz)	$\lvert h_{fe} \rvert$	2.5 50	– 200	–
Noise Figure ($I_C = 100$ µAdc, $V_{CE} = 5.0$ Vdc, $R_S = 1.0$ k ohm, $f = 1.0$ kHz)	NF		6.0	dB

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%

(a)

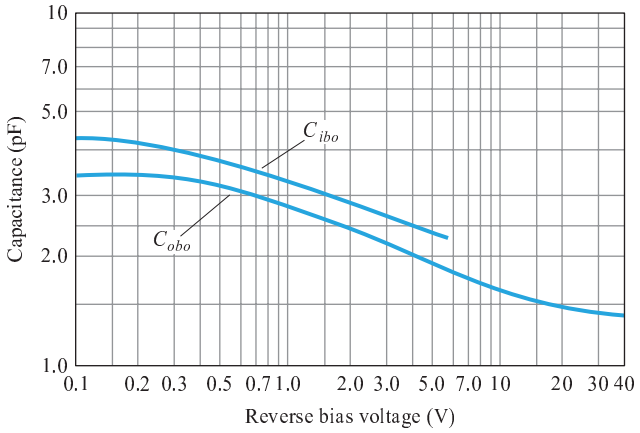
Figure 3.23 Transistor specification sheet.

β

Before leaving this description of the characteristics, take note of the fact that the actual collector characteristics are not provided. In fact, most specification sheets as provided by the range of manufacturers fail to provide the full characteristics. It is expected that the data provided are sufficient to use the device effectively in the design process.

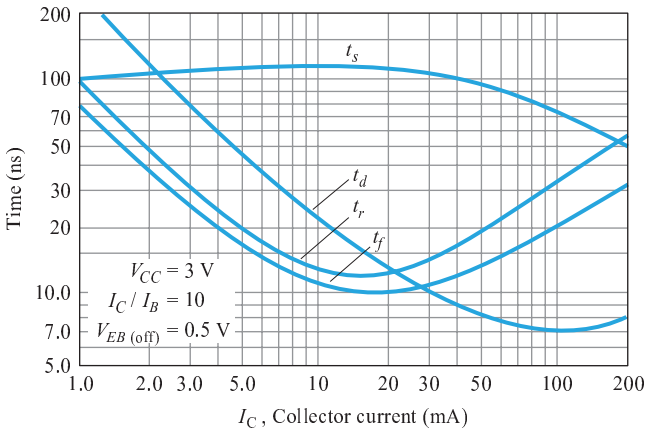
As noted in the introduction to this section, all the parameters of the specification sheet have not been defined in the preceding sections or chapters. However, the specification sheet provided in Fig. 3.23 will be referenced continually in the chapters to follow as parameters are introduced. The specification sheet can be a very valuable tool in the design or analysis mode, and every effort should be made to be aware of the importance of each parameter and how it may vary with changing levels of current, temperature, and so on.

Figure 1 – Capacitance



(b)

Figure 2 – Switching Times



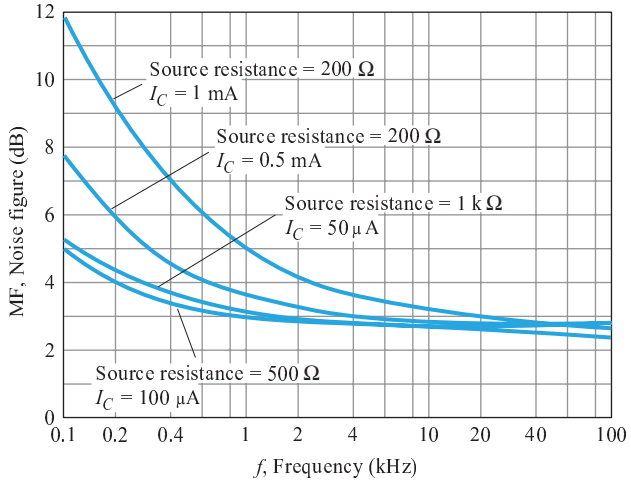
(c)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE

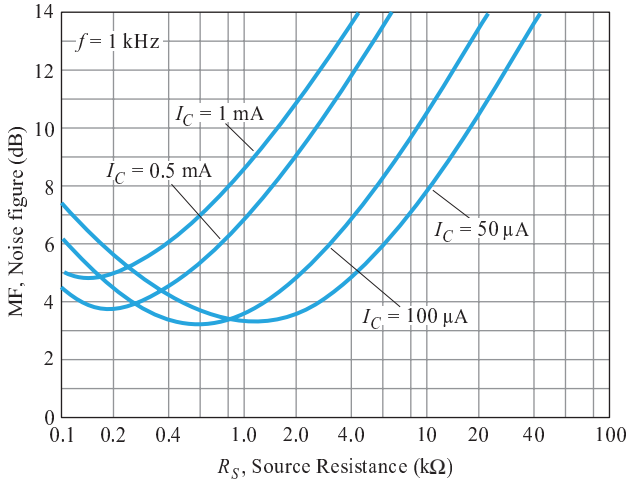
(V_{CE} = 5 Vdc, T_A = 25°C)
Bandwidth = 1.0 Hz

Figure 3 – Frequency Variations



(d)

Figure 4 – Source Resistance



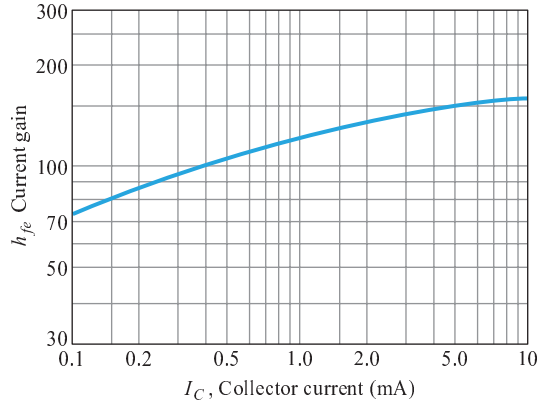
(e)

Figure 3.23 Continued.

h PARAMETERS

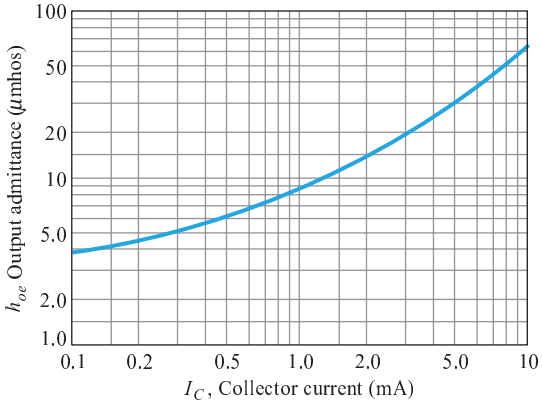
V_{CE} = 10 V, f = 1 kHz, T_A = 25°C

Figure 5 – Current Gain



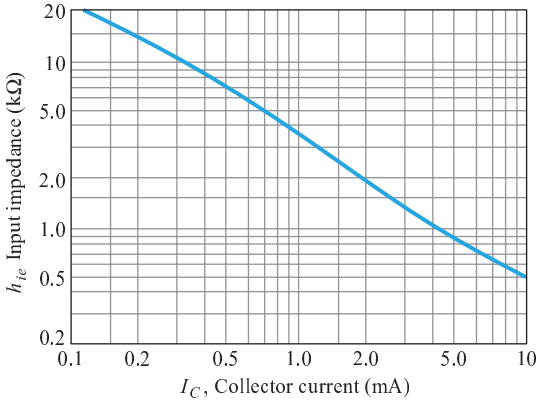
(f)

Figure 6 – Output Admittance



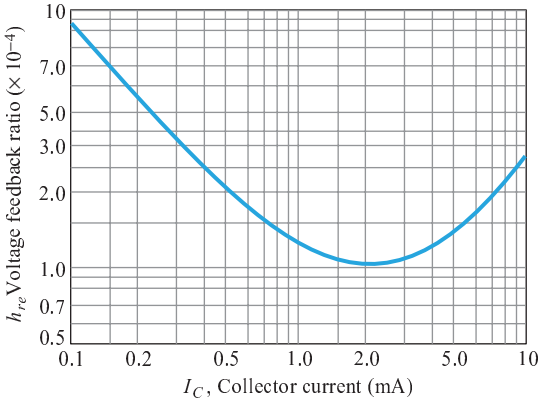
(g)

Figure 7 – Input Impedance



(h)

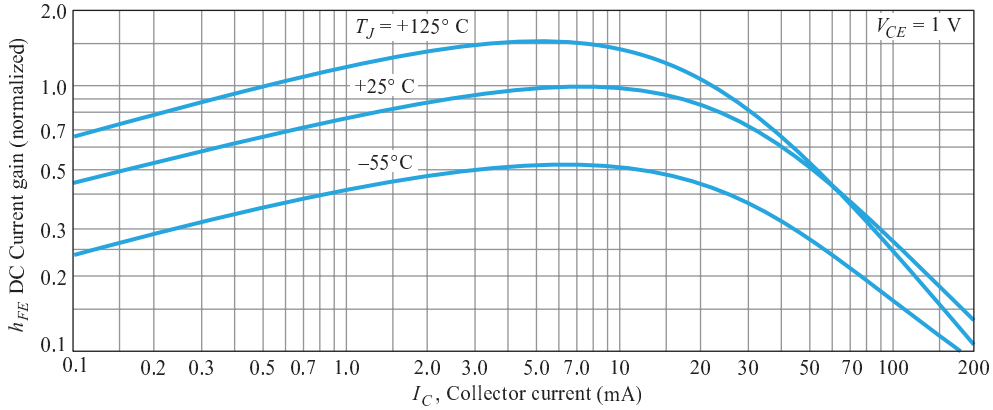
Figure 8 – Voltage Feedback Ratio



(i)

STATIC CHARACTERISTICS

Figure 9 – DC Current Gain



(j)

Figure 3.23 Continued.

β

3.10 TRANSISTOR TESTING

As with diodes, there are three routes one can take to check a transistor: *curve tracer, digital meter,* and *ohmmeter.*

Curve Tracer

The curve tracer of Fig. 1.45 will provide the display of Fig. 3.24 once all the controls have been properly set. The smaller displays to the right reveal the scaling to be applied to the characteristics. The vertical sensitivity is 2 mA/div, resulting in the scale shown to the left of the monitor's display. The horizontal sensitivity is 1 V/div, resulting in the scale shown below the characteristics. The step function reveals that the curves are separated by a difference of 10 μA, starting at 0 μA for the bottom curve. The last scale factor provided can be used to quickly determine the β_{ac} for any region of the characteristics. Simply multiply the displayed factor by the number of divisions between I_B curves in the region of interest. For instance, let us determine β_{ac} at a Q-point of $I_C = 7$ mA and $V_{CE} = 5$ V. In this region of the display, the distance between I_B curves is $\frac{9}{10}$ of a division, as indicated on Fig. 3.25. Using the factor specified, we find that

$$\beta_{ac} = \frac{9}{10}\ \text{div}\left(\frac{200}{\text{div}}\right) = \mathbf{180}$$

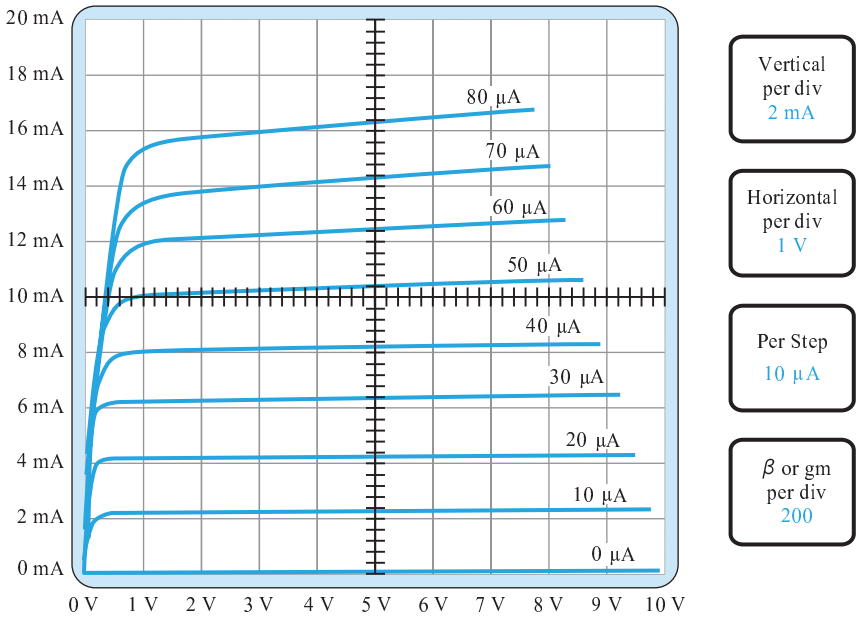


Figure 3.24 Curve tracer response to 2N3904 *npn* transistor.

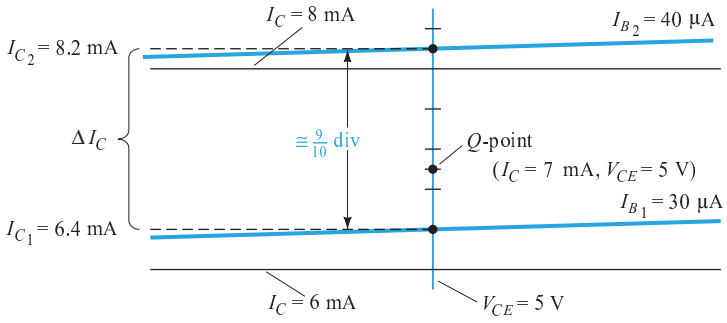


Figure 3.25 Determining β_{ac} for the transistor characteristics of Fig. 3.24 at $I_C = 7$ mA and $V_{CE} = 5$ V.

Using Eq. (3.11) gives us

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}} = \frac{8.2\ \text{mA} - 6.4\ \text{mA}}{40\ \mu\text{A} - 30\ \mu\text{A}}$$

$$= \frac{1.8\ \text{mA}}{10\ \mu\text{A}} = \mathbf{180}$$

verifying the determination above.

Advanced Digital Meters

Advanced digital meters such as that shown in Fig. 3.26 are now available that can provide the level of h_{FE} using the lead sockets appearing at the bottom left of the dial. Note the choice of *pnp* or *npn* and the availability of two emitter connections to handle the sequence of leads as connected to the casing. The level of h_{FE} is determined at a collector current of 2 mA for the Testmate 175A, which is also provided on the digital display. Note that this versatile instrument can also check a diode. It can measure capacitance and frequency in addition to the normal functions of voltage, current, and resistance measurements.

In fact, in the diode testing mode it can be used to check the *p-n* junctions of a transistor. With the collector open the base-to-emitter junction should result in a low voltage of about 0.7 V with the red (positive) lead connected to the base and the black (negative) lead connected to the emitter. A reversal of the leads should result in an OL indication to represent the reverse-biased junction. Similarly, with the emitter open, the forward- and reverse-bias states of the base-to-collector junction can be checked.

Figure 3.26 Transistor tester. (Courtesy Computronics Technology, Inc.)

Ohmmeter

An ohmmeter or the resistance scales of a DMM can be used to check the state of a transistor. Recall that for a transistor in the active region the base-to-emitter junction is forward-biased and the base-to-collector junction is reverse-biased. Essentially, therefore, the forward-biased junction should register a relatively low resistance while the reverse-biased junction shows a much higher resistance. For an *npn* transistor, the forward-biased junction (biased by the internal supply in the resistance mode) from base to emitter should be checked as shown in Fig. 3.27 and result in a reading that will typically fall in the range of 100 Ω to a few kilohms. The reverse-biased base-to-collector junction (again reverse-biased by the internal supply) should be checked as shown in Fig. 3.28 with a reading typically exceeding 100 kΩ. For a *pnp* transistor the leads are reversed for each junction. Obviously, a large or small resistance in both directions (reversing the leads) for either junction of an *npn* or *pnp* transistor indicates a faulty device.

If both junctions of a transistor result in the expected readings the type of transistor can also be determined by simply noting the polarity of the leads as applied to the base-emitter junction. If the positive (+) lead is connected to the base and the negative lead (−) to the emitter a low resistance reading would indicate an *npn* transistor. A high resistance reading would indicate a *pnp* transistor. Although an ohmmeter can also be used to determine the leads (base, collector and emitter) of a transistor it is assumed that this determination can be made by simply looking at the orientation of the leads on the casing.

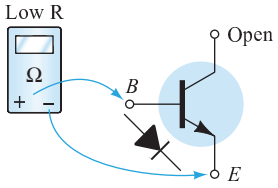


Figure 3.27 Checking the forward-biased base-to-emitter junction of an *npn* transistor.

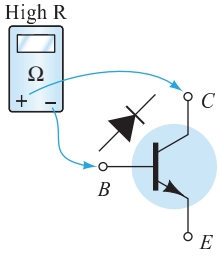


Figure 3.28 Checking the reverse-biased base-to-collector junction of an *npn* transistor.

β

3.11 TRANSISTOR CASING AND TERMINAL IDENTIFICATION

After the transistor has been manufactured using one of the techniques described in Chapter 12, leads of, typically, gold, aluminum, or nickel are then attached and the entire structure is encapsulated in a container such as that shown in Fig. 3.29. Those with the heavy duty construction are high-power devices, while those with the small can (top hat) or plastic body are low- to medium-power devices.

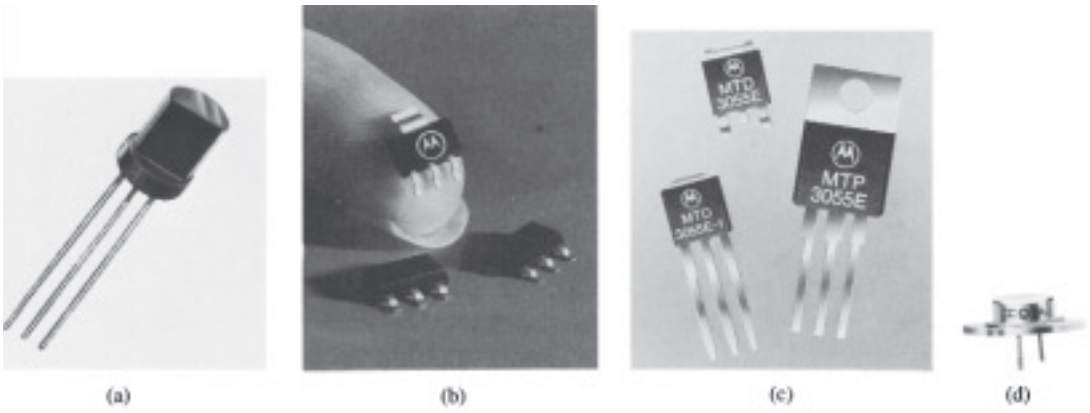


Figure 3.29 Various types of transistors: (a) Courtesy General Electric Company; (b) and (c) Courtesy of Motorola Inc.; (d) Courtesy International Rectifier Corporation.

Whenever possible, the transistor casing will have some marking to indicate which leads are connected to the emitter, collector, or base of a transistor. A few of the methods commonly used are indicated in Fig. 3.30.

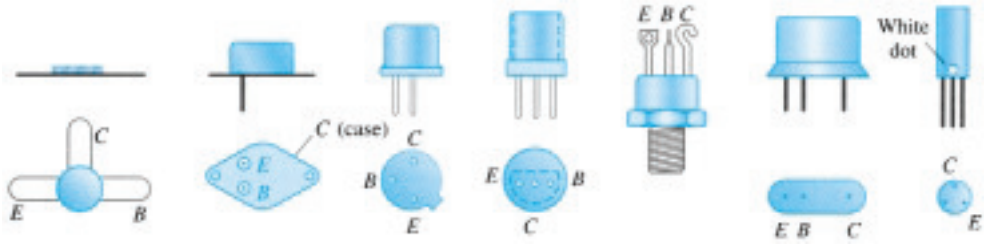


Figure 3.30 Transistor terminal identification.

The internal construction of a TO-92 package in the Fairchild line appears in Fig. 3.31. Note the very small size of the actual semiconductor device. There are gold bond wires, a copper frame, and an epoxy encapsulation.

Four (quad) individual *pnp* silicon transistors can be housed in the 14-pin plastic dual-in-line package appearing in Fig. 3.32a. The internal pin connections appear in Fig. 3.32b. As with the diode IC package, the indentation in the top surface reveals the number 1 and 14 pins.

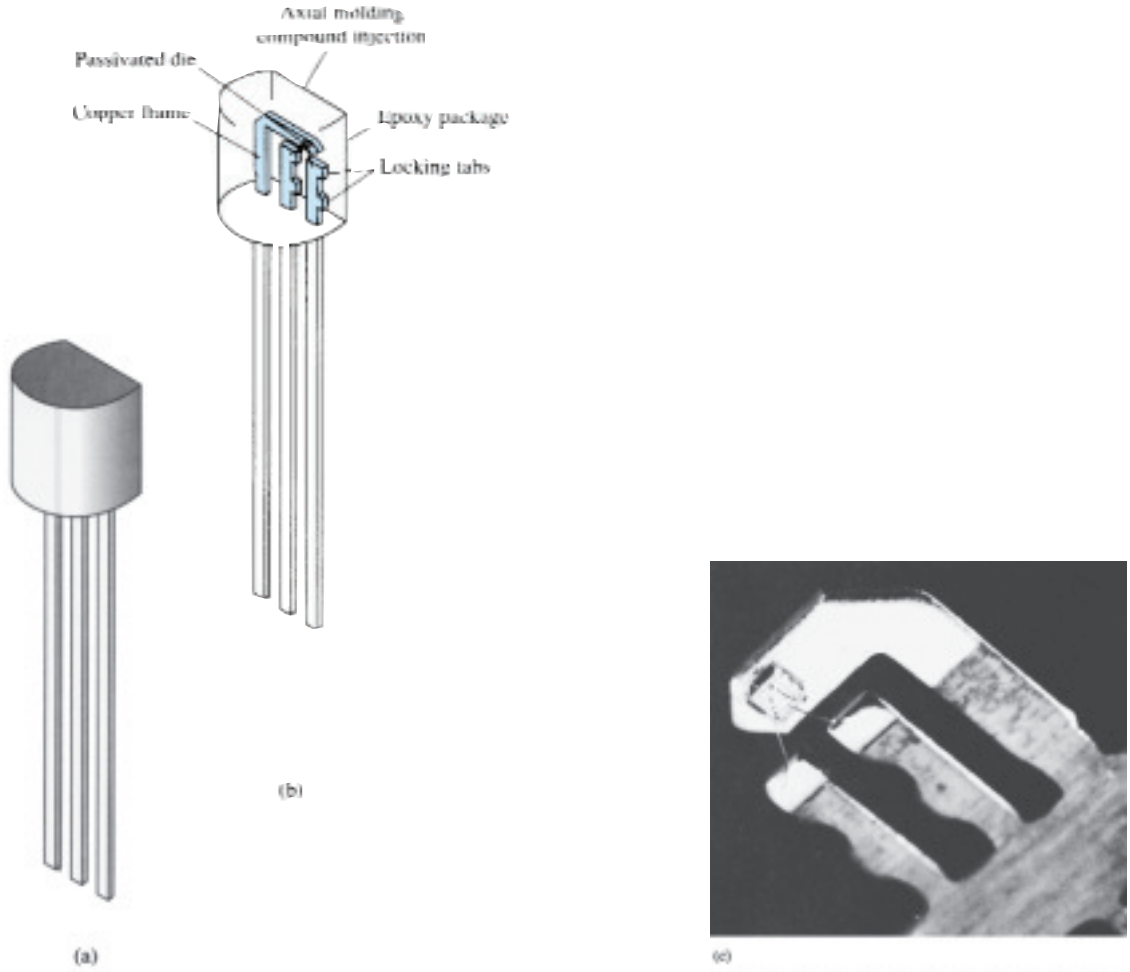


Figure 3.31 Internal construction of a Fairchild transistor in a TO-92 package. (Courtesy Fairchild Camera and Instrument Corporation.)

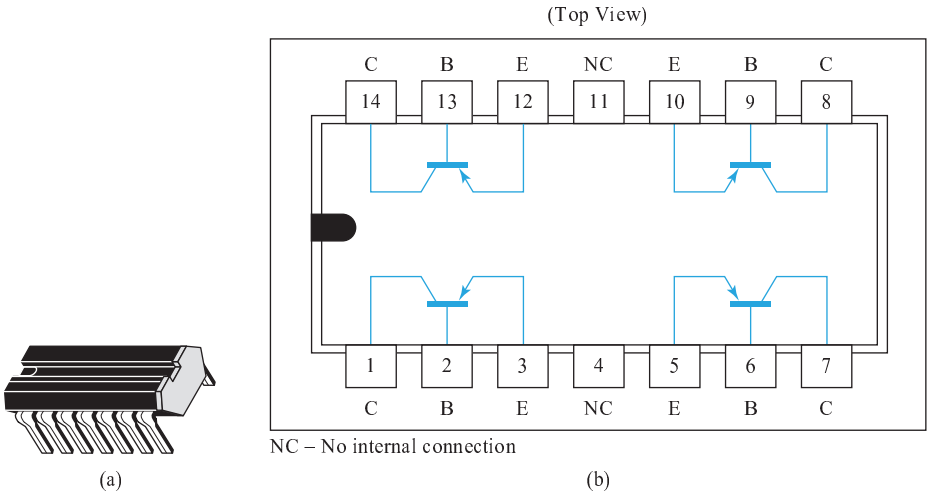


Figure 3.32 Type Q2T2905 Texas Instruments quad *pnp* silicon transistors: (a) appearance; (b) pin connections. (Courtesy Texas Instruments Incorporated.)

3.12 PSPICE WINDOWS

Since the transistor characteristics were introduced in this chapter it seems appropriate that a procedure for obtaining those characteristics using PSpice Windows should be examined. The transistors are listed in the **EVAL.slb** library and start with the letter **Q.** The library includes two *npn* transistors and two *pnp* transistors. The fact that there are a series of curves defined by the levels of I_B will require that a sweep of I_B values (a *nested sweep*) occur within a sweep of collector-to-emitter voltages. This is unnecessary for the diode, however, since only one curve would result.

First, the network in Fig. 3.33 is established using the same procedure defined in Chapter 2. The voltage V_{CC} will establish our main sweep while the voltage V_{BB} will determine the nested sweep. For future reference, note the panel at the top right of the menu bar with the scroll control when building networks. This option allows you to retrieve elements that have been used in the past. For instance, if you placed a resistor a few elements ago, simply return to the scroll bar and scroll until the resistor **R** appears. Click the location once, and the resistor will appear on the screen.

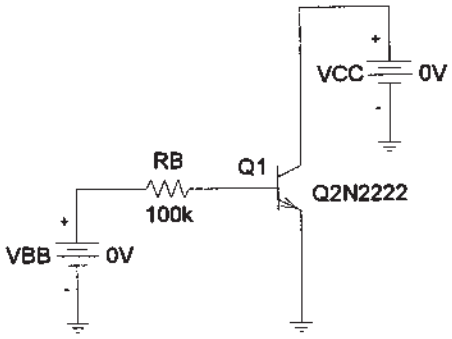


Figure 3.33 Network employed to obtain the collector characteristics of the Q2N2222 transistor.

Next, choose the **Analysis Setup** icon and enable the **DC Sweep.** Click on **DC Sweep,** and choose **Voltage Source** and **Linear.** Type in the **Name** V_{CC} with a **Start Value** of 0 V and an **End Value** of 10 V. Use an **Increment** of 0.01 V to ensure a continuous, detailed plot. Rather than click **OK,** this time we have to choose the **Nested Sweep** at the bottom left of the dialog box. When chosen, a **DC Nested Sweep** dialog box will appear and ask us to repeat the choices just made for the voltage V_{BB}. Again, Voltage Source and Linear are chosen, and the name is inserted as V_{BB}. The **Start Value** will now be 2.7 V to correspond with an initial current of 20 μA as determined by

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{2.7\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega} = \mathbf{20\ \mu A}$$

The Increment will be 2V, corresponding with a change in base current of 20 μA between I_B levels. The final value will be 10.7 V, corresponding with a current of 100 μA. Before leaving the dialog box, be sure to enable the nested sweep. Then, choose **OK,** followed by a closing of the **Analysis Setup,** and we are ready for the analysis. This time we will automatically Run Probe after the analysis by choosing **Analysis-Probe Setup,** followed by selecting **Automatically run Probe after simulation.** After choosing **OK,** followed by a clicking of the **Simulation icon** (recall that it was the

icon with the yellow background and two waveforms), the **OrCAD MicroSim Probe** screen will automatically appear. This time, since V_{CC} is the collector-to-emitter voltage, there is no need to label the voltage at the collector. In fact, since it appears as the horizontal axis of the Probe response, there is no need to touch the **X-Axis Settings** at all if we recognize that V_{CC} is the collector-to-emitter voltage. For the vertical axis, we turn to **Trace-Add** and obtain the **Add Traces** dialog box. Choosing **IC(Q1)** and **OK,** we obtain the transistor characteristics. Unfortunately, however, they extend from −10 to +20 mA on the vertical axis. This can be corrected by choosing **Plot** and then **Y-Axis Settings** to obtain the **Y-Axis Settings** dialog box. By choosing **User Defined,** the range can be set from 0 to 20 mA with a Linear scale. Choose **OK** again, and the characteristics of Fig. 3.34 result.

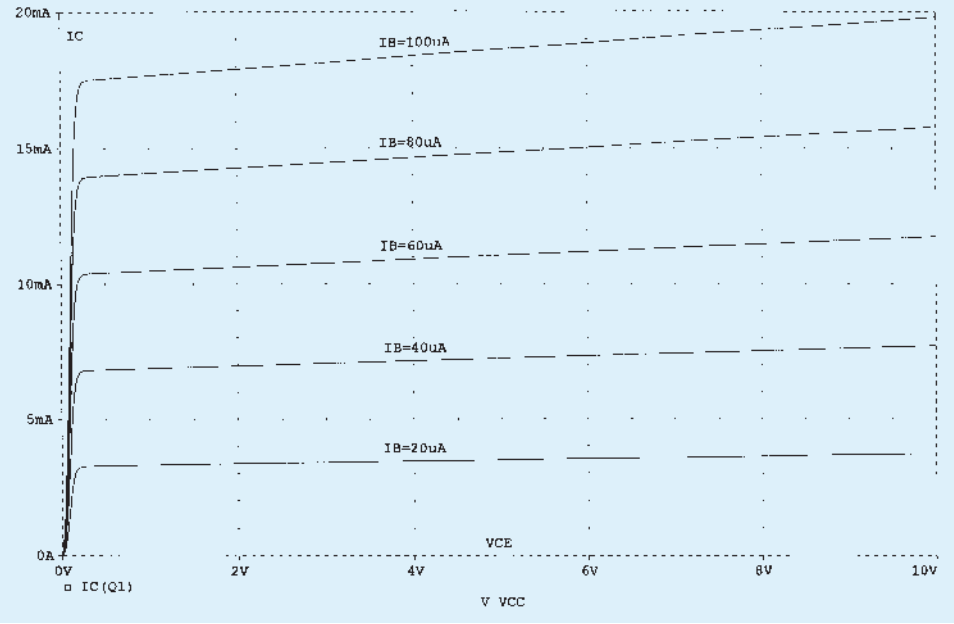


Figure 3.34 Collector characteristics for the transistor of Figure 3.33.

Using the **ABC** icon on the menu bar, the various levels of I_B can be inserted along with the axis labels V_{CE} and I_C. Simply click on the icon, and a dialog box appears asking for the text material. Enter the desired text, click **OK,** and it will appear on the screen. It can then be placed in the desired location.

If the ac beta is determined in the middle of the graph, you will find that its value is about 190—even though **Bf** in the list of specifications is 255.9. Again, like the diode, the other parameters of the element have a noticeable effect on the total operation. However, if we return to the diode specifications through **Edit-Model-Edit Instance Model (Text)** and remove all parameters of the device except Bf = 255.9 (don't forget the close parentheses at the end of the listing) and follow with an **OK** and a **Simulation,** a new set of curves will result. An adjustment of the range of the y-axis to 0–30 mA using the **Y-Axis Settings** will result in the characteristic curves of Fig. 3.35.

Note first that the curves are all horizontal, meaning that the element is void of any resistive elements. In addition, the equal spacing of the curves throughout reveals that beta is the same everywhere (as specified by our new device characteristics). Using a difference of 5 mA between any two curves and dividing by the difference in I_B of 20 μA will result in a β of 250, which is essentially the same as that specified for the device.

β

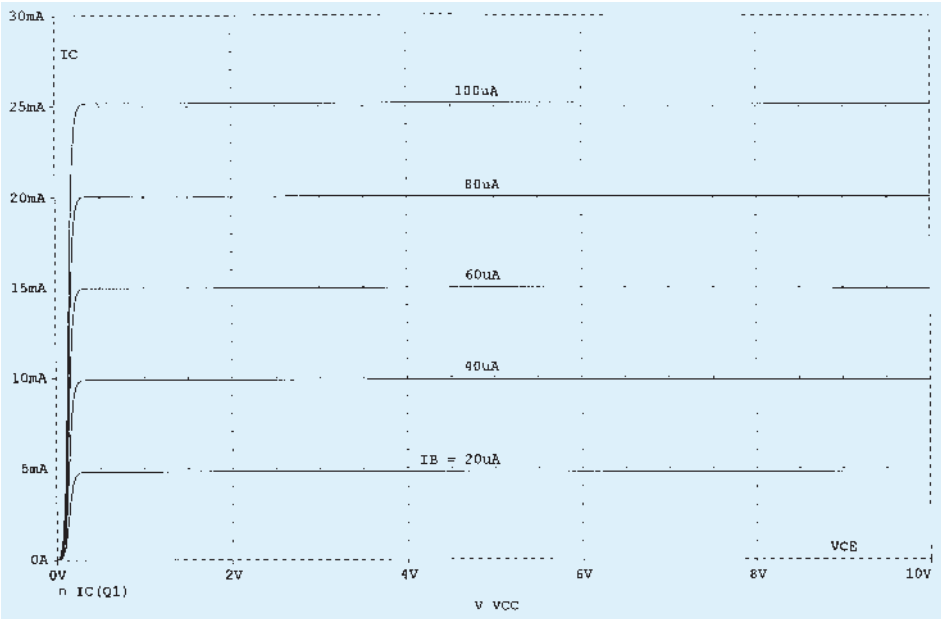


FIGURE 3.35 Ideal collector characteristics for the transistor of Figure 3.33.

PROBLEMS

§ 3.2 Transistor Construction

1. What names are applied to the two types of BJT transistors? Sketch the basic construction of each and label the various minority and majority carriers in each. Draw the graphic symbol next to each. Is any of this information altered by changing from a silicon to a germanium base?
2. What is the major difference between a bipolar and a unipolar device?

§ 3.3 Transistor Operation

3. How must the two transistor junctions be biased for proper transistor amplifier operation?
4. What is the source of the leakage current in a transistor?
5. Sketch a figure similar to Fig. 3.3 for the forward-biased junction of an *npn* transistor. Describe the resulting carrier motion.
6. Sketch a figure similar to Fig. 3.4 for the reverse-biased junction of an *npn* transistor. Describe the resulting carrier motion.
7. Sketch a figure similar to Fig. 3.5 for the majority- and minority-carrier flow of an *npn* transistor. Describe the resulting carrier motion.
8. Which of the transistor currents is always the largest? Which is always the smallest? Which two currents are relatively close in magnitude?
9. If the emitter current of a transistor is 8 mA and I_B is 1/100 of I_C, determine the levels of I_C and I_B.

§ 3.4 Common-Base Configuration

10. From memory, sketch the transistor symbol for a *pnp* and an *npn* transistor, and then insert the conventional flow direction for each current.
11. Using the characteristics of Fig. 3.7, determine V_{BE} at $I_E = 5$ mA for $V_{CB} = 1$, 10, and 20 V. Is it reasonable to assume on an approximate basis that V_{CB} has only a slight effect on the relationship between V_{BE} and I_E?
12. (a) Determine the average ac resistance for the characteristics of Fig. 3.10b.
    (b) For networks in which the magnitude of the resistive elements is typically in kilohms, is the approximation of Fig. 3.10c a valid one [based on the results of part (a)]?

13. (a) Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 4.5$ mA and $V_{CB} = 4$ V.
(b) Repeat part (a) for $I_E = 4.5$ mA and $V_{CB} = 16$ V.
(c) How have the changes in V_{CB} affected the resulting level of I_C?
(d) On an approximate basis, how are I_E and I_C related based on the results above?

14. (a) Using the characteristics of Figs. 3.7 and 3.8, determine I_C if $V_{CB} = 10$ V and $V_{BE} = 800$ mV.
(b) Determine V_{BE} if $I_C = 5$ mA and $V_{CB} = 10$ V.
(c) Repeat part (b) using the characteristics of Fig. 3.10b.
(d) Repeat part (b) using the characteristics of Fig. 3.10c.
(e) Compare the solutions for V_{BE} for parts (b), (c), and (d). Can the difference be ignored if voltage levels greater than a few volts are typically encountered?

15. (a) Given an α_{dc} of 0.998, determine I_C if $I_E = 4$ mA.
(b) Determine α_{dc} if $I_E = 2.8$ mA and $I_B = 20\ \mu$A.
(c) Find I_E if $I_B = 40\ \mu$A and α_{dc} is 0.98.

16. From memory, and memory only, sketch the common-base BJT transistor configuration (for *npn* and *pnp*) and indicate the polarity of the applied bias and resulting current directions.

§ 3.5 Transistor Amplifying Action

17. Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.12 if $V_i = 500$ mV and $R = 1$ kΩ. (The other circuit values remain the same.)

18. Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.12 if the source has an internal resistance of 100 Ω in series with V_i.

§ 3.6 Common-Emitter Configuration

19. Define I_{CBO} and I_{CEO}. How are they different? How are they related? Are they typically close in magnitude?

20. Using the characteristics of Fig. 3.14:
(a) Find the value of I_C corresponding to $V_{BE} = +750$ mV and $V_{CE} = +5$ V.
(b) Find the value of V_{CE} and V_{BE} corresponding to $I_C = 3$ mA and $I_B = 30\ \mu$A.

* **21.** (a) For the common-emitter characteristics of Fig. 3.14, find the dc beta at an operating point of $V_{CE} = +8$ V and $I_C = 2$ mA.
(b) Find the value of α corresponding to this operating point.
(c) At $V_{CE} = +8$ V, find the corresponding value of I_{CEO}.
(d) Calculate the approximate value of I_{CBO} using the dc beta value obtained in part (a).

* **22.** (a) Using the characteristics of Fig. 3.14a, determine I_{CEO} at $V_{CE} = 10$ V.
(b) Determine β_{dc} at $I_B = 10\ \mu$A and $V_{CE} = 10$ V.
(c) Using the β_{dc} determined in part (b), calculate I_{CBO}.

23. (a) Using the characteristics of Fig. 3.14a, determine β_{dc} at $I_B = 80\ \mu$A and $V_{CE} = 5$ V.
(b) Repeat part (a) at $I_B = 5\ \mu$A and $V_{CE} = 15$ V.
(c) Repeat part (a) at $I_B = 30\ \mu$A and $V_{CE} = 10$ V.
(d) Reviewing the results of parts (a) through (c), does the value of β_{dc} change from point to point on the characteristics? Where were the higher values found? Can you develop any general conclusions about the value of β_{dc} on a set of characteristics such as those provided in Fig. 3.14a?

* **24.** (a) Using the characteristics of Fig. 3.14a, determine β_{ac} at $I_B = 80\ \mu$A and $V_{CE} = 5$ V.
(b) Repeat part (a) at $I_B = 5\ \mu$A and $V_{CE} = 15$ V.
(c) Repeat part (a) at $I_B = 30\ \mu$A and $V_{CE} = 10$ V.
(d) Reviewing the results of parts (a) through (c), does the value of β_{ac} change from point to point on the characteristics? Where are the high values located? Can you develop any general conclusions about the value of β_{ac} on a set of collector characteristics?
(e) The chosen points in this exercise are the same as those employed in Problem 23. If Problem 23 was performed, compare the levels of β_{dc} and β_{ac} for each point and comment on the trend in magnitude for each quantity.

25. Using the characteristics of Fig. 3.14a, determine β_{dc} at $I_B = 25\ \mu A$ and $V_{CE} = 10$ V. Then calculate α_{dc} and the resulting level of I_E. (Use the level of I_C determined by $I_C = \beta_{dc} I_B$.)

26. (a) Given that $\alpha_{dc} = 0.987$, determine the corresponding value of β_{dc}.
(b) Given $\beta_{dc} = 120$, determine the corresponding value of α.
(c) Given that $\beta_{dc} = 180$ and $I_C = 2.0$ mA, find I_E and I_B.

27. From memory, and memory only, sketch the common-emitter configuration (for *npn* and *pnp*) and insert the proper biasing arrangement with the resulting current directions for I_B, I_C, and I_E.

§ 3.7 Common-Collector Configuration

28. An input voltage of 2 V rms (measured from base to ground) is applied to the circuit of Fig. 3.21. Assuming that the emitter voltage follows the base voltage exactly and that V_{be} (rms) = 0.1 V, calculate the circuit voltage amplification ($A_v = V_o/V_i$) and emitter current for $R_E = 1\ k\Omega$.

29. For a transistor having the characteristics of Fig. 3.14, sketch the input and output characteristics of the common-collector configuration.

§ 3.8 Limits of Operation

30. Determine the region of operation for a transistor having the characteristics of Fig. 3.14 if $I_{C_{max}} = 7$ mA, $V_{CE_{max}} = 17$ V, and $P_{C_{max}} = 40$ mW.

31. Determine the region of operation for a transistor having the characteristics of Fig. 3.8 if $I_{C_{max}} = 6$ mA, $V_{CB_{max}} = 15$ V, and $P_{C_{max}} = 30$ mW.

§ 3.9 Transistor Specification Sheet

32. Referring to Fig. 3.23, determine the temperature range for the device in degrees Fahrenheit.

33. Using the information provided in Fig. 3.23 regarding $P_{D_{max}}$, $V_{CE_{max}}$, $I_{C_{max}}$ and $V_{CE_{sat}}$, sketch the boundaries of operation for the device.

34. Based on the data of Fig. 3.23, what is the expected value of I_{CEO} using the average value of β_{dc}?

35. How does the range of h_{FE} (Fig. 3.23(j), normalized from $h_{FE} = 100$) compare with the range of h_{fe} (Fig. 3.23(f)) for the range of I_C from 0.1 to 10 mA?

36. Using the characteristics of Fig. 3.23b, determine whether the input capacitance in the common-base configuration increases or decreases with increasing levels of reverse-bias potential. Can you explain why?

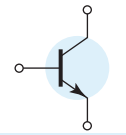
* **37.** Using the characteristics of Fig. 3.23f, determine how much the level of h_{fe} has changed from its value at 1 mA to its value at 10 mA. Note that the vertical scale is a log scale that may require reference to Section 11.2. Is the change one that should be considered in a design situation?

* **38.** Using the characteristics of Fig. 3.23j, determine the level of β_{dc} at $I_C = 10$ mA at the three levels of temperature appearing in the figure. Is the change significant for the specified temperature range? Is it an element to be concerned about in the design process?

§ 3.10 Transistor Testing

39. (a) Using the characteristics of Fig. 3.24, determine β_{ac} at $I_C = 14$ mA and $V_{CE} = 3$ V.
(b) Determine β_{dc} at $I_C = 1$ mA and $V_{CE} = 8$ V.
(c) Determine β_{ac} at $I_C = 14$ mA and $V_{CE} = 3$ V.
(d) Determine β_{dc} at $I_C = 1$ mA and $V_{CE} = 8$ V.
(e) How does the level of β_{ac} and β_{dc} compare in each region?
(f) Is the approximation $\beta_{dc} \cong \beta_{ac}$ a valid one for this set of characteristics?

*Please Note: Asterisks indicate more difficult problems.



CHAPTER

DC Biasing—BJTs 4

4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality, the improved output ac power level is the result of a transfer of energy from the applied dc supplies. The analysis or design of any electronic amplifier therefore has two components: the dc portion and the ac portion. Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In Section 4.2 we specify the range for the BJT amplifier. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point—a number of these networks are analyzed in this chapter. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations—another topic to be investigated in a later section of this chapter.

Although a number of networks are analyzed in this chapter, there is an underlying similarity between the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$V_{BE} = 0.7 \text{ V} \tag{4.1}$$

$$I_E = (\beta + 1)I_B \cong I_C \tag{4.2}$$

$$I_C = \beta I_B \tag{4.3}$$

In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent. In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (4.1) through (4.3) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for I_B are so similar for a num-

ber of configurations that one equation can be derived from another simply by dropping or adding a term or two. The primary function of this chapter is to develop a level of familiarity with the BJT transistor that would permit a dc analysis of any system that might employ the BJT amplifier.

4.2 OPERATING POINT

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive. Figure 4.1 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the *active region.* The maximum ratings are indicated on the characteristics of Fig. 4.1 by a horizontal line for the maximum collector current $I_{C_{max}}$ and a vertical line at the maximum collector-to-emitter voltage $V_{CE_{max}}$. The maximum power constraint is defined by the curve $P_{C_{max}}$ in the same figure. At the lower end of the scales are the *cutoff region*, defined by $I_B \leq 0\ \mu A$, and the *saturation region*, defined by $V_{CE} \leq V_{CE_{sat}}$.

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active* region, one can select many different operating areas or points. The chosen *Q*-point often depends on the intended use of the circuit. Still, we can consider some differences among the

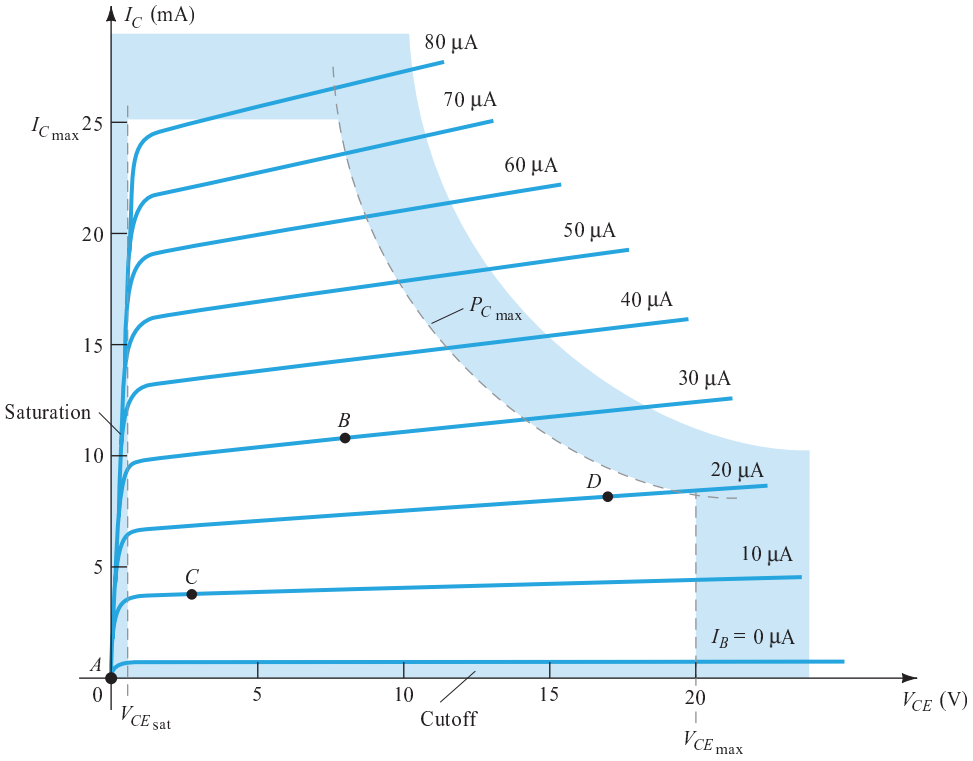
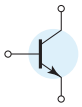


Figure 4.1 Various operating points within the limits of operation of a transistor.



various points shown in Fig. 4.1 to present some basic ideas about the operating point and, thereby, the bias circuit.

If no bias were used, the device would initially be completely off, resulting in a Q-point at A—namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal, point A would not be suitable. For point B, if a signal is applied to the circuit, the device will vary in current and voltage from operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary but not enough to drive the device into *cutoff* or *saturation*. Point C would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0\text{V}/I_C = 0$ mA. Operating at point C also raises some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point B is a region of more linear spacing and therefore more linear operation, as shown in Fig. 4.1. Point D sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point B therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers (Chapter 8) but not the case necessarily for power amplifiers, which will be considered in Chapter 16. In this discussion, we will be concentrating primarily on biasing the transistor for *small-signal* amplification operation.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, the effect of temperature must also be taken into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of *temperature stability* so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a *stability factor*, S, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:

1. The base–emitter junction *must* be forward-biased (p-region voltage more *p*ositive), with a resulting forward-bias voltage of about 0.6 to 0.7 V.
2. The base–collector junction *must* be reverse-biased (n-region more *p*ositive), with the reverse-bias voltage being any value within the maximum limits of the device.

[Note that for forward bias the voltage across the p-n junction is p-*p*ositive, while for reverse bias it is opposite (reverse) with n-*p*ositive. This emphasis on the initial letter should provide a means of helping memorize the necessary voltage polarity.]

Operation in the cutoff, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation:*
   Base–emitter junction forward biased
   Base–collector junction reverse biased

2. *Cutoff-region operation:*
   Base–emitter junction reverse biased
3. *Saturation-region operation:*
   Base–emitter junction forward biased
   Base–collector junction forward biased

4.3 FIXED-BIAS CIRCUIT

The fixed-bias circuit of Fig. 4.2 provides a relatively straightforward and simple introduction to transistor dc bias analysis. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 4.2 are the actual current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 4.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 4.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 4.2.

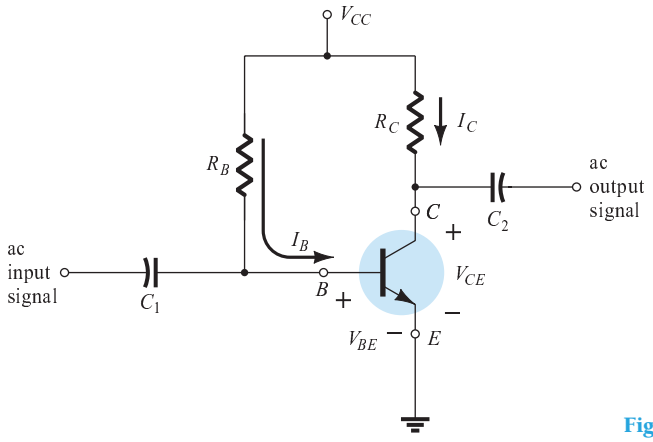


Figure 4.2 Fixed-bias circuit.

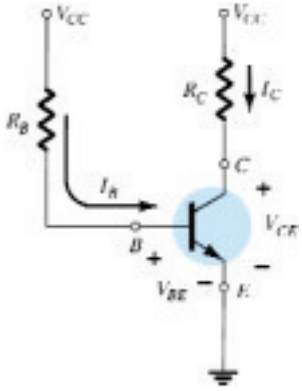


Figure 4.3 dc equivalent of Fig. 4.2.

Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop of Fig. 4.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B will result in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4.4}$$

Equation (4.4) is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through R_B and by Ohm's law that current is the voltage across R_B divided by the resistance R_B. The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}).

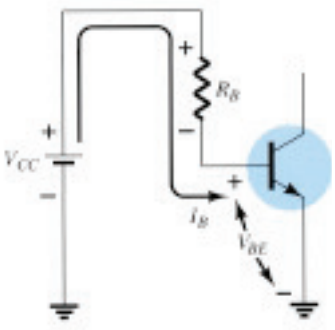


Figure 4.4 Base–emitter loop.

In addition, since the supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor, R_B, sets the level of base current for the operating point.

Collector–Emitter Loop

The collector–emitter section of the network appears in Fig. 4.5 with the indicated direction of current I_C and the resulting polarity across R_C. The magnitude of the collector current is related directly to I_B through

$$I_C = \beta I_B \tag{4.5}$$

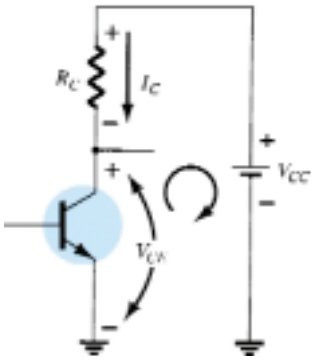


Figure 4.5 Collector–emitter loop.

It is interesting to note that since the base current is controlled by the level of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of the resistance R_C. Change R_C to any level and it will not affect the level of I_B or I_C as long as we remain in the active region of the device. However, as we shall see, the level of R_C will determine the magnitude of V_{CE}, which is an important parameter.

Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig. 4.5 will result in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

and

$$V_{CE} = V_{CC} - I_C R_C \tag{4.6}$$

which states in words that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C.

As a brief review of single- and double-subscript notation recall that

$$V_{CE} = V_C - V_E \tag{4.7}$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground respectively. But *in this case,* since $V_E = 0$ V, we have

$$V_{CE} = V_C \tag{4.8}$$

In addition, since

$$V_{BE} = V_B - V_E \tag{4.9}$$

and $V_E = 0$ V, then

$$V_{BE} = V_B \tag{4.10}$$

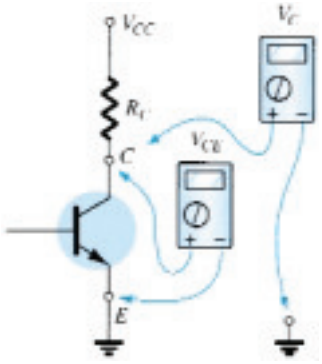


Figure 4.6 Measuring V_{CE} and V_C.

Keep in mind that voltage levels such as V_{CE} are determined by placing the red (positive) lead of the voltmeter at the collector terminal with the black (negative) lead at the emitter terminal as shown in Fig. 4.6. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different. Clearly understanding the difference between the two measurements can prove to be quite important in the troubleshooting of transistor networks.

EXAMPLE 4.1

Determine the following for the fixed-bias configuration of Fig. 4.7.

(a) I_{B_Q} and I_{C_Q}.
(b) V_{CE_Q}.
(c) V_B and V_C.
(d) V_{BC}.

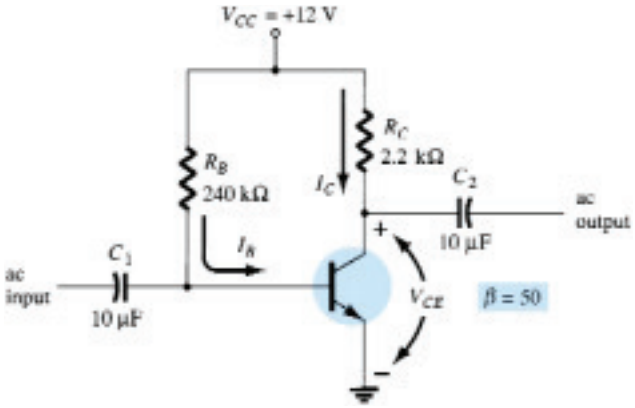


Figure 4.7 dc fixed-bias circuit for Example 4.1.

Solution

(a) Eq. (4.4): $I_{B_Q} = \dfrac{V_{CC} - V_{BE}}{R_B} = \dfrac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \mathbf{47.08\ \mu A}$

Eq. (4.5): $I_{C_Q} = \beta I_{B_Q} = (50)(47.08\ \mu\text{A}) = \mathbf{2.35\ mA}$

(b) Eq. (4.6): $V_{CE_Q} = V_{CC} - I_C R_C$

$= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega)$

$= \mathbf{6.83\ V}$

(c) $V_B = V_{BE} = \mathbf{0.7\ V}$

$V_C = V_{CE} = \mathbf{6.83\ V}$

(d) Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 6.83\text{ V}$$
$$= \mathbf{-6.13\ V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of liquid. For a transistor operating in the saturation region, the current is a maximum value *for the particular design.* Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.

Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation region is depicted in Fig. 4.8a. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below $V_{CE_{sat}}$. In addition, the collector current is relatively high on the characteristics.

If we approximate the curves of Fig. 4.8a by those appearing in Fig. 4.8b, a quick, direct method for determining the saturation level becomes apparent. In Fig. 4.8b, the current is relatively high and the voltage V_{CE} is assumed to be zero volts. Applying Ohm's law the resistance between collector and emitter terminals can be determined as follows:

$$R_{CE} = \frac{V_{CE}}{I_C} = \frac{0\text{ V}}{I_{C_{sat}}} = 0\ \Omega$$

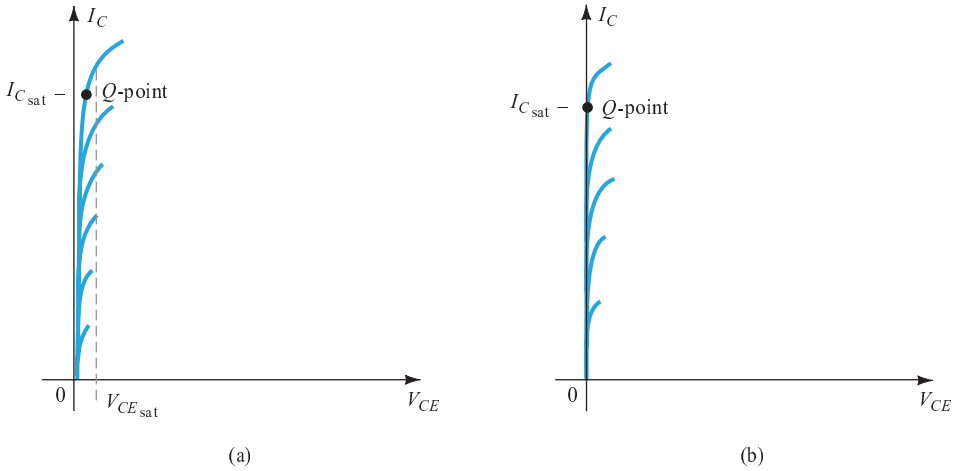


Figure 4.8 Saturation regions: (a) actual; (b) approximate.

Applying the results to the network schematic would result in the configuration of Fig. 4.9.

For the future, therefore, if there were an immediate need to know the approximate maximum collector current (saturation level) for a particular design, simply insert a short-circuit equivalent between collector and emitter of the transistor and calculate the resulting collector current. In short, set $V_{CE} = 0$ V. For the fixed-bias configuration of Fig. 4.10, the short circuit has been applied, causing the voltage across R_C to be the applied voltage V_{CC}. The resulting saturation current for the fixed-bias configuration is

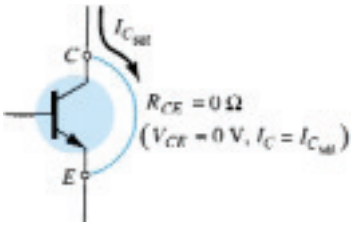


Figure 4.9 Determining $I_{C_{sat}}$.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \tag{4.11}$$

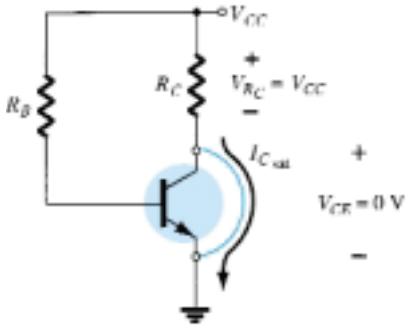


Figure 4.10 Determining $I_{C_{sat}}$ for the fixed-bias configuration.

Once $I_{C_{sat}}$ is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

EXAMPLE 4.2

Determine the saturation level for the network of Fig. 4.7.

Solution

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{12\text{ V}}{2.2\text{ k}\Omega} = \mathbf{5.45\text{ mA}}$$

The design of Example 4.1 resulted in $I_{C_Q} = 2.35$ mA, which is far from the saturation level and about one-half the maximum value for the design.

Load-Line Analysis

The analysis thus far has been performed using a level of β corresponding with the resulting Q-point. We will now investigate how the network parameters define the possible range of Q-points and how the actual Q-point is determined. The network of Fig. 4.11a establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CE} = V_{CC} - I_C R_C \tag{4.12}$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 4.11b.

In essence, therefore, we have a network equation and a set of characteristics that employ the same variables. The common solution of the two occurs where the constraints established by each are satisfied simultaneously. In other words, this is similar to finding the solution of two simultaneous equations: one established by the network and the other by the device characteristics.

The device characteristics of I_C versus V_{CE} are provided in Fig. 4.11b. We must now superimpose the straight line defined by Eq. (4.12) on the characteristics. The most direct method of plotting Eq. (4.12) on the output characteristics is to use the fact that a straight line is defined by two points. If we *choose* I_C to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting $I_C = 0$ mA into Eq. (4.12), we find that

$$V_{CE} = V_{CC} - (0)R_C$$

and

$$V_{CE} = V_{CC}\,|_{I_C = 0\text{ mA}} \tag{4.13}$$

defining one point for the straight line as shown in Fig. 4.12.

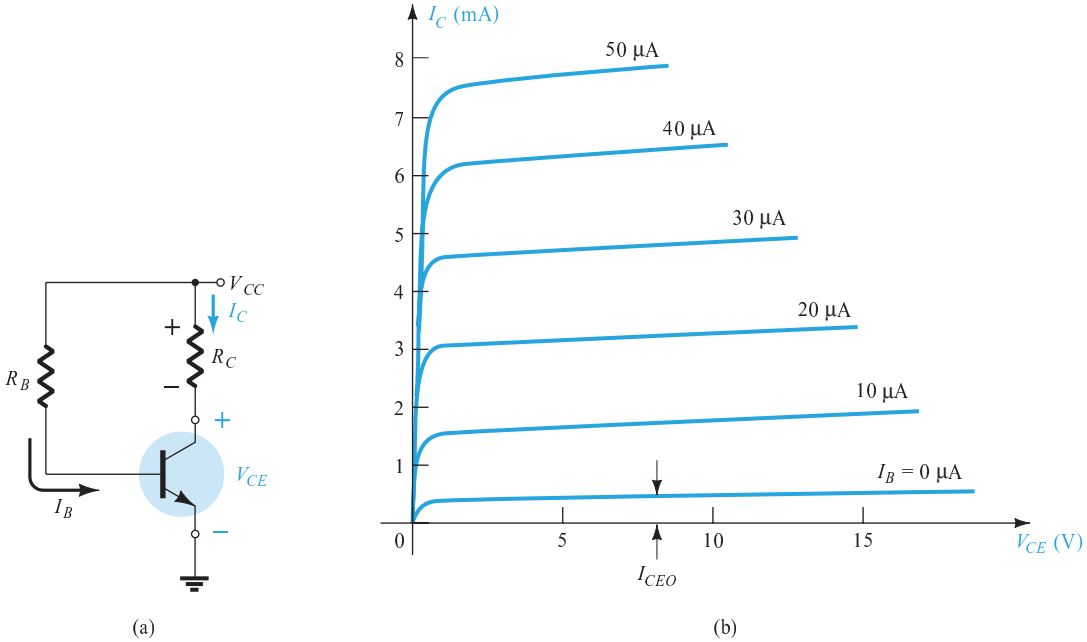


Figure 4.11 Load-line analysis: (a) the network; (b) the device characteristics.

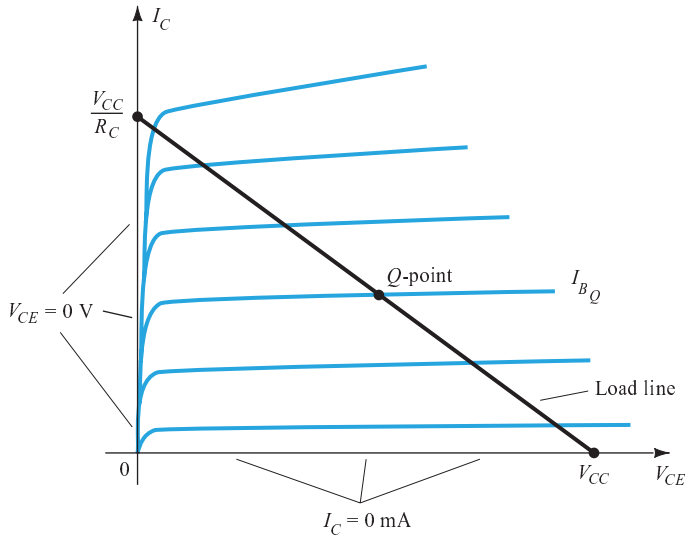


Figure 4.12 Fixed-bias load line.

If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that I_C is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

and

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE} = 0\text{ V}} \tag{4.14}$$

as appearing on Fig. 4.12.

By joining the two points defined by Eqs. (4.13) and (4.14), the straight line established by Eq. (4.12) can be drawn. The resulting line on the graph of Fig. 4.12 is called the *load line* since it is defined by the load resistor R_C. By solving for the resulting level of I_B, the actual Q-point can be established as shown in Fig. 4.12.

If the level of I_B is changed by varying the value of R_B the Q-point moves up or down the load line as shown in Fig. 4.13. If V_{CC} is held fixed and R_C changed, the load line will shift as shown in Fig. 4.14. If I_B is held fixed, the Q-point will move as shown in the same figure. If R_C is fixed and V_{CC} varied, the load line shifts as shown in Fig. 4.15.

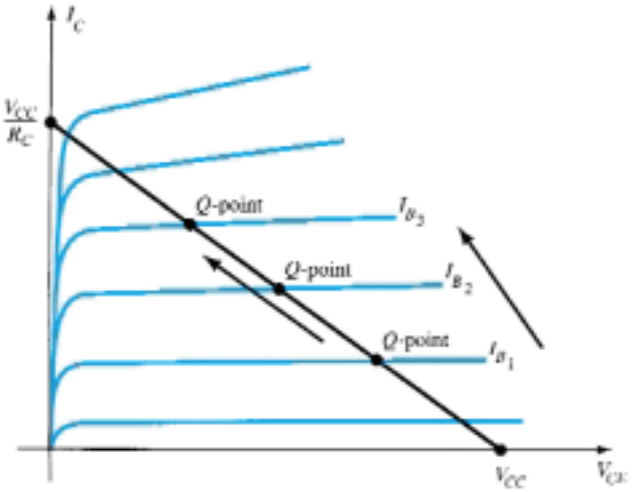


Figure 4.13 Movement of Q-point with increasing levels of I_B.

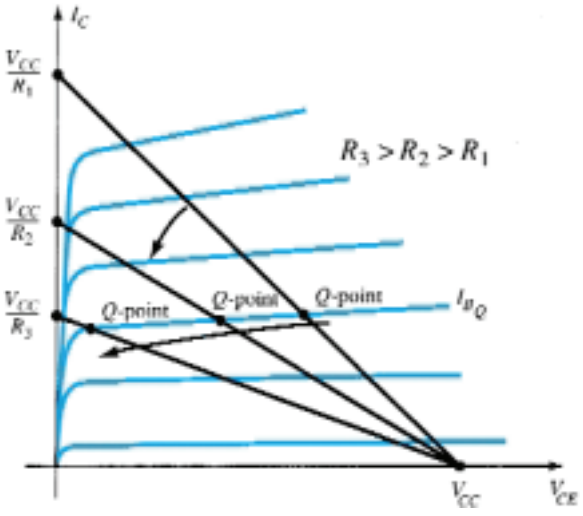


Figure 4.14 Effect of increasing levels of R_C on the load line and Q-point.

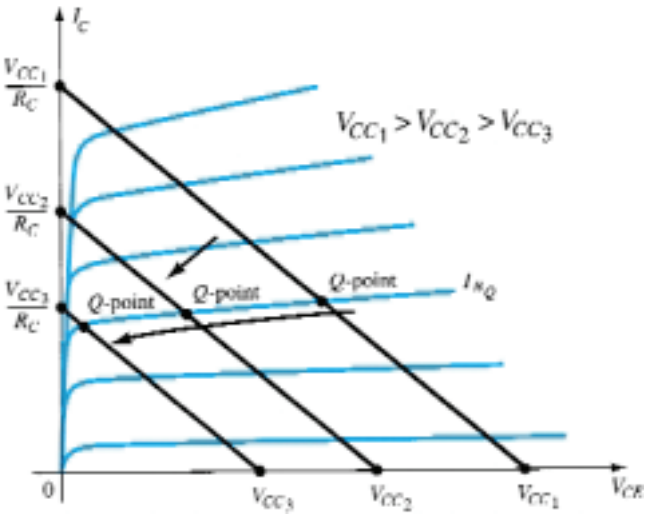


Figure 4.15 Effect of lower values of V_{CC} on the load line and Q-point.

EXAMPLE 4.3

Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

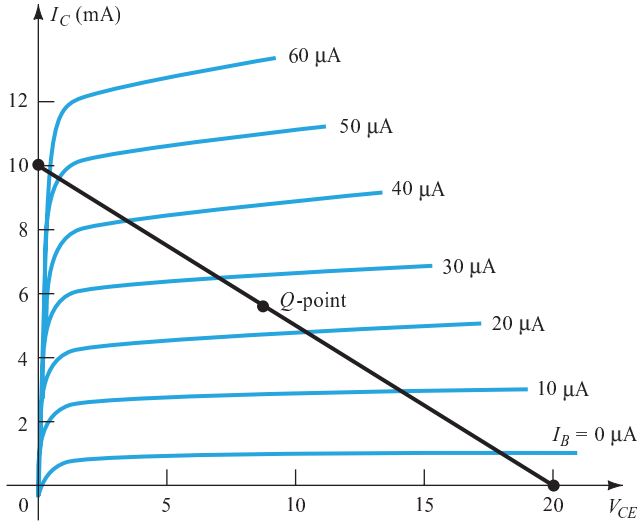


Figure 4.16 Example 4.3

Solution

From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

4.4 EMITTER-STABILIZED BIAS CIRCUIT

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The improved stability will be demonstrated through a numerical example later in the section. The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop.

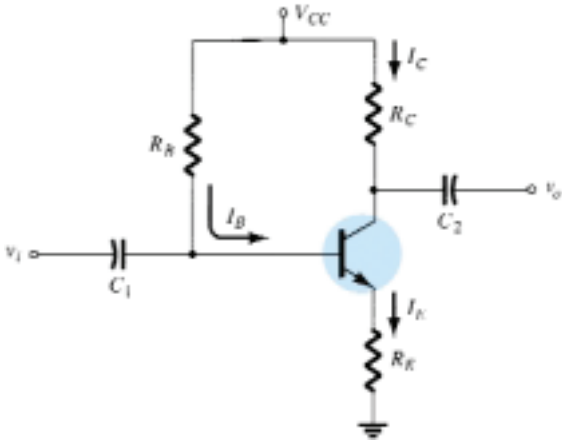


Figure 4.17 BJT bias circuit with emitter resistor.

Base–Emitter Loop

The base–emitter loop of the network of Fig. 4.17 can be redrawn as shown in Fig. 4.18. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \tag{4.15}$$

Recall from Chapter 3 that

$$I_E = (\beta + 1) I_B \tag{4.16}$$

Substituting for I_E in Eq. (4.15) will result in

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I) I_B R_E = 0$$

Grouping terms will then provide the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1) we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

and solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \tag{4.17}$$

Note that the only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(\beta + 1)R_E$.

There is an interesting result that can be derived from Eq. (4.17) if the equation is used to sketch a series network that would result in the same equation. Such is

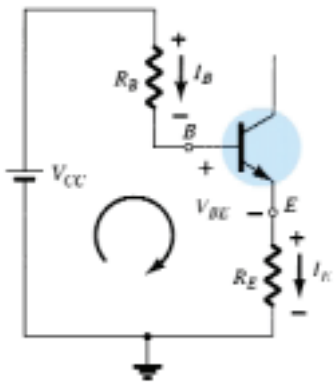


Figure 4.18 Base–emitter loop.

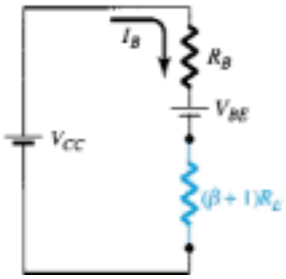


Figure 4.19 Network derived from Eq. (4.17).

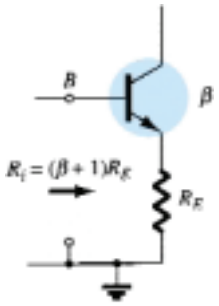


Figure 4.20 Reflected impedance level of R_E.

the case for the network of Fig. 4.19. Solving for the current I_B will result in the same equation obtained above. Note that aside from the base-to-emitter voltage V_{BE}, the resistor R_E is *reflected* back to the input base circuit by a factor $(\beta + 1)$. In other words, the emitter resistor, which is part of the collector–emitter loop, "appears as" $(\beta + 1)R_E$ in the base–emitter loop. Since β is typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 4.20,

$$R_i = (\beta + 1)R_E \tag{4.18}$$

Equation (4.18) is one that will prove useful in the analysis to follow. In fact, it provides a fairly easy way to remember Eq. (4.17). Using Ohm's law, we know that the current through a system is the voltage divided by the resistance of the circuit. For the base–emitter circuit the net voltage is $V_{CC} - V_{BE}$. The resistance levels are R_B plus R_E reflected by $(\beta + 1)$. The result is Eq. (4.17).

Collector–Emitter Loop

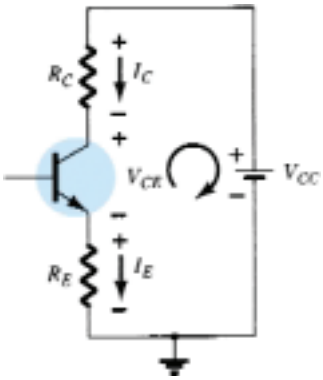


Figure 4.21 Collector–emitter loop.

The collector–emitter loop is redrawn in Fig. 4.21. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction will result in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.19}$$

The single-subscript voltage V_E is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E \tag{4.20}$$

while the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$V_C = V_{CE} + V_E \tag{4.21}$$

or

$$V_C = V_{CC} - I_C R_C \tag{4.22}$$

The voltage at the base with respect to ground can be determined from

$$V_B = V_{CC} - I_B R_B \tag{4.23}$$

or

$$V_B = V_{BE} + V_E \tag{4.24}$$

EXAMPLE 4.4

For the emitter bias network of Fig. 4.22, determine:
(a) I_B.
(b) I_C.
(c) V_{CE}.
(d) V_C.
(e) V_E.
(f) V_B.
(g) V_{BC}.

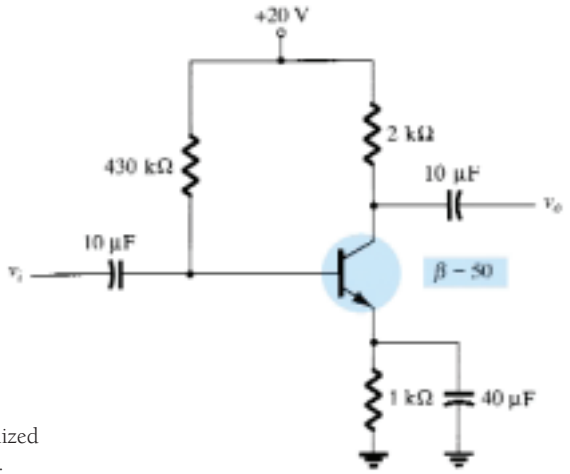


Figure 4.22 Emitter-stabilized bias circuit for Example 4.4.

Solution

(a) Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

(b) $I_C = \beta I_B$
$= (50)(40.1\ \mu\text{A})$
$\cong \mathbf{2.01\ mA}$

(c) Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$
$= \mathbf{13.97\ V}$

(d) $V_C = V_{CC} - I_C R_C$
$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$
$= \mathbf{15.98\ V}$

(e) $V_E = V_C - V_{CE}$
$= 15.98\text{ V} - 13.97\text{ V}$
$= \mathbf{2.01\ V}$

or $V_E = I_E R_E \cong I_C R_E$
$= (2.01\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.01\ V}$

(f) $V_B = V_{BE} + V_E$
$= 0.7\text{ V} + 2.01\text{ V}$
$= \mathbf{2.71\ V}$

(g) $V_{BC} = V_B - V_C$
$= 2.71\text{ V} - 15.98\text{ V}$
$= \mathbf{-13.27\ V}$ (reverse-biased as required)

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change. While a mathematical analysis is provided in Section 4.12, some comparison of the improvement can be obtained as demonstrated by Example 4.5.

EXAMPLE 4.5

Prepare a table and compare the bias voltage and currents of the circuits of Figs. 4.7 and Fig. 4.22 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in I_C and V_{CE} for the same increase in β.

Solution

Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of β. I_B is the same and V_{CE} decreased by 76%.

Using the results calculated in Example 4.4 and then repeating for a value of $\beta = 100$, we have the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

Now the BJT collector current increases by about 81% due to the 100% increase in β. Notice that I_B decreased, helping maintain the value of I_C—or at least reducing the overall change in I_C due to the change in β. The change in V_{CE} has dropped to about 35%. The network of Fig. 4.22 is therefore more stable than that of Fig. 4.7 for the same change in β.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.23 and calculate the resulting collector current. For Fig. 4.23:

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E} \tag{4.25}$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

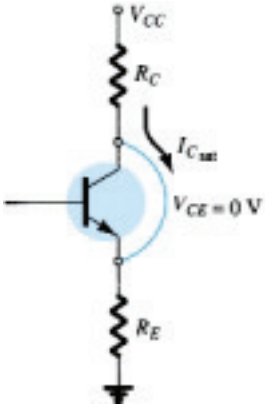


Figure 4.23 Determining $I_{C_{sat}}$ for the emitter-stabilized bias circuit.

Determine the saturation current for the network of Example 4.4.

EXAMPLE 4.6

Solution

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$= \frac{20\ \text{V}}{2\ \text{k}\Omega + 1\ \text{k}\Omega} = \frac{20\ \text{V}}{3\ \text{k}\Omega}$$

$$= \mathbf{6.67\ mA}$$

which is about twice the level of I_{C_Q} for Example 4.4.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I_B as determined by Eq. (4.17) defines the level of I_B on the characteristics of Fig. 4.24 (denoted I_{B_Q}).

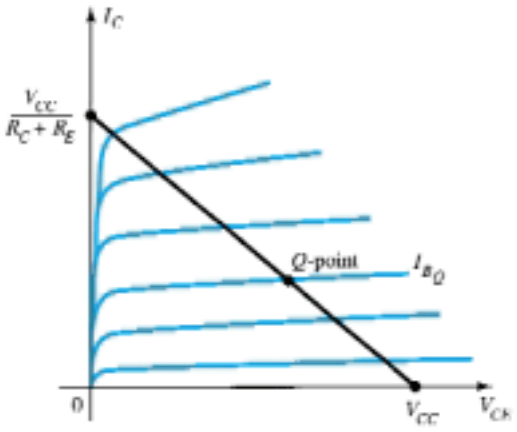


Figure 4.24 Load line for the emitter-bias configuration.

The collector–emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choosing $I_C = 0$ mA gives

$$\boxed{V_{CE} = V_{CC}\big|_{I_C = 0\ \text{mA}}} \tag{4.26}$$

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\ \text{V}}} \tag{4.27}$$

as shown in Fig. 4.24. Different levels of I_{B_Q} will, of course, move the Q-point up or down the load line.

4.5 VOLTAGE-DIVIDER BIAS

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain (β) of the transistor. However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in

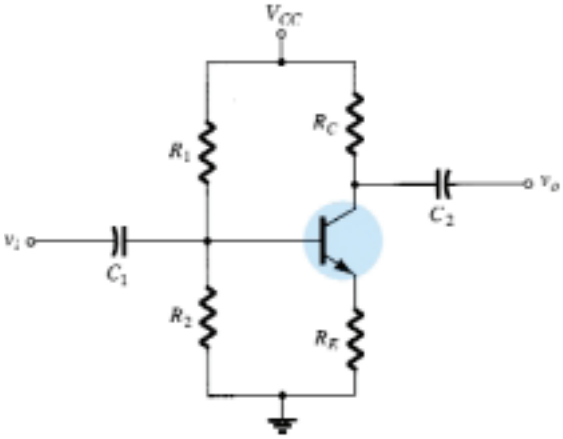


Figure 4.25 Voltage-divider bias configuration.

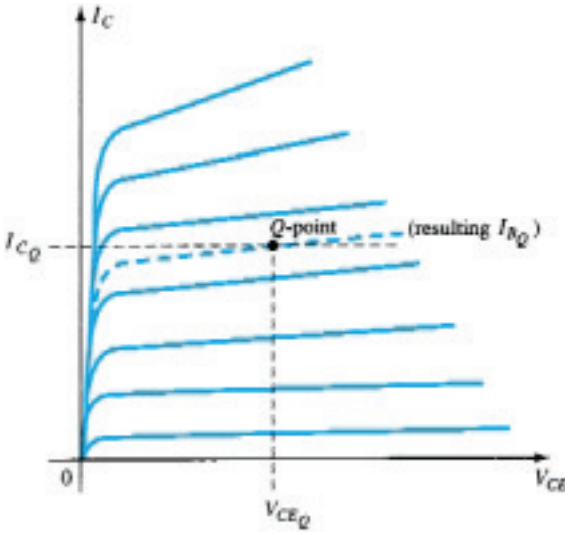


Figure 4.26 Defining the *Q*-point for the voltage-divider bias configuration.

fact, independent of the transistor beta. The voltage-divider bias configuration of Fig. 4.25 is such a network. If analyzed on an exact basis the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{C_Q} and V_{CE_Q} can be almost totally independent of beta. Recall from previous discussions that a *Q*-point is defined by a fixed level of I_{C_Q} and V_{CE_Q} as shown in Fig. 4.26. The level of I_{B_Q} will change with the change in beta, but the operating point on the characteristics defined by I_{C_Q} and V_{CE_Q} can remain fixed if the proper circuit parameters are employed.

As noted above, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method* that can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

Exact Analysis

The input side of the network of Fig. 4.25 can be redrawn as shown in Fig. 4.27 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

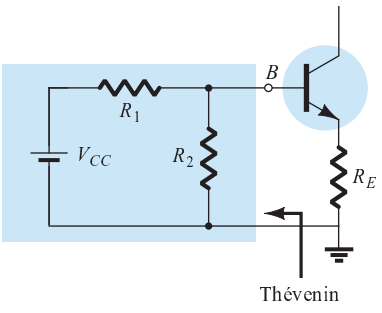


Figure 4.27 Redrawing the input side of the network of Fig. 4.25.

R_{Th}: The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.28.

$$R_{Th} = R_1 \| R_2 \tag{4.28}$$

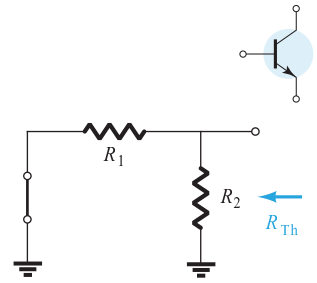


Figure 4.28 Determining R_{Th}.

E_{Th}: The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage of Fig. 4.29 determined as follows:

Applying the voltage-divider rule:

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.29}$$

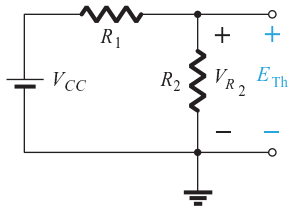


Figure 4.29 Determining E_{Th}.

The Thévenin network is then redrawn as shown in Fig. 4.30, and I_{BQ} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} \tag{4.30}$$

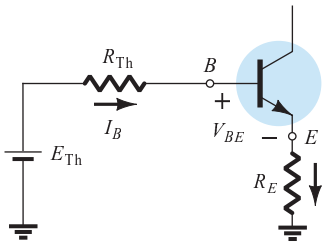


Figure 4.30 Inserting the Thévenin equivalent circuit.

Although Eq. (4.30) initially appears different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is the base resistance plus the emitter resistor reflected by $(\beta + 1)$—certainly very similar to Eq. (4.17).

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.31}$$

which is exactly the same as Eq. (4.19). The remaining equations for V_E, V_C, and V_B are also the same as obtained for the emitter-bias configuration.

EXAMPLE 4.7

Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 4.31.

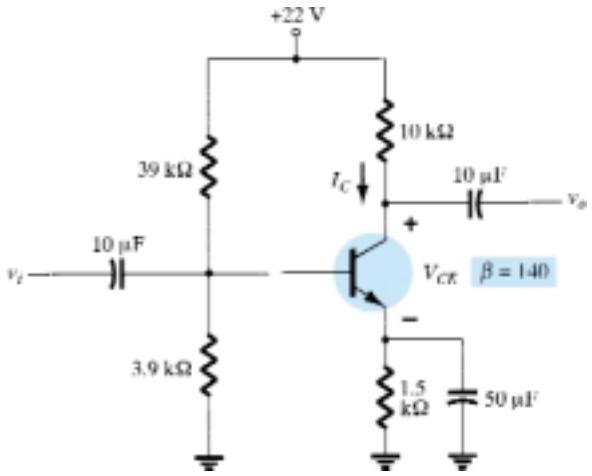


Figure 4.31 Beta-stabilized circuit for Example 4.7.

Solution

Eq. (4.28): $$R_{Th} = R_1 \| R_2$$

$$= \frac{(39\ \text{k}\Omega)(3.9\ \text{k}\Omega)}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 3.55\ \text{k}\Omega$$

Eq. (4.29): $$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 2\ V$$

Eq. (4.30): $$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2\ \text{V} - 0.7\ \text{V}}{3.55\ \text{k}\Omega + (141)(1.5\ \text{k}\Omega)} = \frac{1.3\ \text{V}}{3.55\ \text{k}\Omega + 211.5\ \text{k}\Omega}$$

$$= 6.05\ \mu A$$

$$I_C = \beta I_B$$

$$= (140)(6.05\ \mu\text{A})$$

$$= \mathbf{0.85\ mA}$$

Eq. (4.31): $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22\ \text{V} - (0.85\ \text{mA})(10\ \text{k}\Omega + 1.5\ \text{k}\Omega)$$

$$= 22\ \text{V} - 9.78\ \text{V}$$

$$= \mathbf{12.22\ V}$$

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.32. The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E. Recall from Section 4.4 [Eq. (4.18)] that the reflected resistance between base and emitter is defined by $R_i = (\beta + 1)R_E$. If R_i is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1. If we accept the approximation that I_B is essentially zero amperes compared to I_1 or I_2, then $I_1 = I_2$ and R_1 and R_2 can be considered series ele-

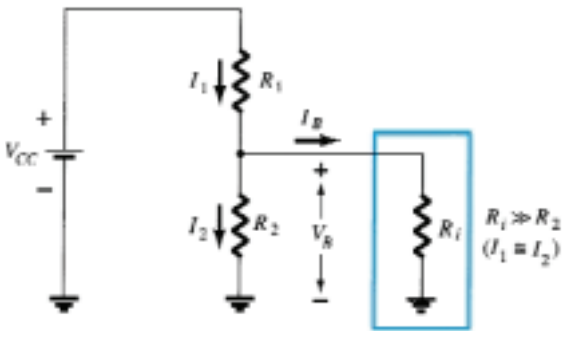


Figure 4.32 Partial-bias circuit for calculating the approximate base voltage V_B.

ments. The voltage across R_2, which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.32}$$

Since $R_i = (\beta + 1)R_E \cong \beta R_E$ the condition that will define whether the approximate approach can be applied will be the following:

$$\beta R_E \geq 10R_2 \tag{4.33}$$

In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE} \tag{4.34}$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \tag{4.35}$$

and

$$I_{C_Q} \cong I_E \tag{4.36}$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but since $I_E \cong I_C$,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) \tag{4.37}$$

Note in the sequence of calculations from Eq. (4.33) through Eq. (4.37) that β does not appear and I_B was not calculated. The Q-point (as determined by I_{C_Q} and V_{CE_Q}) is therefore independent of the value of β.

EXAMPLE 4.8

Repeat the analysis of Fig. 4.31 using the approximate technique, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution

Testing:

$$\beta R_E \geq 10R_2$$

$$(140)(1.5\ \text{k}\Omega) \geq 10(3.9\ \text{k}\Omega)$$

$$210\ \text{k}\Omega \geq 39\ \text{k}\Omega\ (\textit{satisfied})$$

Eq. (4.32):
$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega}$$

$$= 2\ \text{V}$$

Note that the level of V_B is the same as E_{Th} determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of R_{Th} in the exact analysis that separates E_{Th} and V_B.

$$\text{Eq. (4.34):} \quad V_E = V_B - V_{BE}$$
$$= 2\text{ V} - 0.7\text{ V}$$
$$= 1.3\text{ V}$$
$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3\text{ V}}{1.5\text{ k}\Omega} = \mathbf{0.867\text{ mA}}$$

compared to 0.85 mA with the exact analysis. Finally,

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\text{ V} - (0.867\text{ mA})(10\text{ kV} + 1.5\text{ k}\Omega)$$
$$= 22\text{ V} - 9.97\text{ V}$$
$$= \mathbf{12.03\text{ V}}$$

versus 12.22 V obtained in Example 4.7.

The results for I_{C_Q} and V_{CE_Q} are certainly close, and considering the actual variation in parameter values one can certainly be considered as accurate as the other. The larger the level of R_i compared to R_2, the closer the approximate to the exact solution. Example 4.10 will compare solutions at a level well below the condition established by Eq. (4.33).

EXAMPLE 4.9

Repeat the exact analysis of Example 4.7 if β is reduced to 70, and compare solutions for I_{C_Q} and V_{CE_Q}.

Solution

This example is not a comparison of exact versus approximate methods but a testing of how much the Q-point will move if the level of β is cut in half. R_{Th} and E_{Th} are the same:

$$R_{Th} = 3.55\text{ k}\Omega, \qquad E_{Th} = 2\text{ V}$$
$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$
$$= \frac{2\text{ V} - 0.7\text{ V}}{3.55\text{ k}\Omega + (71)(1.5\text{ k}\Omega)} = \frac{1.3\text{ V}}{3.55\text{ k}\Omega + 106.5\text{ k}\Omega}$$
$$= 11.81\ \mu\text{A}$$
$$I_{C_Q} = \beta I_B$$
$$= (70)(11.81\ \mu\text{A})$$
$$= 0.83\text{ mA}$$
$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$
$$= 22\text{ V} - (0.83\text{ mA})(10\text{ k}\Omega + 1.5\text{ k}\Omega)$$
$$= \mathbf{12.46\text{ V}}$$

Tabulating the results, we have:

β	I_{C_Q} (mA)	V_{CE_Q} (V)
140	0.85	12.22
70	0.83	12.46

The results clearly show the relative insensitivity of the circuit to the change in β. Even though β is drastically cut in half, from 140 to 70, the levels of I_{C_Q} and V_{CE_Q} are essentially the same.

EXAMPLE 4.10

Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. 4.33 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) will not be satisfied but the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

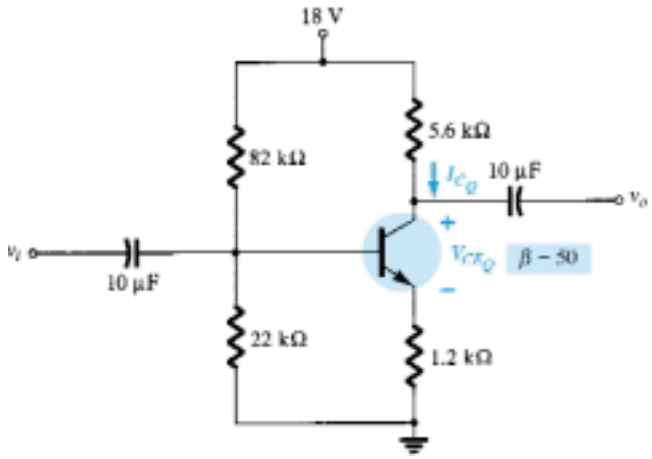


Figure 4.33 Voltage-divider configuration for Example 4.10.

Solution

Exact Analysis

$$\text{Eq. (4.33):} \quad \beta R_E \geq 10R_2$$

$$(50)(1.2\ \text{k}\Omega) \geq 10(22\ \text{k}\Omega)$$

$$60\ \text{k}\Omega \not\geq 220\ \text{k}\Omega\ (\textit{not satisfied})$$

$$R_{\text{Th}} = R_1 \| R_2 = 82\ \text{k}\Omega \| 22\ \text{k}\Omega = 17.35\ \text{k}\Omega$$

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\ \text{k}\Omega(18\ \text{V})}{82\ \text{k}\Omega + 22\ \text{k}\Omega} = 3.81\ \text{V}$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} = \frac{3.81\ \text{V} - 0.7\ \text{V}}{17.35\ \text{k}\Omega + (51)(1.2\ \text{k}\Omega)} = \frac{3.11\ \text{V}}{78.55\ \text{k}\Omega}$$

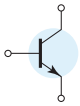
$$= 39.6\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (50)(39.6\ \mu\text{A}) = \mathbf{1.98\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 18\ \text{V} - (1.98\ \text{mA})(5.6\ \text{k}\Omega + 1.2\ \text{k}\Omega)$$

$$= \mathbf{4.54\ V}$$



Approximate Analysis

$$V_B = E_{\text{Th}} = 3.81 \text{ V}$$

$$V_E = V_B - V_{BE} = 3.81 \text{ V} - 0.7 \text{ V} = 3.11 \text{ V}$$

$$I_{C_Q} \cong I_E = \frac{V_E}{R_E} = \frac{3.11 \text{ V}}{1.2 \text{ k}\Omega} = \mathbf{2.59 \text{ mA}}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 18 \text{ V} - (2.59 \text{ mA})(5.6 \text{ k}\Omega + 1.2 \text{ k}\Omega)$$

$$= \mathbf{3.88 \text{ V}}$$

Tabulating the results, we have:

	I_{C_Q} (mA)	V_{CE_Q} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

The results reveal the difference between exact and approximate solutions. I_{C_Q} is about 30% greater with the approximate solution, while V_{CE_Q} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2, the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

Transistor Saturation

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when V_{CE} is set to zero volts on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$I_{C_{\text{sat}}} = I_{C_{\text{max}}} = \frac{V_{CC}}{R_C + R_E} \tag{4.38}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.24, with

$$I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0 \text{ V}} \tag{4.39}$$

and

$$V_{CE} = V_{CC}|_{I_C=0 \text{ mA}} \tag{4.40}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

4.6 DC BIAS WITH VOLTAGE FEEDBACK

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.34. Although the Q-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base–emitter loop with the results applied to the collector–emitter loop.

Base–Emitter Loop

Figure 4.35 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

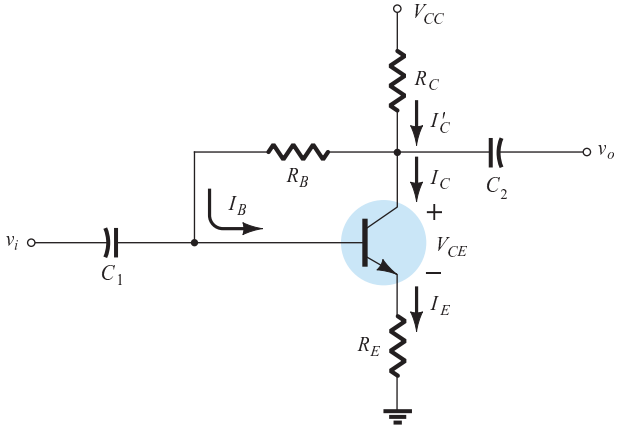


Figure 4.34 dc bias circuit with voltage feedback.

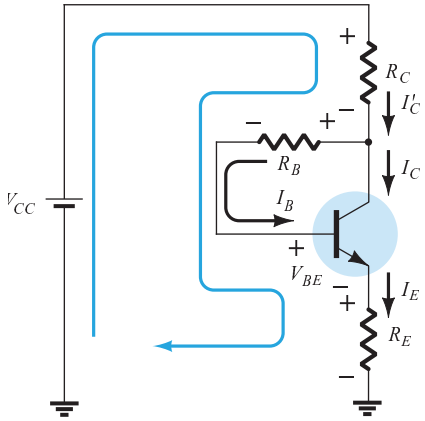


Figure 4.35 Base–emitter loop for the network of Fig. 4.34.

It is important to note that the current through R_C is not I_C but I'_C (where $I'_C = I_C + I_B$). However, the level of I_C and I'_C far exceeds the usual level of I_B and the approximation $I'_C \cong I_C$ is normally employed. Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ will result in

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \tag{4.41}$$

The result is quite interesting in that the format is very similar to equations for I_B obtained for earlier configurations. The numerator is again the difference of available voltage levels, while the denominator is the base resistance plus the collector and emitter resistors reflected by beta. In general, therefore, the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

In general, the equation for I_B has had the following format:

$$I_B = \frac{V'}{R_B + \beta R'}$$

with the absence of R' for the fixed-bias configuration, $R' = R_E$ for the emitter-bias setup (with $(\beta + 1) \cong \beta$), and $R' = R_C + R_E$ for the collector-feedback arrangement. The voltage V' is the difference between two voltage levels.

Since $I_C = \beta I_B$,

$$I_{C_Q} = \frac{\beta V'}{R_B + \beta R'}$$

In general, the larger $\beta R'$ is compared to R_B, the less the sensitivity of I_{C_Q} to variations in beta. Obviously, if $\beta R' \gg R_B$ and $R_B + \beta R' \cong \beta R'$, then

$$I_{C_Q} = \frac{\beta V'}{R_B + \beta R'} \cong \frac{\beta V'}{\beta R'} = \frac{V'}{R'}$$

and I_{C_Q} is independent of the value of beta. Since R' is typically larger for the voltage-feedback configuration than for the emitter-bias configuration, the sensitivity to variations in beta is less. Of course, R' is zero ohms for the fixed-bias configuration and is therefore quite sensitive to variations in beta.

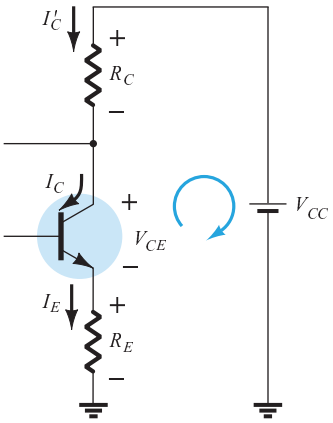


Figure 4.36 Collector–emitter loop for the network of Fig. 4.34.

Collector–Emitter Loop

The collector–emitter loop for the network of Fig. 4.34 is provided in Fig. 4.36. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_E \cong I_C$, we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)} \tag{4.42}$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

EXAMPLE 4.11

Determine the quiescent levels of I_{C_Q} and V_{CE_Q} for the network of Fig. 4.37.

Solution

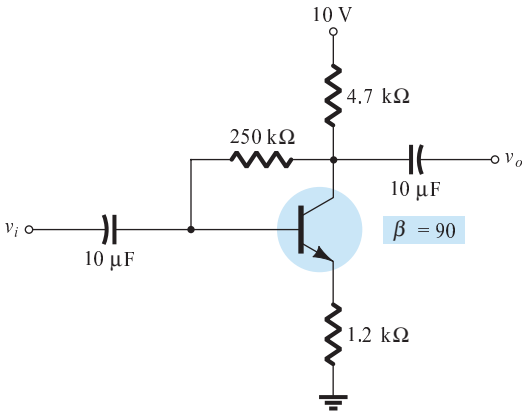


Figure 4.37 Network for Example 4.11.

Eq. (4.41): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (90)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 531\text{ k}\Omega} = \frac{9.3\text{ V}}{781\text{ k}\Omega}$$

$$= 11.91\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (90)(11.91\ \mu\text{A})$$

$$= \mathbf{1.07\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.07\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 6.31\text{ V}$$

$$= \mathbf{3.69\text{ V}}$$

Repeat Example 4.11 using a beta of 135 (50% more than Example 4.11). *EXAMPLE 4.12*

Solution

It is important to note in the solution for I_B in Example 4.11 that the second term in the denominator of the equation is larger than the first. Recall in a recent discussion that the larger this second term is compared to the first, the less the sensitivity to changes in beta. In this example the level of beta is increased by 50%, which will increase the magnitude of this second term even more compared to the first. It is more important to note in these examples, however, that once the second term is relatively large compared to the first, the sensitivity to changes in beta is significantly less.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{10\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (135)(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)}$$

$$= \frac{9.3\text{ V}}{250\text{ k}\Omega + 796.5\text{ k}\Omega} = \frac{9.3\text{ V}}{1046.5\text{ k}\Omega}$$

$$= 8.89\ \mu\text{A}$$

and $$I_{C_Q} = \beta I_B$$

$$= (135)(8.89\ \mu\text{A})$$

$$= \mathbf{1.2\text{ mA}}$$

and $$V_{CE_Q} = V_{CC} - I_C(R_C + R_E)$$

$$= 10\text{ V} - (1.2\text{ mA})(4.7\text{ k}\Omega + 1.2\text{ k}\Omega)$$

$$= 10\text{ V} - 7.08\text{ V}$$

$$= \mathbf{2.92\text{ V}}$$

Even though the level of β increased 50%, the level of I_{C_Q} only increased 12.1% while the level of V_{CE_Q} decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in β would have resulted in a 50% increase in I_{C_Q} and a dramatic change in the location of the Q-point.

Determine the dc level of I_B and V_C for the network of Fig. 4.38. *EXAMPLE 4.13*

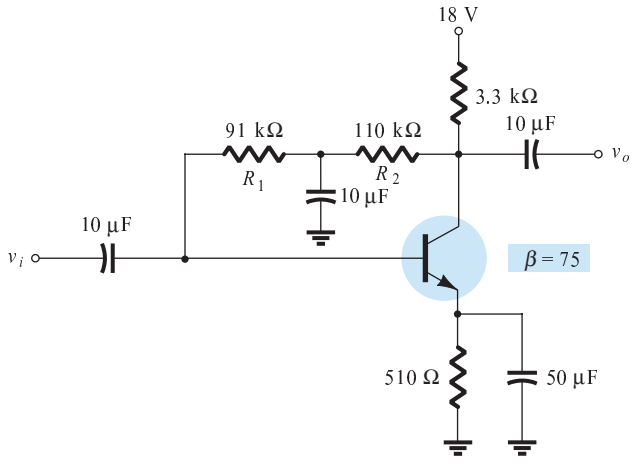
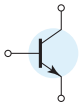


Figure 4.38 Network for Example 4.13.



Solution

In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence and $R_B = R_1 + R_2$.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{18\text{ V} - 0.7\text{ V}}{(91\text{ k}\Omega + 110\text{ k}\Omega) + (75)(3.3\text{ k}\Omega + 0.51\text{ k}\Omega)}$$

$$= \frac{17.3\text{ V}}{201\text{ k}\Omega + 285.75\text{ k}\Omega} = \frac{17.3\text{ V}}{486.75\text{ k}\Omega}$$

$$= \mathbf{35.5\ \mu A}$$

$$I_C = \beta I_B$$

$$= (75)(35.5\ \mu\text{A})$$

$$= 2.66\text{ mA}$$

$$V_C = V_{CC} - I'_C R_C \cong V_{CC} - I_C R_C$$

$$= 18\text{ V} - (2.66\text{ mA})(3.3\text{ k}\Omega)$$

$$= 18\text{ V} - 8.78\text{ V}$$

$$= \mathbf{9.22\text{ V}}$$

Saturation Conditions

Using the approximation $I'_C = I_C$, the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.43}$$

Load-Line Analysis

Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{B_Q} will be defined by the chosen bias configuration.

4.7 MISCELLANEOUS BIAS CONFIGURATIONS

There are a number of BJT bias configurations that do not match the basic mold of those analyzed in the previous sections. In fact, there are variations in design that would require many more pages than is possible in a book of this type. However, the primary purpose here is to emphasize those characteristics of the device that permit a dc analysis of the configuration and to establish a general procedure toward the desired solution. For each configuration discussed thus far, the first step has been the derivation of an expression for the base current. Once the base current is known, the collector current and voltage levels of the output circuit can be determined quite di-

rectly. This is not to imply that all solutions will take this path, but it does suggest a possible route to follow if a new configuration is encountered.

The first example is simply one where the emitter resistor has been dropped from the voltage-feedback configuration of Fig. 4.34. The analysis is quite similar but does require dropping R_E from the applied equation.

EXAMPLE 4.14

For the network of Fig. 4.39:
(a) Determine I_{C_Q} and V_{CE_Q}.
(b) Find V_B, V_C, V_E, and V_{BC}.

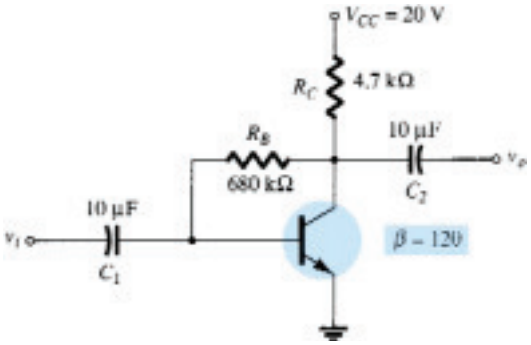


Figure 4.39 Collector feedback with $R_E = 0\ \Omega$.

Solution

(a) The absence of R_E reduces the reflection of resistive levels to simply that of R_C and the equation for I_B reduces to

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

$$= \frac{20\text{ V} - 0.7\text{ V}}{680\text{ k}\Omega + (120)(4.7\text{ k}\Omega)} = \frac{19.3\text{ V}}{1.244\text{ M}\Omega}$$

$$= 15.51\ \mu\text{A}$$

$$I_{C_Q} = \beta I_B = (120)(15.51\ \mu\text{A})$$

$$= \mathbf{1.86\ mA}$$

$$V_{CE_Q} = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (1.86\text{ mA})(4.7\text{ k}\Omega)$$

$$= \mathbf{11.26\ V}$$

$$V_B = V_{BE} = \mathbf{0.7\ V}$$

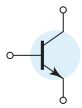
$$V_C = V_{CE} = \mathbf{11.26\ V}$$

$$V_E = \mathbf{0\ V}$$

$$V_{BC} = V_B - V_C = 0.7\text{ V} - 11.26\text{ V}$$

$$= \mathbf{-10.56\ V}$$

In the next example, the applied voltage is connected to the emitter leg and R_C is connected directly to ground. Initially, it appears somewhat unorthodox and quite different from those encountered thus far, but one application of Kirchhoff's voltage law to the base circuit will result in the desired base current.



EXAMPLE 4.15 Determine V_C and V_B for the network of Fig. 4.40.

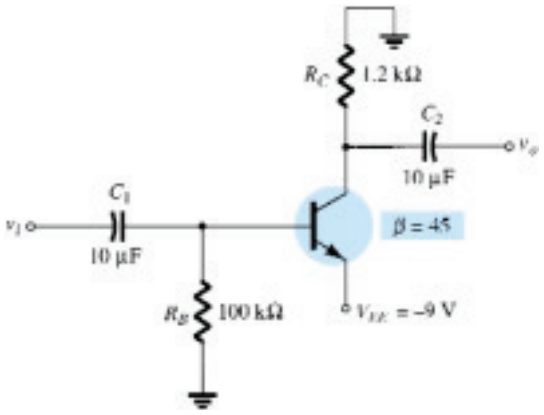


Figure 4.40 Example 4.15

Solution

Applying Kirchhoff's voltage law in the clockwise direction for the base–emitter loop will result in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

and

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

Substitution yields

$$I_B = \frac{9\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega}$$

$$= \frac{8.3\text{ V}}{100\text{ k}\Omega}$$

$$= 83\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (45)(83\ \mu\text{A})$$

$$= 3.735\text{ mA}$$

$$V_C = -I_C R_C$$

$$= -(3.735\text{ mA})(1.2\text{ k}\Omega)$$

$$= \mathbf{-4.48\text{ V}}$$

$$V_B = -I_B R_B$$

$$= -(83\ \mu\text{A})(100\text{ k}\Omega)$$

$$= \mathbf{-8.3\text{ V}}$$

The next example employs a network referred to as an *emitter-follower* configuration. When the same network is analyzed on an ac basis, we will find that the output and input signals are in phase (one following the other) and the output voltage is slightly less than the applied signal. For the dc analysis the collector is grounded and the applied voltage is in the emitter leg.

Determine V_{CE_Q} and I_E for the network of Fig. 4.41.

EXAMPLE 4.16

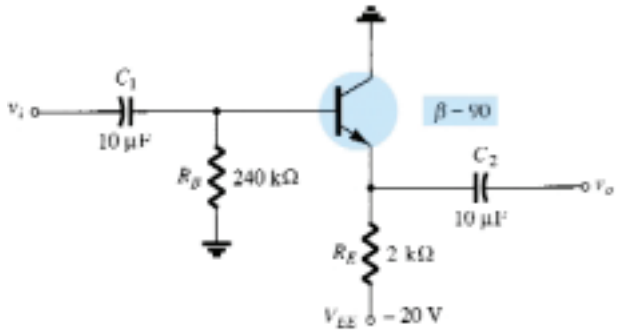


Figure 4.41 Common-collector (emitter-follower) configuration.

Solution

Applying Kirchhoff's voltage law to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

but $$I_E = (\beta + 1) I_B$$

and $$V_{EE} - V_{BE} - (\beta + 1) I_B R_E - I_B R_B = 0$$

with $$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1) R_E}$$

Substituting values yields

$$I_B = \frac{20\ \text{V} - 0.7\ \text{V}}{240\ \text{k}\Omega + (91)(2\ \text{k}\Omega)}$$

$$= \frac{19.3\ \text{V}}{240\ \text{k}\Omega + 182\ \text{k}\Omega} = \frac{19.3\ \text{V}}{422\ \text{k}\Omega}$$

$$= 45.73\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (90)(45.73\ \mu\text{A})$$

$$= 4.12\ \text{mA}$$

Applying Kirchhoff's voltage law to the output circuit, we have

$$-V_{EE} + I_E R_E + V_{CE} = 0$$

but $$I_E = (\beta + 1) I_B$$

and $$V_{CE_Q} = V_{EE} - (\beta + 1) I_B R_E$$

$$= 20\ \text{V} - (91)(45.73\ \mu\text{A})(2\ \text{k}\Omega)$$

$$= \mathbf{11.68\ V}$$

$$I_E = \mathbf{4.16\ mA}$$

All of the examples thus far have employed a common-emitter or common-collector configuration. In the next example we investigate the common-base configuration. In this situation the input circuit will be employed to determine I_E rather than I_B. The collector current is then available to perform an analysis of the output circuit.

EXAMPLE 4.17

Determine the voltage V_{CB} and the current I_B for the common-base configuration of Fig. 4.42.

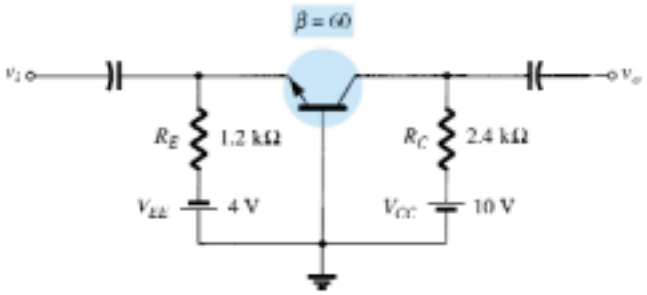


Figure 4.42 Common-base configuration.

Solution

Applying Kirchhoff's voltage law to the input circuit yields

$$-V_{EE} + I_E R_E + V_{BE} = 0$$

and

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

Substituting values, we obtain

$$I_E = \frac{4\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = 2.75\text{ mA}$$

Applying Kirchhoff's voltage law to the output circuit gives

$$-V_{CB} + I_C R_C - V_{CC} = 0$$

and

$$V_{CB} = V_{CC} - I_C R_C \text{ with } I_C \cong I_E$$
$$= 10\text{ V} - (2.75\text{ mA})(2.4\text{ k}\Omega)$$
$$= \mathbf{3.4\text{ V}}$$

$$I_B = \frac{I_C}{\beta}$$
$$= \frac{2.75\text{ mA}}{60}$$
$$= \mathbf{45.8\ \mu A}$$

Example 4.18 employs a split supply and will require the application of Thévenin's theorem to determine the desired unknowns.

Determine V_C and V_B for the network of Fig. 4.43.

EXAMPLE 4.18

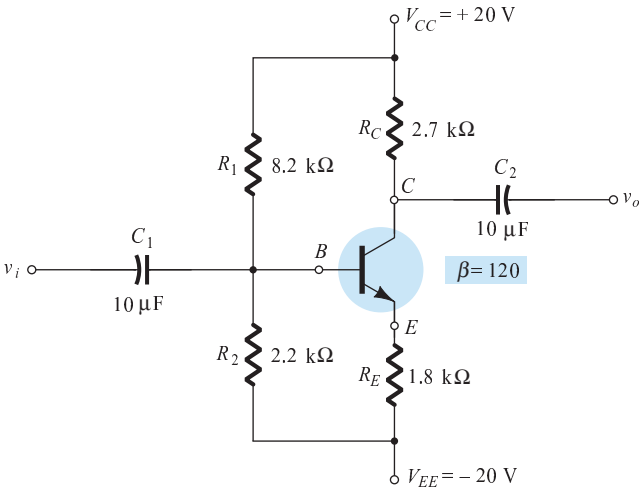


Figure 4.43 Example 4.18

Solution

The Thévenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 4.44 and 4.45.

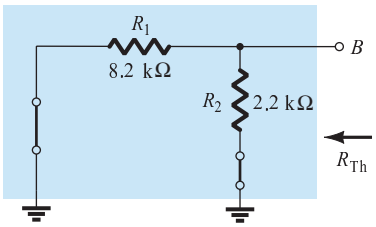


Figure 4.44 Determining R_{Th}.

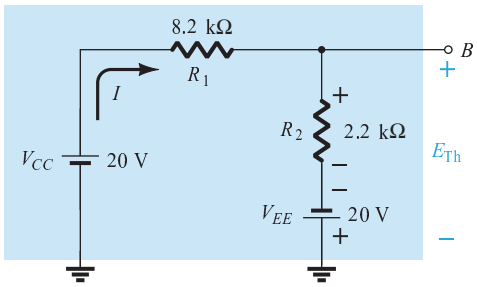


Figure 4.45 Determining E_{Th}.

R_{Th}:

$$R_{Th} = 8.2\ \text{k}\Omega \| 2.2\ \text{k}\Omega = 1.73\ \text{k}\Omega$$

E_{Th}:

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20\ \text{V} + 20\ \text{V}}{8.2\ \text{k}\Omega + 2.2\ \text{k}\Omega} = \frac{40\ \text{V}}{10.4\ \text{k}\Omega}$$

$$= 3.85\ \text{mA}$$

$$E_{Th} = IR_2 - V_{EE}$$

$$= (3.85\ \text{mA})(2.2\ \text{k}\Omega) - 20\ \text{V}$$

$$= -11.53\ \text{V}$$

The network can then be redrawn as shown in Fig. 4.46, where the application of Kirchhoff's voltage law will result in

$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0$$

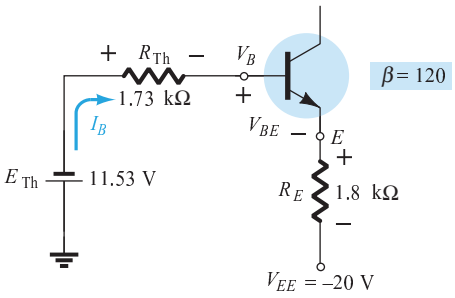


Figure 4.46 Substituting the Thévenin equivalent circuit.

Substituting $I_E = (\beta + 1)I_B$ gives

$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1)I_B R_E - I_B R_{Th} = 0$$

and

$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{20\text{ V} - 11.53\text{ V} - 0.7\text{ V}}{1.73\text{ k}\Omega + (121)(1.8\text{ k}\Omega)}$$

$$= \frac{7.77\text{ V}}{219.53\text{ k}\Omega}$$

$$= 35.39\ \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (120)(35.39\ \mu\text{A})$$

$$= 4.25\text{ mA}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 20\text{ V} - (4.25\text{ mA})(2.7\text{ k}\Omega)$$

$$= \mathbf{8.53\text{ V}}$$

$$V_B = -E_{Th} - I_B R_{Th}$$

$$= -(11.53\text{ V}) - (35.39\ \mu\text{A})(1.73\text{ k}\Omega)$$

$$= \mathbf{-11.59\text{ V}}$$

4.8 DESIGN OPERATIONS

Discussions thus far have focused on the analysis of existing networks. All the elements are in place and it is simply a matter of solving for the current and voltage levels of the configuration. The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined. This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on. In most situations the thinking process is challenged to a higher degree in the design process than in the analysis sequence. The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network.

The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design. Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design. This is certainly a valid approximation considering the tolerances normally associated with resistive elements and the transistor parameters.

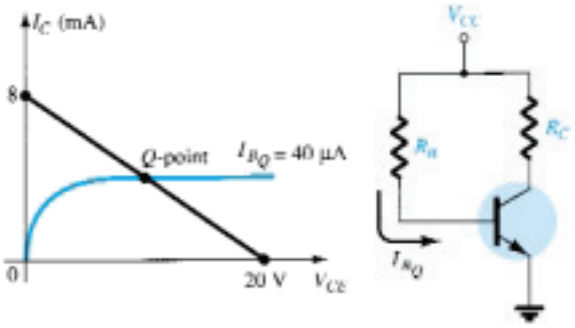
If resistive values are to be determined, one of the most powerful equations is simply Ohm's law in the following form:

$$R_{\text{unk}} = \frac{V_R}{I_R} \tag{4.44}$$

In a particular design the voltage across a resistor can often be determined from specified levels. If additional specifications define the current level, Eq. (4.44) can then be used to calculate the required resistance level. The first few examples will demonstrate how particular elements can be determined from specified levels. A complete design procedure will then be introduced for two popular configurations.

EXAMPLE 4.19

Given the device characteristics of Fig. 4.47a, determine V_{CC}, R_B, and R_C for the fixed-bias configuration of Fig. 4.47b.



(a) (b)

Figure 4.47 Example 4.19

Solution

From the load line

$$V_{CC} = \mathbf{20\ V}$$

$$I_C = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE} = 0\ \text{V}}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{8\ \text{mA}} = \mathbf{2.5\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$= \frac{20\ \text{V} - 0.7\ \text{V}}{40\ \mu\text{A}} = \frac{19.3\ \text{V}}{40\ \mu\text{A}}$$

$$= \mathbf{482.5\ k\Omega}$$

Standard resistor values:

$$R_C = 2.4\ \text{k}\Omega$$

$$R_B = 470\ \text{k}\Omega$$

Using standard resistor values gives

$$I_B = 41.1\ \mu\text{A}$$

which is well within 5% of the value specified.

EXAMPLE 4.20

Given that $I_{C_Q} = 2$ mA and $V_{CE_Q} = 10$ V, determine R_1 and R_C for the network of Fig. 4.48.

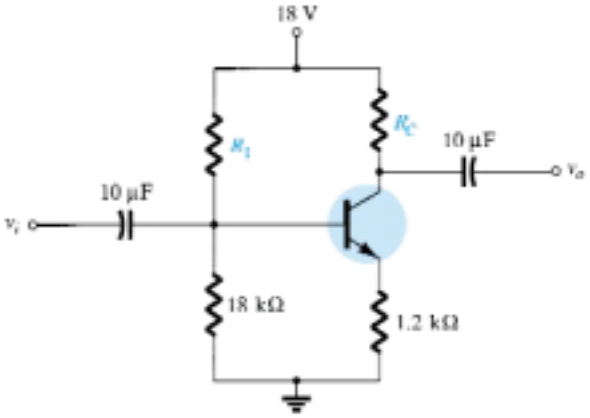


Figure 4.48 Example 4.20

Solution

$$V_E = I_E R_E \cong I_C R_E$$

$$= (2\ \text{mA})(1.2\ \text{k}\Omega) = 2.4\ \text{V}$$

$$V_B = V_{BE} + V_E = 0.7\ \text{V} + 2.4\ \text{V} = 3.1\ \text{V}$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 3.1\ \text{V}$$

and

$$\frac{(18\ \text{k}\Omega)(18\ \text{V})}{R_1 + 18\ \text{k}\Omega} = 3.1\ \text{V}$$

$$324\ \text{k}\Omega = 3.1R_1 + 55.8\ \text{k}\Omega$$

$$3.1R_1 = 268.2\ \text{k}\Omega$$

$$R_1 = \frac{268.2\ \text{k}\Omega}{3.1} = \mathbf{86.52\ k\Omega}$$

Eq. (4.44):

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C}$$

with

$$V_C = V_{CE} + V_E = 10\ \text{V} + 2.4\ \text{V} = 12.4\ \text{V}$$

and

$$R_C = \frac{18\ \text{V} - 12.4\text{V}}{2\text{mA}}$$

$$= \mathbf{2.8\ k\Omega}$$

The nearest standard commercial values to R_1 are 82 and 91 kΩ. However, using the series combination of standard values of 82 kΩ and 4.7 kΩ = 86.7 kΩ would result in a value very close to the design level.

EXAMPLE 4.21

The emitter-bias configuration of Fig. 4.49 has the following specifications: $I_{C_Q} = \frac{1}{2}I_{C_{sat}}$, $I_{C_{sat}} = 8$ mA, $V_C = 18$ V, and $\beta = 110$. Determine R_C, R_E, and R_B.

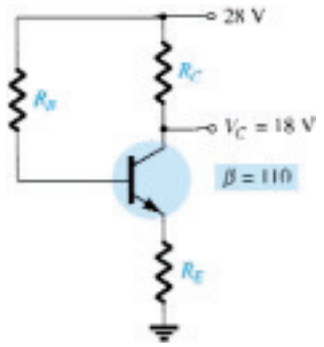


Figure 4.49 Example 4.21

Solution

$$I_{C_Q} = \tfrac{1}{2}I_{C_{sat}} = 4 \text{ mA}$$

$$R_C = \frac{V_{R_C}}{I_{C_Q}} = \frac{V_{CC} - V_C}{I_{C_Q}}$$

$$= \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ m}A} = \mathbf{2.5\ k\Omega}$$

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

and

$$R_C + R_E = \frac{V_{CC}}{I_{C_{sat}}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = 3.5 \text{ k}\Omega - R_C$$

$$= 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega$$

$$= \mathbf{1\ k\Omega}$$

$$I_{B_Q} = \frac{I_{C_Q}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36\ \mu\text{A}$$

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

and

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_Q}}$$

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_Q}} - (\beta + 1)R_E$$

$$= \frac{28 \text{ V} - 0.7 \text{ V}}{36.36\ \mu\text{A}} - (111)(1 \text{ k}\Omega)$$

$$= \frac{27.3 \text{ V}}{36.36\ \mu\text{A}} - 111 \text{ k}\Omega$$

$$= \mathbf{639.8\ k\Omega}$$

For standard values:

$$R_C = 2.4\ \text{k}\Omega$$
$$R_E = 1\ \text{k}\Omega$$
$$R_B = 620\ \text{k}\Omega$$

The discussion to follow will introduce one technique for designing an entire circuit to operate at a specified bias point. Often the manufacturer's specification (spec) sheets provide information on a suggested operating point (or operating region) for a particular transistor. In addition, other system components connected to the given amplifier stage may also define the current swing, voltage swing, value of common supply voltage, and so on, for the design.

In actual practice, many other factors may have to be considered that may affect the selection of the desired operating point. For the moment we shall concentrate, however, on determining the component values to obtain a specified operating point. The discussion will be limited to the emitter-bias and voltage-divider bias configurations, although the same procedure can be applied to a variety of other transistor circuits.

Design of a Bias Circuit with an Emitter Feedback Resistor

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.50. The supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.

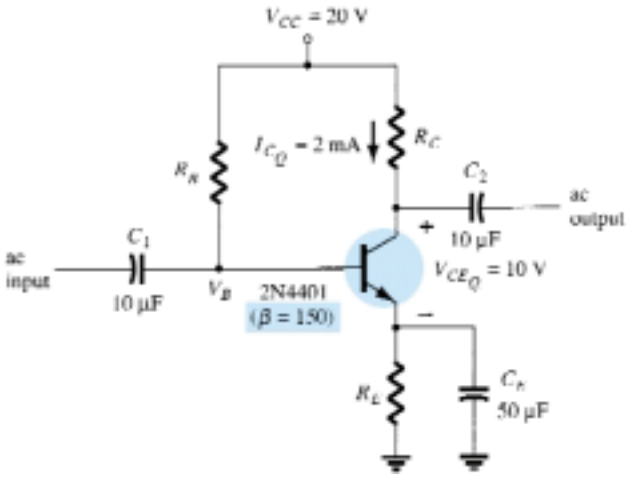


Figure 4.50 Emitter-stabilized bias circuit for design consideration.

The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector–emitter loop has two unknown quantities present—the resistors R_C and R_E. At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be unreasonably large because the voltage across it limits the range of voltage swing of the voltage from collector to emitter (to be noted when the ac re-

sponse is discussed). The examples examined in this chapter reveal that the voltage from emitter to ground is typically around one-fourth to one-tenth of the supply voltage. Selecting the conservative case of one-tenth will permit calculating the emitter resistor R_E and the resistor R_C in a manner similar to the examples just completed. In the next example we perform a complete design of the network of Fig. 4.49 using the criteria just introduced for the emitter voltage.

EXAMPLE 4.22

Determine the resistor values for the network of Fig. 4.50 for the indicated operating point and supply voltage.

Solution

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{2\text{ mA}} = \mathbf{1\ k\Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 10\text{ V} - 2\text{ V}}{2\text{ mA}} = \frac{8\text{ V}}{2\text{ mA}}$$

$$= \mathbf{4\ k\Omega}$$

$$I_B = \frac{I_C}{\beta} = \frac{2\text{ mA}}{150} = 13.33\ \mu\text{A}$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{20\text{ V} - 0.7\text{ V} - 2\text{ V}}{13.33\ \mu\text{A}}$$

$$\cong \mathbf{1.3\ M\Omega}$$

Design of a Current-Gain-Stabilized (Beta-Independent) Circuit

The circuit of Fig. 4.51 provides stabilization both for leakage and current gain (beta) changes. The four resistor values shown must be obtained for the specified operating point. Engineering judgment in selecting a value of emitter voltage, V_E, as in the previous design consideration, leads to a direct straightforward solution for all the resistor values. The design steps are all demonstrated in the next example.

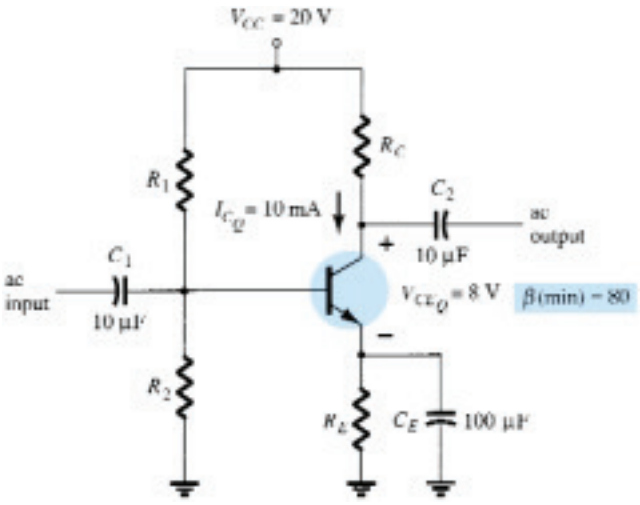
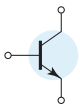


Figure 4.51 Current-gain-stabilized circuit for design considerations.



EXAMPLE 4.23 Determine the levels of R_C, R_E, R_1, and R_2 for the network of Fig. 4.51 for the operating point indicated.

Solution

$$V_E = \tfrac{1}{10}V_{CC} = \tfrac{1}{10}(20\text{ V}) = 2\text{ V}$$

$$R_E = \frac{V_E}{I_E} \cong \frac{V_E}{I_C} = \frac{2\text{ V}}{10\text{ mA}} = \mathbf{200\ \Omega}$$

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{20\text{ V} - 8\text{ V} - 2\text{ V}}{10\text{ mA}} = \frac{10\text{ V}}{10\text{ mA}}$$

$$= \mathbf{1\ k\Omega}$$

$$V_B = V_{BE} + V_E = 0.7\text{ V} + 2\text{ V} = 2.7\text{ V}$$

The equations for the calculation of the base resistors R_1 and R_2 will require a little thought. Using the value of base voltage calculated above and the value of the supply voltage will provide one equation—but there are two unknowns, R_1 and R_2. An additional equation can be obtained from an understanding of the operation of these two resistors in providing the necessary base voltage. For the circuit to operate efficiently, it is assumed that the current through R_1 and R_2 should be approximately equal and much larger than the base current (at least 10:1). This fact and the voltage-divider equation for the base voltage provide the two relationships necessary to determine the base resistors. That is,

$$R_2 \leq \tfrac{1}{10}\beta R_E$$

and

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC}$$

Substitution yields

$$R_2 \leq \tfrac{1}{10}(80)(0.2\text{ k}\Omega)$$

$$= \mathbf{1.6\ k\Omega}$$

$$V_B = 2.7\text{ V} = \frac{(1.6\text{ k}\Omega)(20\text{ V})}{R_1 + 1.6\text{ k}\Omega}$$

and

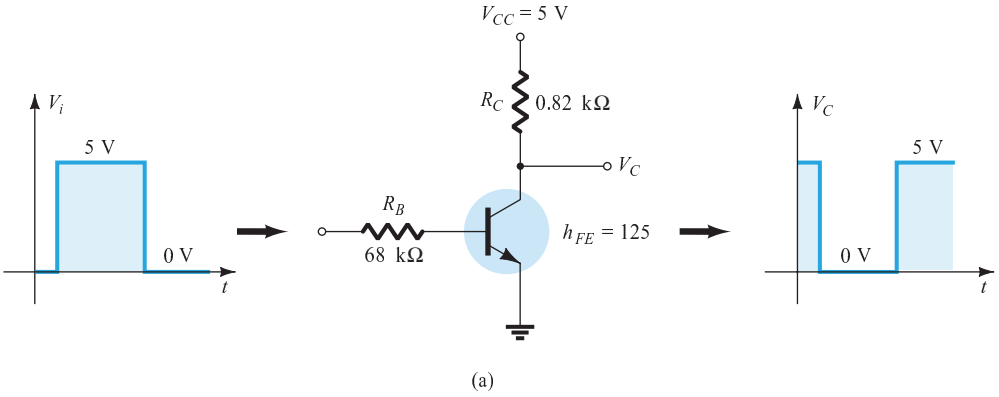
$$2.7R_1 + 4.32\text{ k}\Omega = 32\text{ k}\Omega$$

$$2.7R_1 = 27.68\text{ k}\Omega$$

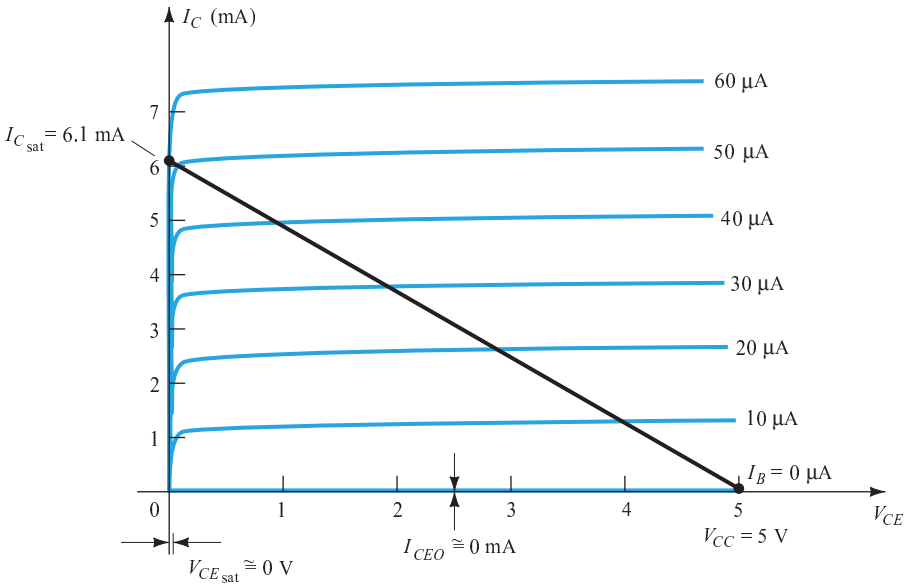
$$R_1 = \mathbf{10.25\ k\Omega} \quad \text{(use 10 k}\Omega\text{)}$$

4.9 TRANSISTOR SWITCHING NETWORKS

The application of transistors is not limited solely to the amplification of signals. Through proper design it can be used as a switch for computer and control applications. The network of Fig. 4.52a can be employed as an *inverter* in computer logic circuitry. Note that the output voltage V_C is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side and for computer applications is typically equal to the magnitude of the "high" side of the applied signal—in this case 5 V.



(a)



(b)

Figure 4.52 Transistor inverter.

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 4.52b. For our purposes we will assume that $I_C = I_{CEO} = 0$ mA when $I_B = 0$ μA (an excellent approximation in light of improving construction techniques), as shown in Fig. 4.52b. In addition, we will assume that $V_{CE} = V_{CE_{sat}} = 0$ V rather than the typical 0.1- to 0.3-V level.

When $V_i = 5$ V, the transistor will be "on" and the design must ensure that the network is heavily saturated by a level of I_B greater than that associated with the I_B curve appearing near the saturation level. In Fig. 4.52b, this requires that $I_B > 50$ μA. The saturation level for the collector current for the circuit of Fig. 4.52a is defined by

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} \tag{4.45}$$

The level of I_B in the active region just before saturation results can be approximated by the following equation:

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

For the saturation level we must therefore ensure that the following condition is satisfied:

$$\boxed{I_B > \frac{I_{C_{sat}}}{\beta_{dc}}} \tag{4.46}$$

For the network of Fig. 4.52b, when $V_i = 5$ V, the resulting level of I_B is the following:

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63\ \mu\text{A}$$

and

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{5\text{ V}}{0.82\text{ k}\Omega} \cong 6.1\text{ mA}$$

Testing Eq. (4.46) gives

$$I_B = 63\ \mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{6.1\text{ mA}}{125} = 48.8\ \mu\text{A}$$

which is satisfied. Certainly, any level of I_B greater than 60 μA will pass through a Q-point on the load line that is very close to the vertical axis.

For $V_i = 0$ V, $I_B = 0$ μA, and since we are assuming that $I_C = I_{CEO} = 0$ mA, the voltage drop across R_C as determined by $V_{R_C} = I_C R_C = 0$ V, resulting in $V_C = +5$ V for the response indicated in Fig. 4.52a.

In addition to its contribution to computer logic, the transistor can also be employed as a switch using the same extremities of the load line. At saturation, the current I_C is quite high and the voltage V_{CE} very low. The result is a resistance level between the two terminals determined by

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}}$$

and depicted in Fig. 4.53.

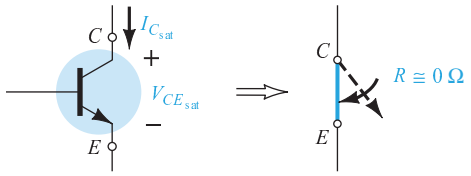


Figure 4.53 Saturation conditions and the resulting terminal resistance.

Using a typical average value of $V_{CE_{sat}}$ such as 0.15 V gives

$$R_{sat} = \frac{V_{CE_{sat}}}{I_{C_{sat}}} = \frac{0.15\text{ V}}{6.1\text{ mA}} = 24.6\ \Omega$$

which is a relatively low value and $\cong 0\ \Omega$ when placed in series with resistors in the kilohm range.

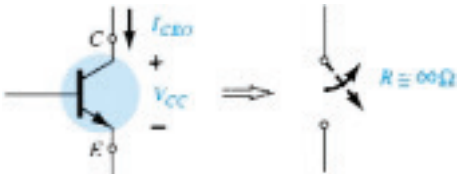


Figure 4.54 Cutoff conditions and the resulting terminal resistance.

For $V_i = 0$ V, as shown in Fig. 4.54, the cutoff condition will result in a resistance level of the following magnitude:

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{0\text{ mA}} = \infty\ \boldsymbol{\Omega}$$

resulting in the open-circuit equivalence. For a typical value of $I_{CEO} = 10\ \mu$A, the magnitude of the cutoff resistance is

$$R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} = \frac{5\text{ V}}{10\ \mu\text{A}} = \mathbf{500\ k\Omega}$$

which certainly approaches an open-circuit equivalence for many situations.

EXAMPLE 4.24

Determine R_B and R_C for the transistor inverter of Fig. 4.55 if $I_{C_{\text{sat}}} = 10$ mA.

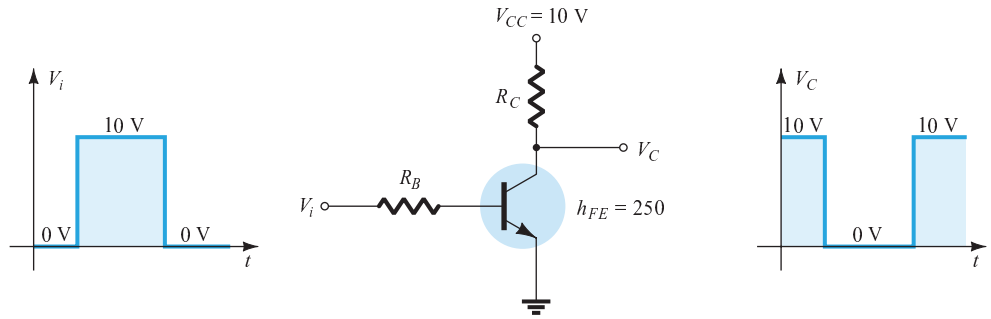


Figure 4.55 Inverter for Example 4.24.

Solution

At saturation:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C}$$

and

$$10\text{ mA} = \frac{10\text{ V}}{R_C}$$

so that

$$R_C = \frac{10\text{ V}}{10\text{ mA}} = 1\text{ k}\Omega$$

At saturation:

$$I_B \cong \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = \frac{10\text{ mA}}{250} = 40\ \mu\text{A}$$

Choosing $I_B = 60\ \mu$A to ensure saturation and using

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B}$$

we obtain $$R_B = \frac{V_i - 0.7\text{ V}}{I_B} = \frac{10\text{ V} - 0.7\text{ V}}{60\ \mu\text{A}} = 155\ \text{k}\Omega$$

Choose $R_B = 150\ \text{k}\Omega$, which is a standard value. Then

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{150\ \text{k}\Omega} = 62\ \mu\text{A}$$

and $$I_B = 62\ \mu\text{A} > \frac{I_{C_{\text{sat}}}}{\beta_{\text{dc}}} = 40\ \mu\text{A}$$

Therefore, use $R_B = \mathbf{150\ k\Omega}$ and $R_C = \mathbf{1\ k\Omega}$.

There are transistors that are referred to as *switching transistors* due to the speed with which they can switch from one voltage level to the other. In Fig. 3.23c the periods of time defined as t_s, t_d, t_r, and t_f are provided versus collector current. Their impact on the speed of response of the collector output is defined by the collector current response of Fig. 4.56. The total time required for the transistor to switch from the "off" to the "on" state is designated as t_{on} and defined by

$$t_{\text{on}} = t_r + t_d \tag{4.47}$$

with t_d the delay time between the changing state of the input and the beginning of a response at the output. The time element t_r is the rise time from 10% to 90% of the final value.

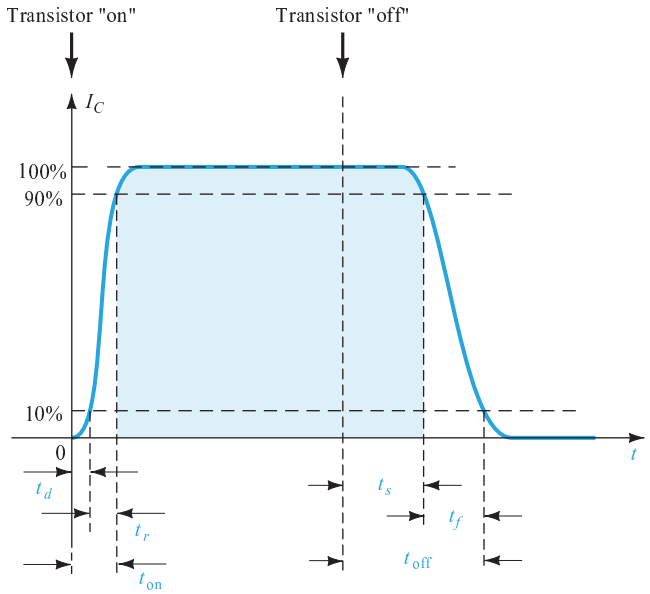


Figure 4.56 Defining the time intervals of a pulse waveform.

The total time required for a transistor to switch from the "on" to the "off" state is referred to as t_{off} and is defined by

$$t_{\text{off}} = t_s + t_f \tag{4.48}$$

where t_s is the storage time and t_f the fall time from 90% to 10% of the initial value.

For the general-purpose transistor of Fig. 3.23c at $I_C = 10$ mA, we find that

$$t_s = 120 \text{ ns}$$

$$t_d = 25 \text{ ns}$$

$$t_r = 13 \text{ ns}$$

and $$t_f = 12 \text{ ns}$$

so that $$t_{on} = t_r + t_d = 13 \text{ ns} + 25 \text{ ns} = \mathbf{38 \text{ ns}}$$

and $$t_{off} = t_s + t_f = 120 \text{ ns} + 12 \text{ ns} = \mathbf{132 \text{ ns}}$$

Comparing the values above with the following parameters of a BSV52L switching transistor reveals one of the reasons for choosing a switching transistor when the need arises.

$$t_{on} = \mathbf{12 \text{ ns}} \quad \text{and} \quad t_{off} = \mathbf{18 \text{ ns}}$$

4.10 TROUBLESHOOTING TECHNIQUES

The art of troubleshooting is such a broad topic that a full range of possibilities and techniques cannot be covered in a few sections of a book. However, the practitioner should be aware of a few basic maneuvers and measurements that can isolate the problem area and possibly identify a solution.

Quite obviously, the first step in being able to troubleshoot a network is to fully understand the behavior of the network and to have some idea of the expected voltage and current levels. For the transistor in the active region, the most important measurable dc level is the base-to-emitter voltage.

For an "on" transistor, the voltage V_{BE} should be in the neighborhood of 0.7 V.

The proper connections for measuring V_{BE} appear in Fig. 4.57. Note that the positive (red) lead is connected to the base terminal for an *npn* transistor and the negative (black) lead to the emitter terminal. Any reading totally different from the expected level of about 0.7 V, such as 0, 4, or 12 V, or negative in value would be suspect and the device or network connections should be checked. For a *pnp* transistor, the same connections can be used but a negative reading should be expected.

A voltage level of equal importance is the collector-to-emitter voltage. Recall from the general characteristics of a BJT that levels of V_{CE} in the neighborhood of 0.3 V suggest a saturated device—a condition that should not exist unless being employed in a switching mode. However:

For the typical transistor amplifier in the active region, V_{CE} is usually about 25% to 75% of V_{CC}.

For $V_{CC} = 20$ V, a reading of V_{CE} of 1 to 2 V or 18 to 20 V as measured in Fig. 4.58 is certainly an uncommon result, and unless knowingly designed for this response the design and operation should be investigated. If $V_{CE} = 20$ V (with $V_{CC} = 20$ V) at least two possibilities exist—either the device (BJT) is damaged and has the

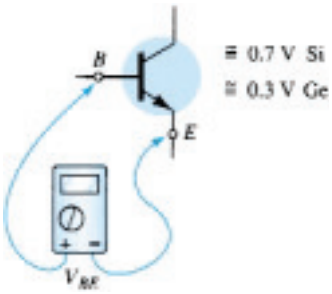


Figure 4.57 Checking the dc level of V_{BE}.

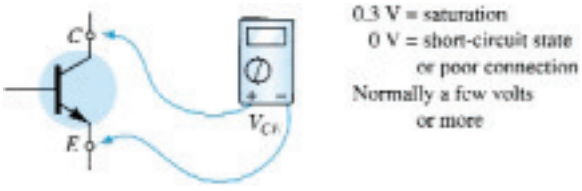


Figure 4.58 Checking the dc level of V_{CE}.

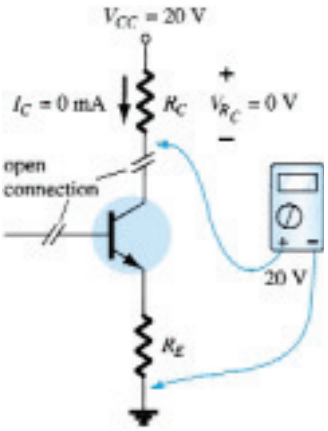


Figure 4.59 Effect of a poor connection or damaged device.

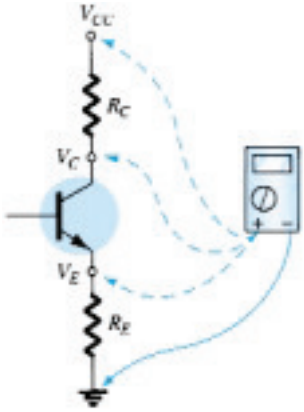


Figure 4.60 Checking voltage levels with respect to ground.

characteristics of an open circuit between collector and emitter terminals or a connection in the collector–emitter or base–emitter circuit loop is open as shown in Fig. 4.59, establishing I_C at 0 mA and $V_{R_C} = 0$ V. In Fig. 4.59, the black lead of the voltmeter is connected to the common ground of the supply and the red lead to the bottom terminal of the resistor. The absence of a collector current and a resulting drop across R_C will result in a reading of 20 V. If the meter is connected to the collector terminal of the BJT, the reading will be 0 V since V_{CC} is blocked from the active device by the open circuit. One of the most common errors in the laboratory experience is the use of the wrong resistance value for a given design. Imagine the impact of using a 680-Ω resistor for R_B rather than the design value of 680 kΩ. For $V_{CC} = 20$ V and a fixed-bias configuration, the resulting base current would be

$$I_B = \frac{20\text{ V} - 0.7\text{ V}}{680\ \Omega} = 28.4\text{ mA}$$

rather than the desired 28.4 μA—a significant difference!

A base current of 28.4 mA would certainly place the design in a saturation region and possibly damage the device. Since actual resistor values are often different from the nominal color-code value (recall the common tolerance levels for resistive elements), it is time well spent to measure a resistor before inserting it in the network. The result is actual values closer to theoretical levels and some insurance that the correct resistance value is being employed.

There are times when frustration will develop. You have checked the device on a curve tracer or other BJT testing instrumentation and it looks good. All resistor levels seem correct, the connections appear solid, and the proper supply voltage has been applied—what next? Now the troubleshooter must strive to attain a higher level of sophistication. Could it be that the internal connection between the wire and the end connection of a lead is faulty? How often has simply touching a lead at the proper point created a "make or break" situation between connections? Perhaps the supply was turned on and set at the proper voltage but the current-limiting knob was left in the zero position, preventing the proper level of current as demanded by the network design. Obviously, the more sophisticated the system, the broader the range of possibilities. In any case, one of the most effective methods of checking the operation of a network is to check various voltage levels with respect to ground by hooking up the black (negative) lead of a voltmeter to ground and "touching" the important terminals with the red (positive) lead. In Fig. 4.60, if the red lead is connected directly to V_{CC}, it should read V_{CC} volts since the network has one common ground for the supply and network parameters. At V_C the reading should be less, as determined by the drop across R_C and V_E should be less than V_C by the collector–emitter voltage V_{CE}. The failure of any of these points to register what would appear to be a reasonable level may be sufficient in itself to define the faulty connection or element. If V_{R_C} and V_{R_E} are reasonable values but V_{CE} is 0 V, the possibility exists that the BJT is damaged and displays a short-circuit equivalence between collector and emitter terminals. As noted earlier, if V_{CE} registers a level of about 0.3 V as defined by $V_{CE} = V_C - V_E$ (the difference of the two levels as measured above), the network may be in saturation with a device that may or may not be defective.

It should be somewhat obvious from the discussion above that the voltmeter section of the VOM or DMM is quite important in the troubleshooting process. Current levels are usually calculated from the voltage levels across resistors rather than "breaking" the network to insert the milliammeter section of a multimeter. On large schematics, specific voltage levels are provided with respect to ground for easy checking and identification of possible problem areas. Of course, for the networks covered in this chapter, one must simply be aware of typical levels within the system as defined by the applied potential and general operation of the network.

All in all, the troubleshooting process is a true test of your clear understanding of the proper behavior of a network and the ability to isolate problem areas using a few basic measurements with the appropriate instruments. Experience is the key, and that will come only with continued exposure to practical circuits.

EXAMPLE 4.25

Based on the readings provided in Fig. 4.61, determine whether the network is operating properly and, if not, the probable cause.

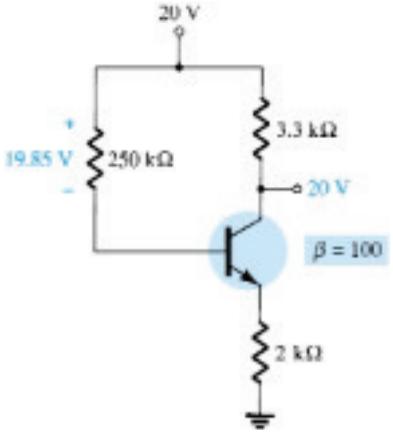


Figure 4.61 Network for Example 4.25.

Solution

The 20 V at the collector immediately reveals that $I_C = 0$ mA, due to an open circuit or a nonoperating transistor. The level of $V_{R_B} = 19.85$ V also reveals that the transistor is "off" since the difference of $V_{CC} - V_{R_B} = 0.15$ V is less than that required to turn "on" the transistor and provide some voltage for V_E. In fact, if we assume a short circuit condition from base to emitter, we obtain the following current through R_B:

$$I_{R_B} = \frac{V_{CC}}{R_B + R_E} = \frac{20\text{ V}}{252\text{ k}\Omega} = 79.4\ \mu\text{A}$$

which matches that obtained from

$$I_{R_B} = \frac{V_{R_B}}{R_B} = \frac{19.85\text{ V}}{250\text{ k}\Omega} = 79.4\ \mu\text{A}$$

If the network were operating properly, the base current should be

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{250\text{ k}\Omega + (101)(2\text{ k}\Omega)} = \frac{19.3\text{ V}}{452\text{ k}\Omega} = 42.7\ \mu\text{A}$$

The result, therefore, is that the transistor is in a damaged state, with a short-circuit condition between base and emitter.

EXAMPLE 4.26

Based on the readings appearing in Fig. 4.62, determine whether the transistor is "on" and the network is operating properly.

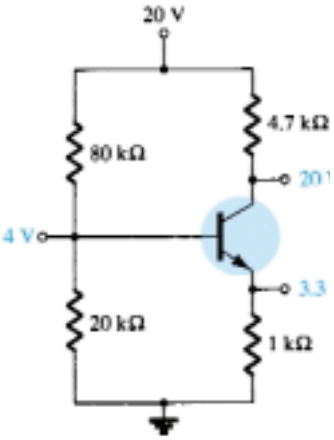


Figure 4.62 Network for Example 4.26.

Solution

Based on the resistor values of R_1 and R_2 and the magnitude of V_{CC}, the voltage $V_B = 4$ V seems appropriate (and in fact it is). The 3.3 V at the emitter results in a 0.7-V drop across the base-to-emitter junction of the transistor, suggesting an "on" transistor. However, the 20 V at the collector reveals that $I_C = 0$ mA, although the connection to the supply must be "solid" or the 20 V would not appear at the collector of the device. Two possibilities exist—there can be a poor connection between R_C and the collector terminal of the transistor or the transistor has an open base-to-collector junction. First, check the continuity at the collector junction using an ohmmeter, and if okay, the transistor should be checked using one of the methods described in Chapter 3.

4.11 *PNP* TRANSISTORS

The analysis thus far has been limited totally to *npn* transistors to ensure that the initial analysis of the basic configurations was as clear as possible and uncomplicated by switching between types of transistors. Fortunately, the analysis of *pnp* transistors follows the same pattern established for *npn* transistors. The level of I_B is first determined, followed by the application of the appropriate transistor relationships to determine the list of unknown quantities. In fact, the only difference between the resulting equations for a network in which an *npn* transistor has been replaced by a *pnp* transistor is the sign associated with particular quantities.

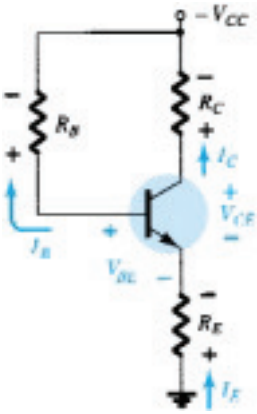


Figure 4.63 *pnp* transistor in an emitter-stabilized configuration.

As noted in Fig. 4.63, the double-subscript notation continues as normally defined. The current directions, however, have been reversed to reflect the actual conduction directions. Using the defined polarities of Fig. 4.63, both V_{BE} and V_{CE} will be negative quantities.

Applying Kirchhoff's voltage law to the base–emitter loop will result in the following equation for the network of Fig. 4.63:

$$-I_E R_E + V_{BE} - I_B R_B + V_{CC} = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{V_{CC} + V_{BE}}{R_B + (\beta + 1)R_E} \tag{4.49}$$

The resulting equation is the same as Eq. (4.17) except for the sign for V_{BE}. However, in this case $V_{BE} = -0.7$ V and the substitution of values will result in the same sign for each term of Eq. (4.49) as Eq. (4.17). Keep in mind that the direction of I_B is now defined opposite of that for a *pnp* transistor as shown in Fig. 4.63.

For V_{CE} Kirchhoff's voltage law is applied to the collector–emitter loop, resulting in the following equation:

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ gives

$$V_{CE} = -V_{CC} + I_C(R_C + R_E) \tag{4.50}$$

The resulting equation has the same format as Eq. (4.19), but the sign in front of each term on the right of the equal sign has changed. Since V_{CC} will be larger than the magnitude of the succeeding term, the voltage V_{CE} will have a negative sign, as noted in an earlier paragraph.

Determine V_{CE} for the voltage-divider bias configuration of Fig. 4.64. **EXAMPLE 4.27**

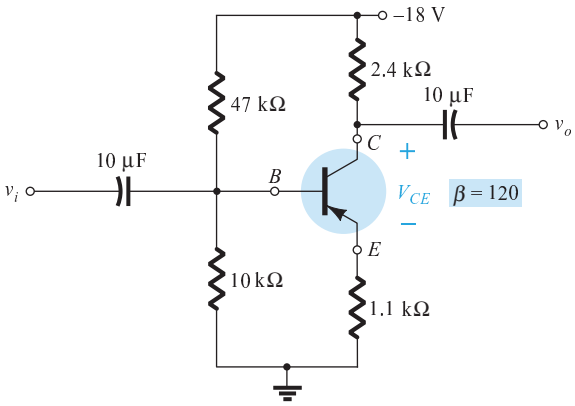


Figure 4.64 *pnp* transistor in a voltage-divider bias configuration.

Solution

Testing the condition

$$\beta R_E \geq 10R_2$$

results in

$$(120)(1.1\ \text{k}\Omega) \geq 10(10\ \text{k}\Omega)$$

$$132\ \text{k}\Omega \geq 100\ \text{k}\Omega\ (\textit{satisfied})$$

Solving for V_B, we have

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{(10\ \text{k}\Omega)(-18\ \text{V})}{47\ \text{k}\Omega + 10\ \text{k}\Omega} = -3.16\ \text{V}$$

Note the similarity in format of the equation with the resulting negative voltage for V_B.

Applying Kirchhoff's voltage law around the base–emitter loop yields

$$+V_B - V_{BE} - V_E = 0$$

and

$$V_E = V_B - V_{BE}$$

Substituting values, we obtain

$$V_E = -3.16\ \text{V} - (-0.7\ \text{V})$$

$$= -3.16\ \text{V} + 0.7\ \text{V}$$

$$= -2.46\ \text{V}$$

Note in the equation above that the standard single- and double-subscript notation is employed. For an *npn* transistor the equation $V_E = V_B - V_{BE}$ would be exactly the same. The only difference surfaces when the values are substituted.

The current

$$I_E = \frac{V_E}{R_E} = \frac{2.46\ \text{V}}{1.1\ \text{k}\Omega} = 2.24\ \text{mA}$$

For the collector–emitter loop:

$$-I_E R_E + V_{CE} - I_C R_C + V_{CC} = 0$$

Substituting $I_E \cong I_C$ and gathering terms, we have

$$V_{CE} = -V_{CC} + I_C(R_C + R_E)$$

Substituting values gives

$$V_{CE} = -18\text{ V} + (2.24\text{ mA})(2.4\text{ k}\Omega + 1.1\text{ k}\Omega)$$
$$= -18\text{ V} + 7.84\text{ V}$$
$$= \mathbf{-10.16\text{ V}}$$

4.12 BIAS STABILIZATION

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β: increases with increase in temperature

$|V_{BE}|$: decreases about 7.5 mV per degree Celsius (°C) increase in temperature

I_{CO} (reverse saturation current): doubles in value for every 10°C increase in temperature

Any or all of these factors can cause the bias point to drift from the designed point of operation. Table 4.1 reveals how the level of I_{CO} and V_{BE} changed with increase in temperature for a particular transistor. At room temperature (about 25°C) $I_{CO} =$ 0.1 nA, while at 100°C (boiling point of water) I_{CO} is about 200 times larger at 20 nA. For the same temperature variation, β increased from 50 to 80 and V_{BE} dropped from 0.65 to 0.48 V. Recall that I_B is quite sensitive to the level of V_{BE}, especially for levels beyond the threshold value.

TABLE 4.1 Variation of Silicon Transistor Parameters with Temperature

T (°C)	I_{CO} (nA)	β	V_{BE}(V)
−65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^{3}	120	0.3

The effect of changes in leakage current (I_{CO}) and current gain (β) on the dc bias point is demonstrated by the common-emitter collector characteristics of Fig. 4.65a and b. Figure 4.65 shows how the transistor collector characteristics change from a temperature of 25°C to a temperature of 100°C. Note that the significant increase in leakage current not only causes the curves to rise but also an increase in beta, as revealed by the larger spacing between curves.

An operating point may be specified by drawing the circuit dc load line on the graph of the collector characteristic and noting the intersection of the load line and the dc base current set by the input circuit. An arbitrary point is marked in Fig. 4.65a at $I_B = 30\ \mu$A. Since the fixed-bias circuit provides a base current whose value depends approximately on the supply voltage and base resistor, neither of which is affected by temperature or the change in leakage current or beta, the same base current magnitude will exist at high temperatures as indicated on the graph of Fig. 4.65b. As the figure shows, this will result in the dc bias point's shifting to a higher collector current and a lower collector–emitter voltage operating point. In the extreme, the transistor could be driven into saturation. In any case, the new operating point may not

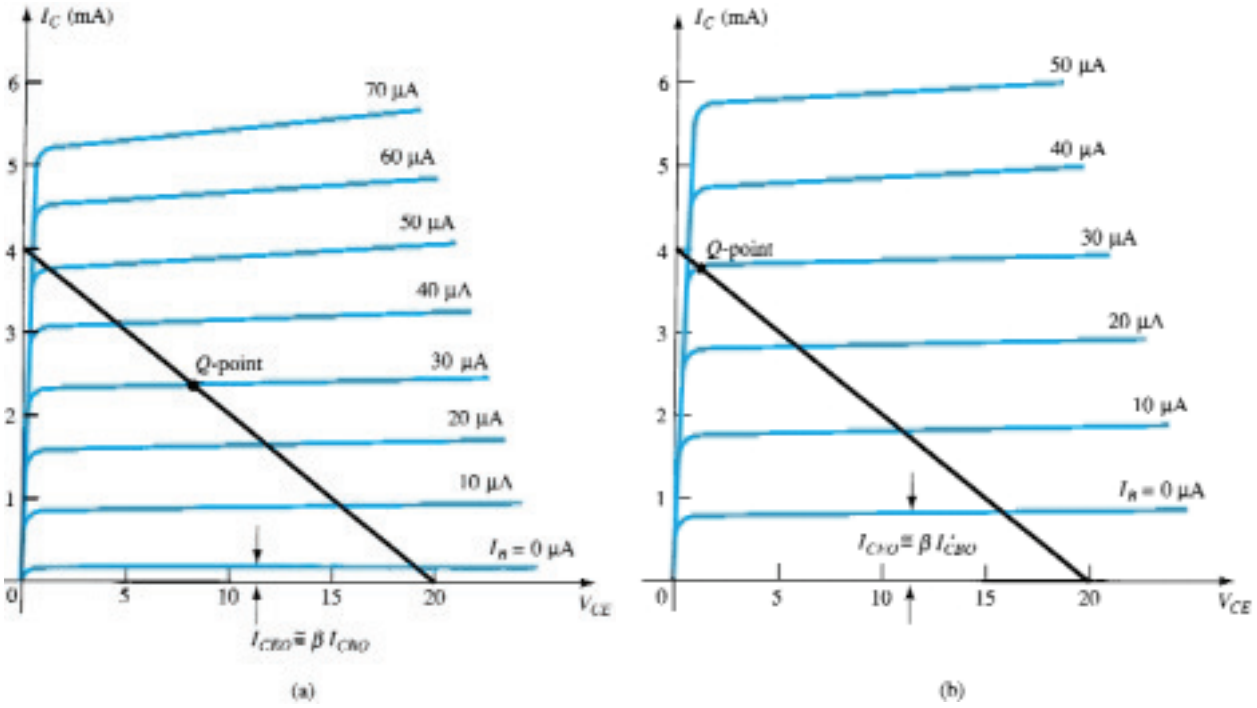


Figure 4.65 Shift in dc bias point (*Q*-point) due to change in temperature: (a) 25°C; (b) 100°C.

be at all satisfactory, and considerable distortion may result because of the bias-point shift. A better bias circuit is one that will stabilize or maintain the dc bias initially set, so that the amplifier can be used in a changing-temperature environment.

Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

A stability factor, S, is defined for each of the parameters affecting bias stability as listed below:

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}} \tag{4.51}$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \tag{4.52}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \tag{4.53}$$

In each case, the delta symbol (Δ) signifies change in that quantity. The numerator of each equation is the change in collector current as established by the change in the quantity in the denominator. For a particular configuration, if a change in I_{CO} fails to produce a significant change in I_C, the stability factor defined by $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$ will be quite small. In other words:

Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.

In some ways it would seem more appropriate to consider the quantities defined by Eqs. (4.51–4.53) to be sensitivity factors because:

The higher the stability factor, the more sensitive the network to variations in that parameter.

The study of stability factors requires the knowledge of differential calculus. Our purpose here, however, is to review the results of the mathematical analysis and to form an overall assessment of the stability factors for a few of the most popular bias configurations. A great deal of literature is available on this subject, and if time permits, you are encouraged to read more on the subject.

$S(I_{CO})$: EMITTER-BIAS CONFIGURATION

For the emitter-bias configuration, an analysis of the network will result in

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{(\beta + 1) + R_B/R_E} \tag{4.54}$$

For $R_B/R_E \gg (\beta + 1)$, Eq. (4.54) will reduce to the following:

$$S(I_{CO}) = \beta + 1 \tag{4.55}$$

as shown on the graph of $S(I_{CO})$ versus R_B/R_E in Fig. 4.66.

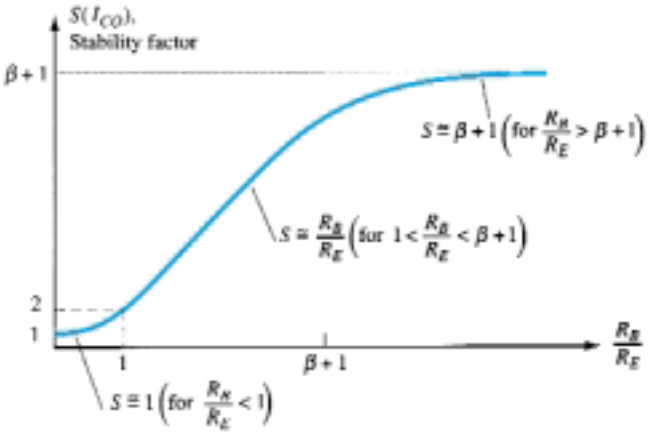


Figure 4.66 Variation of stability factor $S(I_{CO})$ with the resistor ratio R_B/R_E for the emitter-bias configuration.

For $R_B/R_E \ll 1$, Eq. (4.54) will approach the following level (as shown in Fig. 4.66):

$$S(I_{CO}) = (\beta + 1)\frac{1}{(\beta + 1)} = \rightarrow 1 \tag{4.56}$$

revealing that the stability factor will approach its lowest level as R_E becomes sufficiently large. Keep in mind, however, that good bias control normally requires that R_B be greater than R_E. The result therefore is a situation where the best stability levels are associated with poor design criteria. Obviously, a trade-off must occur that will satisfy both the stability and bias specifications. It is interesting to note in Fig. 4.66 that the lowest value of $S(I_{CO})$ is 1, revealing that I_C will always increase at a rate equal to or greater than I_{CO}.

For the range where R_B/R_E ranges between 1 and $(\beta + 1)$, the stability factor will be determined by

$$S(I_{CO}) \cong \frac{R_B}{R_E} \tag{4.57}$$

as shown in Fig. 4.66. The results reveal that the emitter-bias configuration is quite stable when the ratio R_B/R_E is as small as possible and the least stable when the same ratio approaches $(\beta + 1)$.

EXAMPLE 4.28

Calculate the stability factor and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.1 for the following emitter-bias arrangements.
(a) $R_B/R_E = 250$ $(R_B = 250R_E)$
(b) $R_B/R_E = 10$ $(R_B = 10R_E)$.
(c) $R_B/R_E = 0.01$ $(R_E = 100R_B)$.

Solution

(a) $$S(I_{CO}) = (\beta + 1)\,1 + \frac{R_B/R_E}{1 + \beta + R_B/R_E}$$
$$= 51\left(\frac{1 + 250}{51 + 250}\right) = 51\left(\frac{251}{301}\right)$$
$$\cong \mathbf{42.53}$$
which begins to approach the level defined by $\beta + 1 = 51$.

$$\Delta I_C = [S(I_{CO})](\Delta I_{CO}) = (42.53)(19.9\text{ nA})$$
$$\cong \mathbf{0.85\ \mu A}$$

(b) $$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{1 + \beta + R_B/R_E}$$
$$= 51\left(\frac{1 + 10}{51 + 10}\right) = 51\left(\frac{11}{61}\right)$$
$$\cong \mathbf{9.2}$$
$$\Delta I_C = [S(I_{CO})](\Delta\, I_{CO}) = (9.2)(19.9\text{ nA})$$
$$\cong \mathbf{0.18\ \mu A}$$

(c) $$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_E}{1 + \beta + R_B/R_E}$$
$$= 51\left(\frac{1 + 0.01}{51 + 0.01}\right) = 51\left(\frac{1.01}{51.01}\right)$$
$$\cong \mathbf{1.01}$$

which is certainly very close to the level of 1 forecast if $R_B/R_E \ll 1$.

$$\Delta I_C = [S(I_{CO})](\Delta\, I_{CO}) = 1.01(19.9\text{ nA})$$
$$= \mathbf{20.1\ nA}$$

Example 4.28 reveals how lower and lower levels of I_{CO} for the modern-day BJT transistor have improved the stability level of the basic bias configurations. Even though the change in I_C is considerably different in a circuit having ideal stability $(S = 1)$ from one having a stability factor of 42.53, the change in I_C is not that significant. For example, the amount of change in I_C from a dc bias current set at, say, 2 mA, would be from 2 to 2.085 mA in the worst case, which is obviously small enough to be ignored for most applications. Some power transistors exhibit larger leakage currents, but for most amplifier circuits the lower levels of I_{CO} have had a very positive impact on the stability question.

FIXED-BIAS CONFIGURATION

For the fixed-bias configuration, if we multiply the top and bottom of Eq. (4.54) by R_E and then plug in $R_E = 0\ \Omega$, the following equation will result:

$$\boxed{S(I_{CO}) = \beta + 1} \tag{4.58}$$

Note that the resulting equation matches the maximum value for the emitter-bias configuration. The result is a configuration with a poor stability factor and a high sensitivity to variations in I_{CO}.

Voltage-Divider Bias Configuration

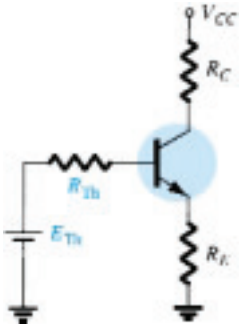


Figure 4.67 Equivalent circuit for the voltage-divider configuration.

Recall from Section 4.5 the development of the Thévenin equivalent network appearing in Fig. 4.67, for the voltage-divider bias configuration. For the network of Fig. 4.67, the equation for $S(I_{CO})$ is the following:

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_{Th}/R_E}{(\beta + 1) + R_{Th}/R_E} \tag{4.59}$$

Note the similarities with Eq. (4.54), where it was determined that $S(I_{CO})$ had its lowest level and the network had its greatest stability when $R_E > R_B$. For Eq. (4.59), the corresponding condition is $R_E > R_{Th}$ or R_{Th}/R_E should be as small as possible. For the voltage-divider bias configuration, R_{Th} can be much less than the corresponding R_B of the emitter-bias configuration and still have an effective design.

Feedback-Bias Configuration (R_E 5 0 Ω)

In this case,

$$S(I_{CO}) = (\beta + 1)\frac{1 + R_B/R_C}{(\beta + 1) + R_B/R_C} \tag{4.60}$$

Since the equation is similar in format to that obtained for the emitter-bias and voltage-divider bias configurations, the same conclusions regarding the ratio R_B/R_C can be applied here also.

Physical Impact

Equations of the type developed above often fail to provide a physical sense for why the networks perform as they do. We are now aware of the relative levels of stability and how the choice of parameters can affect the sensitivity of the network, but without the equations it may be difficult for us to explain in words why one network is more stable than another. The next few paragraphs attempt to fill this void through the use of some of the very basic relationships associated with each configuration.

For the fixed-bias configuration of Fig. 4.68a, the equation for the base current is the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

with the collector current determined by

$$I_C = \beta I_B + (\beta + 1)I_{CO} \tag{4.61}$$

If I_C as defined by Eq. (4.61) should increase due to an increase in I_{CO}, there is nothing in the equation for I_B that would attempt to offset this undesirable increase in current level (assuming V_{BE} remains constant). In other words, the level of I_C would continue to rise with temperature, with I_B maintaining a fairly constant value—a very unstable situation.

For the emitter-bias configuration of Fig. 4.68b, however, an increase in I_C due to an increase in I_{CO} will cause the voltage $V_E = I_E R_E \cong I_C R_E$ to increase. The result is a drop in the level of I_B as determined by the following equation:

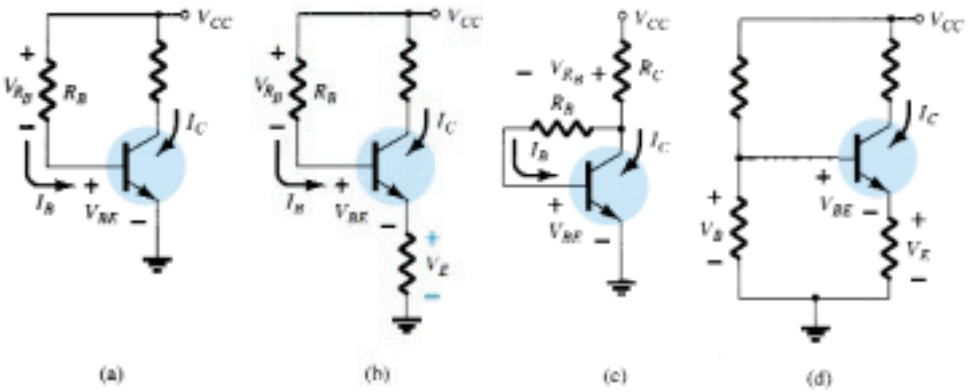


Figure 4.68 Review of biasing managements and the stability factor $S(I_{CO})$.

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_E \uparrow}{R_B} \tag{4.62}$$

A drop in I_B will have the effect of reducing the level of I_C through transistor action and thereby offset the tendency of I_C to increase due to an increase in temperature. In total, therefore, the configuration is such that there is a reaction to an increase in I_C that will tend to oppose the change in bias conditions.

The feedback configuration of Fig. 4.68c operates in much the same way as the emitter-bias configuration when it comes to levels of stability. If I_C should increase due to an increase in temperature, the level of V_{R_C} will increase in the following equation:

$$I_B \downarrow = \frac{V_{CC} - V_{BE} - V_{R_C} \uparrow}{R_B} \tag{4.63}$$

and the level of I_B will decrease. The result is a stabilizing effect as described for the emitter-bias configuration. One must be aware that the action described above does not happen in a step-by-step sequence. Rather, it is a simultaneous action to maintain the established bias conditions. In other words, the very instant I_C begins to rise the network will sense the change and the balancing effect described above will take place.

The most stable of the configurations is the voltage-divider bias network of Fig. 4.68d. If the condition $\beta R_E \geqslant 10R_2$ is satisfied, the voltage V_B will remain fairly constant for changing levels of I_C. The base-to-emitter voltage of the configuration is determined by $V_{BE} = V_B - V_E$. If I_C should increase, V_E will increase as described above, and for a constant V_B the voltage V_{BE} will drop. A drop in V_{BE} will establish a lower level of I_B, which will try to offset the increased level of I_C.

$S(V_{BE})$

The stability factor defined by

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}}$$

will result in the following equation for the emitter-bias configuration:

$$S(V_{BE}) = \frac{-\beta}{R_B + (\beta + 1)R_E} \tag{4.64}$$

Substituting $R_E = 0\ \Omega$ as occurs for the fixed-bias configuration will result in

$$S(V_{BE}) = -\frac{\beta}{R_B} \tag{4.65}$$

Equation (4.64) can be written in the following form:

$$S(V_{BE}) = \frac{-\beta/R_E}{R_B/R_E + (\beta + 1)} \tag{4.66}$$

Substituting the condition $(\beta + 1) \gg R_B/R_E$ will result in the following equation for $S(V_{BE})$:

$$\boxed{S(V_{BE}) \cong \frac{-\beta/R_E}{\beta + 1} \cong \frac{-\beta/R_E}{\beta} = -\frac{1}{R_E}} \tag{4.67}$$

revealing that the larger the resistance R_E, the lower the stability factor and the more stable the system.

EXAMPLE 4.29

Determine the stability factor $S(V_{BE})$ and the change in I_C from 25°C to 100°C for the transistor defined by Table 4.1 for the following bias arrangements.
(a) Fixed-bias with $R_B = 240\ \text{k}\Omega$ and $\beta = 100$.
(b) Emitter-bias with $R_B = 240\ \text{k}\Omega$, $R_E = 1\ \text{k}\Omega$, and $\beta = 100$.
(c) Emitter-bias with $R_B = 47\ \text{k}\Omega$, $R_E = 4.7\ \text{k}\Omega$, and $\beta = 100$.

Solution

(a) Eq. (4.65): $S(V_{BE}) = -\dfrac{\beta}{R_B}$

$$= -\frac{100}{240\ \text{k}\Omega}$$

$$= \mathbf{-0.417 \times 10^{-3}}$$

and $\Delta I_C = [S(V_{BE})](\Delta V_{BE})$

$$= (-0.417 \times 10^{-3})(0.48\ \text{V} - 0.65\ \text{V})$$

$$= (-0.417 \times 10^{-3})(-0.17\ \text{V})$$

$$= \mathbf{70.9\ \mu A}$$

(b) In this case, $(\beta + 1) = 101$ and $R_B/R_E = 240$. The condition $(\beta + 1) \gg R_B/R_E$ is not satisfied, negating the use of Eq. (4.67) and requiring the use of Eq. (4.64).

Eq. (4.64): $S(V_{BE}) = \dfrac{-\beta}{R_B + (\beta + 1)R_E}$

$$= \frac{-100}{240\ \text{k}\Omega + (101)1\ \text{k}\Omega} = -\frac{100}{341\ \text{k}\Omega}$$

$$= \mathbf{-0.293 \times 10^{-3}}$$

which is about 30% less than the fixed-bias value due to the additional $(\beta + 1)R_E$ term in the denominator of the $S(V_{BE})$ equation.

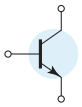
$$\Delta I_C = [S(V_{BE})](\Delta V_{BE})$$

$$= (-0.293 \times 10^{-3})(-0.17\ V)$$

$$\cong \mathbf{50\ \mu A}$$

(c) In this case,

$$(\beta + 1) = 101 \gg \frac{R_B}{R_E} = \frac{47\ \text{k}\Omega}{4.7\ \text{k}\Omega} = 10\ (\textit{satisfied})$$



Eq. (4.67): $$S(V_{BE}) = -\frac{1}{R_E}$$

$$= -\frac{1}{4.7\ \text{k}\Omega}$$

$$= \mathbf{-0.212 \times 10^{-3}}$$

and $$\Delta I_C = [S(V_{BE})](\Delta V_{BE})$$

$$= (-0.212 \times 10^{-3})(-0.17\ \text{V})$$

$$= \mathbf{36.04\ \mu A}$$

In Example 4.29, the increase of 70.9 μA will have some impact on the level of I_{C_Q}. For a situation where $I_{C_Q} = 2$ mA, the resulting collector current will increase to

$$I_{C_Q} = 2\ \text{mA} + 70.9\ \mu\text{A}$$

$$= 2.0709\ \text{mA}$$

a 3.5% increase.

For the voltage-divider configuration, the level of R_B will be changed to R_{Th} in Eq. (4.64) (as defined by Fig. 4.67). In Example 4.29, the use of $R_B = 47\ \text{k}\Omega$ is a questionable design. However, R_{Th} for the voltage-divider configuration can be this level or lower and still maintain good design characteristics. The resulting equation for $S(V_{BE})$ for the feedback network will be similar to that of Eq. (4.64) with R_E replaced by R_C.

S(β)

The last stability factor to be investigated is that of $S(\beta)$. The mathematical development is more complex than that encountered for $S(I_{CO})$ and $S(V_{BE})$, as suggested by the following equation for the emitter-bias configuration:

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)} \tag{4.68}$$

The notation I_{C1} and β_1 is used to define their values under one set of network conditions, while the notation β_2 is used to define the new value of beta as established by such causes as temperature change, variation in β for the same transistor, or a change in transistors.

EXAMPLE 4.30

Determine I_{C_Q} at a temperature of 100°C if $I_{C_Q} = 2$ mA at 25°C. Use the transistor described by Table 4.1, where $\beta_1 = 50$ and $\beta_2 = 80$, and a resistance ratio R_B/R_E of 20.

Solution

Eq. (4.68): $$S(\beta) = \frac{I_{C_1}(1 + R_B/R_E)}{\beta_1(1 + \beta_2 + R_B/R_E)}$$

$$= \frac{(2 \times 10^{-3})(1 + 20)}{(50)(1 + 80 + 20)} = \frac{42 \times 10^{-3}}{5050}$$

$$= \mathbf{8.32 \times 10^{-6}}$$

and $$\Delta I_C = [S(\beta)][\Delta\beta]$$

$$= (8.32 \times 10^{-6})(30)$$

$$\cong \mathbf{0.25\ mA}$$

In conclusion therefore the collector current changed from 2 mA at room temperature to 2.25 mA at 100°C, representing a change of 12.5%.

The fixed-bias configuration is defined by $S(\beta) = I_{C_1}/\beta_1$ and R_B of Eq. (4.68) can be replaced by R_{Th} for the voltage-divider configuration.

For the collector feedback configuration with $R_E = 0\ \Omega$,

$$S(\beta) = \frac{I_{C_1}(R_B + R_C)}{\beta_1(R_B + R_C(1 + \beta_2))} \tag{4.69}$$

Summary

Now that the three stability factors of importance have been introduced, the total effect on the collector current can be determined using the following equation:

$$\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta \tag{4.70}$$

The equation may initially appear quite complex, but take note that each component is simply a stability factor for the configuration multiplied by the resulting change in a parameter between the temperature limits of interest. In addition, the ΔI_C to be determined is simply the change in I_C from the level at room temperature.

For instance, if we examine the fixed-bias configuration, Eq. (4.70) becomes the following:

$$\Delta I_C = (\beta + 1)\Delta I_{CO} - \frac{\beta}{R_B}\Delta V_{BE} + \frac{I_{C_1}}{\beta_1}\Delta\beta \tag{4.71}$$

after substituting the stability factors as derived in this section. Let us now use Table 4.1 to find the change in collector current for a temperature change from 25°C (room temperature) to 100°C (the boiling point of water). For this range the table reveals that

$$\Delta I_{CO} = 20\ \text{nA} - 0.1\ \text{nA} = 19.9\ \text{nA}$$

$$\Delta V_{BE} = 0.48\ \text{V} - 0.65\ \text{V} = -0.17\ \text{V} \quad \text{(note the sign)}$$

and

$$\Delta\beta = 80 - 50 = 30$$

Starting with a collector current of 2 mA with an R_B of 240 kΩ, the resulting change in I_C due to an increase in temperature of 75°C is the following:

$$\Delta I_C = (50 + 1)(19.9\ \text{nA}) - \frac{50}{240\ \text{k}\Omega}(-0.17\ \text{V}) + \frac{2\ \text{mA}}{50}(30)$$

$$= 1.01\ \mu\text{A} + 35.42\ \mu\text{A} + 1200\ \mu\text{A}$$

$$= 1.236\ \text{mA}$$

which is a significant change due primarily to the change in β. The collector current has increased from 2 to 3.236 mA—but this was expected in the sense that we recognize from the content of this section that the fixed-bias configuration is the least stable.

If the more stable voltage-divider configuration were employed with a ratio $R_{\text{Th}}/R_E = 2$ and $R_E = 4.7\ k\Omega$, then

$$S(I_{CO}) = 2.89, \qquad S(V_{BE}) = -0.2 \times 10^{-3}, \qquad S(\beta) = 1.445 \times 10^{-6}$$

and

$$\Delta I_C = (2.89)(19.9\ \text{nA}) - 0.2 \times 10^{-3}(-0.17\ \text{V}) + 1.445 \times 10^{-6}(30)$$

$$= 57.51\ \text{nA} + 34\ \mu\text{A} + 43.4\ \mu\text{A}$$

$$= 0.077\ \text{mA}$$

The resulting collector current is 2.077 mA, or essentially 2.1 mA, compared to the 2.0 mA at 25°C. The network is obviously a great deal more stable than the fixed-bias configuration, as mentioned in earlier discussions. In this case, $S(\beta)$ did not override the other two factors and the effects of $S(V_{BE})$ and $S(I_{CO})$ were equally important. In fact, at higher temperatures, the effects of $S(I_{CO})$ and $S(V_{BE})$ will be greater than $S(\beta)$ for the device of Table 4.1. For temperatures below 25°C, I_C will decrease with increasingly negative temperature levels.

The effect of $S(I_{CO})$ in the design process is becoming a lesser concern because of improved manufacturing techniques that continue to lower the level of $I_{CO} = I_{CBO}$. It should also be mentioned that for a particular transistor the variation in levels of I_{CBO} and V_{BE} from one transistor to another in a lot is almost negligible compared to the variation in beta. In addition, the results of the analysis above support the fact that for a good stabilized design:

The ratio R_B/R_E or R_{Th}/R_E should be as small as possible with due consideration to all aspects of the design, including the ac response.

Although the analysis above may have been clouded by some of the complex equations for some of the sensitivities, the purpose here was to develop a higher level of awareness of the factors that go into a good design and to be more intimate with the transistor parameters and their impact on the network's performance. The analysis of the earlier sections was for idealized situations with nonvarying parameter values. We are now more aware of how the dc response of the design can vary with the parameter variations of a transistor.

4.13 PSPICE WINDOWS

Voltage-Divider Configuration

The results of Example 4.7 will now be verified using PSpice Windows. Using methods described in previous chapters, the network of Fig. 4.69 can be constructed. Recall that the transistor can be found in the **EVAL.slb** library, the dc source under **SOURCE.slb,** and the resistor under **ANALOG.slb.** The capacitor will also appear in the **ANALOG.slb** library. Three **VIEWPOINTS** appear in Fig. 4.69 as obtained from the **SPECIAL.slb** library. The collector current will be sensed by the **IPROBE** option, also appearing in the **SPECIAL.slb** library. Recall that a positive result is obtained for **IPROBE** if the direction of conventional current enters that side of the symbol with the internal curve representing the scale of the meter. We will want to set the value of beta for the transistor to match that of the example. This is accom-

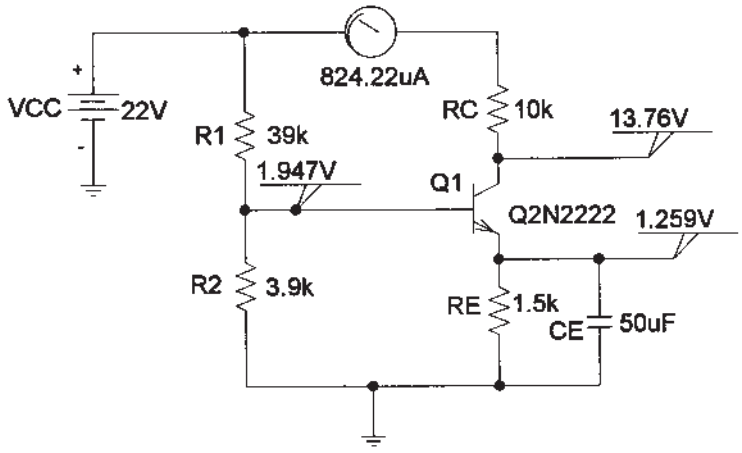


Figure 4.69 Applying PSpice Windows to the voltage-divider configuration of Example 4.7.

plished by clicking on the transistor symbol (to obtain the red outline) followed by **Edit-Model-Edit Instance Model (text)** to obtain the **Model Editor.** Then **Bf** is changed to 140 to match the value of Example 4.7. Click **OK,** and the network is set up for the analysis.

In this case, since we are only interested in the dc response, the **Probe Setup** under **Analysis** should enable **Do not auto-run Probe.** It will save us from having to deal with the Probe response before viewing the output file or screen. The sequence **Analysis-Simulate** will result in the dc levels appearing in Fig. 4.69, which closely match those of Example 4.7. The collector-to-emitter voltage is 13.76 V − 1.259 V = 12.5 V, versus 12.22 V of Example 4.7, and the collector current is 0.824 mA, versus 0.85 mA. Any differences are due to the fact that we are using an actual transistor with a host of parameters not considered in our analysis. Recall the difference in beta from the specification value and the value obtained from the plot of the previous chapter.

Since the voltage-divider network is one that is to have a low sensitivity to changes in beta, let us return to the transistor and replace the beta of 140 with the default value of 225.9 and examine the results. The analysis will result in the dc levels appearing in Fig. 4.70, which are very close to those of Fig. 4.69.

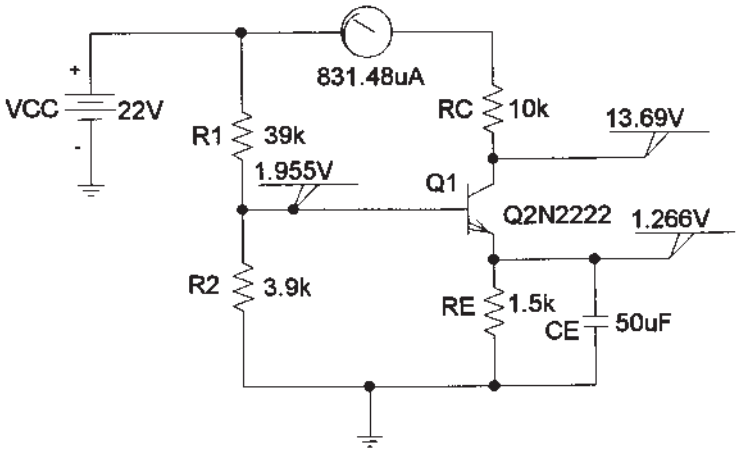


Figure 4.70 Response obtained after changing β from 140 to 255.9 for the network of Figure 4.69.

The collector-to-emitter voltage is 13.69 V − 1.266 V = 12.42 V, which is very close to that obtained with a much lower beta. The collector current is actually closer to the hand-calculated level, 0.832 mA versus 0.85 mA. There is no question, therefore, that the voltage-divider configuration demonstrates a low sensitivity to changes in beta. Recall, however, that the fixed-bias configuration was very sensitive to changes in beta, and let us proceed with the same type of analysis for the fixed-bias configuration and compare notes.

Fixed-Bias Configuration

The fixed-bias configuration of Fig. 4.71 is from Example 4.1 to permit a comparison of results. Beta was set to 50 using the procedure described above. In this case, we will use a **VIEWPOINT** to read the collector-to-emitter voltage and enable the display of bias currents (using the icon with the large capital **I**). In addition, we will inhibit the display of some bias currents using the icon with the smaller capital **I** and the diode symbol. The final touch is to move some of the currents displayed to clean up the presentation.

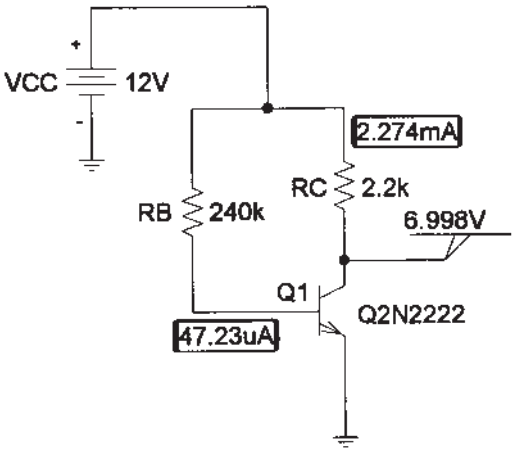


Figure 4.71 Fixed-bias configuration with a β of 50.

A PSpice analysis of the network will result in the levels appearing in Fig. 4.71. These are a close match with the hand-written solution, with the collector voltage at 6.998 V versus 6.83 V, the collector current at 2.274 mA versus 2.35 mA, and the base current at 47.23 μA versus 47.08 μA.

Let us now test the sensitivity to changes in beta by changing to the default value of 255.9. The results appear in Fig. 4.72. Note the dramatic drop in V_C to 0.113 V compared to 6.83 V and the significant rise in I_D to 5.4 mA versus the solution of 2.35 mA. The fixed-bias configuration is obviously very beta-sensitive.

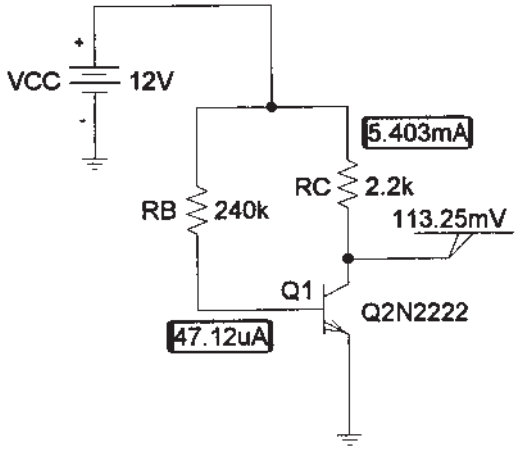


Figure 4.72 Network of Figure 4.71 with a β of 255.9.

PROBLEMS

§ 4.3 Fixed-Bias Circuit

1. For the fixed-bias configuration of Fig. 4.73, determine:
(a) I_{B_Q}.
(b) I_{C_Q}.
(c) V_{CE_Q}.
(d) V_C.
(e) V_B.
(f) V_E.

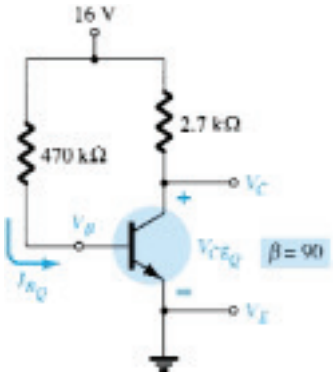


Figure 4.73 Problems 1, 4, 11, 47, 51, 52, 53

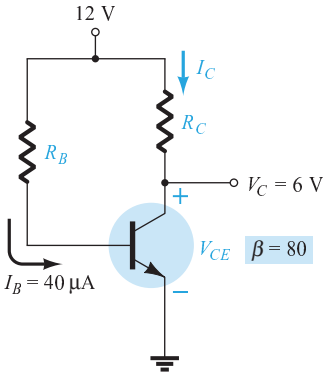


Figure 4.74 Problem 2

2. Given the information appearing in Fig. 4.74, determine:
(a) I_C.
(b) R_C.
(c) R_B.
(d) V_{CE}.

3. Given the information appearing in Fig. 4.75, determine:
(a) I_C.
(b) V_{CC}.
(c) β.
(d) R_B.

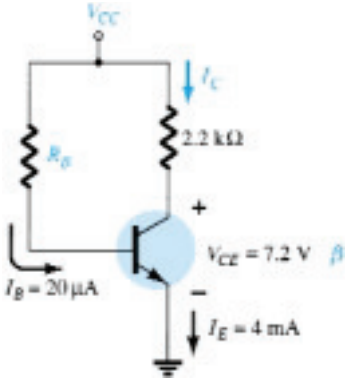


Figure 4.75 Problem 3

4. Find the saturation current ($I_{C_{sat}}$) for the fixed-bias configuration of Fig. 4.73.

*** 5.** Given the BJT transistor characteristics of Fig. 4.76:
(a) Draw a load line on the characteristics determined by $E = 21$ V and $R_C = 3$ kΩ for a fixed-bias configuration.
(b) Choose an operating point midway between cutoff and saturation. Determine the value of R_B to establish the resulting operating point.
(c) What are the resulting values of I_{C_Q} and V_{CE_Q}?
(d) What is the value of β at the operating point?
(e) What is the value of α defined by the operating point?
(f) What is the saturation ($I_{C_{sat}}$) current for the design?
(g) Sketch the resulting fixed-bias configuration.
(h) What is the dc power dissipated by the device at the operating point?
(i) What is the power supplied by V_{CC}?
(j) Determine the power dissipated by the resistive elements by taking the difference between the results of parts (h) and (i).

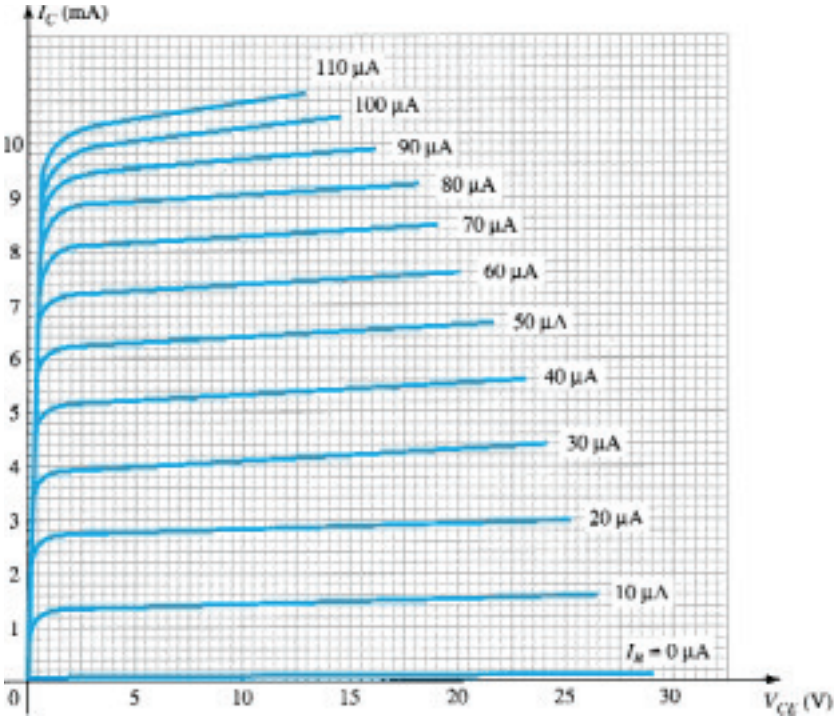


Figure 4.76 Problems 5, 10, 19, 35, 36

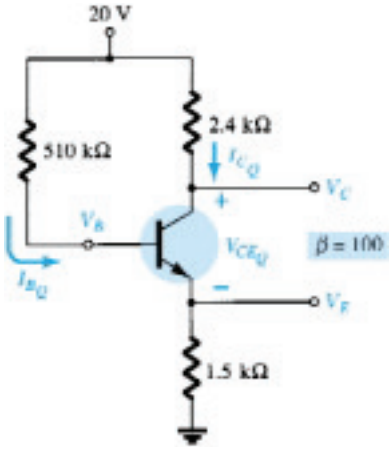


Figure 4.77 Problems 6, 9, 11, 20, 24, 48, 51, 54

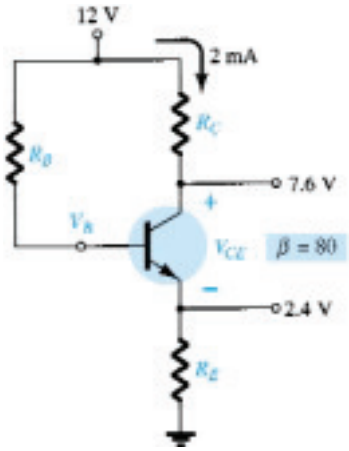


Figure 4.78 Problem 7

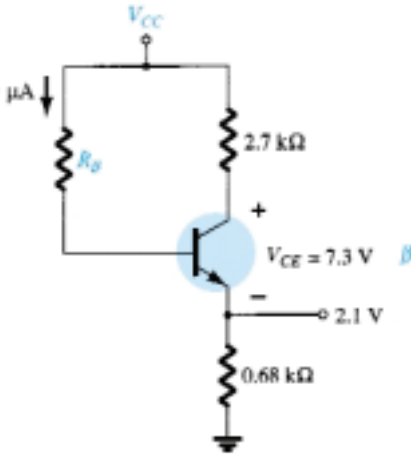


Figure 4.79 Problem 8

§ 4.4 Emitter-Stabilized Bias Circuit

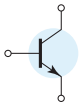
6. For the emitter-stabilized bias circuit of Fig. 4.77, determine:
(a) I_{B_Q}.
(b) I_{C_Q}.
(c) V_{CE_Q}.
(d) V_C.
(e) V_B.
(f) V_E.

7. Given the information provided in Fig. 4.78, determine:
(a) R_C.
(b) R_E.
(c) R_B.
(d) V_{CE}.
(e) V_B.

8. Given the information provided in Fig. 4.79, determine:
(a) β.
(b) V_{CC}.
(c) R_B.

9. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.77.

* **10.** Using the characteristics of Fig. 4.76, determine the following for an emitter-bias configuration if a Q-point is defined at $I_{C_Q} = 4$ mA and $V_{CE_Q} = 10$ V.
(a) R_C if $V_{CC} = 24$ V and $R_E = 1.2$ kΩ.
(b) β at the operating point.
(c) R_B.
(d) Power dissipated by the transistor.
(e) Power dissipated by the resistor R_C.



* **11.** (a) Determine I_C and V_{CE} for the network of Fig. 4.73.
(b) Change β to 135 and determine the new value of I_C and V_{CE} for the network of Fig. 4.73.
(c) Determine the magnitude of the percent change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left| \frac{I_{C(\text{part b})} - I_{C(\text{part a})}}{I_{C(\text{part a})}} \right| \times 100\%, \qquad \%\Delta V_{CE} = \left| \frac{V_{CE(\text{part b})} - V_{CE(\text{part a})}}{V_{CE(\text{part a})}} \right| \times 100\%$$

(d) Determine I_C and V_{CE} for the network of Fig. 4.77.
(e) Change β to 150 and determine the new value of I_C and V_{CE} for the network of Fig. 4.77.
(f) Determine the magnitude of the percent change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left| \frac{I_{C(\text{part e})} - I_{C(\text{part d})}}{I_{C(\text{part d})}} \right| \times 100\%, \qquad \%\Delta V_{CE} = \left| \frac{V_{CE(\text{part e})} - V_{CE(\text{part d})}}{V_{CE(\text{part d})}} \right| \times 100\%$$

(g) In each of the above, the magnitude of β was increased 50%. Compare the percent change in I_C and V_{CE} for each configuration, and comment on which seems to be less sensitive to changes in β.

§ 4.5 Voltage-Divider Bias

12. For the voltage-divider bias configuration of Fig. 4.80, determine:
(a) I_{B_Q}.
(b) I_{C_Q}.
(c) V_{CE_Q}.
(d) V_C.
(e) V_E.
(f) V_B.

13. Given the information provided in Fig. 4.81, determine:
(a) I_C.
(b) V_E.
(c) V_B.
(d) R_1.

14. Given the information appearing in Fig. 4.82, determine:
(a) I_C.
(b) V_E.
(c) V_{CC}.
(d) V_{CE}.
(e) V_B.
(f) R_1.

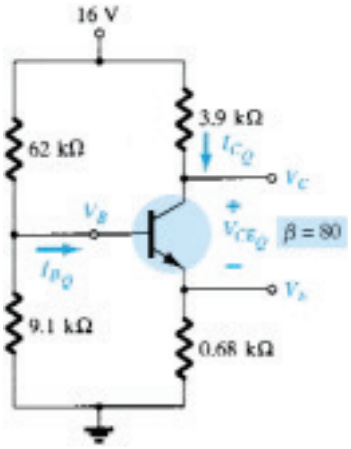


Figure 4.80 Problems 12, 15, 18, 20, 24, 49, 51, 52, 55

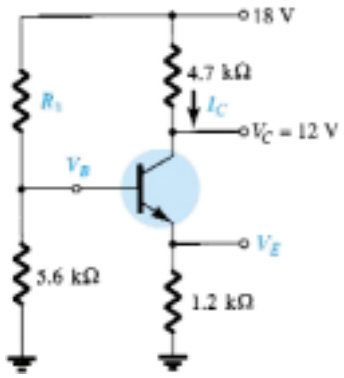


Figure 4.81 Problem 13

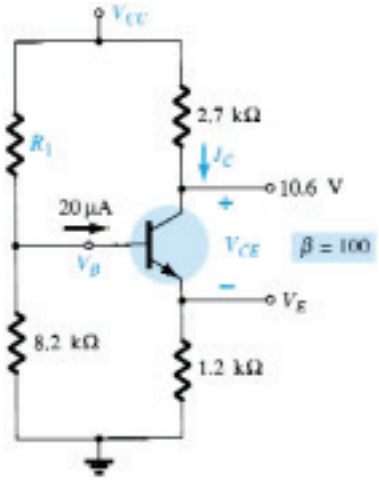


Figure 4.82 Problem 14

15. Determine the saturation current ($I_{C_{sat}}$) for the network of Fig. 4.80.

* 16. Determine the following for the voltage-divider configuration of Fig. 4.83 using the approximate approach if the condition established by Eq. (4.33) is satisfied.
(a) I_C.
(b) V_{CE}.
(c) I_B.
(d) V_E.
(e) V_B.

* 17. Repeat Problem 16 using the exact (Thévenin) approach and compare solutions. Based on the results, is the approximate approach a valid analysis technique if Eq. (4.33) is satisfied?

18. (a) Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} for the network of Problem 12 (Fig. 4.80) using the approximate approach even though the condition established by Eq. (4.33) is not satisfied.
(b) Determine I_{C_Q}, V_{CE_Q}, and I_{B_Q} using the exact approach.
(c) Compare solutions and comment on whether the difference is sufficiently large to require standing by Eq. (4.33) when determining which approach to employ.

* 19. (a) Using the characteristics of Fig. 4.76, determine R_C and R_E for a voltage-divider network having a Q-point of $I_{C_Q} = 5$ mA and $V_{CE_Q} = 8$ V. Use $V_{CC} = 24$ V and $R_C = 3R_E$.
(b) Find V_E.
(c) Determine V_B.
(d) Find R_2 if $R_1 = 24\ \text{k}\Omega$ assuming that $\beta R_E > 10R_2$.
(e) Calculate β at the Q-point.
(f) Test Eq. (4.33), and note whether the assumption of part (d) is correct.

* 20. (a) Determine I_C and V_{CE} for the network of Fig. 4.80.
(b) Change β to 120 (50% increase), and determine the new values of I_C and V_{CE} for the network of Fig. 4.80.
(c) Determine the magnitude of the percent change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left| \frac{I_{C_{(\text{part b})}} - I_{C_{(\text{part a})}}}{I_{C_{(\text{part a})}}} \right| \times 100\%, \qquad \%\Delta V_{CE} = \left| \frac{V_{CE_{(\text{part b})}} - V_{CE_{(\text{part a})}}}{V_{CE_{(\text{part a})}}} \right| \times 100\%$$

(d) Compare the solution to part (c) with the solutions obtained for parts (c) and (f) of Problem 11. If not performed, note the solutions provided in Appendix E.
(e) Based on the results of part (d), which configuration is least sensitive to variations in β?

* 21. (a) Repeat parts (a) through (e) of Problem 20 for the network of Fig. 4.83. Change β to 180 in part (b).
(b) What general conclusions can be made about networks in which the condition $\beta R_E > 10R_2$ is satisfied and the quantities I_C and V_{CE} are to be determined in response to a change in β?

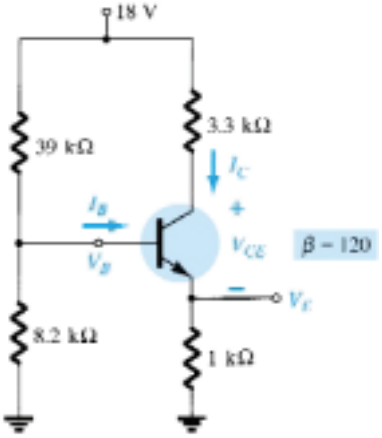


Figure 4.83 Problems 16, 17, 21

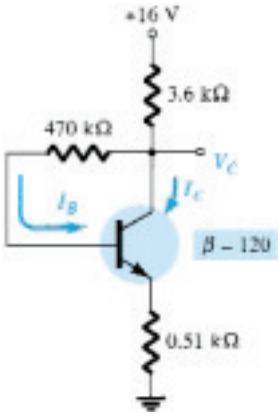


Figure 4.84 Problems 22, 50, 56

§ 4.6 DC Bias with Voltage Feedback

22. For the collector feedback configuration of Fig. 4.84, determine:
(a) I_B.
(b) I_C.
(c) V_C.

23. For the voltage feedback network of Fig. 4.85, determine:
(a) I_C.
(b) V_C.
(c) V_E.
(d) V_{CE}.

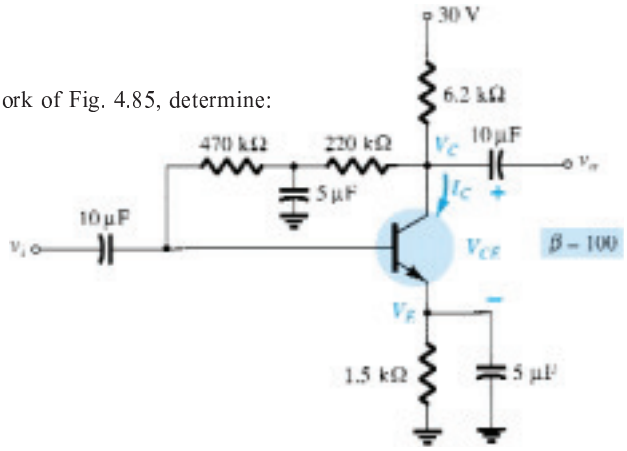
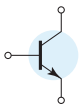


Figure 4.85 Problem 23



* **24.** (a) Determine the level of I_C and V_{CE} for the network of Fig. 4.86.
(b) Change β to 135 (50% increase), and calculate the new levels of I_C and V_{CE}.
(c) Determine the magnitude of the percent change in I_C and V_{CE} using the following equations:

$$\%\Delta I_C = \left| \frac{I_{C_{(\text{part b})}} - I_{C_{(\text{part a})}}}{I_{C_{(\text{part a})}}} \right| \times 100\%, \qquad \%\Delta V_{CE} = \left| \frac{V_{CE_{(\text{part b})}} - V_{CE_{(\text{part a})}}}{V_{CE_{(\text{part a})}}} \right| \times 100\%$$

(d) Compare the results of part (c) with those of Problems 11(c), 11(f), and 20(c). How does the collector-feedback network stack up against the other configurations in sensitivity to changes in β?

25. Determine the range of possible values for V_C for the network of Fig. 4.87 using the 1-MΩ potentiometer.

* **26.** Given $V_B = 4$ V for the network of Fig. 4.88, determine:
(a) V_E.
(b) I_C.
(c) V_C.
(d) V_{CE}.
(e) I_B.
(f) β.

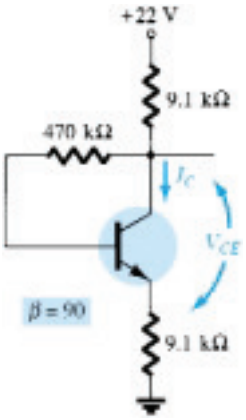


Figure 4.86 Problem 24

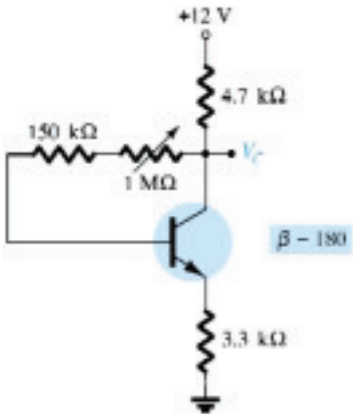


Figure 4.87 Problem 25

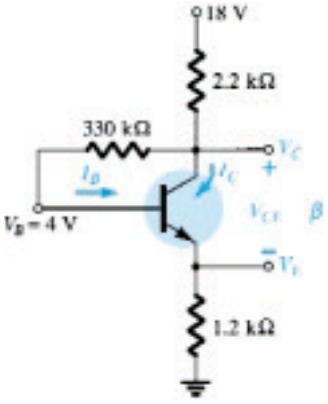


Figure 4.88 Problem 26

§ 4.7 Miscellaneous Bias Configurations

27. Given $V_C = 8$ V for the network of Fig. 4.89, determine:
(a) I_B.
(b) I_C.
(c) β.
(d) V_{CE}.

* **28.** For the network of Fig. 4.90, determine:
(a) I_B.
(b) I_C.
(c) V_{CE}.
(d) V_C.

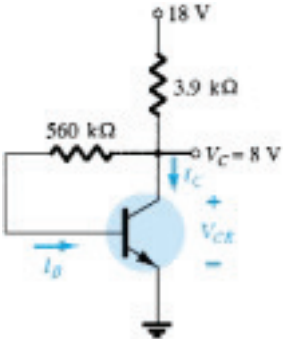


Figure 4.89 Problem 27

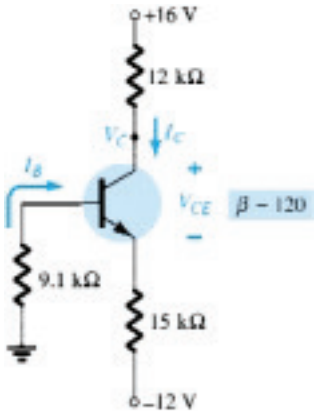


Figure 4.90 Problem 28

* **29.** For the network of Fig. 4.91, determine:
  (a) I_B.
  (b) I_C.
  (c) V_E.
  (d) V_{CE}.

* **30.** Determine the level of V_E and I_E for the network of Fig. 4.92.

* **31.** For the network of Fig. 4.93, determine:
  (a) I_E.
  (b) V_C.
  (c) V_{CE}.

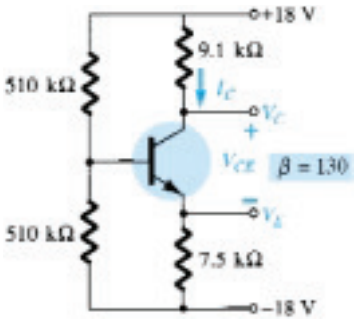


Figure 4.91 Problem 29

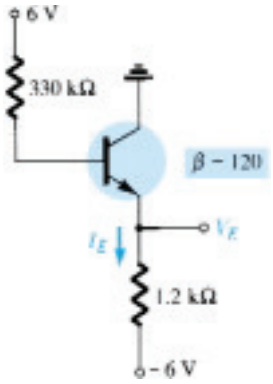


Figure 4.92 Problem 30

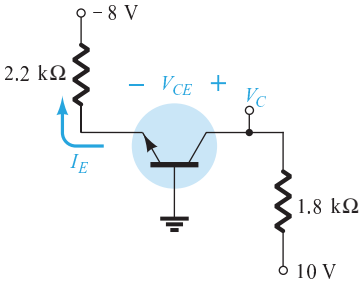


Figure 4.93 Problem 31

§ 4.8 Design Operations

32. Determine R_C and R_B for a fixed-bias configuration if $V_{CC} = 12$ V, $\beta = 80$, and $I_{C_Q} = 2.5$ mA with $V_{CE_Q} = 6$ V. Use standard values.

33. Design an emitter-stabilized network at $I_{C_Q} = \frac{1}{2}I_{C_{sat}}$ and $V_{CE_Q} = \frac{1}{2}V_{CC}$. Use $V_{CC} = 20$ V, $I_{C_{sat}} = 10$ mA, $\beta = 120$, and $R_C = 4R_E$. Use standard values.

34. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of $I_{C_Q} = 4$ mA and $V_{CE_Q} = 8$ V. Choose $V_E = \frac{1}{8}V_{CC}$. Use standard values.

* **35.** Using the characteristics of Fig. 4.76, design a voltage-divider configuration to have a saturation level of 10 mA and a Q-point one-half the distance between cutoff and saturation. The available supply is 28 V, and V_E is to be one-fifth of V_{CC}. The condition established by Eq. (4.33) should also be met to provide a high stability factor. Use standard values.

§ 4.9 Transistor Switching Networks

* **36.** Using the characteristics of Fig. 4.76, determine the appearance of the output waveform for the network of Fig. 4.94. Include the effects of $V_{CE_{sat}}$, and determine I_B, $I_{B_{max}}$, and $I_{C_{sat}}$ when $V_i = 10$ V. Determine the collector-to-emitter resistance at saturation and cutoff.

* **37.** Design the transistor inverter of Fig. 4.95 to operate with a saturation current of 8 mA using a transistor with a beta of 100. Use a level of I_B equal to 120% of $I_{B_{max}}$ and standard resistor values.

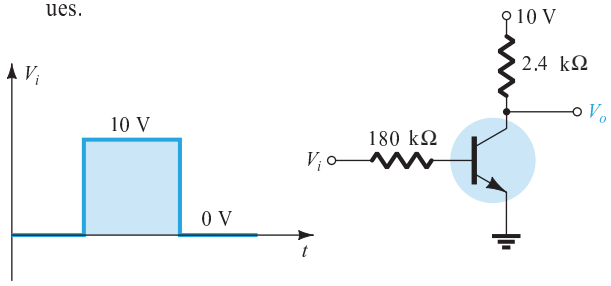


Figure 4.94 Problem 36

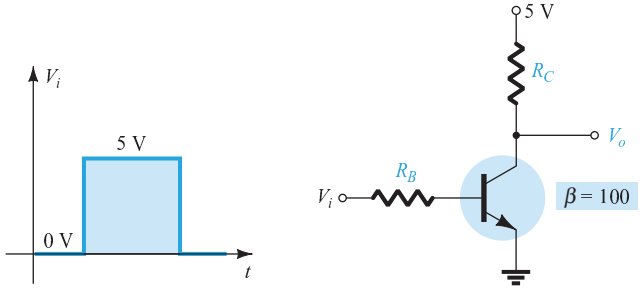


Figure 4.95 Problem 37

38. (a) Using the characteristics of Fig. 3.23c, determine t_{on} and t_{off} at a current of 2 mA. Note the use of log scales and the possible need to refer to Section 11.2.
(b) Repeat part (a) at a current of 10 mA. How have t_{on} and t_{off} changed with increase in collector current?
(c) For parts (a) and (b), sketch the pulse waveform of Fig. 4.56 and compare results.

§ 4.10 Troubleshooting Techniques

* **39.** The measurements of Fig. 4.96 all reveal that the network is not functioning correctly. List as many reasons as you can for the measurements obtained.

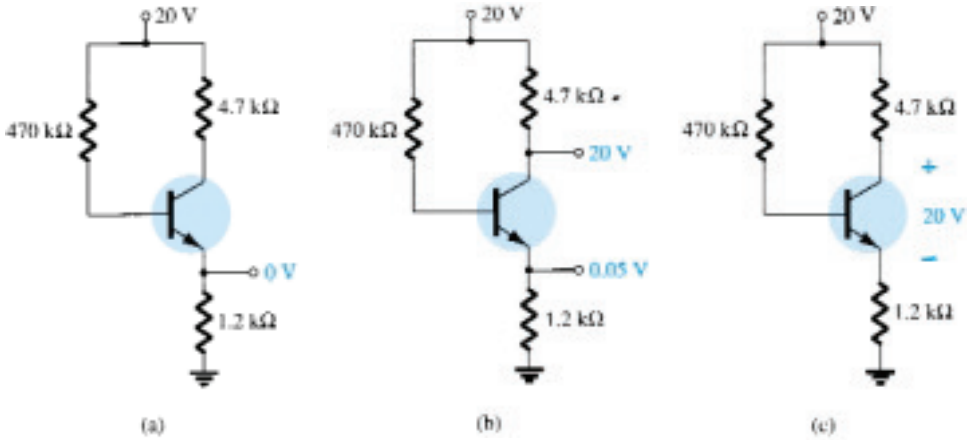


Figure 4.96 Problem 39

* **40.** The measurements appearing in Fig. 4.97 reveal that the networks are not operating properly. Be specific in describing why the levels obtained reflect a problem with the expected network behavior. In other words, the levels obtained reflect a very specific problem in each case.

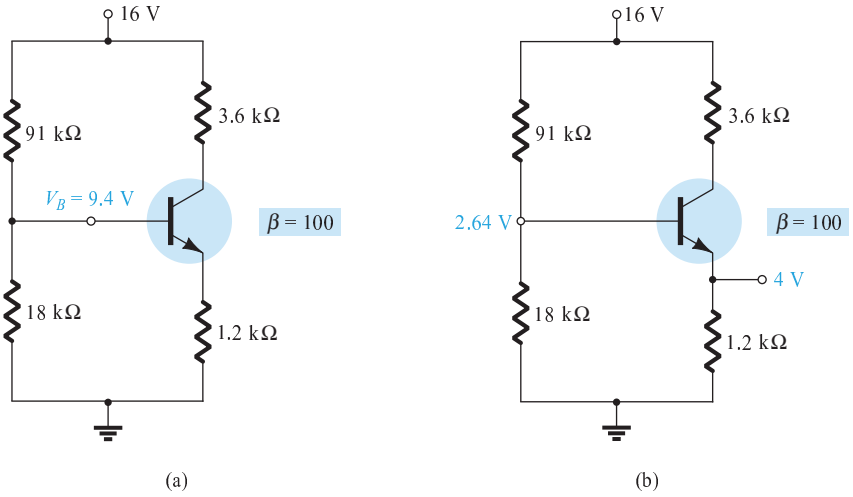


Figure 4.97 Problem 40

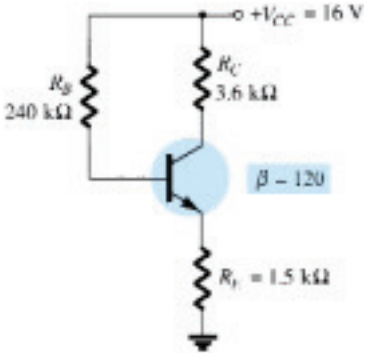


Figure 4.98 Problem 41

41. For the circuit of Fig. 4.98:
(a) Does V_C increase or decrease if R_B is increased?
(b) Does I_C increase or decrease if β is reduced?
(c) What happens to the saturation current if β is increased?
(d) Does the collector current increase or decrease if V_{CC} is reduced?
(e) What happens to V_{CE} if the transistor is replaced by one with smaller β?

42. Answer the following questions about the circuit of Fig. 4.99.
(a) What happens to the voltage V_C if the transistor is replaced by one having a larger value of β?
(b) What happens to the voltage V_{CE} if the ground leg of resistor R_{B_2} opens (does not connect to ground)?
(c) What happens to I_C if the supply voltage is low?
(d) What voltage V_{CE} would occur if the transistor base–emitter junction fails by becoming open?
(e) What voltage V_{CE} would result if the transistor base–emitter junction fails by becoming a short?

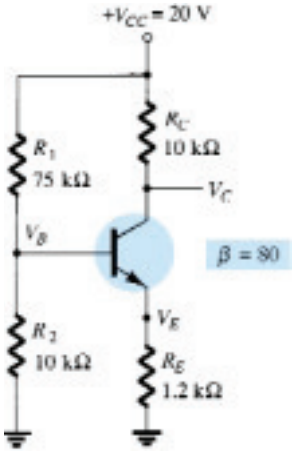


Figure 4.99 Problem 42

* **43.** Answer the following questions about the circuit of Fig. 4.100.
(a) What happens to the voltage V_C if the resistor R_B is open?
(b) What should happen to V_{CE} if β increases due to temperature?
(c) How will V_E be affected when replacing the collector resistor with one whose resistance is at the lower end of the tolerance range?
(d) If the transistor collector connection becomes open, what will happen to V_E?
(e) What might cause V_{CE} to become nearly 18 V?

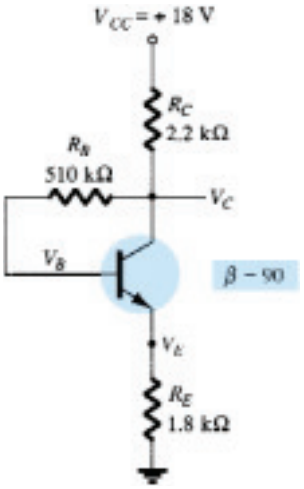


Figure 4.100 Problem 43

§ 4.11 *PNP* Transistors

44. Determine V_C, V_{CE}, and I_C for the network of Fig. 4.101.

45. Determine V_C and I_B for the network of Fig. 4.102.

46. Determine I_E and V_C for the network of Fig. 4.103.

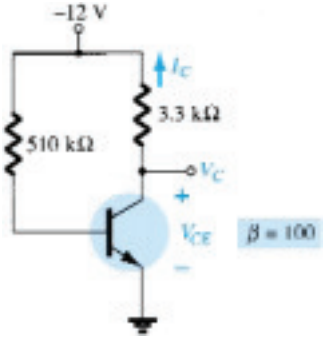


Figure 4.101 Problem 44

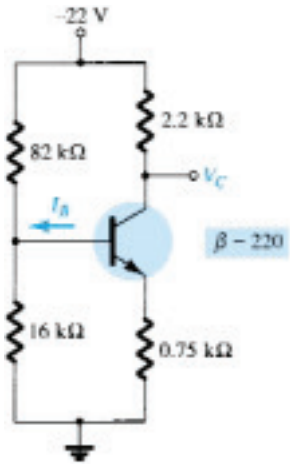


Figure 4.102 Problem 45

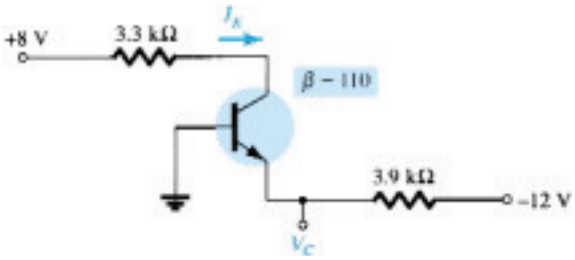
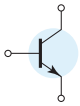


Figure 4.103 Problem 46



§ 4.12 Bias Stabilization

47. Determine the following for the network of Fig. 4.73.
(a) $S(I_{CO})$.
(b) $S(V_{BE})$.
(c) $S(\beta)$ using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
(d) Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V, and β increases 25%.

* **48.** For the network of Fig. 4.77, determine:
(a) $S(I_{CO})$.
(b) $S(V_{BE})$.
(c) $S(\beta)$ using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
(d) Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V, and β increases 25%.

* **49.** For the network of Fig. 4.80, determine:
(a) $S(I_{CO})$.
(b) $S(V_{BE})$.
(c) $S(\beta)$ using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
(d) Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V, and β increases 25%.

* **50.** For the network of Fig. 4.89, determine:
(a) $S(I_{CO})$.
(b) $S(V_{BE})$.
(c) $S(\beta)$ using T_1 as the temperature at which the parameter values are specified and $\beta(T_2)$ as 25% more than $\beta(T_1)$.
(d) Determine the net change in I_C if a change in operating conditions results in I_{CO} increasing from 0.2 to 10 μA, V_{BE} drops from 0.7 to 0.5 V, and β increases 25%.

* **51.** Compare the relative values of stability for Problems 47 through 50. The results for Exercises 47 and 49 can be found in Appendix E. Can any general conclusions be derived from the results?

* **52.** (a) Compare the levels of stability for the fixed-bias configuration of Problem 47.
(b) Compare the levels of stability for the voltage-divider configuration of Problem 49.
(c) Which factors of parts (a) and (b) seem to have the most influence on the stability of the system, or is there no general pattern to the results?

§ 4.13 PSpice Windows

53. Perform a PSpice analysis of the network of Fig. 4.73. That is, determine I_C, V_{CE}, band I_B.

54. Repeat Problem 53 for the network of Fig. 4.77.

55. Repeat Problem 53 for the network of Fig. 4.80.

56. Repeat Problem 53 for the network of Fig. 4.84.

*Please Note: Asterisks indicate more difficult problems.

I_{DDS}/V_P

CHAPTER

Field-Effect Transistors 5

5.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in Chapters 3 and 4. Although there are important differences between the two types of devices, there are also many similarities that will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that the BJT transistor is a *current-controlled* device as depicted in Fig. 5.1a, while the JFET transistor is a *voltage-controlled* device as shown in Fig. 5.1b. In other words, the current I_C in Fig. 5.1a is a direct function of the level of I_B. For the FET the current I will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 5.1b. In each case the current of the output circuit is being controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

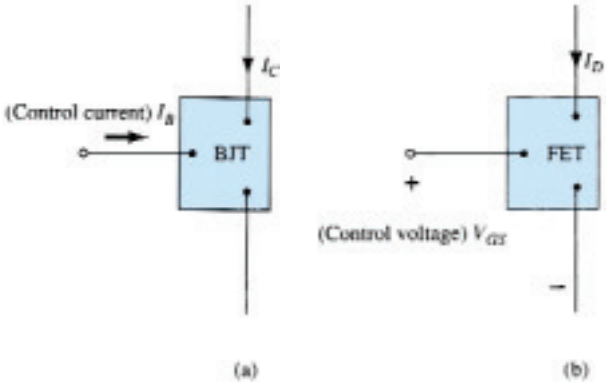


Figure 5.1 (a) Current-controlled and (b) voltage-controlled amplifiers.

Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi-* revealing that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

The term field-effect in the chosen name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to the magnet without the need for actual contact. The magnetic field of the permanent magnet has enveloped the filings and attracted them to the magnet through an effort on the part of the magnetic flux lines to be as short as possible. For the FET an *electric field* is established by the charges present that will control the conduction path of the output

circuit without the need for direct contact between the controlling and controlled quantities.

There is a natural tendency when introducing a second device with a range of applications similar to one already introduced to compare some of the general characteristics of one versus the other. One of the most important characteristics of the FET is its *high input impedance*. At a level of 1 to several hundred megohms it far exceeds the typical input resistance levels of the BJT transistor configurations—a very important characteristic in the design of linear ac amplifier systems. On the other hand, the BJT transistor has a much higher sensitivity to changes in the applied signal. In other words, the variation in output current is typically a great deal more for BJTs than FETs for the same change in applied voltage. For this reason, typical ac voltage gains for BJT amplifiers are a great deal more than for FETs. In general, FETs are more temperature stable than BJTs, and FETs are usually smaller in construction than BJTs, making them particularly useful in *integrated-circuit (IC)* chips. The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Two types of FETs will be introduced in this chapter: the *junction field-effect transistor* (JFET) and the *metal-oxide-semiconductor field-effect transistor (MOSFET)*. The MOSFET category is further broken down into depletion and enhancement types, which are both described. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design. However, as a discrete element in a typical top-hat container, it must be handled with care (to be discussed in a later section).

Once the FET construction and characteristics have been introduced, the biasing arrangements will be covered in Chapter 6. The analysis performed in Chapter 4 using BJT transistors will prove helpful in the derivation of the important equations and understanding the results obtained for FET circuits.

Drs. Ian Munro Ross (front) and G. C. Dacey jointly developed an experimental procedure for measuring the characteristics of a field-effect transistor in 1955. (Courtesy of AT&T Archives.)

Dr. Ross Born: Southport, England
PhD Gonville and Caius College, Cambridge
University President emeritus of AT&T Bell Labs Fellow—IEEE, Member of the National Science Board
Chairman—National Advisory Committee on Semiconductors

Dr. Dacey Born: Chicago, Illinois
PhD California Institute of Technology
Director of Solid-State Electronics Research at Bell Labs
Vice President, Research at Sandia Corporation
Member IRE, Tau Beta Pi, Eta Kappa Nu

5.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two. In our discussion of the BJT transistor the *npn* transistor was employed through the major part of the analysis and design sections, with a section devoted to the impact of using a *pnp* transistor. For the JFET transistor the *n*-channel device will appear as the prominent device, with paragraphs and sections devoted to the impact of using a *p*-channel JFET.

The basic construction of the *n*-channel JFET is shown in Fig. 5.2. Note that the major part of the structure is the *n*-type material that forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D),* while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S)*. The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p-n* junctions under no-bias conditions. The result is a depletion region at each junction as shown in Fig. 5.2 that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is that region void of free carriers and therefore unable to support conduction through the region.

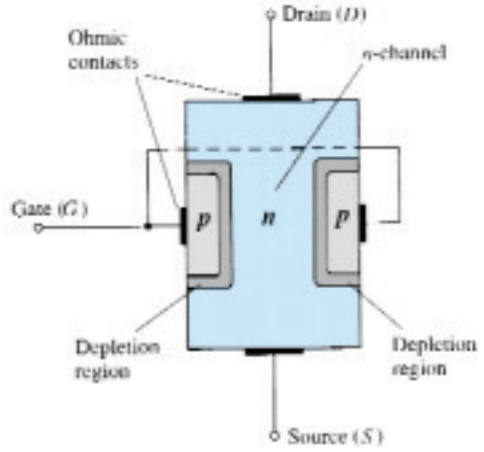


Figure 5.2 Junction field-effect transistor (JFET).

Analogies are seldom perfect and at times can be misleading, but the water analogy of Fig. 5.3 does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source that will establish a flow of water (electrons) from the spigot (source). The "gate," through an applied signal (potential), controls the flow of water (charge) to the "drain." The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 5.2 because the terminology is defined for electron flow.

Figure 5.3 Water analogy for the JFET control mechanism.

$V_{GS} = 0$ V, V_{DS} Some Positive Value

In Fig. 5.4, a positive voltage V_{DS} has been applied across the channel and the gate has been connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 5.2. The instant the voltage V_{DD} ($= V_{DS}$) is applied, the electrons will be drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 5.4. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions appearing in Fig. 5.4, the flow of charge is relatively uninhibited and limited solely by the resistance of the *n*-channel between drain and source.

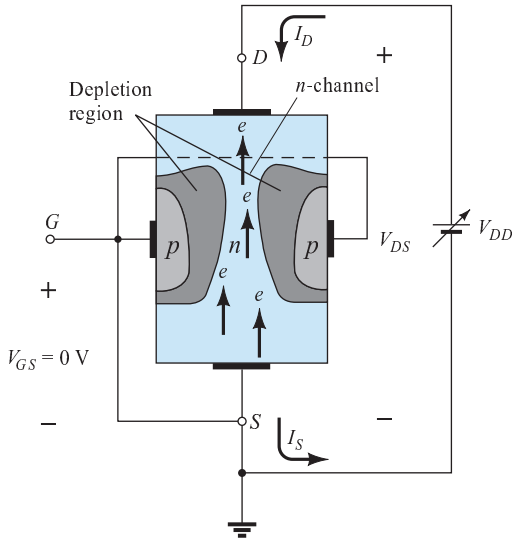


Figure 5.4 JFET in the $V_{GS} = 0$ V and $V_{DS} > 0$ V.

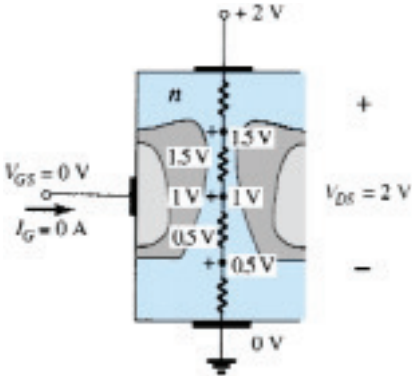


Figure 5.5 Varying reverse-bias potentials across the *p-n* junction of an *n*-channel JFET.

It is important to note that the depletion region is wider near the top of both *p*-type materials. The reason for the change in width of the region is best described through the help of Fig. 5.5. Assuming a uniform resistance in the *n*-channel, the resistance of the channel can be broken down to the divisions appearing in Fig. 5.5. The current I_D will establish the voltage levels through the channel as indicated on the same figure. The result is that the upper region of the *p*-type material will be reverse-biased by about 1.5 V, with the lower region only reverse-biased by 0.5 V. Recall from the discussion of the diode operation that the greater the applied reverse bias, the wider the depletion region—hence the distribution of the depletion region as shown in Fig. 5.5. The fact that the *p-n* junction is reverse-biased for the length of the channel results in a gate current of zero amperes as shown in the same figure. The fact that $I_G = 0$ A is an important characteristic of the JFET.

As the voltage V_{DS} is increased from 0 to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear as shown in Fig. 5.6. The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P in Fig. 5.6, the depletion regions of Fig. 5.4 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 5.6 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" as shown in Fig. 5.7, a condition referred to as *pinch-off* will result. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P as shown in Fig. 5.6. In actuality, the term *pinch-off* is a misnomer in that it suggests the current I_D is pinched off and drops to 0 A. As shown in Fig. 5.6, however, this is hardly the case—I_D maintains a saturation level defined as I_{DSS} in Fig. 5.6. In reality a very small channel still exists, with a current of very high density. The fact that I_D does not drop off at pinch-off and maintains the saturation level indicated in Fig. 5.6 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the *n*-channel material to establish the varying levels of reverse bias along the *p-n* junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

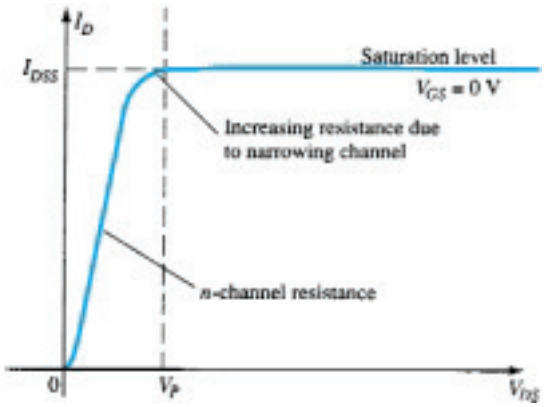


Figure 5.6 I_D versus V_{DS} for $V_{GS} = 0$ V.

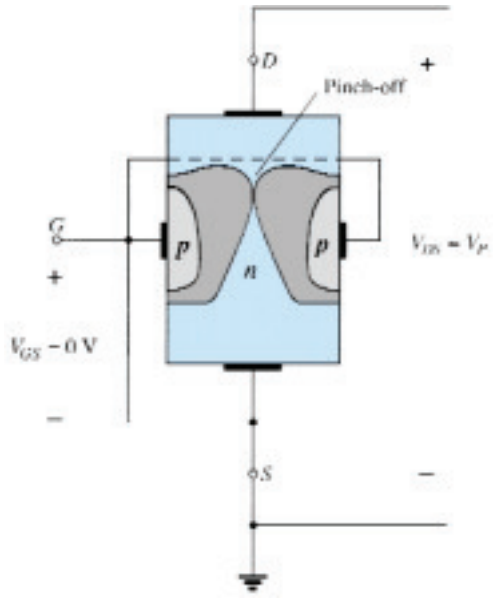


Figure 5.7 Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions will increase in length along the channel, but the level of I_D remains essentially the same. In essence, therefore, once $V_{DS} > V_P$ the JFET has the characteristics of a current source. As shown in Fig. 5.8, the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels $> V_P$) is determined by the applied load.

The choice of notation I_{DSS} is derived from the fact that it is the *D*rain-to-*S*ource current with a *S*hort-circuit connection from gate to source. As we continue to investigate the characteristics of the device we will find that:

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > |V_P|$.

Note in Fig. 5.6 that $V_{GS} = 0$ V for the entire length of the curve. The next few paragraphs will describe how the characteristics of Fig. 5.6 are affected by changes in the level of V_{GS}.

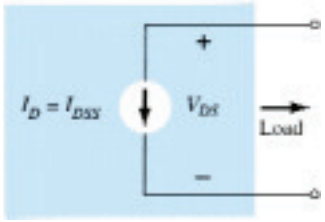


Figure 5.8 Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

$V_{GS} < 0$ V

The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET. Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET. For the *n*-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

In Fig. 5.9 a negative voltage of -1 V has been applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS} as shown in Fig. 5.10 for $V_{GS} = -1$ V. The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative. Note also on Fig. 5.10 how the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off." In summary:

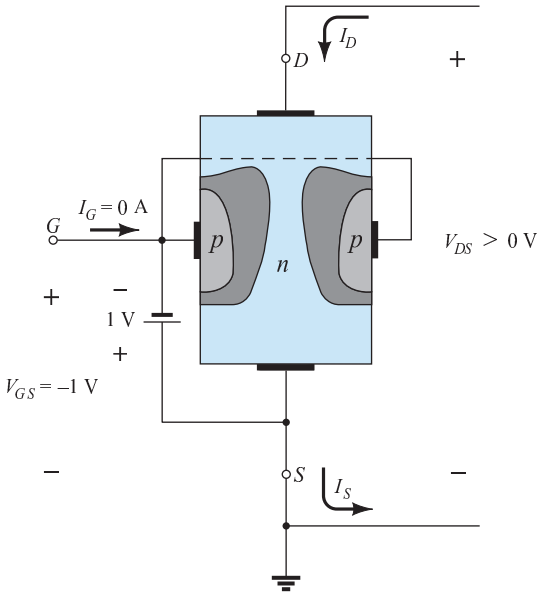


Figure 5.9 Application of a negative voltage to the gate of a JFET.

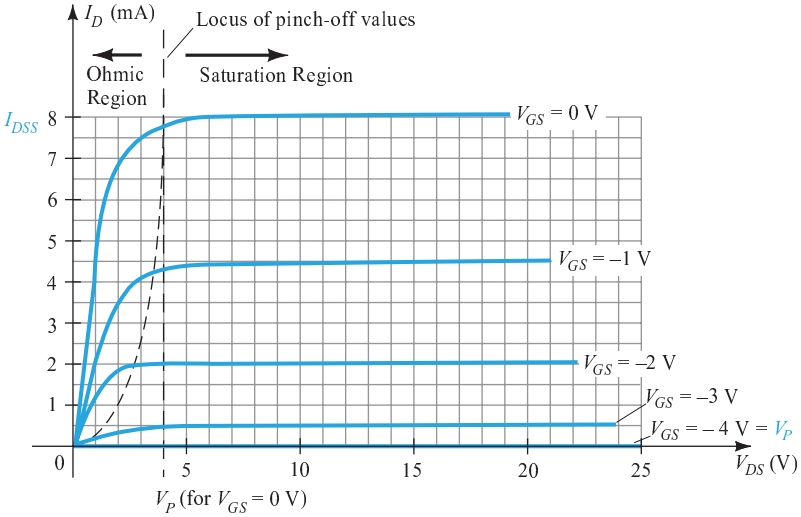


Figure 5.10 *n*-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

On most specification sheets the pinch-off voltage is specified as $V_{GS(off)}$ rather than V_P. A specification sheet will be reviewed later in the chapter when the primary elements of concern have been introduced. The region to the right of the pinch-off locus of Fig. 5.10 is the region typically employed in linear amplifiers (amplifiers with minimum distortion of the applied signal) and is commonly referred to as the *constant-current, saturation,* or *linear amplification region.*

Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 5.10 is referred to as the *ohmic* or *voltage-controlled resistance region.* In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage. Note in Fig. 5.10 that the slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} < V_P$ is a function of the applied voltage V_{GS}. As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding with an increasing resistance level. The following equation will provide a good first approximation to the resistance level in terms of the applied voltage V_{GS}.

$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2} \tag{5.1}$$

where r_o is the resistance with $V_{GS} = 0$ V and r_d the resistance at a particular level of V_{GS}.

For an *n*-channel JFET with r_o equal to 10 kΩ ($V_{GS} = 0$ V, $V_P = -6$ V), Eq. (5.1) will result in 40 kΩ at $V_{GS} = -3$ V.

p-Channel Devices

The *p*-channel JFET is constructed in exactly the same manner as the *n*-channel device of Fig. 5.2, but with a reversal of the *p*- and *n*-type materials as shown in Fig. 5.11.

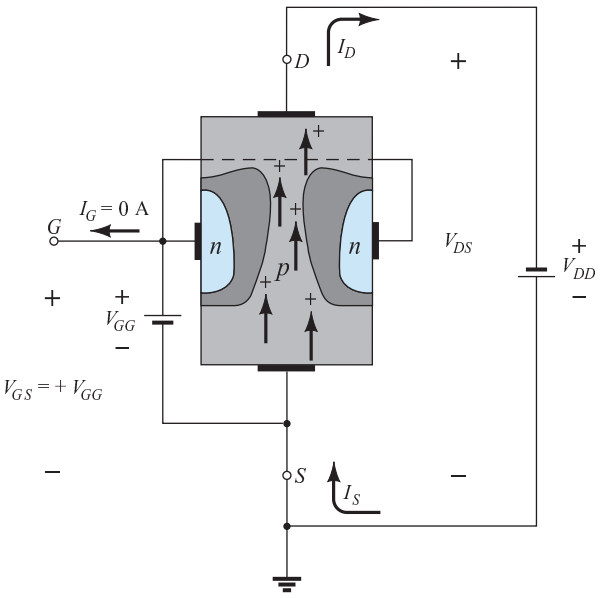


Figure 5.11 *p*-Channel JFET.

The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 5.12, which has an I_{DSS} of 6 mA and a pinch-off voltage of $V_{GS} = +6$ V. Do not let the minus signs for V_{DS} confuse you. They simply indicate that the source is at a higher potential than the drain.

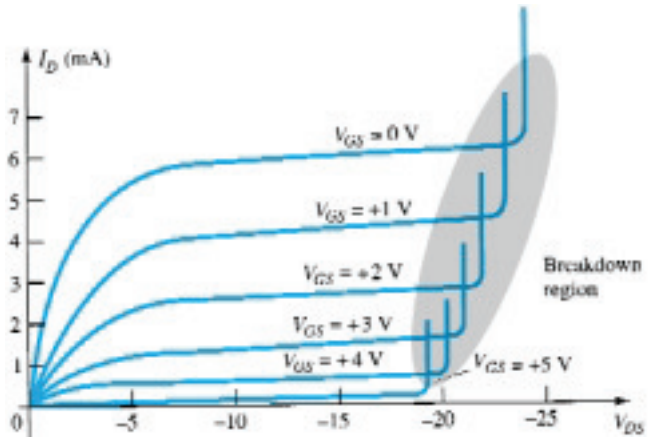


Figure 5.12 *p*-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_P = +6$ V.

Note at high levels of V_{DS} that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel (in the same direction as normally encountered) is now limited solely by the external circuit. Although not appearing in Fig. 5.10 for the *n*-channel device, they do occur for the *n*-channel device if sufficient voltage is applied. This region can be avoided if the level of $V_{DS_{max}}$ is noted on the specification sheet and the design is such that the actual level of V_{DS} is less than this value for *all* values of V_{GS}.

Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 5.13. Note that the arrow is pointing in for the *n*-channel device of Fig. 5.13a to represent the direction in which I_G would flow if the *p*-*n* junction were forward-biased. For the *p*-channel device (Fig. 5.13b) the only difference in the symbol is the direction of the arrow.

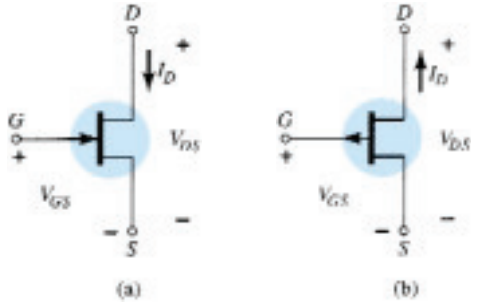


Figure 5.13 JFET symbols: (a) *n*-channel; (b) *p*-channel.

Summary

A number of important parameters and relationships were introduced in this section. A few that will surface frequently in the analysis to follow in this chapter and the next for *n*-channel JFETs include the following:

The maximum current is defined as I_{DSS} and occurs when $V_{GS} = 0$ V and $V_{DS} \geq |V_P|$ as shown in Fig. 5.14a.

For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A ($I_D = 0$ A) as appearing in Fig. 5.14b.

For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as reviewed by Fig. 5.14c.

For p-channel JFETs a similar list can be developed.

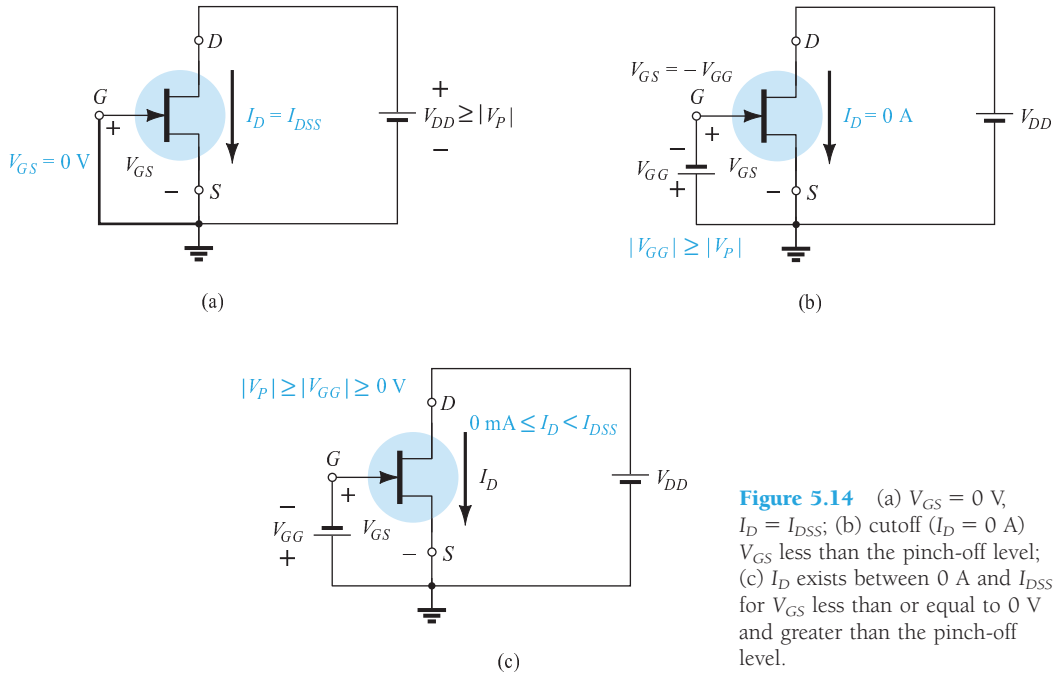


Figure 5.14 (a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D exists between 0 A and I_{DSS} for V_{GS} less than or equal to 0 V and greater than the pinch-off level.

5.3 TRANSFER CHARACTERISTICS

Derivation

For the BJT transistor the output current I_C and input controlling current I_B were related by beta, which was considered constant for the analysis to be performed. In equation form,

$$I_C = f(I_B) = \beta I_B \qquad (5.2)$$

(control variable; constant)

In Eq. (5.2) a linear relationship exists between I_C and I_B. Double the level of I_B and I_C will increase by a factor of two also.

Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by *Shockley's equation:*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (5.3)$$

(control variable; constants)

The squared term of the equation will result in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}.

For the dc analysis to be performed in Chapter 6, a graphical rather than mathematical approach will in general be more direct and easier to apply. The graphical approach, however, will require a plot of Eq. (5.3) to represent the device and a plot of the network equation relating the same variables. The solution is defined by the point of intersection of the two curves. It is important to keep in mind when applying the graphical approach that the device characteristics will be *unaffected* by the network in which the device is employed. The network equation may change along with the intersection between the two curves, but the transfer curve defined by Eq. (5.3) is unaffected. In general, therefore:

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

The transfer curve can be obtained using Shockley's equation or from the output characteristics of Fig. 5.10. In Fig. 5.15 two graphs are provided, with the vertical

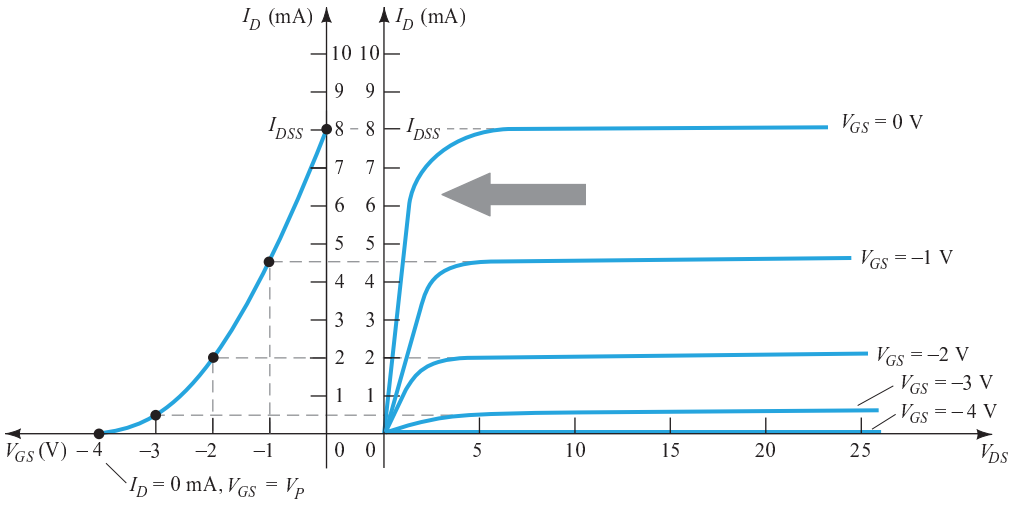
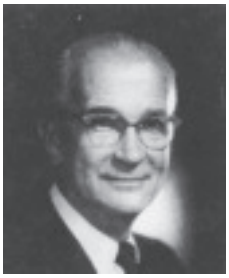


Figure 5.15 Obtaining the transfer curve from the drain characteristics.



William Bradford Shockley (1910–1989), co-inventor of the first transistor and formulator of the "field-effect" theory employed in the development of the transistor and FET. (Courtesy of AT&T Archives.)

Born: London, England
PhD Harvard, 1936
Head, Transistor Physics Department–Bell Laboratories
President, Shockley Transistor Corp.
Poniatoff Professor of Engineering Science at Stanford University
Nobel Prize in physics in 1956 with Drs. Brattain and Bardeen

scaling in milliamperes for each graph. One is a plot of I_D versus V_{DS}, while the other is I_D versus V_{GS}. Using the drain characteristics on the right of the "y" axis, a horizontal line can be drawn from the saturation region of the curve denoted $V_{GS} = 0$ V to the I_D axis. The resulting current level for both graphs is I_{DSS}. The point of intersection on the I_D versus V_{GS} curve will be as shown since the vertical axis is defined as $V_{GS} = 0$ V.

In review:

When $V_{GS} = 0$ V, $I_D = I_{DSS}$.

When $V_{GS} = V_P = -4$ V, the drain current is zero milliamperes, defining another point on the transfer curve. That is:

When $V_{GS} = V_P$, $I_D = 0$ mA.

Before continuing, it is important to realize that the drain characteristics relate one output (or drain) quantity to another output (or drain) quantity—both axes are defined by variables in the same region of the device characteristics. The transfer characteristics are a plot of an output (or drain) current versus an input-controlling quantity. There is therefore a direct "transfer" from input to output variables when employing the curve to the left of Fig. 5.15. If the relationship were linear, the plot of I_D versus V_{GS} would result in a straight line between I_{DSS} and V_P. However, a parabolic curve will result because the vertical spacing between steps of V_{GS} on the drain characteristics of Fig. 5.15 decreases noticeably as V_{GS} becomes more and more negative. Compare the spacing between $V_{GS} = 0$ V and $V_{GS} = -1$ V to that between $V_{GS} = -3$ V and pinch-off. The change in V_{GS} is the same, but the resulting change in I_D is quite different.

If a horizontal line is drawn from the $V_{GS} = -1$ V curve to the I_D axis and then extended to the other axis, another point on the transfer curve can be located. Note that $V_{GS} = -1$ V on the bottom axis of the transfer curve with $I_D = 4.5$ mA. Note in the definition of I_D at $V_{GS} = 0$ V and -1 V that the saturation levels of I_D are employed and the ohmic region ignored. Continuing with $V_{GS} = -2$ V and -3 V, the transfer curve can be completed. It is the transfer curve of I_D versus V_{GS} that will receive extended use in the analysis of Chapter 6 and not the drain characteristics of Fig. 5.15. The next few paragraphs will introduce a quick, efficient method of plotting I_D versus V_{GS} given only the levels of I_{DSS} and V_P and Shockley's equation.

Applying Shockley's Equation

The transfer curve of Fig. 5.15 can also be obtained directly from Shockley's equation (5.3) given simply the values of I_{DSS} and V_P. The levels of I_{DSS} and V_P define the limits of the curve on both axes and leave only the necessity of finding a few intermediate plot points. The validity of Eq. (5.3) as a source of the transfer curve of Fig. 5.15 is best demonstrated by examining a few specific levels of one variable and finding the resulting level of the other as follows:

Substituting $V_{GS} = 0$ V gives

$$\text{Eq. (5.3):} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}(1 - 0)^2$$

and

$$\boxed{I_D = I_{DSS}\,\big|_{V_{GS} = 0\text{ V}}} \tag{5.4}$$

Substituting $V_{GS} = V_P$ yields

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$
$$= I_{DSS}(1 - 1)^2 = I_{DSS}(0)$$
$$\boxed{I_D = 0\ \text{A}\big|_{V_{GS} = V_P}} \tag{5.5}$$

For the drain characteristics of Fig. 5.15, if we substitute $V_{GS} = -1$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= 8\ \text{mA}\left(1 - \frac{-1\ \text{V}}{-4\ \text{V}}\right)^2 = 8\ \text{mA}\left(1 - \frac{1}{4}\right)^2 = 8\ \text{mA}(0.75)^2$$
$$= 8\ \text{mA}(0.5625)$$
$$\mathbf{= 4.5\ mA}$$

as shown in Fig. 5.15. Note the care taken with the negative signs for V_{GS} and V_P in the calculations above. The loss of one sign would result in a totally erroneous result.

It should be obvious from the above that given I_{DSS} and V_P (as is normally provided on specification sheets) the level of I_D can be found for any level of V_{GS}. Conversely, by using basic algebra we can obtain [from Eq. (5.3)] an equation for the resulting level of V_{GS} for a given level of I_D. The derivation is quite straight forward and will result in

$$\boxed{V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)} \tag{5.6}$$

Let us test Eq. (5.6) by finding the level of V_{GS} that will result in a drain current of 4.5 mA for the device with the characteristics of Fig. 5.15.

$$V_{GS} = -4\ \text{V}\left(1 - \sqrt{\frac{4.5\ \text{mA}}{8\ \text{mA}}}\right)$$
$$= -4\ \text{V}(1 - \sqrt{0.5625}) = -4\ \text{V}(1 - 0.75)$$
$$= -4\ \text{V}(0.25)$$
$$\mathbf{= -1\ V}$$

as substituted in the above calculation and verified by Fig. 5.15.

Shorthand Method

Since the transfer curve must be plotted so frequently, it would be quite advantageous to have a shorthand method for plotting the curve in the quickest, most efficient manner while maintaining an acceptable degree of accuracy. The format of Eq. (5.3) is such that specific levels of V_{GS} will result in levels of I_D that can be memorized to provide the plot points needed to sketch the transfer curve. If we specify V_{GS} to be one-half the pinch-off value V_P, the resulting level of I_D will be the following, as determined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$
$$= I_{DSS}(0.25)$$

and
$$I_D = \frac{I_{DSS}}{4}\bigg|_{V_{GS} = V_P/2} \tag{5.7}$$

Now it is important to realize that Eq. (5.7) is not for a particular level of V_P. It is a general equation for any level of V_P as long as $V_{GS} = V_P/2$. The result specifies that the drain current will always be one-fourth of the saturation level I_{DSS} as long as the gate-to-source voltage is one-half the pinch-off value. Note the level of I_D for $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$ in Fig. 5.15.

If we choose $I_D = I_{DSS}/2$ and substitute into Eq. (5.6), we find that

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

and
$$V_{GS} \cong 0.3V_P\big|_{I_D = I_{DSS}/2} \tag{5.8}$$

Additional points can be determined, but the transfer curve can be sketched to a satisfactory level of accuracy simply using the four plot points defined above and reviewed in Table 5.1. In fact, in the analysis of Chapter 6, a maximum of four plot points are used to sketch the transfer curves. On most occasions using just the plot point defined by $V_{GS} = V_P/2$ and the axis intersections at I_{DSS} and V_P will provide a curve accurate enough for most calculations.

TABLE 5.1 V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
0.3 V_P	$I_{DSS}/2$
0.5 V_P	$I_{DSS}/4$
V_P	0 *mA*

EXAMPLE 5.1 Sketch the transfer curve defined by $I_{DSS} = 12$ mA and $V_P = -6$ V.

Solution

Two plot points are defined by

$$I_{DSS} = \mathbf{12\text{ mA}} \quad \text{and} \quad V_{GS} = \mathbf{0\text{ V}}$$

and
$$I_D = \mathbf{0\text{ mA}} \quad \text{and} \quad V_{GS} = \boldsymbol{V_P}$$

At $V_{GS} = V_P/2 = -6\text{ V}/2 = \mathbf{-3\text{ V}}$ the drain current will be determined by $I_D = I_{DSS}/4 = 12\text{ mA}/4 = \mathbf{3\text{ mA}}$. At $I_D = I_{DSS}/2 = 12\text{ mA}/2 = \mathbf{6\text{ mA}}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\text{ V}) = \mathbf{-1.8\text{ V}}$. All four plot points are well defined on Fig. 5.16 with the complete transfer curve.

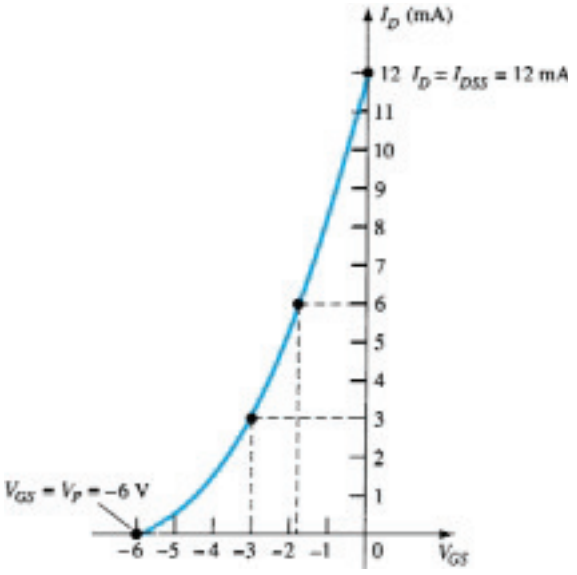


Figure 5.16 Transfer curve for Example 5.1.

For *p*-channel devices Shockley's equation (5.3) can still be applied exactly as it appears. In this case, both V_P and V_{GS} will be positive and the curve will be the mirror image of the transfer curve obtained with an *n*-channel and the same limiting values.

EXAMPLE 5.2

Sketch the transfer curve for a *p*-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

Solution

At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\text{ V}}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\text{ mA}}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\text{ mA}}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\text{ V}}$. Both plot points appear in Fig. 5.17 along with the points defined by I_{DSS} and V_P.

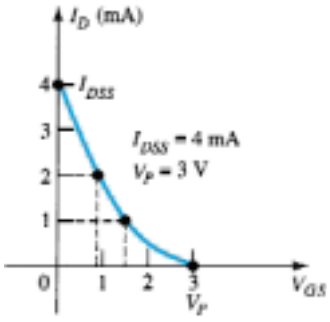


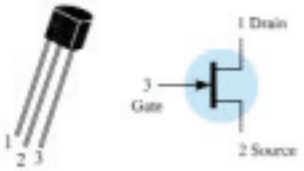
Figure 5.17 Transfer curve for the *p*-channel device of Example 5.2.

5.4 SPECIFICATION SHEETS (JFETs)

Although the general content of specification sheets may vary from the absolute minimum to an extensive display of graphs and charts, there are a few fundamental parameters that will be provided by all manufacturers. A few of the most important are discussed in the following paragraphs. The specification sheet for the 2N5457 *n*-channel JFET as provided by Motorola is provided as Fig. 5.18.

2N5457

CASE 29-04, STYLE 5
TO-92 (TO-226AA)



JFETs
GENERAL PURPOSE
N-CHANNEL—DEPLETION

Refer to 2N4220 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	-25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = -10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	-25	–	–	Vdc
Gate Reverse Current (V_{GS} = -15 Vdc, V_{DS} = 0) (V_{GS} = -15 Vdc, V_{DS} = 0, T_A = 100°C)		I_{GSS}	– –	– –	-1.0 -200	nAdc
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	-0.5	–	-6.0	Vdc
Gate Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc)	2N5457	V_{GS}	–	-2.5	–	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5457	$\|Y_{fs}\|$	1000	–	5000	μmhos
Output Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|Y_{os}\|$	–	10	50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	3.0	pF

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

Figure 5.18 2N5457 Motorola *n*-channel JFET.

Maximum Ratings

The maximum rating list usually appears at the beginning of the specification sheet, with the maximum voltages between specific terminals, maximum current levels, and the maximum power dissipation level of the device. The specified maximum levels for V_{DS} and V_{DG} must not be exceeded at any point in the design operation of the device. The applied source V_{DD} can exceed these levels, but the actual level of voltage between these terminals must never exceed the level specified. Any good design will

try to avoid these levels by a good margin of safety. The term *reverse* in V_{GSR} defines the maximum voltage with the source positive with respect to the gate (as normally biased for an *n*-channel device) before breakdown will occur. On some specification sheets it is referred to as BV_{DSS}—the *B*reakdown *V*oltage with the *D*rain-*S*ource *S*horted ($V_{DS} = 0$ V). Although normally designed to operate with $I_G = 0$ mA, if *forced* to accept a gate current it could withstand 10 mA before damage would occur. The total device dissipation at 25°C (room temperature) is the maximum power the device can dissipate under normal operating conditions and is defined by

$$P_D = V_{DS}I_D \tag{5.9}$$

Note the similarity in format with the maximum power dissipation equation for the BJT transistor.

The derating factor is discussed in detail in Chapter 3, but for the moment recognize that the 2.82 mW/°C rating reveals that the dissipation rating *decreases* by 2.82 mW for each *increase* in temperature of 1°C above 25°C.

Electrical Characteristics

The electrical characteristics include the level of V_P in the OFF CHARACTERISTICS and I_{DSS} in the ON CHARACTERISTICS. In this case $V_P = V_{GS(\text{off})}$ has a range from -0.5 to -6.0 V and I_{DSS} from 1 to 5 mA. The fact that both will vary from device to device with the same nameplate identification must be considered in the design process. The other quantities are defined under conditions appearing in parentheses. The small-signal characteristics are discussed in Chapter 9.

Case Construction and Terminal Identification

This particular JFET has the appearance provided on the specification sheet of Fig. 5.18. The terminal identification is also provided directly under the figure. JFETs are also available in top-hat containers, as shown in Fig. 5.19 with its terminal identification.

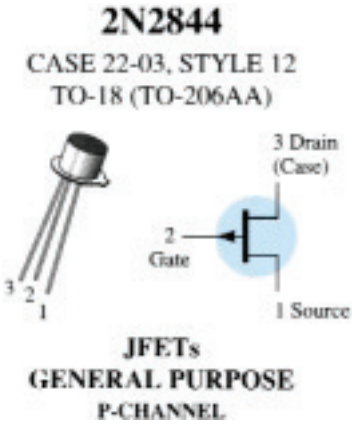


Figure 5.19 Top-hat container and terminal identification for a *p*-channel JFET.

Operating Region

The specification sheet and the curve defined by the pinch-off levels at each level of V_{GS} define the region of operation for linear amplification on the drain characteristics as shown in Fig. 5.20. The ohmic region defines the minimum permissible values of V_{DS} at each level of V_{GS}, and $V_{DS_{\max}}$ specifies the maximum value for this pa-

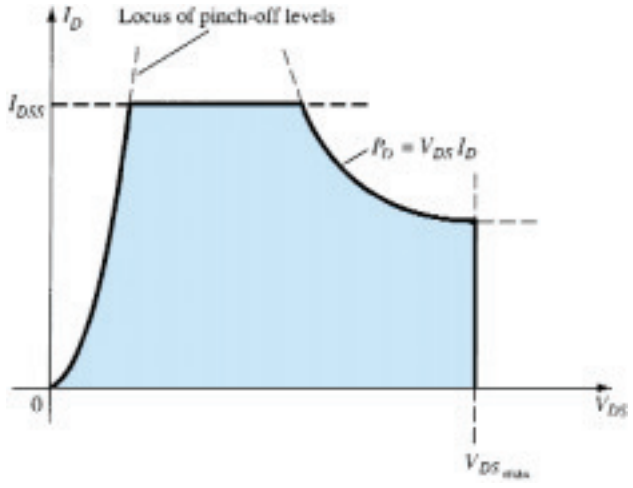


Figure 5.20 Normal operating region for linear amplifier design.

rameter. The saturation current I_{DSS} is the maximum drain current, and the maximum power dissipation level defines the curve drawn in the same manner as described for BJT transistors. The resulting shaded region is the normal operating region for amplifier design.

5.5 INSTRUMENTATION

Recall from Chapter 3 that hand-held instruments are available to measure the level of β_{dc} for the BJT transistor. Similar instrumentation is not available to measure the levels of I_{DSS} and V_P. However, the curve tracer introduced for the BJT transistor can also display the drain characteristics of the JFET transistor through a proper setting of the various controls. The vertical scale (in milliamperes) and the horizontal scale (in volts) have been set to provide a full display of the characteristics, as shown in Fig. 5.21. For the JFET of Fig. 5.21, each vertical division (in centimeters) reflects a 1-mA change in I_C while each horizontal division has a value of 1 V. The step voltage is 500 mV/step (0.5 V/step), revealing that the top curve is defined by $V_{GS} = 0$ V and the next curve down -0.5 V for the *n*-channel device. Using the same step voltage the next curve is -1 V, then -1.5 V, and finally -2 V. By drawing a line from the top curve over to the I_D axis, the level of I_{DSS} can be estimated to be about 9 mA. The level of V_P can be estimated by noting the V_{GS} value of the bottom curve and taking into account the shrinking distance between curves as V_{GS} becomes more and more negative. In this case, V_P is certainly more negative than -2 V and perhaps V_P is close to -2.5 V. However, keep in mind that the V_{GS} curves contract very quickly as they approach the cutoff condition, and perhaps $V_P = -3$ V is a better choice. It

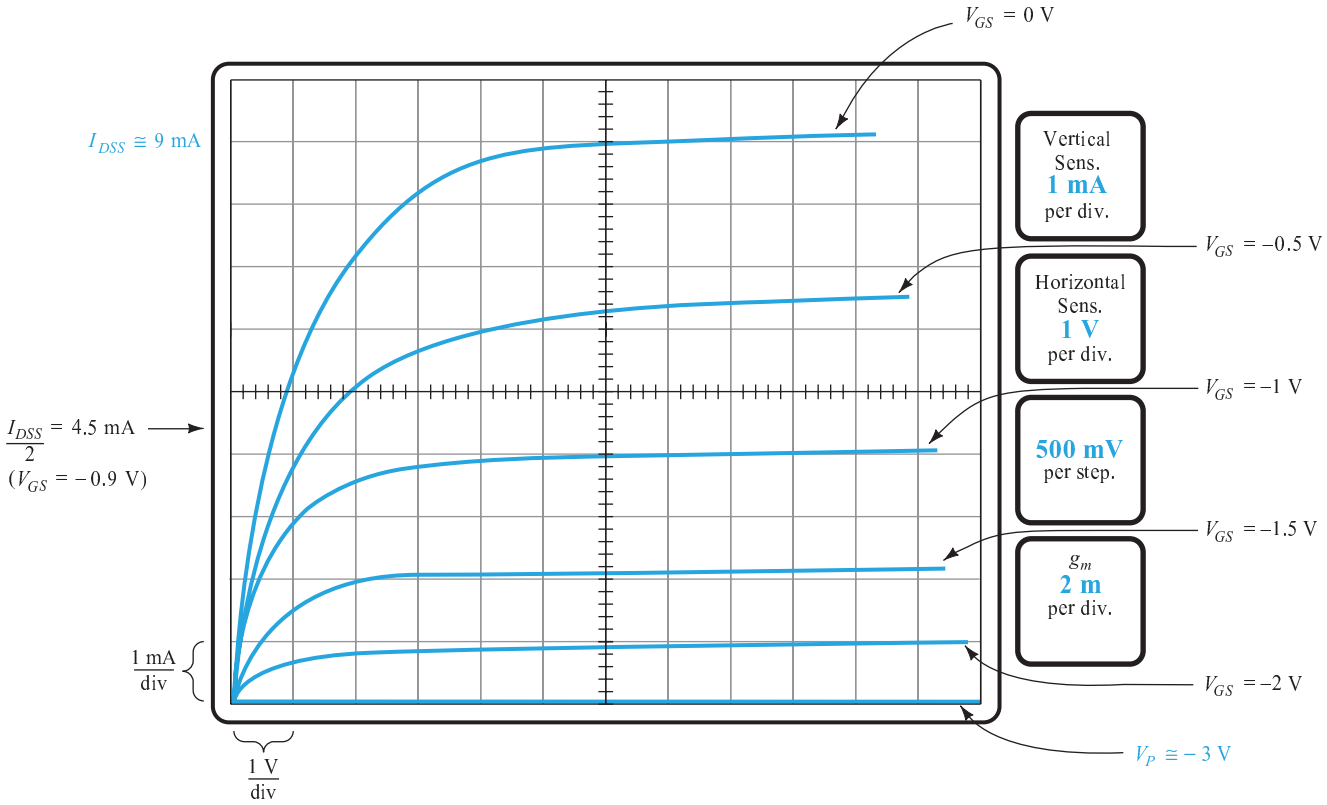


Figure 5.21 Drain characteristics for a 2N4416 JFET transistor as displayed on a curve tracer.

should also be noted that the step control is set for a 5-step display, limiting the displayed curves to $V_{GS} = 0, -0.5, -1, -1.5$, and -2 V. If the step control had been increased to 10, the voltage per step could be reduced to 250 mV = 0.25 V and the curve for $V_{GS} = -2.25$ V would have been included as well as an additional curve between each step of Fig. 5.21. The $V_{GS} = -2.25$ V curve would reveal how quickly the curves are closing in on each other for the same step voltage. Fortunately, the level of V_P can be estimated to a reasonable degree of accuracy simply by applying a condition appearing in Table 5.1. That is, when $I_D = I_{DSS}/2$, then $V_{GS} = 0.3V_P$. For the characteristics of Fig. 5.21, $I_D = I_{DSS}/2 = 9$ mA/2 = 4.5 mA, and as visible from Fig. 5.21 the corresponding level of V_{GS} is about -0.9 V. Using this information we find that $V_P = V_{GS}/0.3 = -0.9$ V/0.3 $= -3$ V, which will be our choice for this device. Using this value we find that at $V_{GS} = -2$ V,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 9 \text{ mA}\left(1 - \frac{-2 \text{ V}}{-3 \text{ V}}\right)^2$$

$$\cong 1 \text{ mA}$$

as supported by Fig. 5.21.

At $V_{GS} = -2.5$ V, Shockley's equation will result in $I_D = 0.25$ mA, with $V_P = -3$ V clearly revealing how quickly the curves contract near V_P. The importance of the parameter g_m and how it is determined from the characteristics of Fig. 5.21 are described in Chapter 8 when small-signal ac conditions are examined.

5.6 IMPORTANT RELATIONSHIPS

A number of important equations and operating characteristics have been introduced in the last few sections that are of particular importance for the analysis to follow for the dc and ac configurations. In an effort to isolate and emphasize their importance, they are repeated below next to a corresponding equation for the BJT transistor. The JFET equations are defined for the configuration of Fig. 5.22a, while the BJT equations relate to Fig. 5.22b.

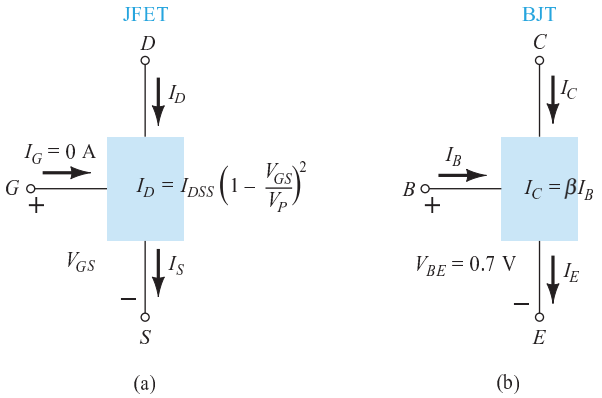


Figure 5.22 (a) JFET versus (b) BJT.

JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

(5.10)

A clear understanding of the impact of each of the equations above is sufficient background to approach the most complex of dc configurations. Recall that $V_{BE} = 0.7$ V was often the key to initiating an analysis of a BJT configuration. Similarly, the condition $I_G = 0$ A is often the starting point for the analysis of a JFET configuration. For the BJT configuration, I_B is normally the first parameter to be determined. For the JFET, it is normally V_{GS}. The number of similarities between the analysis of BJT and JFET dc configurations will become quite apparent in Chapter 6.

5.7 DEPLETION-TYPE MOSFET

As noted in the chapter introduction, there are two types of FETs: JFETs and MOSFETs. MOSFETs are further broken down into *depletion type* and *enhancement type*. The terms *depletion* and *enhancement* define their basic mode of operation, while the label MOSFET stands for *m*etal-*o*xide-*s*emiconductor-*f*ield-*e*ffect *t*ransistor. Since there are differences in the characteristics and operation of each type of MOSFET, they are covered in separate sections. In this section we examine the depletion-type MOSFET, which happens to have characteristics similar to those of a JFET between cutoff and saturation at I_{DSS} but then has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 5.23. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation upon which the device will be constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device, such as that appearing in Fig. 5.23. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a *dielectric* that sets up opposing (as revealed by

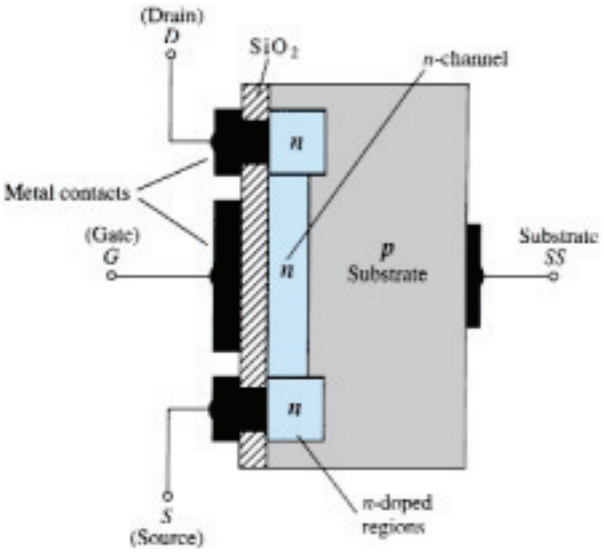


Figure 5.23 *n*-Channel depletion-type MOSFET.

the prefix *di-*) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer reveals the following fact:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

In addition:

It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is often that of the typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. The very high input impedance continues to fully support the fact that the gate current (I_G) is essentially zero amperes for dc-biased configurations.

The reason for the label metal-oxide-semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the *oxide* for the silicon dioxide insulating layer, and the *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and channel has resulted in another name for the device: *insulated-gate FET* or *IGFET,* although this label is used less and less in current literature.

Basic Operation and Characteristics

In Fig. 5.24 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the *free* electrons of the *n*-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS}, as shown in Fig. 5.25.

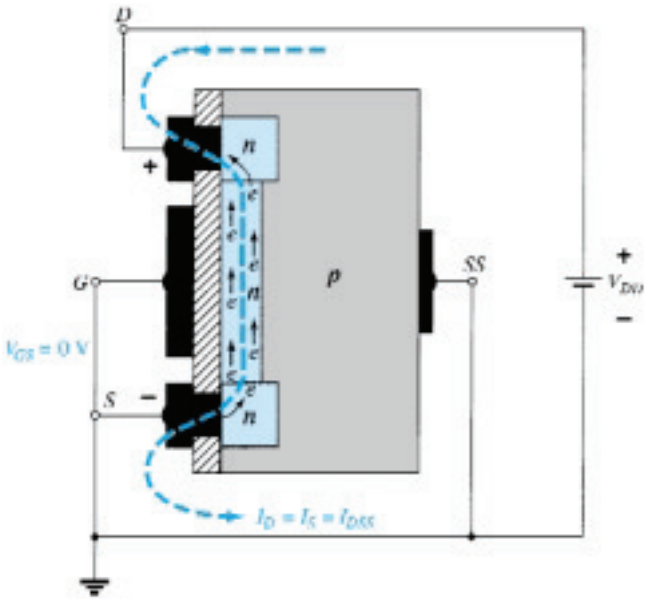


Figure 5.24 *n*-Channel depletion-type MOSFET with $V_{GS} = 0$ V and an applied voltage V_{DD}.

I_{DDS}/V_P

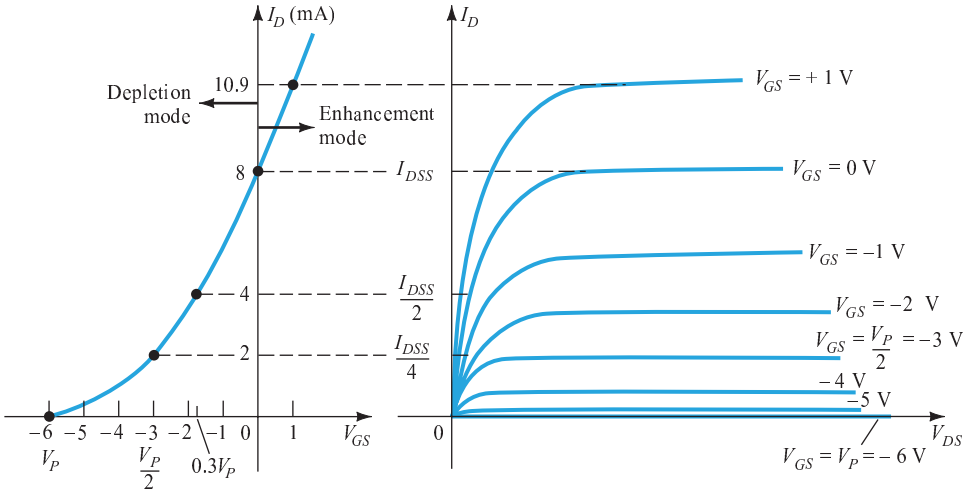


Figure 5.25 Drain and transfer characteristics for an *n*-channel depletion-type MOSFET.

In Fig. 5.26, V_{GS} has been set at a negative voltage such as -1 V. The negative potential at the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 5.26. Depending on the magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} as shown in Fig. 5.25 for $V_{GS} = -1$ V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceeds exactly as described for the JFET.

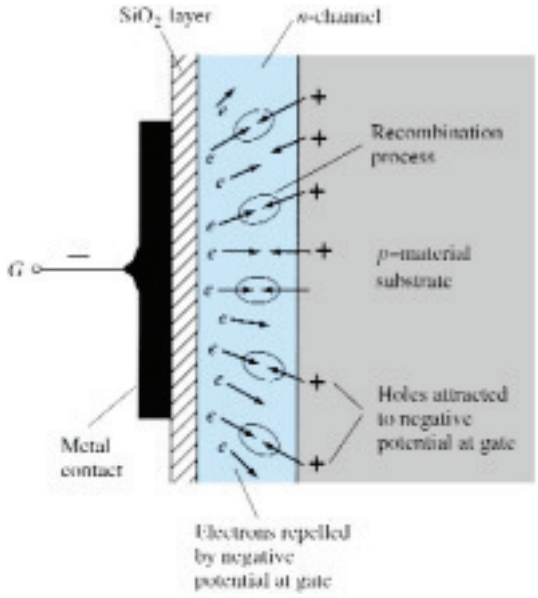


Figure 5.26 Reduction in free carriers in channel due to a negative potential at the gate terminal.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 5.25 reveals that the drain current will increase at a rapid rate for the reasons listed above. The

vertical spacing between the $V_{GS} = 0$ V and $V_{GS} = +1$ V curves of Fig. 5.25 is a clear indication of how much the current has increased for the 1-V change in V_{GS}. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 5.25, the application of a voltage $V_{GS} = +4$ V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region,* with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region.*

It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.

EXAMPLE 5.3

Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Solution

$$\text{At } V_{GS} = 0 \text{ V}, \qquad I_D = I_{DSS} = 10 \text{ mA}$$

$$V_{GS} = V_P = -4 \text{ V}, \qquad I_D = 0 \text{ mA}$$

$$V_{GS} = \frac{V_P}{2} = \frac{-4 \text{ V}}{2} = -2 \text{ V}, \qquad I_D = \frac{I_{DSS}}{4} = \frac{10 \text{ mA}}{4} = 2.5 \text{ mA}$$

and at $I_D = \dfrac{I_{DSS}}{2}$, $\qquad V_{GS} = 0.3V_P = 0.3(-4 \text{ V}) = -1.2 \text{ V}$

all of which appear in Fig. 5.27.

Before plotting the positive region of V_{GS}, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we will try +1 V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10 \text{ mA}\left(1 - \frac{+1 \text{ V}}{-4 \text{ V}}\right)^2 = 10 \text{ mA}(1 + 0.25)^2 = 10 \text{ mA}(1.5625)$$

$$\cong 15.63 \text{ mA}$$

which is sufficiently high to finish the plot.

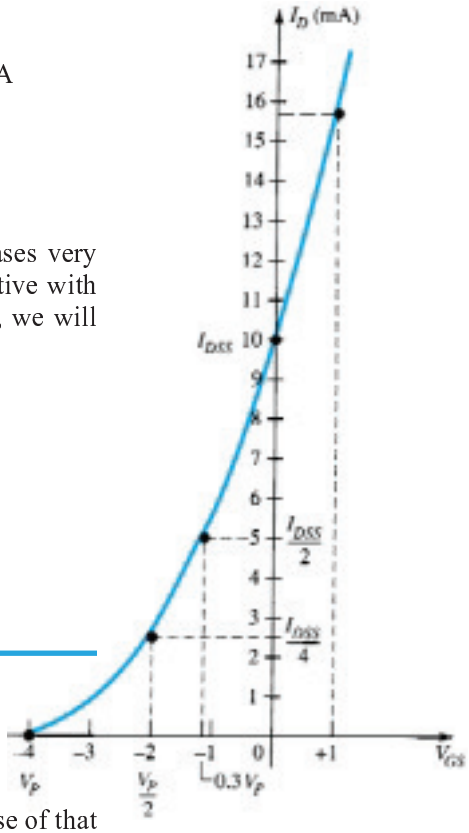


Figure 5.27 Transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

p-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 5.23. That is, there is now an *n*-type substrate and a *p*-type channel, as shown in Fig. 5.28a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 5.25 but with V_{DS} having negative val-

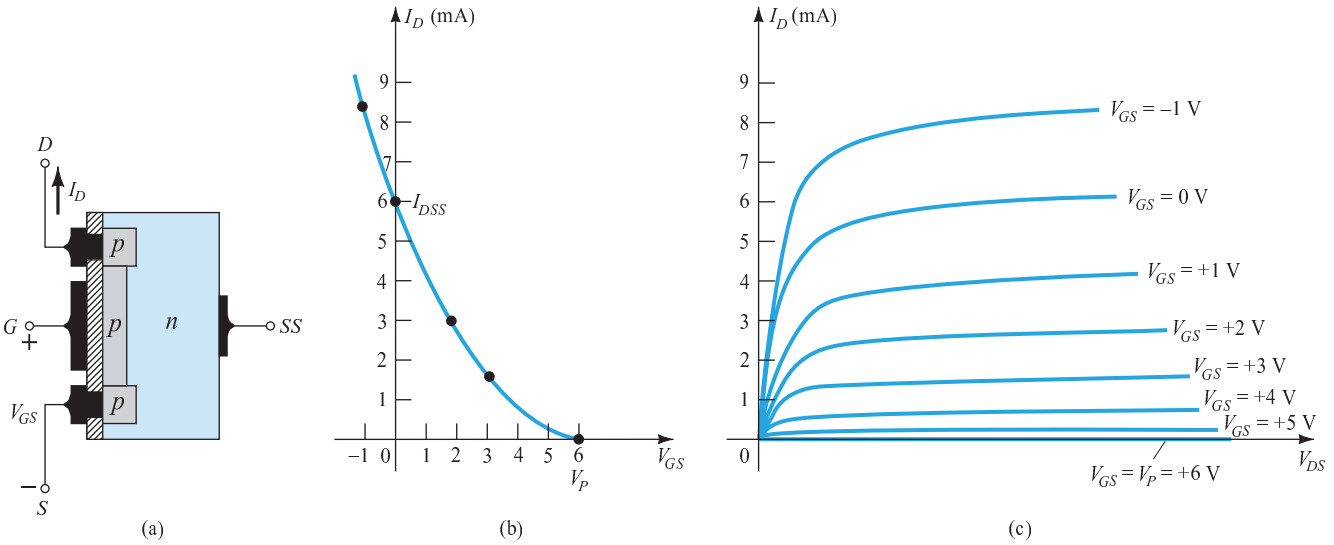


Figure 5.28 *p*-Channel depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = +6$ V.

ues, I_D having positive values as indicated (since the defined direction is now reversed), and V_{GS} having the opposite polarities as shown in Fig. 5.28c. The reversal in V_{GS} will result in a mirror image (about the I_D axis) for the transfer characteristics as shown in Fig. 5.28b. In other words, the drain current will increase from cutoff at $V_{GS} = V_P$ in the positive V_{GS} region to I_{DSS} and then continue to increase for increasingly negative values of V_{GS}. Shockley's equation is still applicable and requires simply placing the correct sign for both V_{GS} and V_P in the equation.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for an *n*- and *p*-channel depletion-type MOSFET are provided in Fig. 5.29. Note how the symbols chosen try to reflect the actual construction of the device. The lack of a direct connection (due to the gate insulation) between the gate and channel is represented by a space between the gate and the other terminals of the symbol. The vertical line representing the channel is connected between the drain and source and is "supported" by the substrate. Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available while in others it is not. For most of the analysis to follow in Chapter 6, the substrate and source will be connected and the lower symbols will be employed.

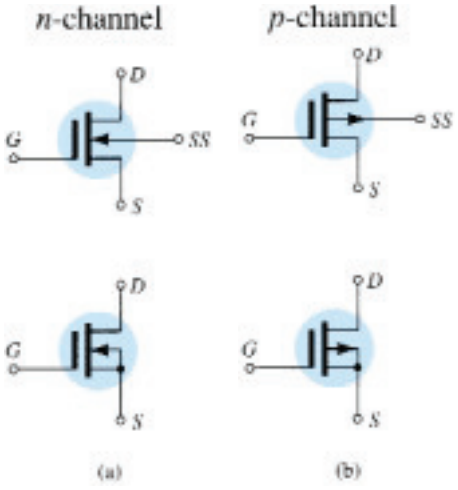


Figure 5.29 Graphic symbols for (a) *n*-channel depletion-type MOSFETs and (b) *p*-channel depletion-type MOSFETs.

The device appearing in Fig. 5.30 has three terminals, with the terminal identification appearing in the same figure. The specification sheet for a depletion-type MOSFET is similar to that of a JFET. The levels of V_P and I_{DSS} are provided along with a list of maximum values and typical "on" and "off" characteristics. In addition, how-

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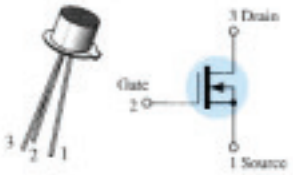


MOSFETs
LOW POWER AUDIO

N-CHANNEL – DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage 2N3797	V_{DS}	20	Vdc
Gate–Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{stg}	–65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain Source Breakdown Voltage (V_{GS} = –7.0 V, I_D = 5.0 µA)	2N3797	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) (V_{GS} = –10 V, V_{DS} = 0) (V_{GS} = –10 V, V_{DS} = 0, T_A = 150°C)		I_{GSS}	– –	– –	1.0 200	pAdc
Gate Source Cutoff Voltage (I_D = 2.0 µA, V_{DS} = 10 V)	2N3797	$V_{GS(off)}$	–	–5.0	–7.0	Vdc
Drain-Gate Reverse Current (1) (V_{DG} = 10 V, I_S = 0)		I_{DGO}	–	–	1.0	pAdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0)	2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current (V_{DS} = 10 V, V_{GS} = +3.5 V)	2N3797	$I_{D(on)}$	9.0	14	18	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\|Y_{fs}\|$	1500	2300	3000	µmhos
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797		1500	–	–	
Output Admittance (I_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3797	$\|Y_{os}\|$	–	27	60	µmhos
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3797	C_{iss}	–	6.0	8.0	pF
Reverse Transfer Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	0.5	0.8	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz, R_S = 3 megohms)		NF	–	3.8	–	dB

(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

Figure 5.30 2N3797 Motorola *n*-channel depletion-type MOSFET.

ever, since I_D can extend beyond the I_{DSS} level, another point is normally provided that reflects a typical value of I_D for some positive voltage (for an *n*-channel device). For the unit of Fig. 5.30, I_D is specified as $I_{D(on)} = 9$ mA dc, with $V_{DS} = 10$ V and $V_{GS} = 3.5$ V.

5.8 ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an *n*-channel device is now effected by a positive gate-to-source voltage rather than the range of negative voltages encountered for *n*-channel JFETs and *n*-channel depletion-type MOSFETs.

Basic Construction

The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 5.31. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 5.31 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material. In summary, therefore, the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

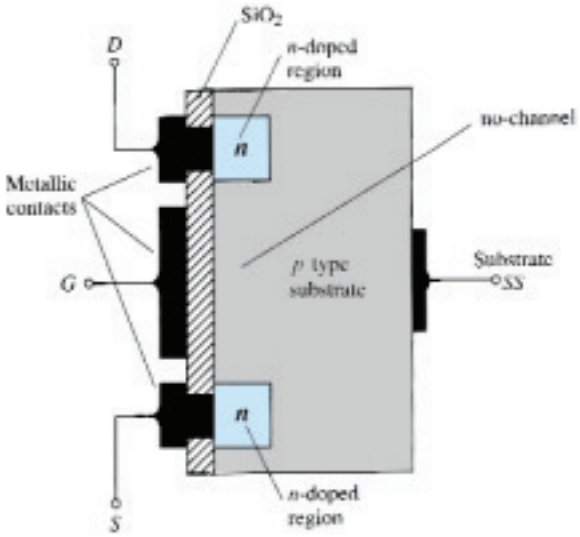


Figure 5.31 *n*-Channel enhancement-type MOSFET.

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 5.31, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion-type MOSFET and JFET where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the *n*-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p*-*n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source.

In Fig. 5.32 both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the *p*-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced *n*-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET*. Both depletion- and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

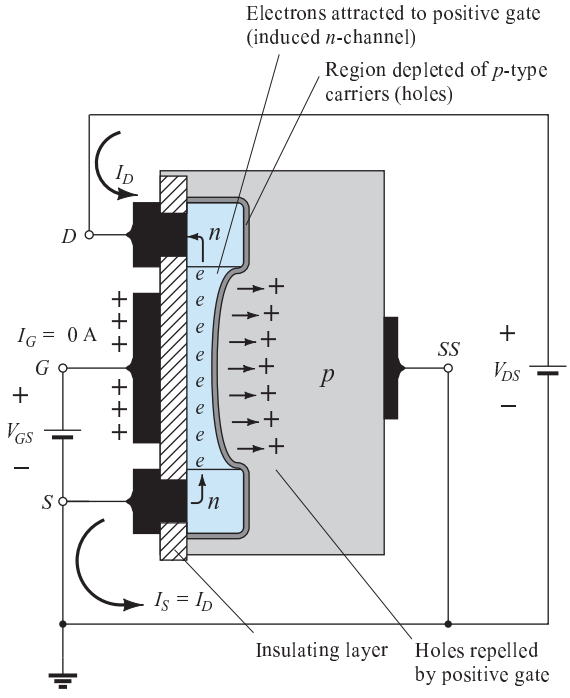


Figure 5.32 Channel formation in the *n*-channel enhancement-type MOSFET.

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 5.33. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 5.33, we find that

$$V_{DG} = V_{DS} - V_{GS} \tag{5.11}$$

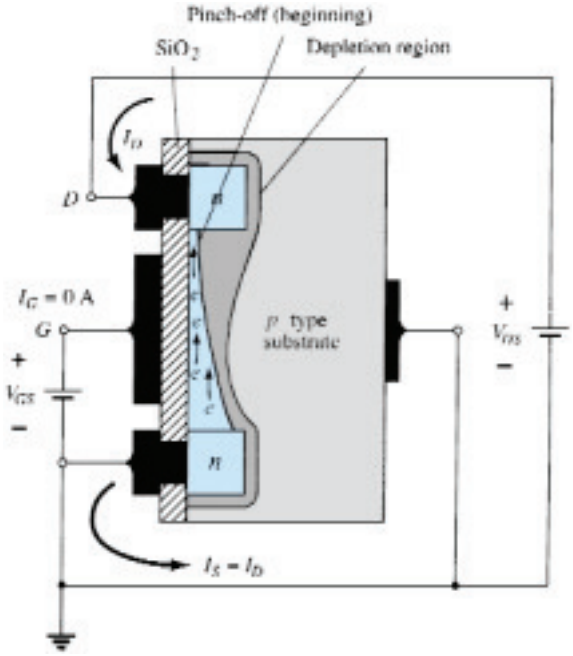


Figure 5.33 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}.

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 to 5 V, the voltage V_{DG} [by Eq. (5.11)] will drop from -6 to -3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established as described earlier for the JFET and depletion-type MOSFET. In other words, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered.

The drain characteristics of Fig. 5.34 reveal that for the device of Fig. 5.33 with $V_{GS} = 8$ V, saturation occurred at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$V_{DS_{\text{sat}}} = V_{GS} - V_T \tag{5.12}$$

Obviously, therefore, for a fixed value of V_T, then the higher the level of V_{GS}, the more the saturation level for V_{DS}, as shown in Fig. 5.33 by the locus of saturation levels.

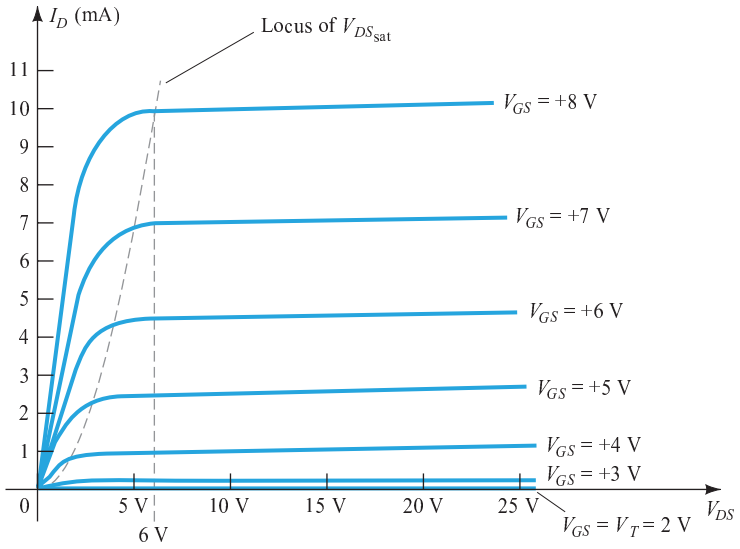


Figure 5.34 Drain characteristics of an *n*-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

For the characteristics of Fig. 5.33 the level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA. In general, therefore:

For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

Figure 5.34 clearly reveals that as the level of V_{GS} increased from V_T to 8 V, the resulting saturation level for I_D also increased from a level of 0 to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increased as the magnitude of V_{GS} increased, resulting in ever-increasing increments in drain current.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$I_D = k(V_{GS} - V_T)^2 \tag{5.13}$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (5.13)] where $I_{D(on)}$ and $V_{GS(on)}$ are the values for each at a particular point on the characteristics of the device.

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \tag{5.14}$$

Substituting $I_{D(on)} = 10$ mA when $V_{GS(on)} = 8$ V from the characteristics of Fig. 5.34 yields

$$k = \frac{10 \text{ mA}}{(8 \text{ V} - 2 \text{ V})^2} = \frac{10 \text{ mA}}{(6 \text{ V})^2} = \frac{10 \text{ mA}}{36 \text{ V}^2}$$
$$= \mathbf{0.278 \times 10^{-3} \text{ A/V}^2}$$

and a general equation for I_D for the characteristics of Fig. 5.34 results in:

$$I_D = 0.278 \times 10^{-3}(V_{GS} - 2 \text{ V})^2$$

Substituting $V_{GS} = 4$ V, we find that

$$I_D = 0.278 \times 10^{-3}(4\text{ V} - 2\text{ V})^2 = 0.278 \times 10^{-3}(2)^2$$
$$= 0.278 \times 10^{-3}(4) = \mathbf{1.11\ mA}$$

as verified by Fig. 5.34. At $V_{GS} = V_T$, the squared term is 0 and $I_D = 0$ mA.

For the dc analysis of enhancement-type MOSFETs to appear in Chapter 6, the transfer characteristics will again be the characteristics to be employed in the graphical solution. In Fig. 5.35 the drain and transfer characteristics have been set side by side to describe the transfer process from one to the other. Essentially, it proceeds as introduced earlier for the JFET and depletion-type MOSFETs. In this case, however, it must be remembered that the drain current is 0 mA for $V_{GS} \leq V_T$. At this point a measurable current will result for I_D and will increase as defined by Eq. (5.13). Note that in defining the points on the transfer characteristics from the drain characteristics, only the saturation levels are employed, thereby limiting the region of operation to levels of V_{DS} greater than the saturation levels as defined by Eq. (5.12).

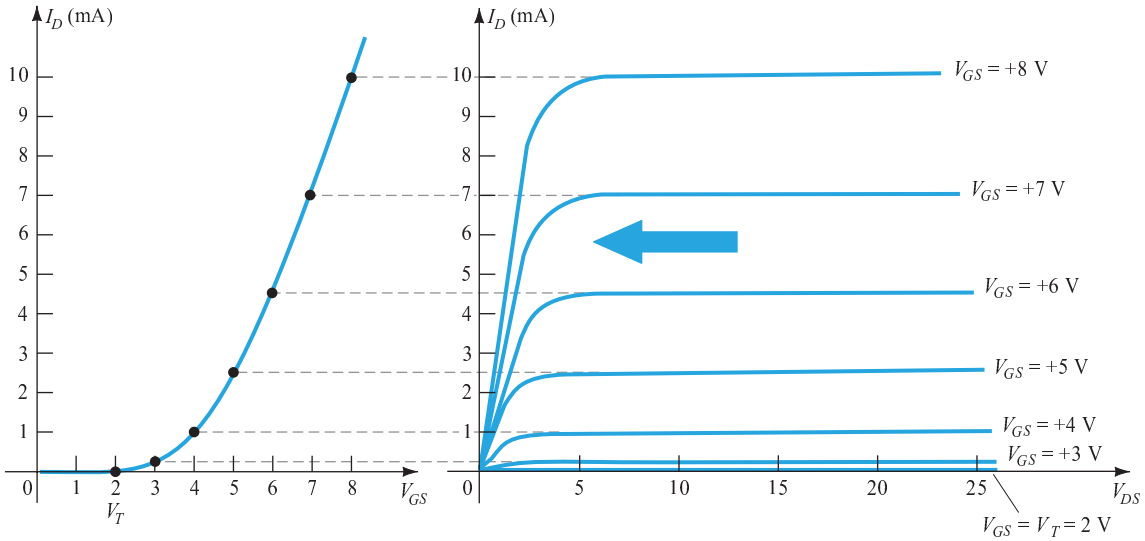


Figure 5.35 Sketching the transfer characteristics for an *n*-channel enhancement-type MOSFET from the drain characteristics.

The transfer curve of Fig. 5.35 is certainly quite different from those obtained earlier. For an *n*-channel (induced) device, it is now totally in the positive V_{GS} region and does not rise until $V_{GS} = V_T$. The question now surfaces as to how to plot the transfer characteristics given the levels of k and V_T as included below for a particular MOSFET:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2$$

First, a horizontal line is drawn at $I_D = 0$ mA from $V_{GS} = 0$ V to $V_{GS} = 4$ V as shown in Fig. 5.36a. Next, a level of V_{GS} greater than V_T such as 5 V is chosen and substituted into Eq. (5.13) to determine the resulting level of I_D as follows:

$$I_D = 0.5 \times 10^{-3}(V_{GS} - 4\text{ V})^2$$
$$= 0.5 \times 10^{-3}(5\text{ V} - 4\text{ V})^2 = 0.5 \times 10^{-3}(1)^2$$
$$\mathbf{= 0.5\ mA}$$

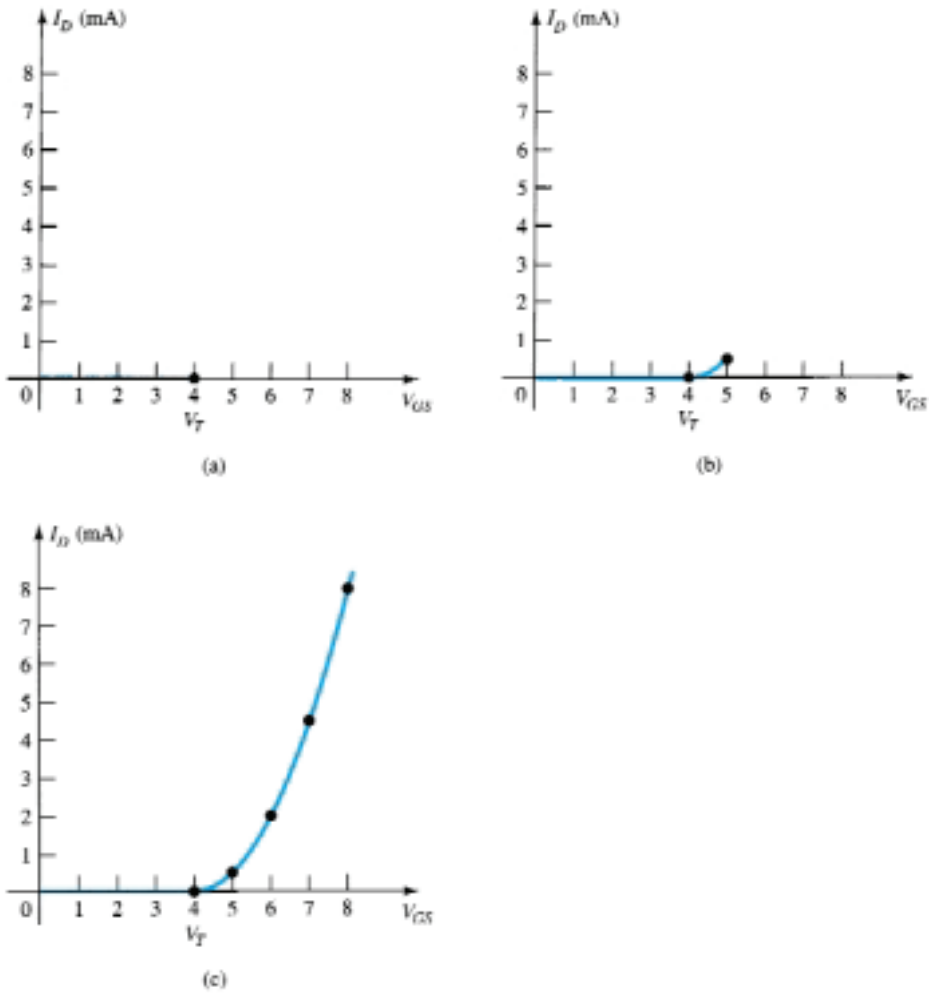


Figure 5.36 Plotting the transfer characteristics of an *n*-channel enhancement-type MOSFET with $k = 0.5 \times 10^{-3}$ A/V^2 and $V_T = 4$ V.

and a point on the plot is obtained as shown in Fig. 5.36b. Finally, additional levels of V_{GS} are chosen and the resulting levels of I_D obtained. In particular, at $V_{GS} = 6$, 7, and 8 V, the level of I_D is 2, 4.5, and 8 mA, respectively, as shown on the resulting plot of Fig. 5.36c.

p-Channel Enhancement-Type MOSFETs

The construction of a *p*-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 5.31, as shown in Fig. 5.37a. That is, there is now an *n*-type substrate and *p*-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 5.37c, with increasing levels of current resulting from increasingly negative values of V_{GS}. The transfer characteristics will be the mirror image (about the I_D axis) of the transfer curve of Fig. 5.35, with I_D increasing with increasingly negative values of V_{GS} beyond V_T, as shown in Fig. 5.37b. Equations (5.11) through (5.14) are equally applicable to *p*-channel devices.

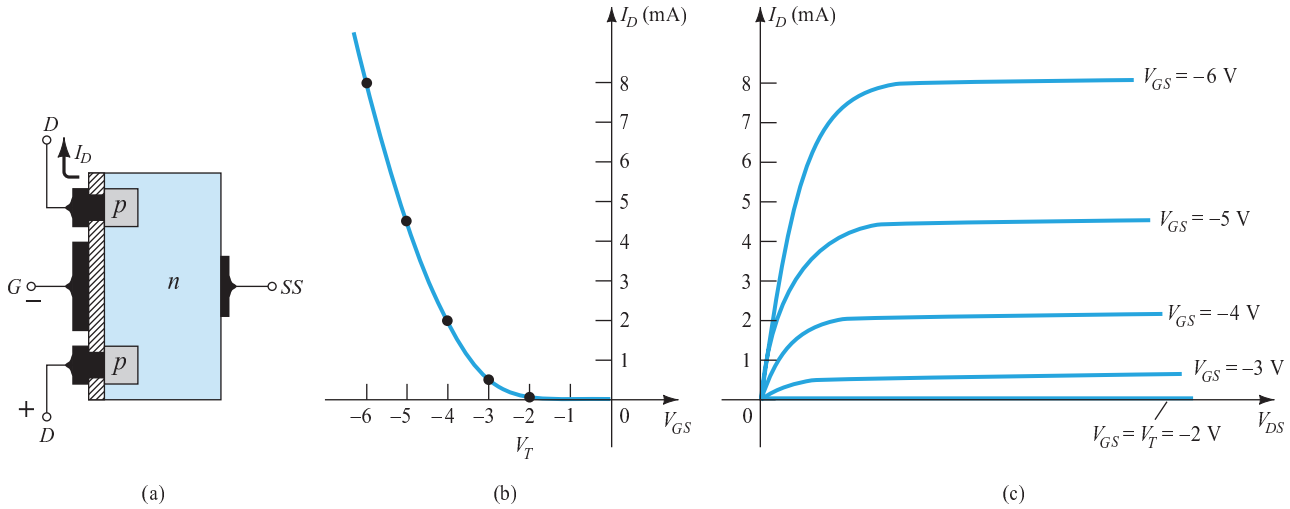


Figure 5.37 *p*-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V^2.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for the *n*- and *p*-channel enhancement-type MOSFETs are provided as Fig. 5.38. Again note how the symbols try to reflect the actual construction of the device. The dashed line between drain and source was chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.

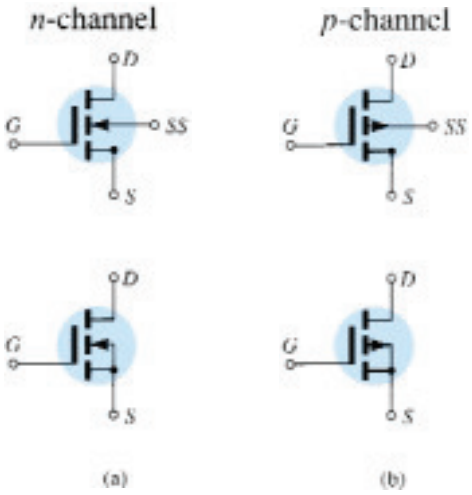
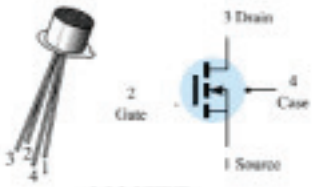


Figure 5.38 Symbols for (a) *n*-channel enhancement-type MOSFETs and (b) *p*-channel enhancement-type MOSFETs.

The specification sheet for a Motorola *n*-channel enhancement-type MOSFET is provided as Fig. 5.39. The case construction and terminal identification are provided next to the maximum ratings, which now include a maximum drain current of 30 mA dc. The specification sheet provides the level of I_{DSS} under "off" conditions, which is now simply 10 nA dc (at $V_{DS} = 10$ V and $V_{GS} = 0$ V) compared to the milliampere range for the JFET and depletion-type MOSFET. The threshold voltage is specified

2N4351

CASE 20-03, STYLE 2
TO-72 (TO-206AF)



MOSFET SWITCHING
N-CHANNEL – ENHANCEMENT

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	30	Vdc
Gate–Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.7	mW mW/°C
Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (I_D = 10 μA, V_{GS} = 0)	$V_{(BR)DSX}$	25	–	Vdc
Zero-Gate-Voltage Drain Current (V_{DS} = 10 V, V_{GS} = 0) T_A = 25°C T_A = 150°C	I_{DSS}	– –	10 10	nAdc μAdc
Gate Reverse Current (V_{GS} = ± 15 Vdc, V_{DS} = 0)	I_{GSS}	–	± 10	pAdc
ON CHARACTERISTICS				
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 10 μA)	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage (I_D = 2.0 mA, V_{GS} = 10V)	$V_{DS(on)}$	–	1.0	V
On-State Drain Current (V_{GS} = 10 V, V_{DS} = 10 V)	$I_{D(on)}$	3.0	–	mAdc
SMALL-SIGNAL CHARACTERISTICS				
Forward Transfer Admittance (V_{DS} = 10 V, I_D = 2.0 mA, f = 1.0 kHz)	$\lvert y_{fs} \rvert$	1000	–	μmho
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz)	C_{iss}	–	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 0, f = 140 kHz)	C_{rss}	–	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = 10 V, f = 140 kHz)	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance (V_{GS} = 10 V, I_D = 0, f = 1.0 kHz)	$r_{ds(on)}$	–	300	ohms
SWITCHING CHARACTERISTICS				
Turn-On Delay (Fig. 5)	t_{d1}	–	45	ns
Rise Time (Fig. 6)	t_r	–	65	ns
Turn-Off Delay (Fig. 7)	t_{d2}	–	60	ns
Fall Time (Fig. 8)	t_f	–	100	ns

(I_D = 2.0 mAdc, V_{DS} = 10 Vdc, (V_{GS} = 10 Vdc) (See Figure 9; Times Circuit Determined))

Figure 5.39 2N4351 Motorola *n*-channel enhancement-type MOSFET.

as $V_{GS(\text{Th})}$ and has a range of 1 to 5 V dc, depending on the unit employed. Rather than provide a range of k in Eq. (5.13), a typical level of $I_{D(\text{on})}$ (3 mA in this case) is specified at a particular level of $V_{GS(\text{on})}$ (10 V for the specified I_D level). In other words, when $V_{GS} = 10$ V, $I_D = 3$ mA. The given levels of $V_{GS(\text{Th})}$, $I_{D(\text{on})}$, and $V_{GS(\text{on})}$ permit a determination of k from Eq. (5.14) and a writing of the general equation for the transfer characteristics. The handling requirements of MOSFETs are reviewed in Section 5.9.

EXAMPLE 5.4

Using the data provided on the specification sheet of Fig. 5.39 and an average threshold voltage of $V_{GS(\text{Th})} = 3$ V, determine:
(a) The resulting value of k for the MOSFET.
(b) The transfer characteristics.

Solution

(a) Eq. (5.14): $$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$
$$= \frac{3 \text{ mA}}{(10 \text{ V} - 3 \text{ V})^2} = \frac{3 \text{ mA}}{(7 \text{ V})^2} = \frac{3 \times 10^{-3}}{49} \text{ A/V}^2$$
$$= \mathbf{0.061 \times 10^{-3} \text{ A/V}^2}$$

(b) Eq. (5.13): $$I_D = k(V_{GS} - V_T)^2$$
$$= 0.061 \times 10^{-3}(V_{GS} - 3 \text{ V})^2$$

For $V_{GS} = 5$ V,

$$I_D = 0.061 \times 10^{-3}(5 \text{ V} - 3 \text{ V})^2 = 0.061 \times 10^{-3}(2)^2$$
$$= 0.061 \times 10^{-3}(4) = 0.244 \text{ mA}$$

For $V_{GS} = 8$, 10, 12, and 14 V, I_D will be 1.525, 3 (as defined), 4.94, and 7.38 mA, respectively. The transfer characteristics are sketched in Fig. 5.40.

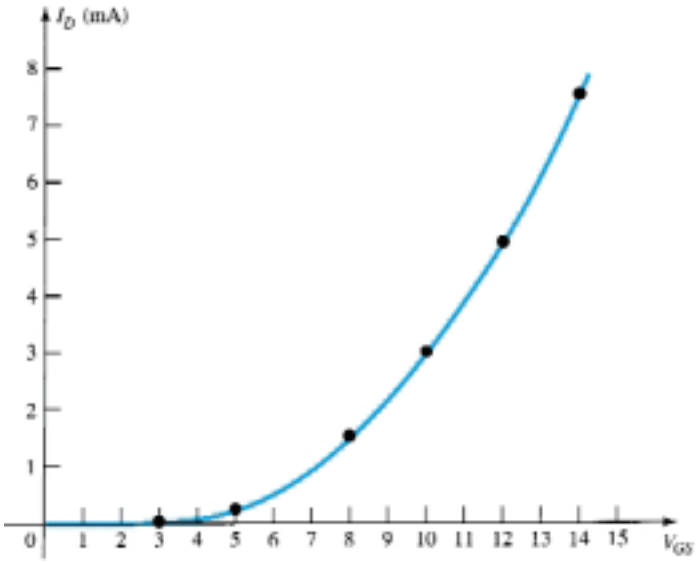


Figure 5.40 Solution to Example 5.4.

5.9 MOSFET HANDLING

The thin SiO_2 layer between the gate and channel of MOSFETs has the positive effect of providing a high-input-impedance characteristic for the device, but because of its extremely thin layer, it introduces a concern for its handling that was not present for the BJT or JFET transistors. There is often sufficient accumulation of static charge (that we pick up from our surroundings) to establish a potential difference across the thin layer that can break down the layer and establish conduction through it. It is therefore imperative that we leave the shorting (or conduction) shipping foil (or ring)

connecting the leads of the device together until the device is to be inserted in the system. The shorting ring prevents the possibility of applying a potential across any two terminals of the device. With the ring the potential difference between any two terminals is maintained at 0 V. At the very least always touch ground to permit discharge of the accumulated static charge before handling the device, and always pick up the transistor by the casing.

There are often transients (sharp changes in voltage or current) in a network when elements are removed or inserted if the power is on. The transient levels can often be more than the device can handle, and therefore the power should always be off when network changes are made.

The maximum gate-to-source voltage is normally provided in the list of maximum ratings of the device. One method of ensuring that this voltage is not exceeded (perhaps by transient effects) for either polarity is to introduce two Zener diodes, as shown in Fig. 5.41. The Zeners are back to back to ensure protection for either polarity. If both are 30-V Zeners and a positive transient of 40 V appears, the lower Zener will "fire" at 30 V and the upper will turn on with a 0-V drop (ideally—for the positive "on" region of a semiconductor diode) across the other diode. The result is a maximum of 30 V for the gate-to-source voltage. One disadvantage introduced by the Zener protection is that the off resistance of a Zener diode is less than the input impedance established by the SiO_2 layer. The result is a reduction in input resistance, but even so it is still high enough for most applications. So many of the discrete devices now have the Zener protection that some of the concerns listed above are not as troublesome. However, it is still best to be somewhat cautious when handling discrete MOSFET devices.

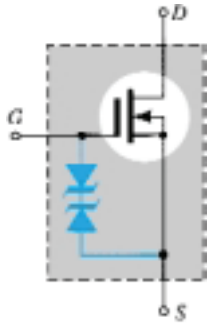


Figure 5.41 Zener-protected MOSFET.

5.10 VMOS

One of the disadvantages of the typical MOSFET is the reduced power-handling levels (typically, less than 1 W) compared to BJT transistors. This shortfall for a device with so many positive characteristics can be softened by changing the construction mode from one of a planar nature such as shown in Fig. 5.23 to one with a vertical structure as shown in Fig. 5.42. All the elements of the planar MOSFET are present in the vertical metal-oxide-silicon FET (VMOS)—the metallic surface connection to the terminals of the device—the SiO_2 layer between the gate and the *p*-type region between the drain and source for the growth of the induced *n*-channel (enhancement-

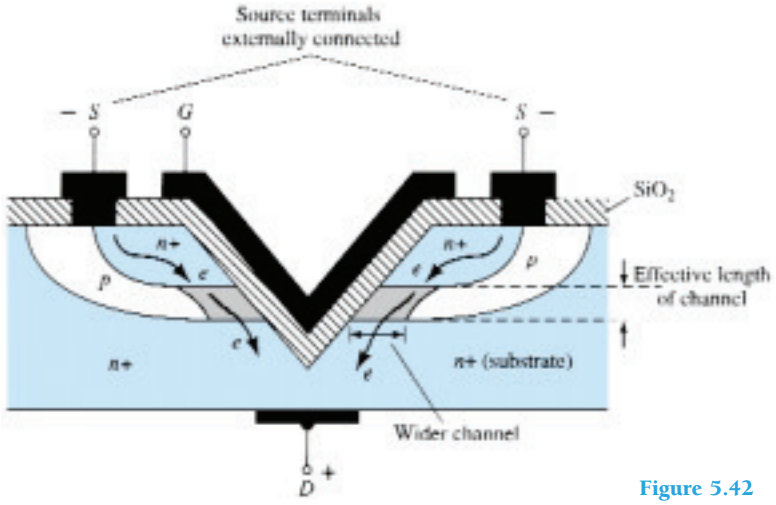


Figure 5.42 VMOS construction.

mode operation). The term *vertical* is due primarily to the fact that the channel is now formed in the vertical direction rather than the horizontal direction for the planar device. However, the channel of Fig. 5.42 also has the appearance of a "V" cut in the semiconductor base, which often stands out as a characteristic for mental memorization of the name of the device. The construction of Fig. 5.42 is somewhat simplistic in nature, leaving out some of the transition levels of doping, but it does permit a description of the most important facets of its operation.

The application of a positive voltage to the drain and a negative voltage to the source with the gate at 0 V or some typical positive "on" level as shown in Fig. 5.42 will result in the induced *n*-channel in the narrow *p*-type region of the device. The length of the channel is now defined by the vertical height of the *p*-region, which can be made significantly less than that of a channel using planar construction. On a horizontal plane the length of the channel is limited to 1 to 2 μm (1 μm = 10^{-6} m). Diffusion layers (such as the *p*-region of Fig. 5.42) can be controlled to small fractions of a micrometer. Since decreasing channel lengths result in reduced resistance levels, the power dissipation level of the device (power lost in the form of heat) at operating current levels will be reduced. In addition, the contact area between the channel and the n^+ region is greatly increased by the vertical mode construction, contributing to a further decrease in the resistance level and an increased area for current between the doping layers. There is also the existence of two conduction paths between drain and source, as shown in Fig. 5.42, to further contribute to a higher current rating. The net result is a device with drain currents that can reach the ampere levels with power levels exceeding 10 W.

In general:

Compared with commercially available planar MOSFETs, VMOS FETs have reduced channel resistance levels and higher current and power ratings.

An additional important characteristic of the vertical construction is:

VMOS FETs have a positive temperature coefficient that will combat the possibility of thermal runaway.

If the temperature of a device should increase due to the surrounding medium or currents of the device, the resistance levels will increase, causing a reduction in drain current rather than an increase as encountered for a conventional device. Negative temperature coefficients result in decreased levels of resistance with increases in temperature that fuel the growing current levels and result in further temperature instability and thermal runaway.

Another positive characteristic of the VMOS configuration is:

The reduced charge storage levels result in faster switching times for VMOS construction compared to those for conventional planar construction.

In fact, VMOS devices typically have switching times less than one-half that encountered for the typical BJT transistor.

5.11 CMOS

A very effective logic circuit can be established by constructing a *p*-channel and an *n*-channel MOSFET on the same substrate as shown in Fig. 5.43. Note the induced *p*-channel on the left and the induced *n*-channel on the right for the *p*- and *n*-channel devices, respectively. The configuration is referred to as a *complementary MOSFET* arrangement (CMOS) that has extensive applications in computer logic design. The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as *CMOS logic design.*

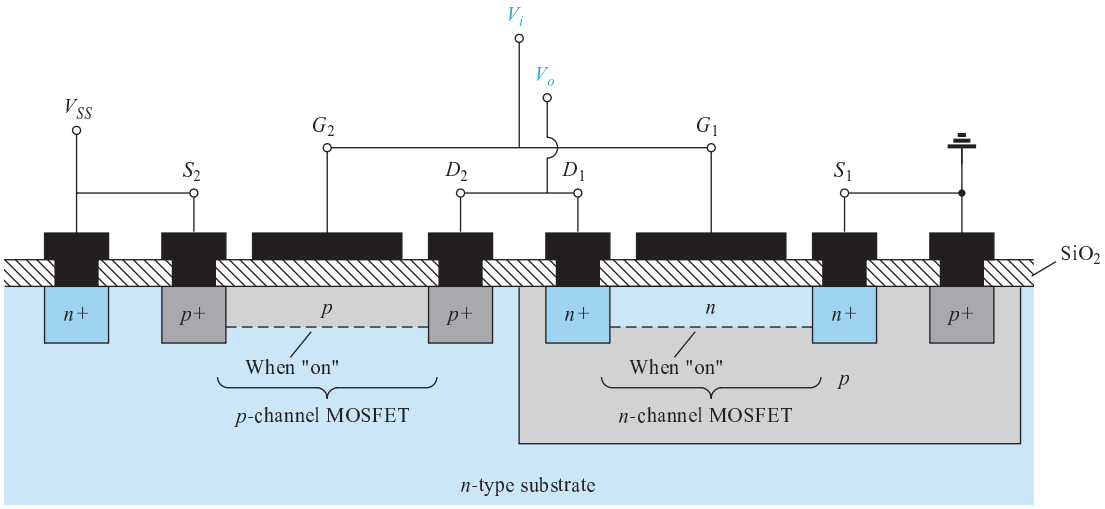


Figure 5.43 CMOS with the connections indicated in Fig. 5.44.

One very effective use of the complementary arrangement is as an inverter, as shown in Fig. 5.44. As introduced for switching transistors, an inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa. Note in Fig. 5.44 that both gates are connected to the applied signal and both drain to the output V_o. The source of the p-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS}, while the source of the n-channel MOSFET (Q_1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V at the output. With 5 V at V_i (with respect to ground), $V_{GS_1} = V_i$ and Q_1 is "on," resulting in a relatively low resistance between drain and source as shown in Fig. 5.45. Since V_i and V_{SS} are at 5 V, $V_{GS_2} = 0$ V, which is less than the required V_T for the device, resulting in an "off" state. The resulting resistance level between drain and source is quite high for Q_2, as shown in Fig. 5.45. A simple application of the voltage-divider rule will reveal that V_o is very close to 0 V or the 0-state, establishing the desired inversion process. For an applied voltage V_i of 0 V (0-state), $V_{GS_1} = 0$ V and Q_1 will be off with $V_{SS_2} = -5$ V, turning on the p-channel MOSFET. The result is that Q_2 will present a small resistance level, Q_1 a high resistance, and $V_o = V_{SS} = 5$ V (the 1-state). Since the drain current that flows for either case is limited by the "off" transistor to the leakage value, the power dissipated by the device in either state is very low. Additional comment on the application of CMOS logic is presented in Chapter 17.

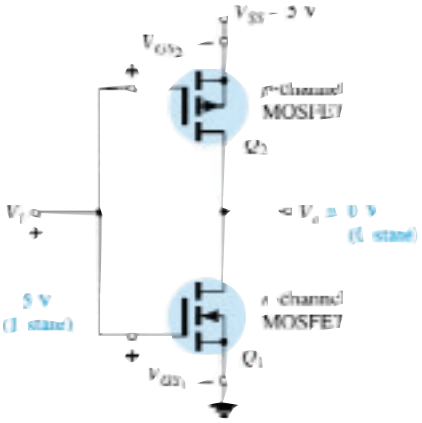


Figure 5.44 CMOS inverter.

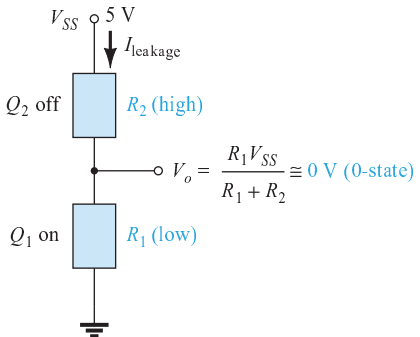
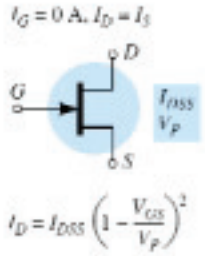
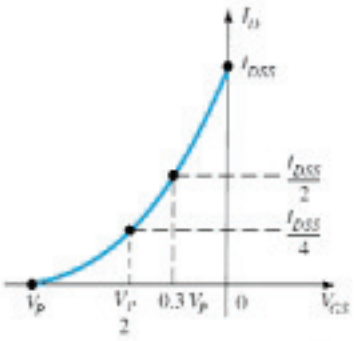
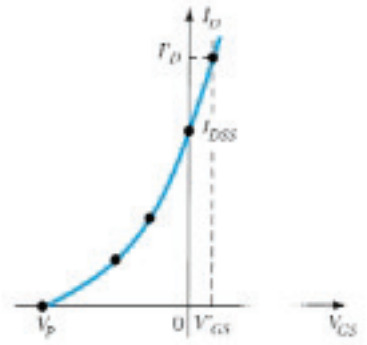
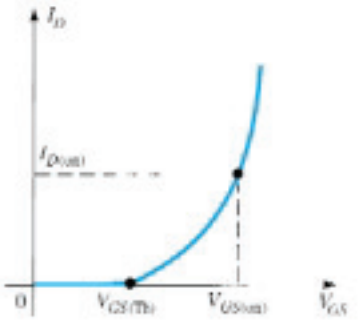


Figure 5.45 Relative resistance levels for $V_i = 5$ V (1-state).

5.12 SUMMARY TABLE

Since the transfer curves and some important characteristics vary from one type of FET to another, Table 5.2 was developed to clearly display the differences from one device to the next. A clear understanding of all the curves and parameters of the table will provide a sufficient background for the dc and ac analyses to follow in Chapters 6 and 8. Take a moment to ensure that each curve is recognizable and its derivation understood, and then establish a basis for comparison of the levels of the important parameters of R_i and C_i for each device.

TABLE 5.2 Field Effect Transistors

Type	*-Symbol- Basic Relationships*	*Transfer Curve*	*Input Resistance and Capacitance*
JFET (*n*-channel)			$R_i > 100$ MΩ C_i: (1 − 10) pF
MOSFET depletion-type (*n*-channel)			$R_i > 10^{10}$ Ω C_i: (1 − 10) pF
MOSFET enhancement-type (*n*-channel)			$R_i > 10^{10}$ Ω C_i: (1 − 10) pF

5.13 PSPICE WINDOWS

The characteristics of an *n*-channel JFET can be found in much the same manner as employed for the bipolar transistor. The series of curves for various levels of V will require a nested sweep under the main sweep for the drain-to-source voltage. The configuration required appears in Fig. 5.46. Note the absence of any resistors since the input impedance is assumed to be infinite, resulting in $I_G = 0$ A. Calling up the device specifications through **Edit-Model-Edit Instance Model (Text)** will result in a display having at the head of the listing a parameter **Beta.** For the junction-field-effect transistor **Beta** is defined by

$$\text{Beta} = \frac{I_{DSS}}{|V_p|^2} \tag{5.15}$$

The parameter **Vto =** -3 defines $V_{GS} = V_P = -3$ V as the pinch-off voltage—something to check when we obtain our characteristics. Choosing the **Setup Analysis** icon (recall that it has the horizontal blue line at the top), the **DC Sweep** is first enabled and then activated to produce the **DC Sweep** dialog box. Select **Voltage Source-Linear,** and insert the **Name:** VDD, the **Start Value** of 0 V, **End Value** of 10 V, and **Increment** of 0.01 V. Then, the **Nested Sweep** is chosen, and **Voltage** and **Linear** are chosen once more. Finally, the **Name:** VGG is entered, the **Start Value** of 0 V is chosen, the **End Value** of -5 V is entered, and the **Increment** is set at -1 V. Then, be sure to **Enable Nested Sweep** before clicking on **OK** and closing. With the **Automatically run Probe after Simulation** enabled, clicking on the analysis icon will result in the **OrCAD-MicroSim Probe** screen. There is no need to call up the **X-Axis Settings** because the horizontal axis has the correct range and the voltage V_{DD} is actually the drain-to-source voltage. By choosing the **Trace** icon, the **Add Traces** dialog box will appear. **ID(J1)** is chosen, followed by **OK.** The result is the set of characteristics appearing in Fig. 5.47. The remaining labels were added using the **ABC** icon.

Note that the pinch-off voltage is -3 V, as expected by the **Vto** parameter. The value of I_{DSS} is very close to 12 mA.

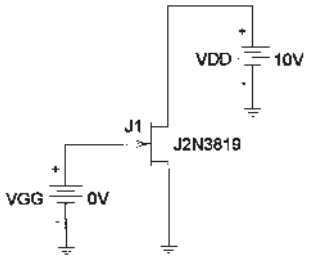


Figure 5.46 Network employed to obtain the characteristics of the *n*-channel J2N3819 JFET.

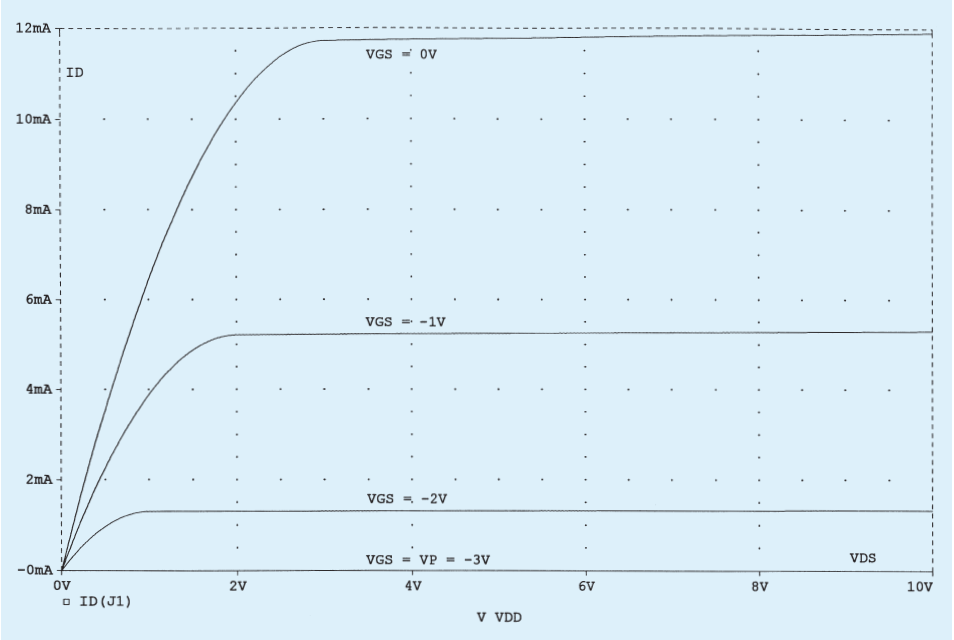


Figure 5.47 Drain characteristics for the *n*-channel J2N3819 JFET of Figure 5.46.

The transfer characteristics can be obtained by returning to the network configuration and choosing the **Analysis-Setup** icon. The **DC Sweep** is again enabled, and the **DC Sweep** is chosen. This time, since the result will only be one curve, a nested operation will not be performed. After choosing **Voltage Source** and **Linear,** the **Name** will be VGG, the **Start Value** −3 V (since we now know that $V_P = -3$ V), the **End Value** 0 V, and the **Increment** 0.01 V to get a good continuous plot. After an **OK** followed by a **Close,** the **Simulation** icon can be chosen. Once the **Probe** screen appears, choose **Plot-X-Axis Settings-Axis Variable** and choose **V(J1:g)** for the gate-to-source voltage. Choose **OK** and we're back to the **X-Axis Settings** dialog box to choose the **User Defined** range of −3 V to 0 V (which already appears because of our sweep settings). Choose **OK** again and the **Trace** ID(J1) can be chosen to result in the transfer characteristics of Fig. 5.48.

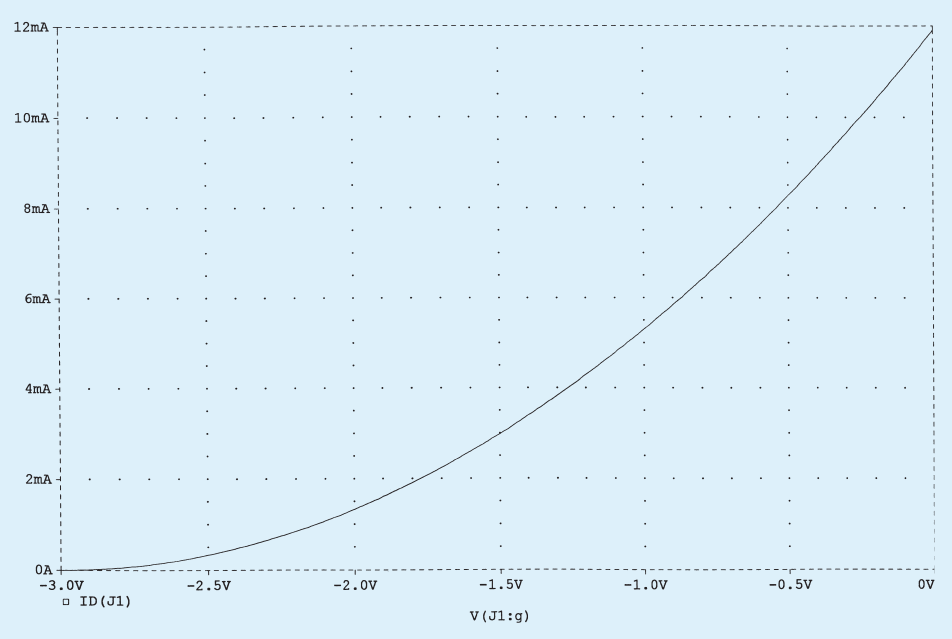


Figure 5.48 Transfer characteristics for the *n*-channel J2N3819 JFET of Figure 5.46.

PROBLEMS

§ 5.2 Construction and Characteristics of JFETs

1. (a) Draw the basic construction of a *p*-channel JFET.
(b) Apply the proper biasing between drain and source and sketch the depletion region for $V_{GS} = 0$ V.

2. Using the characteristics of Fig. 5.10, determine I_D for the following levels of V_{GS} (with $V_{DS} > V_P$).
(a) $V_{GS} = 0$ V.
(b) $V_{GS} = -1$ V.
(c) $V_{GS} = -1.5$ V.
(d) $V_{GS} = -1.8$ V.
(e) $V_{GS} = -4$ V.
(f) $V_{GS} = -6$ V.

3. (a) Determine V_{DS} for $V_{GS} = 0$ V and $I_D = 6$ mA using the characteristics of Fig. 5.10.
(b) Using the results of part (a), calculate the resistance of the JFET for the region $I_D = 0$ to 6 mA for $V_{GS} = 0$ V.
(c) Determine V_{DS} for $V_{GS} = -1$ V and $I_D = 3$ mA.
(d) Using the results of part (c), calculate the resistance of the JFET for the region $I_D = 0$ to 3 mA for $V_{GS} = -1$ V.
(e) Determine V_{DS} for $V_{GS} = -2$ V and $I_D = 1.5$ mA.
(f) Using the results of part (e), calculate the resistance of the JFET for the region $I_D = 0$ to 1.5 mA for $V_{GS} = -2$ V.
(g) Defining the result of part (b) as r_o, determine the resistance for $V_{GS} = -1$ V using Eq. (5.1) and compare with the results of part (d).
(h) Repeat part (g) for $V_{GS} = -2$ V using the same equation, and compare the results with part (f).
(i) Based on the results of parts (g) and (h), does Eq. (5.1) appear to be a valid approximation?

4. Using the characteristics of Fig. 5.10:
(a) Determine the difference in drain current (for $V_{DS} > V_P$) between $V_{GS} = 0$ V and $V_{GS} = -1$ V.
(b) Repeat part (a) between $V_{GS} = -1$ and -2 V.
(c) Repeat part (a) between $V_{GS} = -2$ and -3 V.
(d) Repeat part (a) between $V_{GS} = -3$ and -4 V.
(e) Is there a marked change in the difference in current levels as V_{GS} becomes increasingly negative?
(f) Is the relationship between the change in V_{GS} and the resulting change in I_D linear or nonlinear? Explain.

5. What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? Compare the units of each axis and the controlling variable. How does I_C react to increasing levels of I_B versus changes in I_D to increasingly negative values of V_{GS}? How does the spacing between steps of I_B compare to the spacing between steps of V_{GS}? Compare $V_{C_{sat}}$ to V_P in defining the nonlinear region at low levels of output voltage.

6. (a) Describe in your own words why I_G is effectively zero amperes for a JFET transistor.
(b) Why is the input impedance to a JFET so high?
(c) Why is the terminology *field effect* appropriate for this important three-terminal device?

7. Given $I_{DSS} = 12$ mA and $|V_P| = 6$ V, sketch a probable distribution of characteristic curves for the JFET (similar to Fig. 5.10).

8. In general, comment on the polarity of the various voltages and direction of the currents for an *n*-channel JFET versus a *p*-channel JFET.

§ 5.3 Transfer Characteristics

9. Given the characteristics of Fig. 5.49:
(a) Sketch the transfer characteristics directly from the drain characteristics.
(b) Using Fig. 5.49 to establish the values of I_{DSS} and V_P, sketch the transfer characteristics using Shockley's equation.
(c) Compare the characteristics of parts (a) and (b). Are there any major differences?

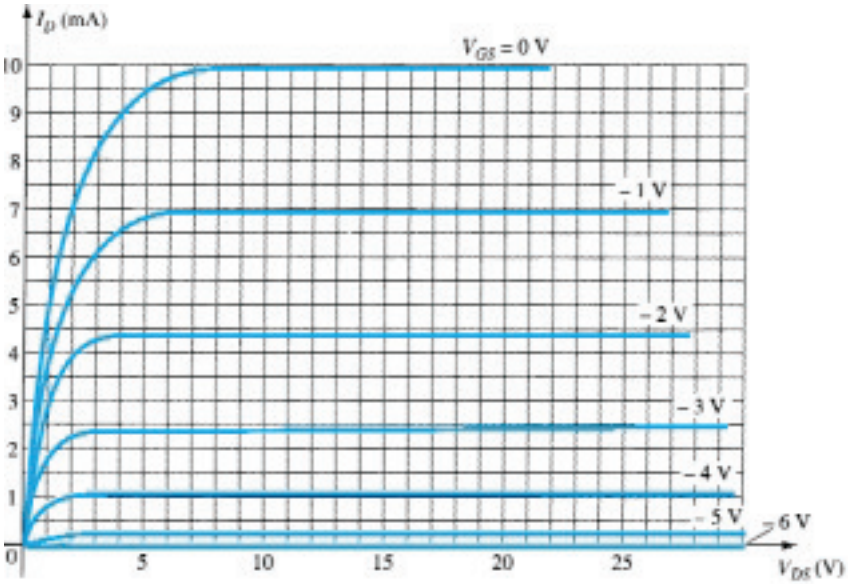


Figure 5.49 Problems 9, 17

10. (a) Given $I_{DSS} = 12$ mA and $V_P = -4$ V, sketch the transfer characteristics for the JFET transistor.
(b) Sketch the drain characteristics for the device of part (a).

11. Given $I_{DSS} = 9$ mA and $V_P = -3.5$ V, determine I_D when:
(a) $V_{GS} = 0$ V.
(b) $V_{GS} = -2$ V.
(c) $V_{GS} = -3.5$ V.
(d) $V_{GS} = -5$ V.

12. Given $I_{DSS} = 16$ mA and $V_P = -5$ V, sketch the transfer characteristics using the data points of Table 5.1. Determine the value of I_D at $V_{GS} = -3$ V from the curve, and compare it to the value determined using Shockley's equation. Repeat the above for $V_{GS} = -1$ V.

13. A *p*-channel JFET has device parameters of $I_{DSS} = 7.5$ mA and $V_P = 4$ V. Sketch the transfer characteristics.

14. Given $I_{DSS} = 6$ mA and $V_P = -4.5$ V:
(a) Determine I_D at $V_{GS} = -2$ and -3.6 V.
(b) Determine V_{GS} at $I_D = 3$ and 5.5 mA.

15. Given a *Q*-point of $I_{D_Q} = 3$ mA and $V_{GS} = -3$ V, determine I_{DSS} if $V_P = -6$ V.

§ 5.4 Specification Sheets (JFETs)

16. Define the region of operation for the 2N5457 JFET of Fig. .5.18 using the range of I_{DSS} and V_P provided. That is, sketch the transfer curve defined by the maximum I_{DSS} and V_P and the transfer curve for the minimum I_{DSS} and V_P. Then, shade in the resulting area between the two curves.

17. Define the region of operation for the JFET of Fig. 5.49 if $V_{DS_{max}} = 25$ V and $P_{D_{max}} = 120$ mW.

§ 5.5 Instrumentation

18. Using the characteristics of Fig. 5.21, determine I_D at $V_{GS} = -0.7$ V and $V_{DS} = 10$ V.

19. Referring to Fig. 5.21, is the locus of pinch-off values defined by the region of $V_{DS} < |V_P| = 3$ V?

20. Determine V_P for the characteristics of Fig. 5.21 using I_{DSS} and I_D at some value of V_{GS}. That is, simply substitute into Shockley's equation and solve for V_P. Compare the result to the assumed value of -3 V from the characteristics.

21. Using $I_{DSS} = 9$ mA and $V_P = -3$ V for the characteristics of Fig. 5.21, calculate I_D at $V_{GS} = -1$ V using Shockley's equation and compare to the level appearing in Fig. 5.21.

22. (a) Calculate the resistance associated with the JFET of Fig. 5.21 for $V_{GS} = 0$ V from $I_D = 0$ to 4 mA.
(b) Repeat part (a) for $V_{GS} = -0.5$ V from $I_D = 0$ to 3 mA.
(c) Assigning the label r_o to the result of part (a) and r_d to that of part (b), use Eq. (5.1) to determine r_d and compare to the result of part (b).

§ 5.7 Depletion-Type MOSFET

23. (a) Sketch the basic construction of a *p*-channel depletion-type MOSFET.
(b) Apply the proper drain-to-source voltage and sketch the flow of electrons for $V_{GS} = 0$ V.

24. In what ways is the construction of a depletion-type MOSFET similar to that of a JFET? In what ways is it different?

25. Explain in your own words why the application of a positive voltage to the gate of an *n*-channel depletion-type MOSFET will result in a drain current exceeding I_{DSS}.

26. Given a depletion-type MOSFET with $I_{DSS} = 6$ mA and $V_P = -3$ V, determine the drain current at $V_{GS} = -1$, 0, 1, and 2 V. Compare the difference in current levels between -1 and 0 V with the difference between 1 and 2 V. In the positive V_{GS} region, does the drain current increase at a significantly higher rate than for negative values? Does the I_D curve become more and more vertical with increasing positive values of V_{GS}? Is there a linear or a nonlinear relationship between I_D and V_{GS}? Explain.

27. Sketch the transfer and drain characteristics of an *n*-channel depletion-type MOSFET with $I_{DSS} = 12$ mA and $V_P = -8$ V for a range of $V_{GS} = -V_P$ to $V_{GS} = 1$ V.

28. Given $I_D = 14$ mA and $V_{GS} = 1$ V, determine V_P if $I_{DSS} = 9.5$ mA for a depletion-type MOSFET.

29. Given $I_D = 4$ mA at $V_{GS} = -2$ V, determine I_{DSS} if $V_P = -5$ V.

30. Using an average value of 2.9 mA for the I_{DSS} of the 2N3797 MOSFET of Fig. 5.30, determine the level of V_{GS} that will result in a maximum drain current of 20 mA if $V_P = -5$ V.

31. If the drain current for the 2N3797 MOSFET of Fig. 5.30 is 8 mA, what is the maximum permissible value of V_{DS} utilizing the maximum power rating?

§ 5.8 Enhancement-Type MOSFET

32. (a) What is the significant difference between the construction of an enhancement-type MOSFET and a depletion-type MOSFET?
(b) Sketch a *p*-channel enhancement-type MOSFET with the proper biasing applied ($V_{DS} > 0$ V, $V_{GS} > V_T$) and indicate the channel, the direction of electron flow, and the resulting depletion region.
(c) In your own words, briefly describe the basic operation of an enhancement-type MOSFET.

33. (a) Sketch the transfer and drain characteristics of an *n*-channel enhancement-type MOSFET if $V_T = 3.5$ V and $k = 0.4 \times 10^{-3}$ A/V^2.
(b) Repeat part (a) for the transfer characteristics if V_T is maintained at 3.5 V but k is increased by 100% to 0.8×10^{-3} A/V^2.

34. (a) Given $V_{GS(Th)} = 4$ V and $I_{D(on)} = 4$ mA at $V_{GS(on)} = 6$ V, determine k and write the general expression for I_D in the format of Eq. (5.13).
(b) Sketch the transfer characteristics for the device of part (a).
(c) Determine I_D for the device of part (a) at $V_{GS} = 2$, 5, and 10 V.

35. Given the transfer characteristics of Fig. 5.50, determine V_T and k and write the general equation for I_D.

36. Given $k = 0.4 \times 10^{-3}$ A/V^2 and $I_{D(on)} = 3$ mA with $V_{GS(on)} = 4$ V, determine V_T.

37. The maximum drain current for the 2N4351 *n*-channel enhancement-type MOSFET is 30 mA. Determine V_{GS} at this current level if $k = 0.06 \times 10^{-3}$ A/V^2 and V_T is the maximum value.

I_{DDS}/V_P

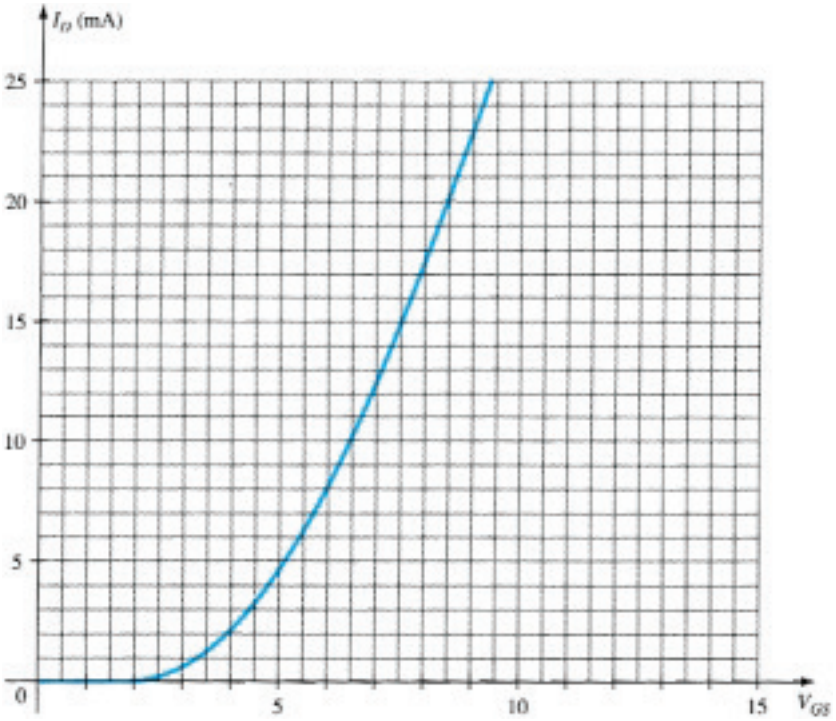


Figure 5.50 Problem 35

38. Does the current of an enhancement-type MOSFET increase at about the same rate as a depletion-type MOSFET for the conduction region? Carefully review the general format of the equations, and if your mathematics background includes differential calculus, calculate dI_D/dV_{GS} and compare its magnitude.

39. Sketch the transfer characteristics of a *p*-channel enhancement-type MOSFET if $V_T = -5$ V and $k = 0.45 \times 10^{-3}$ A/V^2.

40. Sketch the curve of $I_D = 0.5 \times 10^{-3}(V_{GS}^2)$ and $I_D = 0.5 \times 10^{-3}(V_{GS} - 4)^2$ for V_{GS} from 0 to 10 V. Does $V_T = 4$ V have a significant impact on the level of I_D for this region?

§ 5.10 VMOS

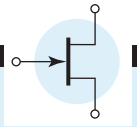
41. (a) Describe in your own words why the VMOS FET can withstand a higher current and power rating than the standard construction technique.
(b) Why do VMOS FETs have reduced channel resistance levels?
(c) Why is a positive temperature coefficient desirable?

§ 5.11 CMOS

* **42.** (a) Describe in your own words the operation of the network of Fig. 5.44 with $V_i = 0$ V.
(b) If the "on" MOSFET of Fig. 5.44 (with $V_i = 0$ V) has a drain current of 4 mA with $V_{DS} = 0.1$ V, what is the approximate resistance level of the device? If $I_D = 0.5$ μA for the "off" transistor, what is the approximate resistance of the device? Do the resulting resistance levels suggest that the desired output voltage level will result?

43. Research CMOS logic at your local or college library, and describe the range of applications and basic advantages of the approach.

*Please Note: Asterisks indicate more difficult problems.



CHAPTER

6 FET Biasing

6.1 INTRODUCTION

In Chapter 5 we found that the biasing levels for a silicon transistor configuration can be obtained using the characteristic equations $V_{BE} = 0.7$ V, $I_C = \beta I_B$, and $I_C \cong I_E$. The linkage between input and output variables is provided by β, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B. Doubling the value of I_B will double the level of I_C, and so on.

For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, while nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers. Since the graphical approach is in general the most popular, the analysis of this chapter will have a graphical orientation rather than direct mathematical techniques.

Another distinct difference between the analysis of BJT and FET transistors is that the input controlling variable for a BJT transistor is a current level, while for the FET a voltage is the controlling variable. In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0 \text{ A} \tag{6.1}$$

and

$$I_D = I_S \tag{6.2}$$

For JFETS and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(\frac{1 - V_{GS}}{V_P}\right)^2 \tag{6.3}$$

For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2 \tag{6.4}$$

It is particularly important to realize that all of the equations above are for the *device only!* They do not change with each network configuration so long as the device is in the active region. The network simply defines the level of current and voltage associated with the operating point through its own set of equations. In reality, the dc solution of BJT and FET networks is the solution of simultaneous equations established by the device and network. The solution can be determined using a mathematical or graphical approach—a fact to be demonstrated by the first few networks to be analyzed. However, as noted earlier, the graphical approach is the most popular for FET networks and is employed in this book.

The first few sections of this chapter are limited to JFETs and the graphical approach to analysis. The depletion-type MOSFET will then be examined with its increased range of operating points, followed by the enhancement-type MOSFET. Finally, problems of a design nature are investigated to fully test the concepts and procedures introduced in the chapter.

6.2 FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 6.1. Referred to as the fixed-bias configuration, it is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach. Both methods are included in this section to demonstrate the difference between the two philosophies and also to establish the fact that the same solution can be obtained using either method.

The configuration of Fig. 6.1 includes the ac levels V_i and V_o and the coupling capacitors (C_1 and C_2). Recall that the coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis (Chapter 9). For the dc analysis,

$$I_G \cong 0 \text{ A}$$

and

$$V_{R_G} = I_G R_G = (0 \text{ A})R_G = 0 \text{ V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 6.2 specifically redrawn for the dc analysis.

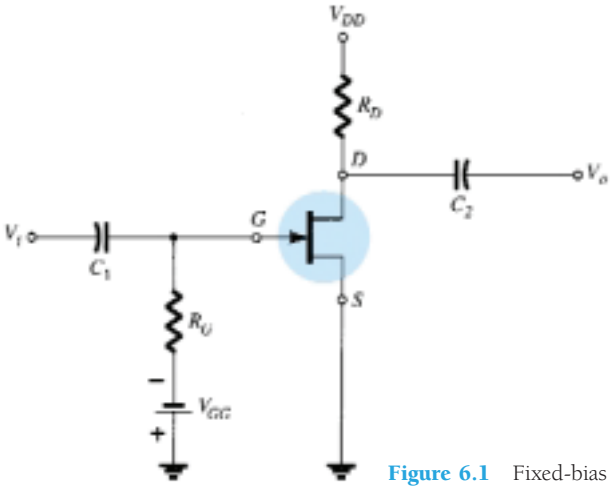


Figure 6.1 Fixed-bias configuration.

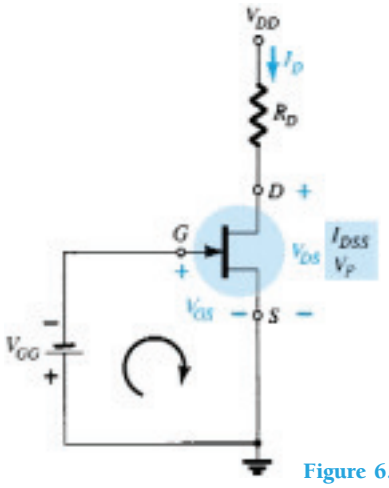


Figure 6.2 Network for dc analysis.

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 6.2 will result in

$$-V_{GG} - V_{GS} = 0$$

and

$$\boxed{V_{GS} = -V_{GG}} \tag{6.5}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the notation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated. This is one of the few instances in which a mathematical solution to a FET configuration is quite direct.

A graphical analysis would require a plot of Shockley's equation as shown in Fig. 6.3. Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.

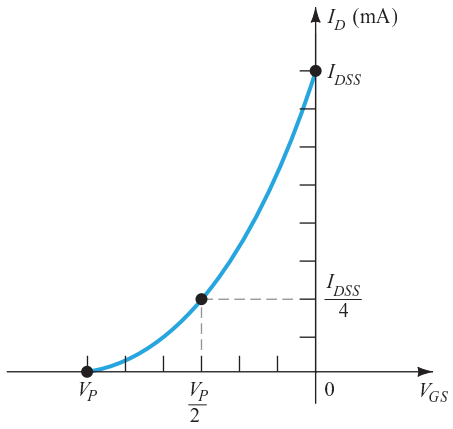


Figure 6.3 Plotting Shockley's equation.

In Fig. 6.4, the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves

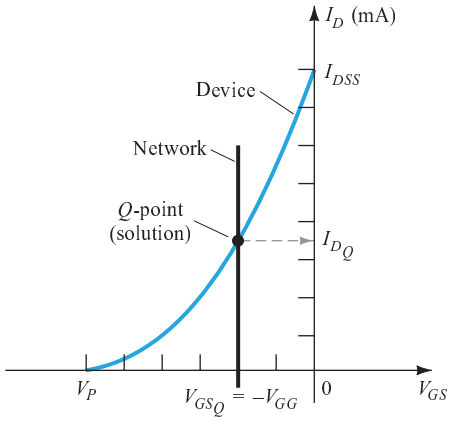


Figure 6.4 Finding the solution for the fixed-bias configuration.

intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point*. The subscript Q will be applied to drain current and gate-to-source voltage to identify their levels at the Q-point. Note in Fig. 6.4 that the quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis as shown in Fig. 6.4. It is important to realize that once the network of Fig. 6.1 is constructed and operating, the dc levels of I_D and V_{GS} that will be measured by the meters of Fig. 6.5 are the quiescent values defined by Fig. 6.4.

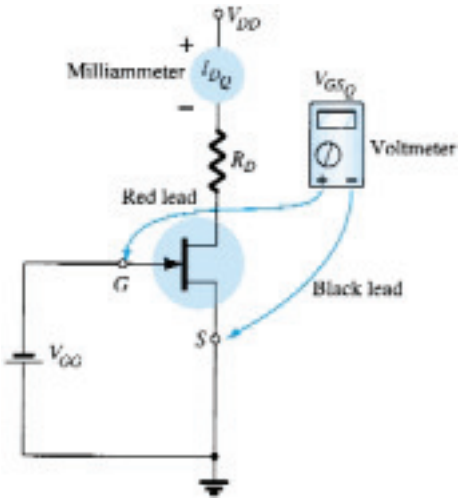


Figure 6.5 Measuring the quiescent values of I_D and V_{GS}.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D} \tag{6.6}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground. For the configuration of Fig. 6.2,

$$\boxed{V_S = 0 \text{ V}} \tag{6.7}$$

Using double-subscript notation:

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0 \text{ V}$$

and

$$\boxed{V_D = V_{DS}} \tag{6.8}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0 \text{ V}$$

and

$$\boxed{V_G = V_{GS}} \tag{6.9}$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0$ V, but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc supplies, its use is limited and will not be included in the forthcoming list of the most common FET configurations.

EXAMPLE 6.1

Determine the following for the network of Fig. 6.6.

(a) V_{GSQ}.
(b) I_{DQ}.
(c) V_{DS}.
(d) V_D.
(e) V_G.
(f) V_S.

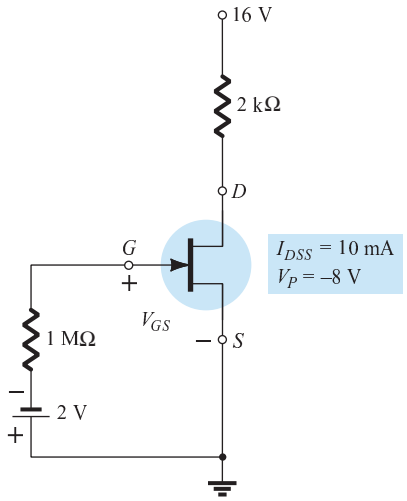


Figure 6.6 Example 6.1.

Solution

Mathematical Approach:

(a) $V_{GSQ} = -V_{GG} = \mathbf{-2\ V}$

(b) $$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

(c) $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

(d) $V_D = V_{DS} = \mathbf{4.75\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

Graphical Approach:

The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 6.7. It is certainly difficult to read beyond the second place without significantly in-

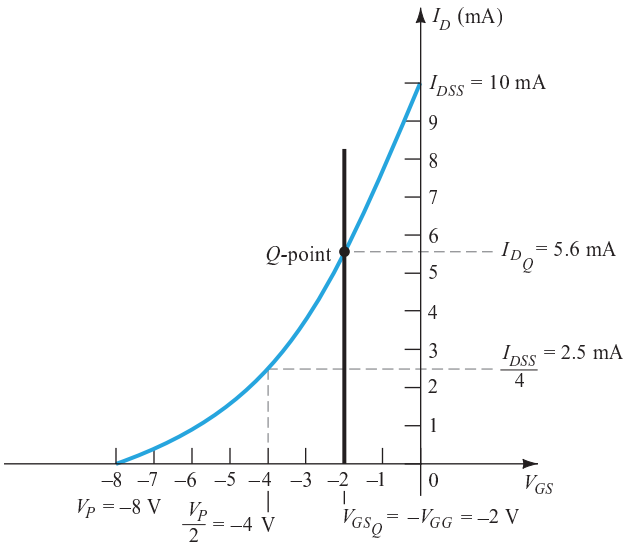


Figure 6.7 Graphical solution for the network of Fig. 6.6.

creasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 6.7 is quite acceptable. Therefore, for part (a),

$$V_{GSQ} = -V_{GG} = \mathbf{-2\ V}$$

(b) $I_{DQ} = \mathbf{5.6\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\ \text{V} - (5.6\ \text{mA})(2\ \text{k}\Omega)$
$= 16\ \text{V} - 11.2\ \text{V} = \mathbf{4.8\ V}$

(d) $V_D = V_{DS} = \mathbf{4.8\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

6.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 6.8.

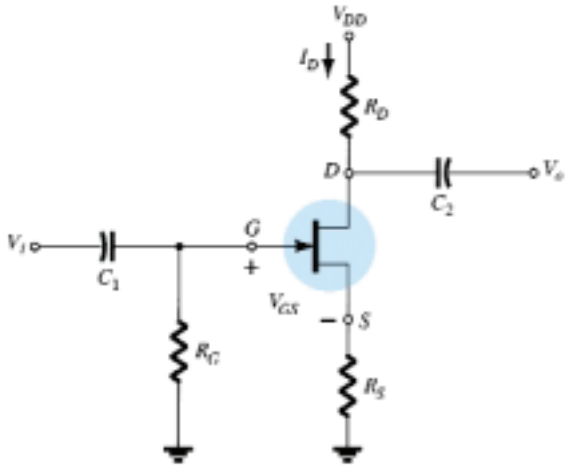


Figure 6.8 JFET self-bias configuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 6.9 for the important dc analysis.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 6.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$\boxed{V_{GS} = -I_D R_S} \tag{6.10}$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

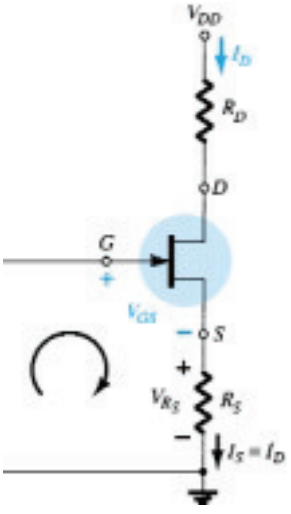


Figure 6.9 DC analysis of the self-bias configuration.

Equation (6.10) is defined by the network configuration, and Shockley's equation relates the input and output quantities of the device. Both equations relate the same two variables, permitting either a mathematical or graphical solution.

A mathematical solution could be obtained simply by substituting Eq. (6.10) into Shockley's equation as shown below:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

or

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, an equation of the following form can be obtained:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D.

The sequence above defines the mathematical approach. The graphical approach requires that we first establish the device transfer characteristics as shown in Fig. 6.10. Since Eq. (6.10) defines a straight line on the same graph, let us now identify two points on the graph that are on the line and simply draw a straight line between the two points. The most obvious condition to apply is $I_D = 0$ A since it results in $V_{GS} = -I_D R_S = (0 \text{ A}) R_S = 0$ V. For Eq. (6.10), therefore, one point on the straight line is defined by $I_D = 0$ A and $V_{GS} = 0$ V, as appearing on Fig. 6.10.

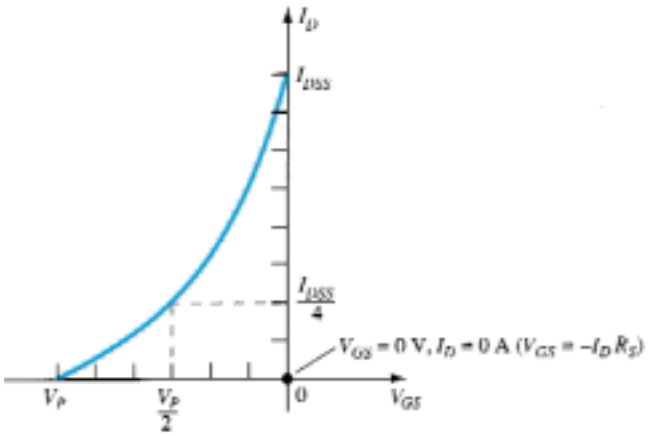


Figure 6.10 Defining a point on the self-bias line.

The second point for Eq. (6.10) requires that a level of V_{GS} or I_D be chosen and the corresponding level of the other quantity be determined using Eq. (6.10). The resulting levels of I_D and V_{GS} will then define another point on the straight line and permit an actual drawing of the straight line. Suppose, for example, that we choose a level of I_D equal to one-half the saturation level. That is,

$$I_D = \frac{I_{DSS}}{2}$$

then

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

The result is a second point for the straight-line plot as shown in Fig. 6.11. The straight line as defined by Eq. (6.10) is then drawn and the quiescent point obtained at the in-

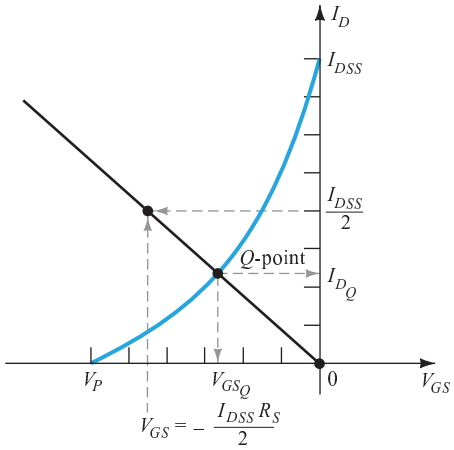


Figure 6.11 Sketching the self-bias line.

tersection of the straight-line plot and the device characteristic curve. The quiescent values of I_D and V_{GS} can then be determined and used to find the other quantities of interest.

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and
$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

but
$$I_D = I_S$$

and
$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \tag{6.11}$$

In addition:

$$\boxed{V_S = I_D R_S} \tag{6.12}$$

$$\boxed{V_G = 0\ \text{V}} \tag{6.13}$$

and
$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}} \tag{6.14}$$

EXAMPLE 6.2

Determine the following for the network of Fig. 6.12.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_S.
(e) V_G.
(f) V_D.

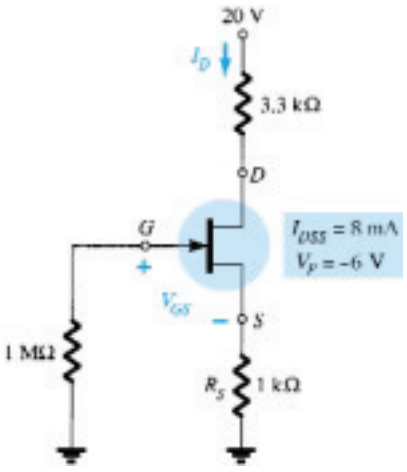


Figure 6.12 Example 6.2.

Solution

(a) The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4$ mA, we obtain

$$V_{GS} = -(4 \text{ mA})(1 \text{ k}\Omega) = -4 \text{ V}$$

The result is the plot of Fig. 6.13 as defined by the network.

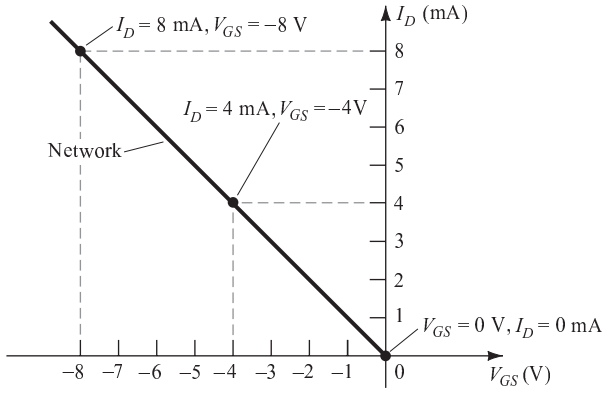


Figure 6.13 Sketching the self-bias line for the network of Fig. 6.12.

If we happen to choose $I_D = 8$ mA, the resulting value of V_{GS} would be -8 V, as shown on the same graph. In either case, the same straight line will result, clearly demonstrating that any appropriate value of I_D can be chosen as long as the corresponding value of V_{GS} as determined by Eq. (6.10) is employed. In addition, keep in mind that the value of V_{GS} could be chosen and the value of I_D calculated with the same resulting plot.

For Shockley's equation, if we choose $V_{GS} = V_P/2 = -3$ V, we find that $I_D = I_{DSS}/4 = 8 \text{ mA}/4 = 2$ mA, and the plot of Fig. 6.14 will result, representing the characteristics of the device. The solution is obtained by superimposing the network characteristics defined by Fig. 6.13 on the device characteristics of Fig. 6.14 and finding the point of intersection of the two as indicated on Fig. 6.15. The resulting operating point results in a quiescent value of gate-to-source voltage of

$$V_{GS_Q} = \mathbf{-2.6 \text{ V}}$$

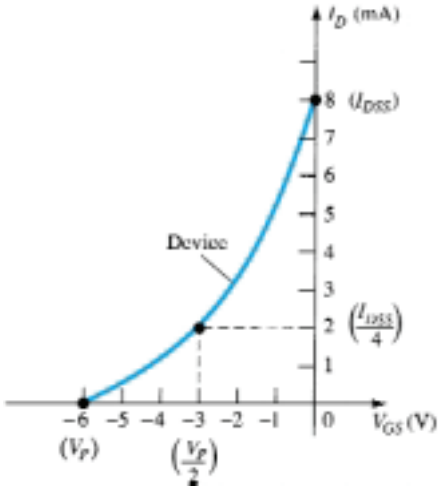


Figure 6.14 Sketching the device characteristics for the JFET of Fig. 6.12.

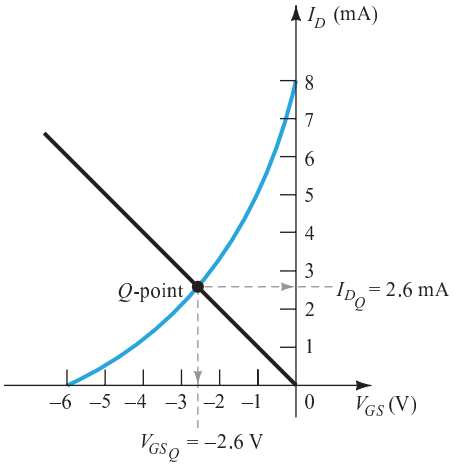


Figure 6.15 Determining the *Q*-point for the network of Fig. 6.12.

(b) At the quiescent point:

$$I_{DQ} = \mathbf{2.6\ mA}$$

(c) Eq. (6.11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\ \text{V} - (2.6\ \text{mA})(1\ \text{k}\Omega + 3.3\ \text{k}\Omega)$
$= 20\ \text{V} - 11.18\ \text{V}$
$= \mathbf{8.82\ V}$

(d) Eq. (6.12): $V_S = I_D R_S$
$= (2.6\ \text{mA})(1\ \text{k}\Omega)$
$= \mathbf{2.6\ V}$

(e) Eq. (6.13): $V_G = \mathbf{0\ V}$

(f) Eq. (6.14): $V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$

or $V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$

EXAMPLE 6.3

Find the quiescent point for the network of Fig. 6.12 if:
(a) $R_S = 100\ \Omega$.
(b) $R_S = 10\ \text{k}\Omega$.

Solution

Note Fig. 6.16.

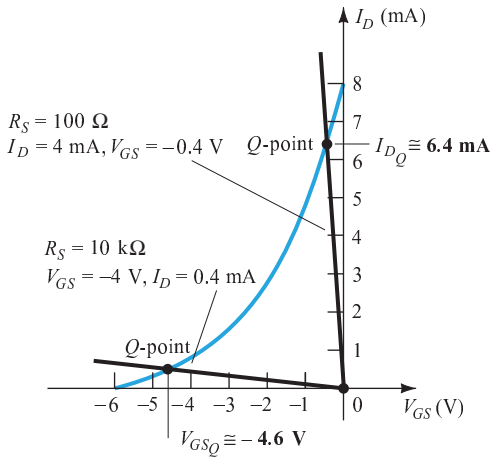


Figure 6.16 Example 6.3.

(a) With the I_D scale,

$$I_{DQ} \cong \mathbf{6.4\ mA}$$

From Eq. (6.10),

$$V_{GS_Q} \cong \mathbf{-0.64\ V}$$

(b) With the V_{GS} scale,

$$V_{GS_Q} \cong \mathbf{-4.6\ V}$$

From Eq. (6.10),

$$I_{DQ} \cong \mathbf{0.46\ mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis while increasing levels of R_S bring the load line closer to the V_{GS} axis.

EXAMPLE 6.4

Determine the following for the common-gate configuration of Fig. 6.17.

(a) V_{GSQ}.
(b) I_{DQ}.
(c) V_D.
(d) V_G.
(e) V_S.
(f) V_{DS}.

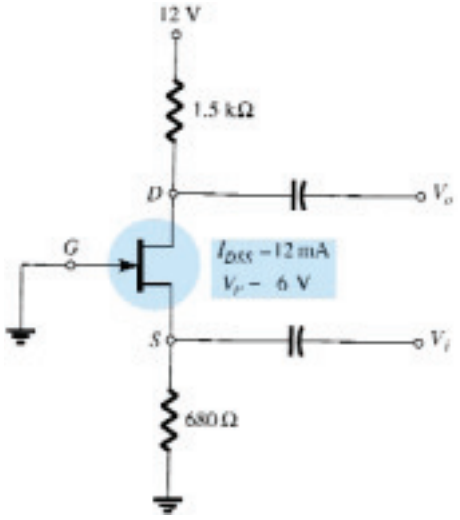


Figure 6.17 Example 6.4.

Solution

The grounded gate terminal and the location of the input establish strong similarities with the common-base BJT amplifier. Although different in appearance from the basic structure of Fig. 6.8, the resulting dc network of Fig. 6.18 has the same basic structure as Fig. 6.9. The dc analysis can therefore proceed in the same manner as recent examples.

(a) The transfer characteristics and load line appear in Fig. 6.19. In this case, the second point for the sketch of the load line was determined by choosing (arbitrarily) $I_D = 6$ mA and solving for V_{GS}. That is,

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

as shown in Fig. 6.19. The device transfer curve was sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}$$

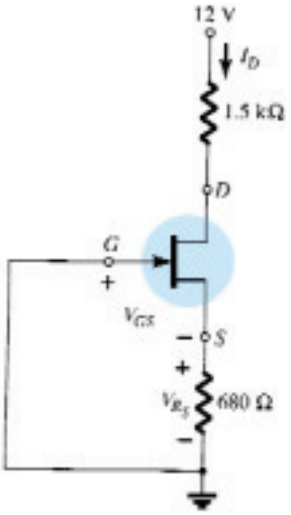


Figure 6.18 Sketching the dc equivalent of the network of Fig. 6.17.

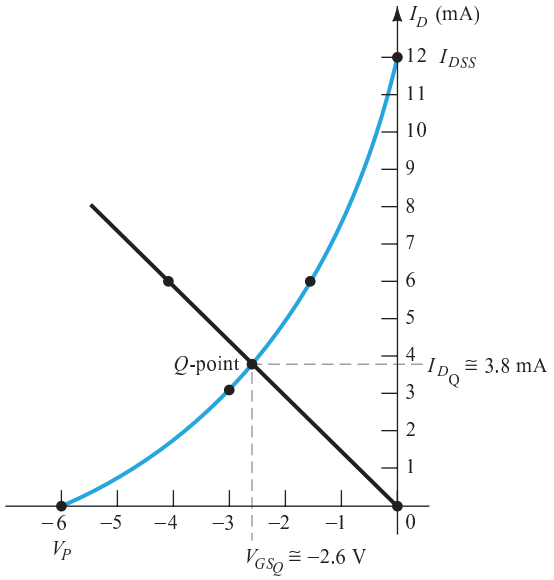


Figure 6.19 Determining the *Q*-point for the network of Fig. 6.17.

and the associated value of V_{GS}:

$$V_{GS} = \frac{V_P}{2} = -\frac{6\text{ V}}{2} = -3\text{ V}$$

as shown on Fig. 6.19. Using the resulting quiescent point of Fig. 6.19 results in

$$V_{GSQ} \cong \mathbf{-2.6\text{ V}}$$

(b) From Fig. 6.19,

$$I_{DQ} \cong \mathbf{3.8\text{ mA}}$$

(c) $V_D = V_{DD} - I_D R_D$
$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$
$= \mathbf{6.3\text{ V}}$

(d) $V_G = \mathbf{0\text{ V}}$

(e) $V_S = I_D R_S = (3.8\text{ mA})(680\ \Omega)$
$= \mathbf{2.58\text{ V}}$

(f) $V_{DS} = V_D - V_S$
$= 6.3\text{ V} - 2.58\text{ V}$
$= \mathbf{3.72\text{ V}}$

6.4 VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 6.20. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$ A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provided the link between input and output circuits for the BJT voltage-divider configuration while V_{GS} will do the same for the FET configuration.

The network of Fig. 6.20 is redrawn as shown in Fig. 6.21 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent. In addition, the source V_{DD} was separated into two equiv-

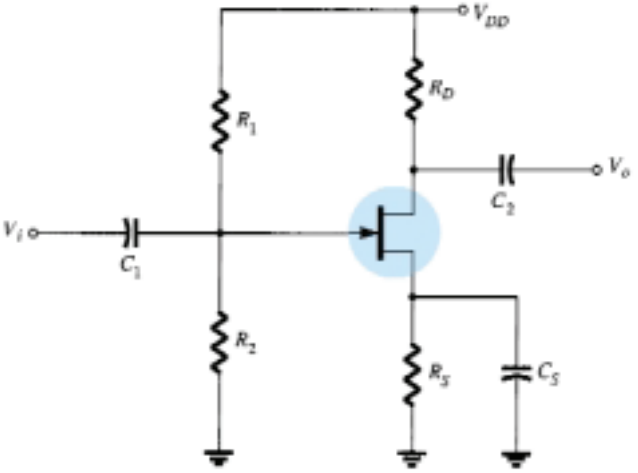


Figure 6.20 Voltage-divider bias arrangement.

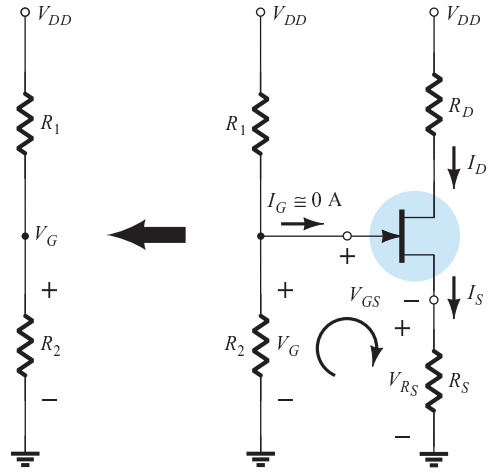


Figure 6.21 Redrawn network of Fig. 6.20 for dc analysis.

alent sources to permit a further separation of the input and output regions of the network. Since $I_G = 0$ A, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$ and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{6.15}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 6.21 will result in

$$V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S \tag{6.16}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D. The quantities V_G and R_S are fixed by the network construction. Equation (6.16) is still the equation for a straight line, but the origin is no longer a point in the plotting of the line. The procedure for plotting Eq. (6.16) is not a difficult one and will proceed as follows. Since any straight line requires two points to be defined, let us first use the fact that *anywhere on the horizontal axis* of Fig. 6.22 the current $I_D = 0$ mA. If we therefore *select* I_D to be 0 mA, we are in essence stating that we are somewhere on the horizontal axis. The exact location can be determined simply by substituting $I_D = 0$ mA into Eq. (6.16) and finding the resulting value of V_{GS} as follows:

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0 \text{ mA}) R_S$$

and

$$V_{GS} = V_G|_{I_D = 0 \text{ mA}} \tag{6.17}$$

The result specifies that whenever we plot Eq. (6.16), if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts. The point just determined appears in Fig. 6.22.

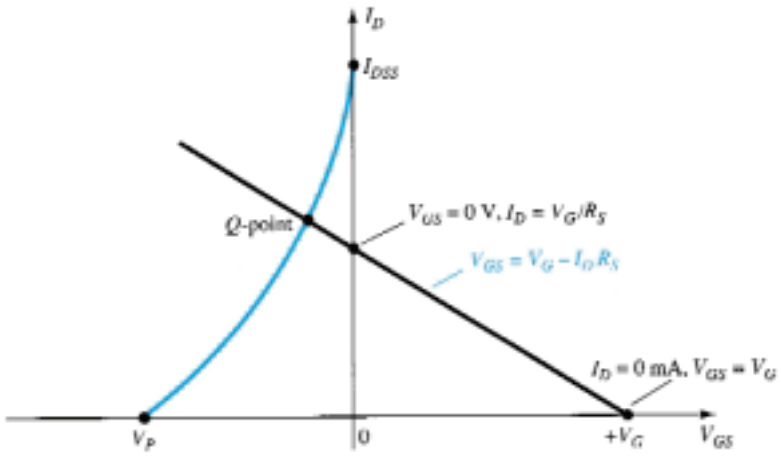


Figure 6.22 Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0$ V and solve for the resulting value of I_D:

$$V_{GS} = V_G - I_D R_S$$

$$0 \text{ V} = V_G - I_D R_S$$

and

$$\boxed{I_D = \left.\frac{V_G}{R_S}\right|_{V_{GS} = 0 \text{ V}}} \tag{6.18}$$

The result specifies that whenever we plot Eq. (6.16), if $V_{GS} = 0$ V, the level of I_D is determined by Eq. (6.18). This intersection also appears on Fig. 6.22.

The two points defined above permit the drawing of a straight line to represent Eq. (6.16). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS}.

Since the intersection on the vertical axis is determined by $I_D = V_G/R_S$ and V_G is fixed by the input network, increasing values of R_S will reduce the level of the I_D intersection as shown in Fig. 6.23. It is fairly obvious from Fig. 6.23 that:

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}.

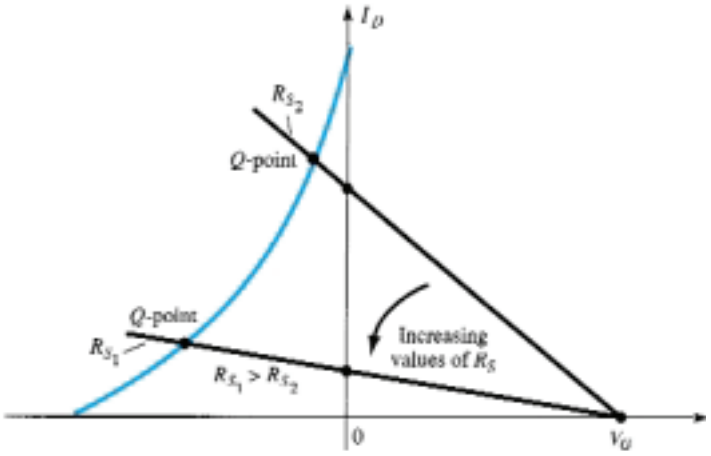


Figure 6.23 Effect of R_S on the resulting Q-point.

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)} \tag{6.19}$$

$$\boxed{V_D = V_{DD} - I_D R_D} \tag{6.20}$$

$$\boxed{V_S = I_D R_S} \tag{6.21}$$

$$\boxed{I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}} \tag{6.22}$$

EXAMPLE 6.5

Determine the following for the network of Fig. 6.24.

(a) I_{DQ} and V_{GSQ}.
(b) V_D.
(c) V_S.
(d) V_{DS}.
(e) V_{DG}.

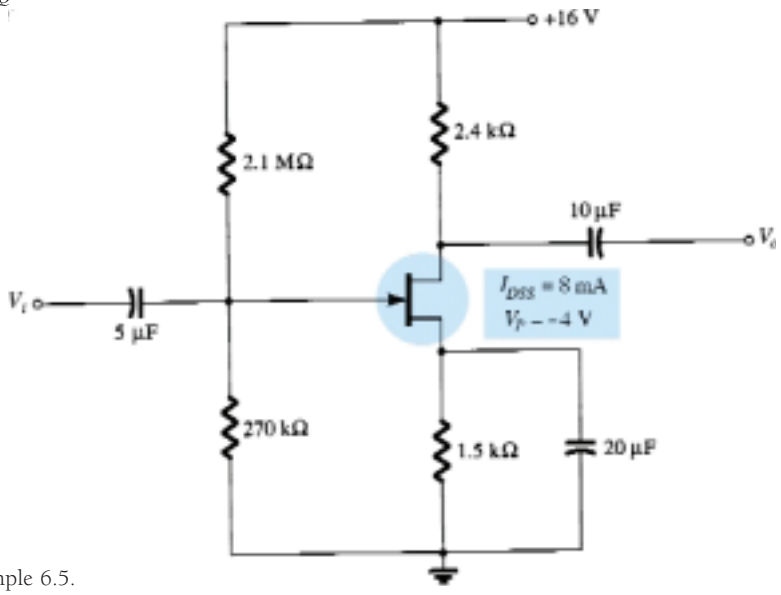


Figure 6.24 Example 6.5.

Solution

(a) For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 6.25. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega}$$

$$= 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$

When $I_D = 0$ mA:

$$V_{GS} = +1.82\text{ V}$$

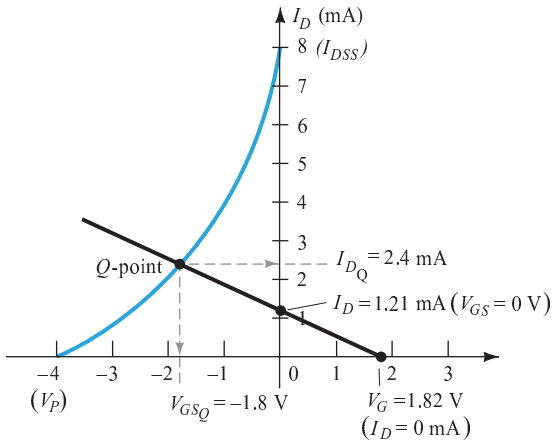


Figure 6.25 Determining the *Q*-point for the network of Fig. 6.24.

When $V_{GS} = 0$ V:

$$I_D = \frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$$

The resulting bias line appears on Fig. 6.25 with quiescent values of

$$I_{DQ} = \mathbf{2.4 \text{ mA}}$$

and

$$V_{GSQ} = \mathbf{-1.8 \text{ V}}$$

(b) $V_D = V_{DD} - I_D R_D$
$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega)$
$= \mathbf{10.24 \text{ V}}$

(c) $V_S = I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega)$
$= \mathbf{3.6 \text{ V}}$

(d) $V_{DS} = V_{DD} - I_D(R_D + R_S)$
$= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega)$
$= \mathbf{6.64 \text{ V}}$
or $V_{DS} = V_D - V_S = 10.24 \text{ V} - 3.6 \text{ V}$
$= \mathbf{6.64 \text{ V}}$

(e) Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$
$$= 10.24 \text{ V} - 1.82 \text{ V}$$
$$= \mathbf{8.42 \text{ V}}$$

Although the basic construction of the network in the next example is quite different from the voltage-divider bias arrangement, the resulting equations require a solution very similar to that just described. Note that the network employs a supply at the drain and source.

EXAMPLE 6.6

Determine the following for the network of Fig. 6.26.
(a) I_{DQ} and V_{GSQ}.
(b) V_{DS}.
(c) V_D.
(d) V_S.

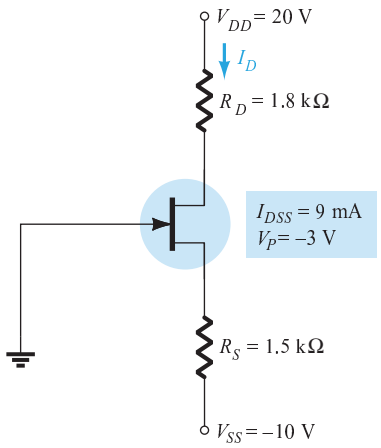


Figure 6.26 Example 6.6.

Solution

(a) An equation for V_{GS} in terms of I_D is obtained by applying Kirchhoff's voltage law to the input section of the network as redrawn in Fig. 6.27.

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

or
$$V_{GS} = V_{SS} - I_S R_S$$

but
$$I_S = I_D$$

and
$$\boxed{V_{GS} = V_{SS} - I_D R_S} \tag{6.23}$$

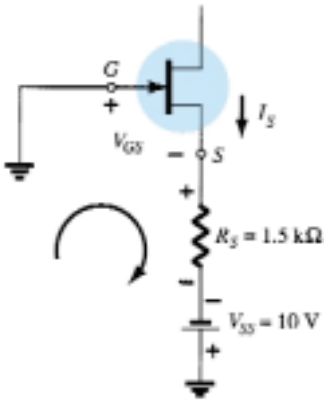


Figure 6.27 Determining the network equation for the configuration of Fig. 6.26.

The result is an equation very similar in format to Eq. (6.16) that can be superimposed on the transfer characteristics using the procedure described for Eq. (6.16). That is, for this example,

$$V_{GS} = 10\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

For $I_D = 0$ mA,

$$V_{GS} = V_{SS} = 10\ \text{V}$$

For $V_{GS} = 0$ V,

$$0 = 10\ \text{V} - I_D(1.5\ \text{k}\Omega)$$

and
$$I_D = \frac{10\ \text{V}}{1.5\ \text{k}\Omega} = 6.67\ \text{mA}$$

The resulting plot points are identified on Fig. 6.28.

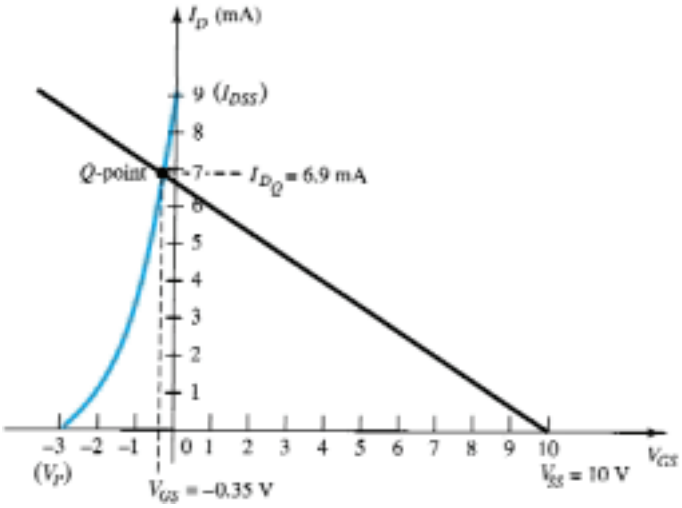


Figure 6.28 Determining the *Q*-point for the network of Fig. 6.26.

The transfer characteristics are sketched using the plot point established by $V_{GS} = V_P/2 = -3\ \text{V}/2 = -1.5\ \text{V}$ and $I_D = I_{DSS}/4 = 9\ \text{mA}/4 = 2.25\ \text{mA}$, as also appearing on Fig. 6.28. The resulting operating point establishes the following quiescent levels:

$$I_{D_Q} = \mathbf{6.9\ mA}$$

$$V_{GS_Q} = \mathbf{-0.35\ V}$$

(b) Applying Kirchhoff's voltage law to the output side of Fig. 6.26 will result in

$$-V_{SS} + I_S R_S + V_{DS} + I_D R_D - V_{DD} = 0$$

Substituting $I_S = I_D$ and rearranging gives

$$V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S) \tag{6.24}$$

which for this example results in

$$\begin{aligned} V_{DS} &= 20\text{ V} + 10\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega + 1.5\text{ k}\Omega) \\ &= 30\text{ V} - 22.77\text{ V} \\ &= \mathbf{7.23\text{ V}} \end{aligned}$$

(c) $V_D = V_{DD} - I_D R_D$
$= 20\text{ V} - (6.9\text{ mA})(1.8\text{ k}\Omega) = 20\text{ V} - 12.42\text{ V}$
$= \mathbf{7.58\text{ V}}$

(d) $V_{DS} = V_D - V_S$
or $V_S = V_D - V_{DS}$
$= 7.58\text{ V} - 7.23\text{ V}$
$= \mathbf{0.35\text{ V}}$

6.5 DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network. A few examples will reveal the impact of the change in device on the resulting analysis.

EXAMPLE 6.7

For the *n*-channel depletion-type MOSFET of Fig. 6.29, determine:
(a) I_{DQ} and V_{GSQ}.
(b) V_{DS}.

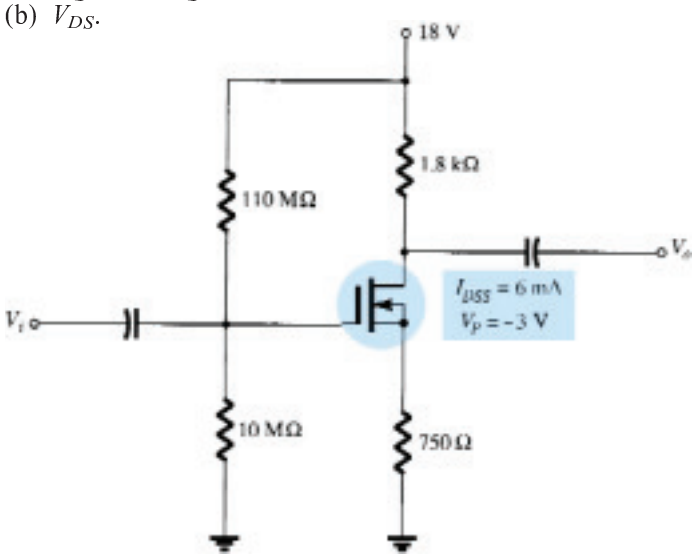


Figure 6.29 Example 6.7.

Solution

(a) For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778)$$

$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. 6.30. Proceeding as described for JFETs, we have:

$$\text{Eq. (6.15):}\quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$

$$\text{Eq. (6.16):}\quad V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

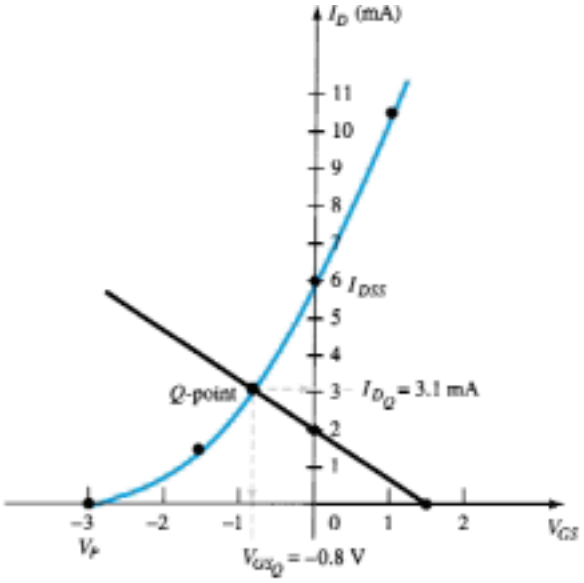


Figure 6.30 Determining the *Q*-point for the network of Fig. 6.29.

Setting $I_D = 0\text{ mA}$ results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0\text{ V}$ yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The plot points and resulting bias line appear in Fig. 6.30. The resulting operating point:

$$I_{D_Q} = \mathbf{3.1\text{ mA}}$$

$$V_{GS_Q} = \mathbf{-0.8\text{ V}}$$

(b) Eq. (6.19): $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega)$

$\cong \mathbf{10.1\text{ V}}$

EXAMPLE 6.8

Repeat Example 6.7 with $R_S = 150\ \Omega$.

Solution

(a) The plot points are the same for the transfer curve as shown in Fig. 6.31. For the bias line,

$$V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(150\ \Omega)$$

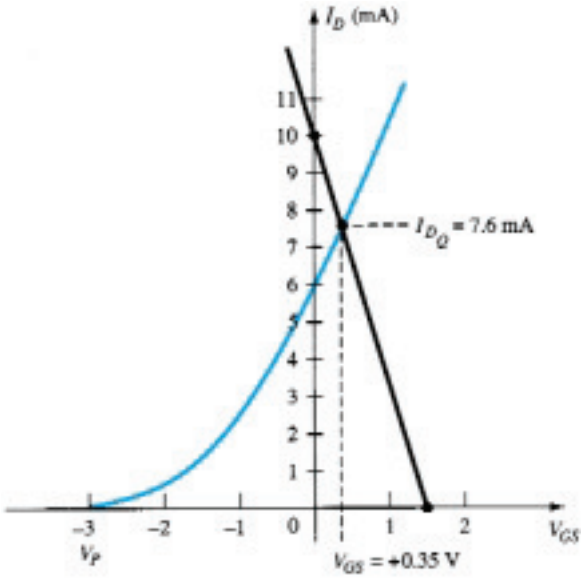


Figure 6.31 Example 6.8.

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{150\ \Omega} = 10\text{ mA}$$

The bias line is included on Fig. 6.31. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result:

$$I_{D_Q} = \mathbf{7.6\text{ mA}}$$

$$V_{GS_Q} = \mathbf{+0.35\text{ V}}$$

(b) Eq. (6.19): $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18\text{ V} - (7.6\text{ mA})(1.8\text{ k}\Omega + 150\ \Omega)$

$= \mathbf{3.18\text{ V}}$

EXAMPLE 6.9

Determine the following for the network of Fig. 6.32.

(a) I_{DQ} and V_{GSQ}.
(b) V_D.

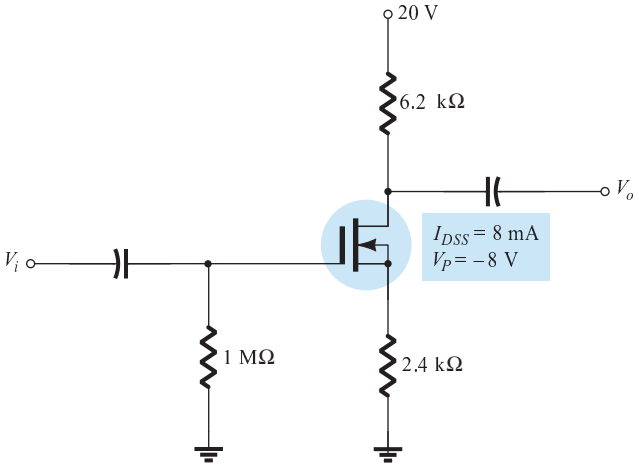


Figure 6.32 Example 6.9.

Solution

(a) The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than zero volts. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0$ V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8 \text{ mA}}{4} = 2 \text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8 \text{ V}}{2} = -4 \text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2 \text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8 \text{ mA}\left(1 - \frac{+2 \text{ V}}{-8 \text{ V}}\right)^2$$

$$= 12.5 \text{ mA}$$

The resulting transfer curve appears in Fig. 6.33. For the network bias line, at $V_{GS} = 0$ V, $I_D = 0$ mA. Choosing $V_{GS} = -6$ V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6 \text{ V}}{2.4 \text{ k}\Omega} = 2.5 \text{ mA}$$

The resulting Q-point:

$$I_{D_Q} = \mathbf{1.7 \text{ mA}}$$
$$V_{GS_Q} = \mathbf{-4.3 \text{ V}}$$

(b) $V_D = V_{DD} - I_D R_D$
$= 20 \text{ V} - (1.7 \text{ mA})(6.2 \text{ k}\Omega)$
$= \mathbf{9.46 \text{ V}}$

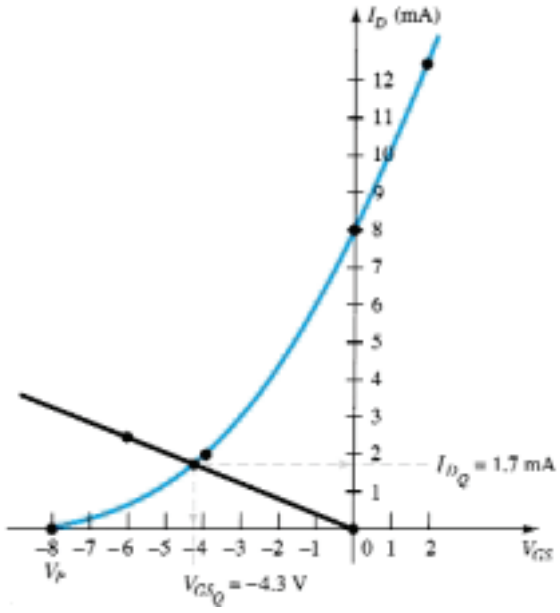


Figure 6.33 Determining the *Q*-point for the network of Fig. 6.32.

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

EXAMPLE 6.10

Determine V_{DS} for the network of Fig. 6.34.

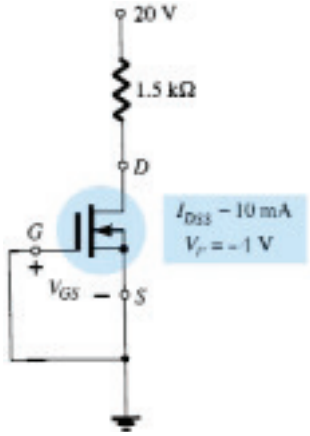


Figure 6.34 Example 6.10.

Solution

The direct connection between the gate and source terminals requires that

$$V_{GS} = 0 \text{ V}$$

Since V_{GS} is fixed at 0 V, the drain current must be I_{DSS} (by definition). In other words,

$$V_{GS_Q} = \mathbf{0 \text{ V}}$$

and

$$I_{D_Q} = \mathbf{10 \text{ mA}}$$

There is therefore no need to draw the transfer curve and

$$V_D = V_{DD} - I_D R_D = 20 \text{ V} - (10 \text{ mA})(1.5 \text{ k}\Omega)$$
$$= 20 \text{ V} - 15 \text{ V}$$
$$= \mathbf{5 \text{ V}}$$

6.6 ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(\text{Th})}$, as shown in Fig. 6.35. For levels of V_{GS} greater than $V_{GS(\text{Th})}$, the drain current is defined by

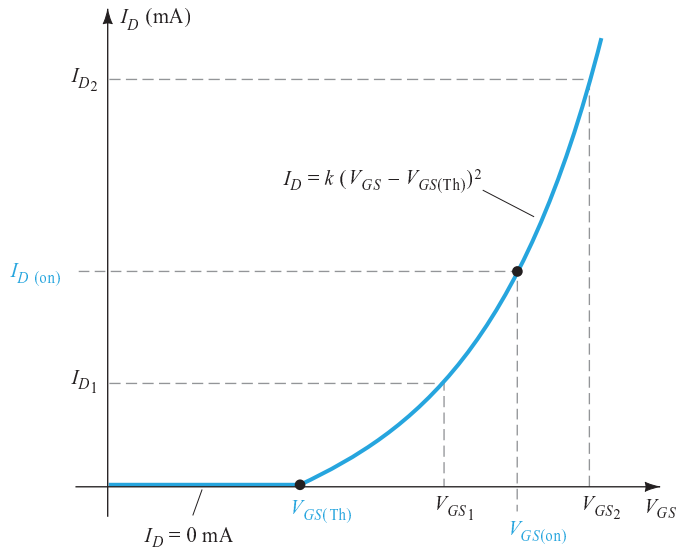


Figure 6.35 Transfer characteristics of an *n*-channel enhancement-type MOSFET.

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2 \tag{6.25}$$

Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(\text{on})}$) and its corresponding level of $V_{GS(\text{on})}$, two points are defined immediately as shown in Fig. 6.35. To complete the curve, the constant k of Eq. (6.25) must be determined from the specification sheet data by substituting into Eq. (6.25) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$I_{D(\text{on})} = k(V_{GS(\text{on})} - V_{GS(\text{Th})})^2$$

and

$$k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2} \tag{6.26}$$

Once k is defined, other levels of I_D can be determined for chosen values of V_{GS}. Typically, a point between $V_{GS(\text{Th})}$ and $V_{GS(\text{on})}$ and one just greater than $V_{GS(\text{on})}$ will provide a sufficient number of points to plot Eq. (6.25) (note I_{D_1} and I_{D_2} on Fig. 6.35).

Feedback Biasing Arrangement

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 6.36. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on." Since $I_G = 0$ mA and $V_{R_G} = 0$ V, the dc equivalent network appears as shown in Fig. 6.37.

A direct connection now exists between drain and gate, resulting in

$$V_D = V_G$$

and

$$V_{DS} = V_{GS} \tag{6.27}$$

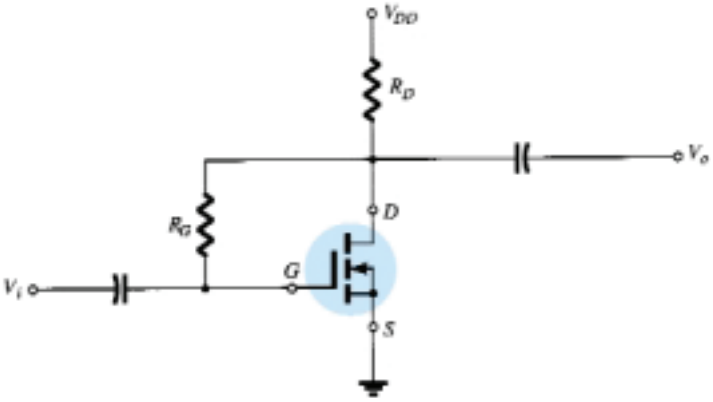


Figure 6.36 Feedback biasing arrangement.

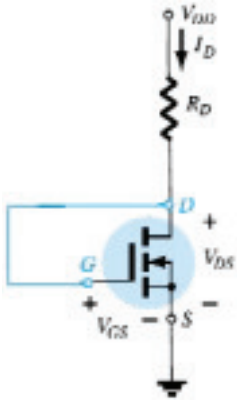


Figure 6.37 DC equivalent of the network of Fig. 6.36.

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D$$

which becomes the following after substituting Eq. (6.27):

$$\boxed{V_{GS} = V_{DD} - I_D R_D} \tag{6.28}$$

The result is an equation that relates the same two variables as Eq. (6.25), permitting the plot of each on the same set of axes.

Since Eq. (6.28) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Substituting $I_D = 0$ mA into Eq. (6.28) gives

$$\boxed{V_{GS} = V_{DD}|_{I_D = 0\text{ mA}}} \tag{6.29}$$

Substituting $V_{GS} = 0$ V into Eq. (6.28), we have

$$\boxed{I_D = \left.\frac{V_{DD}}{R_D}\right|_{V_{GS} = 0\text{ V}}} \tag{6.30}$$

The plots defined by Eqs. (6.25) and (6.28) appear in Fig. 6.38 with the resulting operating point.

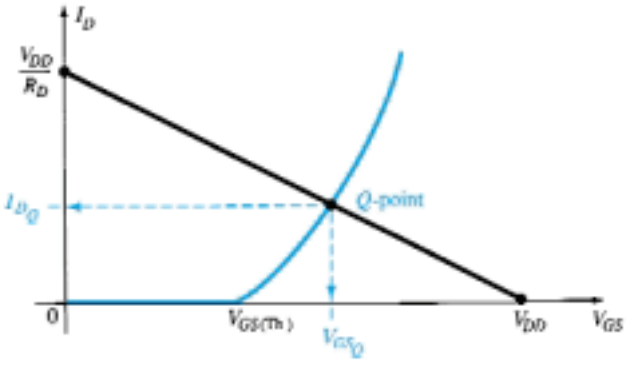


Figure 6.38 Determining the *Q*-point for the network of Fig. 6.36.

Determine I_{DQ} and V_{DSQ} for the enhancement-type MOSFET of Fig. 6.39. *EXAMPLE 6.11*

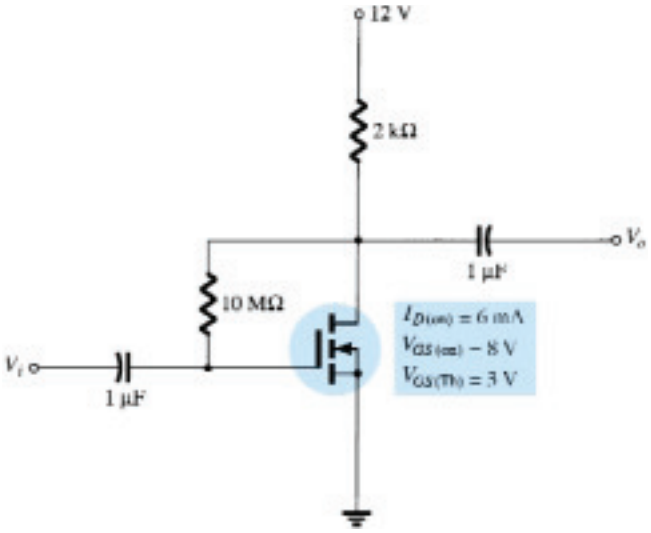


Figure 6.39 Example 6.11.

Solution

Plotting the Transfer Curve:

Two points are defined immediately as shown in Fig. 6.40. Solving for k:

$$\text{Eq. (6.26):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{6 \text{ mA}}{(8 \text{ V} - 3 \text{ V})^2} = \frac{6 \times 10^{-3}}{25} \text{A/v}^2$$

$$= \mathbf{0.24 \times 10^{-3} \text{ A/V}^2}$$

For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6 \text{ V} - 3 \text{ V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16 \text{ mA}$$

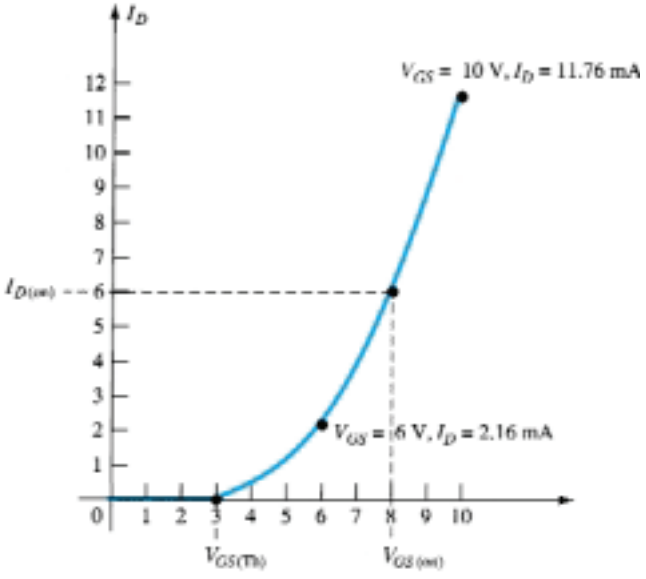


Figure 6.40 Plotting the transfer curve for the MOSFET of Fig. 6.39.

as shown on Fig. 6.40. For $V_{GS} = 10$ V (slightly greater than $V_{GS(\text{Th})}$):

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$
$$= 11.76\text{ mA}$$

as also appearing on Fig. 6.40. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 6.40.

For the Network Bias Line:

$$V_{GS} = V_{DD} - I_D R_D$$
$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$

Eq. (6.29): $V_{GS} = V_{DD} = 12\text{ V}\big|_{I_D = 0\text{ mA}}$

Eq. (6.30): $I_D = \dfrac{V_{DD}}{R_D} = \dfrac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}\big|_{V_{GS} = 0\text{ V}}$

The resulting bias line appears in Fig. 6.41.

At the operating point:

$$I_{D_Q} = \mathbf{2.75\text{ mA}}$$

and $$V_{GS_Q} = 6.4\text{ V}$$

with $$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\text{ V}}$$

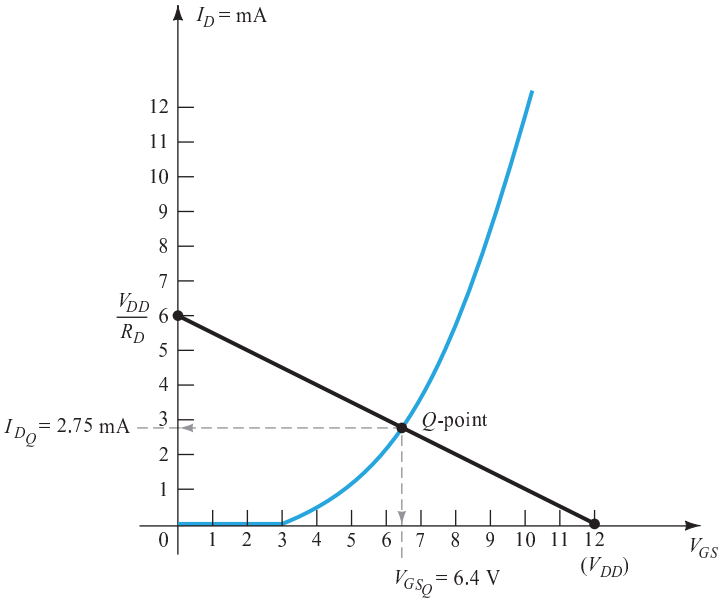


Figure 6.41 Determining the *Q*-point for the network of Fig. 6.39.

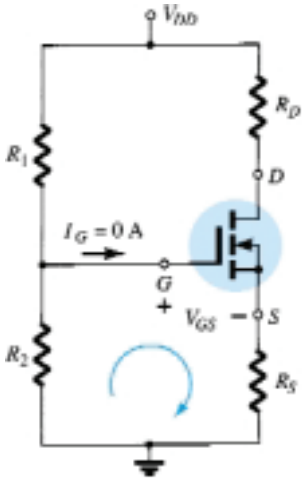


Figure 6.42 Voltage-divider biasing arrangement for an *n*-channel enhancement MOSFET.

Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 6.42. The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{6.31}$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 6.42 will result in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$\boxed{V_{GS} = V_G - I_D R_S} \tag{6.32}$$

For the output section:

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)} \tag{6.33}$$

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (6.32) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{D_Q} and V_{GS_Q} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

EXAMPLE 6.12

Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 6.43.

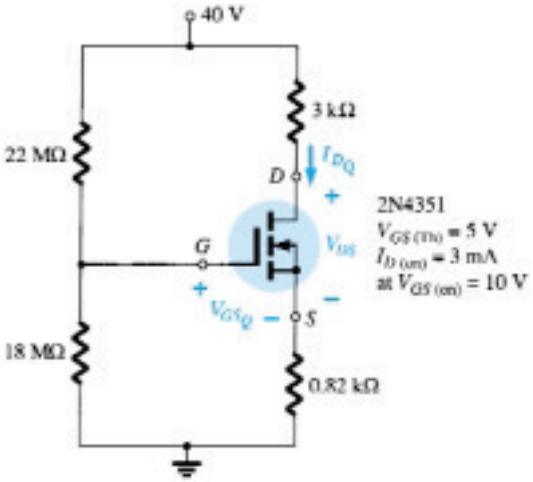


Figure 6.43 Example 6.12.

Solution

Network:

$$\text{Eq. (6.31):} \quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\ \text{M}\Omega)(40\ \text{V})}{22\ \text{M}\Omega + 18\ \text{M}\Omega} = 18\ \text{V}$$

$$\text{Eq. (6.32):} \quad V_{GS} = V_G - I_D R_S = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

When $I_D = 0$ mA,

$$V_{GS} = 18\ \text{V} - (0\ \text{mA})(0.82\ \text{k}\Omega) = 18\ \text{V}$$

as appearing on Fig. 6.44. When $V_{GS} = 0$ V,

$$V_{GS} = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$0 = 18\ \text{V} - I_D(0.82\ \text{k}\Omega)$$

$$I_D = \frac{18\ \text{V}}{0.82\ \text{k}\Omega} = 21.95\ \text{mA}$$

as appearing on Fig. 6.44.

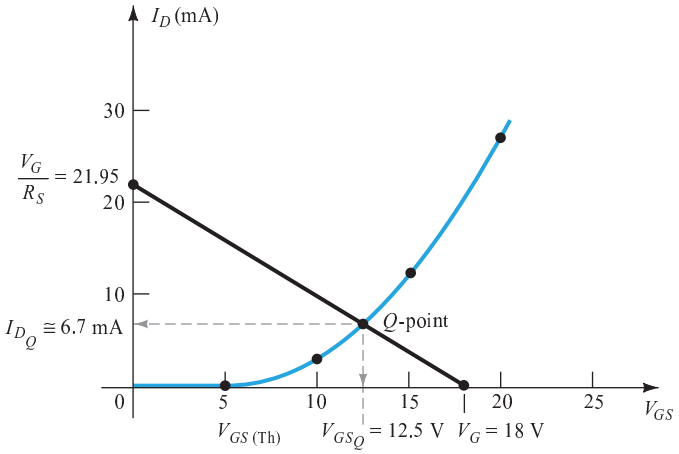


Figure 6.44 Determining the *Q*-point for the network of Example 6.12.

Device:

$$V_{GS(\text{Th})} = 5\text{ V}, \qquad I_{D(\text{on})} = 3\text{ mA with } V_{GS(\text{on})} = 10\text{ V}$$

$$\text{Eq. (6.26):} \quad k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$$

$$= \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

and

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

which is plotted on the same graph (Fig. 6.44). From Fig. 6.44,

$$I_{D_Q} \cong \mathbf{6.7\text{ mA}}$$

$$V_{GS_Q} = \mathbf{12.5\text{ V}}$$

$$\text{Eq. (6.33):} \quad V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$= 40\text{ V} - (6.7\text{ mA})(0.82\text{ k}\Omega + 3.0\text{ k}\Omega)$$

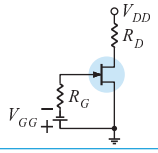
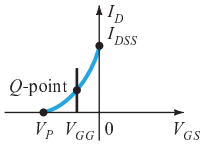
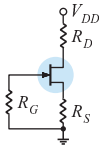
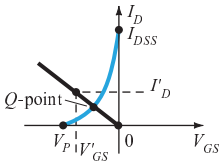
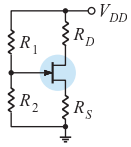
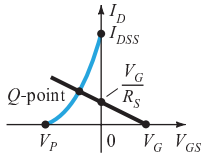
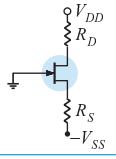
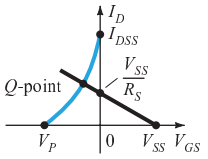
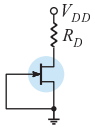
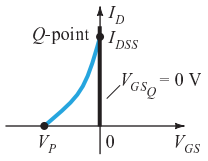
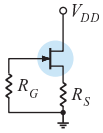
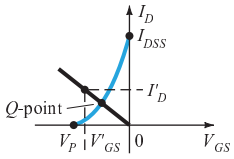
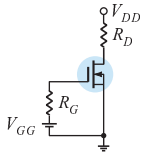
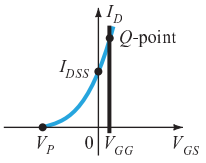
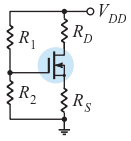
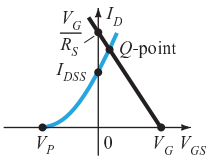
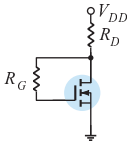
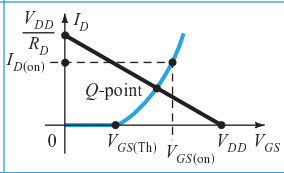
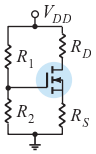
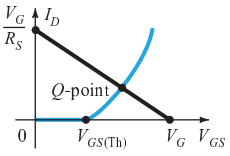
$$= 40\text{ V} - 25.6\text{ V}$$

$$= \mathbf{14.4\text{ V}}$$

6.7 SUMMARY TABLE

Now that the most popular biasing arrangements for the various FETs have been introduced, Table 6.1 reviews the basic results and demonstrates the similarity in approach for a number of configurations. It also reveals that the general analysis of dc configurations for FETs is not overly complex. Once the transfer characteristics are established, the network self-bias line can be drawn and the *Q*-point determined at the intersection of the device transfer characteristic and the network bias curve. The remaining analysis is simply an application of the basic laws of circuit analysis.

TABLE 6.1 FET Bias Configurations

Type	*Configuration*	*Pertinent Equations*	*Graphical Solution*
JFET Fixed-bias		$V_{GSQ} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($V_{GSQ} = 0$ V)		$V_{GSQ} = 0$ V $I_{DQ} = I_{DSS}$	
JFET ($R_D = 0\ \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
Depletion-type MOSFET Fixed-bias		$V_{GSQ} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement- type MOSFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	

6.8 COMBINATION NETWORKS

Now that the dc analysis of a variety of BJT and FET configurations is established, the opportunity to analyze networks with both types of devices presents itself. Fundamentally, the analysis simply requires that we *first* approach the device that will provide a terminal voltage or current level. The door is then usually open to calculate other quantities and concentrate on the remaining unknowns. These are usually particularly interesting problems due to the challenge of finding the opening and then using the results of the past few sections and Chapter 5 to find the important quantities for each device. The equations and relationships used are simply those we have now employed on more than one occasion—no need to develop any new methods of analysis.

EXAMPLE 6.13 Determine the levels of V_D and V_C for the network of Fig. 6.45.

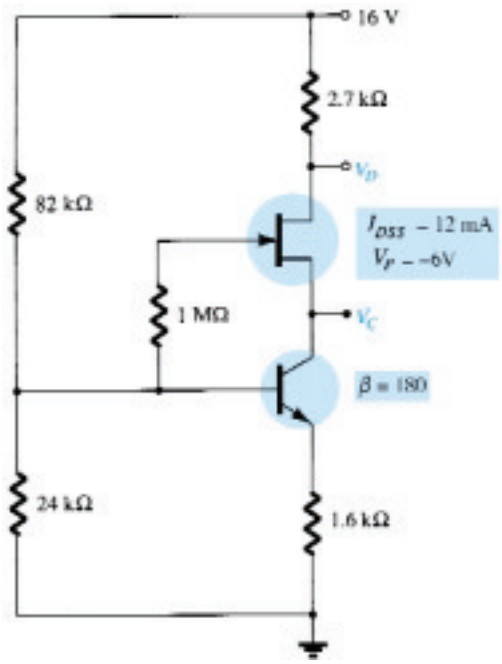


Figure 6.45 Example 6.13.

Solution

From past experience we now realize that V_{GS} is typically an important quantity to determine or write an equation for when analyzing JFET networks. Since V_{GS} is a level for which an immediate solution is not obvious, let us turn our attention to the transistor configuration. The voltage-divider configuration is one where the approximate technique can be applied ($\beta R_E = (180 \times 1.6\,\text{k}\Omega) = 288\,\text{k}\Omega > 10R_2 = 240\,\text{k}\Omega$), permitting a determination of V_B using the voltage-divider rule on the input circuit.

For V_B:

$$V_B = \frac{24\,\text{k}\Omega(16\text{ V})}{82\,\text{k}\Omega + 24\,\text{k}\Omega} = 3.62\text{ V}$$

Using the fact that $V_{BE} = 0.7$ V results in

$$V_E = V_B - V_{BE} = 3.62\text{ V} - 0.7\text{ V}$$
$$= 2.92\text{ V}$$

and $$I_E = \frac{V_{RE}}{R_E} = \frac{V_E}{R_E} = \frac{2.92\ \text{V}}{1.6\ \text{k}\Omega} = 1.825\ \text{mA}$$

with $$I_C \cong I_E = 1.825\ \text{mA}$$

Continuing, we find for this configuration that

$$I_D = I_S = I_C$$

and $$V_D = 16\ \text{V} - I_D(2.7\ \text{k}\Omega)$$
$$= 16\ \text{V} - (1.825\ \text{mA})(2.7\ \text{k}\Omega) = 16\ \text{V} - 4.93\ \text{V}$$
$$= \mathbf{11.07\ V}$$

The question of how to determine V_C is not as obvious. Both V_{CE} and V_{DS} are unknown quantities preventing us from establishing a link between V_D and V_C or from V_E to V_D. A more careful examination of Fig. 6.45 reveals that V_C is linked to V_B by V_{GS} (assuming that $V_{R_G} = 0$ V). Since we know V_B if we can find V_{GS}, V_C can be determined from

$$V_C = V_B - V_{GS}$$

The question then arises as to how to find the level of V_{GS_Q} from the quiescent value of I_D. The two are related by Shockley's equation:

$$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2$$

and V_{GS_Q} could be found mathematically by solving for V_{GS_Q} and substituting numerical values. However, let us turn to the graphical approach and simply work in the reverse order employed in the preceding sections. The JFET transfer characteristics are first sketched as shown in Fig. 6.46. The level of I_{D_Q} is then established by a horizontal line as shown in the same figure. V_{GS_Q} is then determined by dropping a line down from the operating point to the horizontal axis, resulting in

$$V_{GS_Q} = \mathbf{-3.7\ V}$$

The level of V_C:

$$V_C = V_B - V_{GS_Q} = 3.62\ \text{V} - (-3.7\ \text{V})$$
$$= \mathbf{7.32\ V}$$

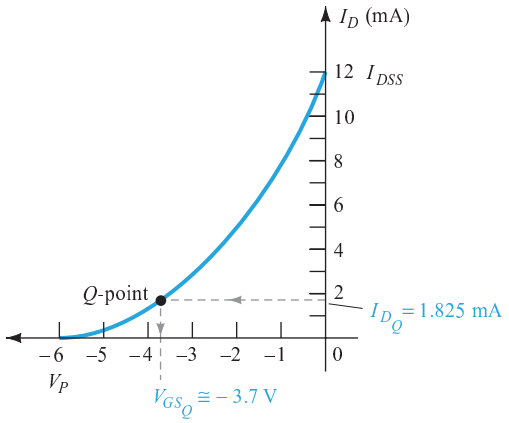


Figure 6.46 Determining the *Q*-point for the network of Fig. 6.45.

EXAMPLE 6.14

Determine V_D for the network of Fig. 6.47.

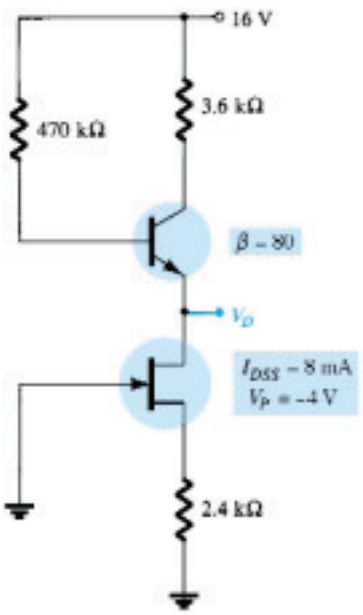


Figure 6.47 Example 6.14.

Solution

In this case, there is no obvious path to determine a voltage or current level for the transistor configuration. However, turning to the self-biased JFET, an equation for V_{GS} can be derived and the resulting quiescent point determined using graphical techniques. That is,

$$V_{GS} = -I_D R_S = -I_D(2.4\ \text{k}\Omega)$$

resulting in the self-bias line appearing in Fig. 6.48 that establishes a quiescent point at

$$V_{GS_Q} = -2.6\ \text{V}$$
$$I_{D_Q} = 1\ \text{mA}$$

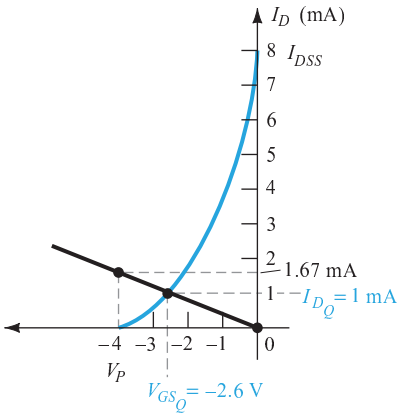


Figure 6.48 Determining the *Q*-point for the network of Fig. 6.47.

For the transistor,

$$I_E \cong I_C = I_D = 1\ \text{mA}$$

and

$$I_B = \frac{I_C}{\beta} = \frac{1\ \text{mA}}{80} = 12.5\ \mu\text{A}$$

$$V_B = 16\ \text{V} - I_B(470\ \text{k}\Omega)$$
$$= 16\ \text{V} - (12.5\ \mu\text{A})(470\ \text{k}\Omega) = 16\ \text{V} - 5.875\ \text{V}$$
$$= 10.125\ \text{V}$$

and

$$V_E = V_D = V_B - V_{BE}$$
$$= 10.125\ \text{V} - 0.7\ \text{V}$$
$$= \mathbf{9.425\ V}$$

6.9 DESIGN

The design process is one that is not limited solely to dc conditions. The area of application, level of amplification desired, signal strength, and operating conditions are just a few of the conditions that enter into the total design process. However, we will first concentrate on establishing the chosen dc conditions.

For example, if the levels of V_D and I_D are specified for the network of Fig. 6.49, the level of V_{GS_Q} can be determined from a plot of the transfer curve and R_S can then be determined from $V_{GS} = -I_D R_S$. If V_{DD} is specified, the level of R_D can then be calculated from $R_D = (V_{DD} - V_D)/I_D$. Of course, the value of R_S and R_D may not be standard commercial values, requiring that the nearest commercial value be employed. However, with the tolerance (range of values) normally specified for the parameters of a network, the slight variation due to the choice of standard values will seldom cause a real concern in the design process.

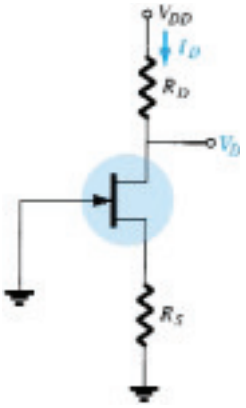


Figure 6.49 Self-bias configuration to be designed.

The above is only one possibility for the design phase involving the network of Fig. 6.49. It is possible that only V_{DD} and R_D are specified together with the level of V_{DS}. The device to be employed may have to be specified along with the level of R_S. It appears logical that the device chosen should have a maximum V_{DS} greater than the specified value by a safe margin.

In general, it is good design practice for linear amplifiers to choose operating points that do not crowd the saturation level (I_{DSS}) or cutoff (V_P) regions. Levels of V_{GS_Q} close to $V_P/2$ or I_{D_Q} near $I_{DSS}/2$ are certainly reasonable starting points in the design. Of course, in every design procedure the maximum levels of I_D and V_{DS} as appearing on the specification sheet must not be considered as exceeded.

The examples to follow have a design or synthesis orientation in that specific levels are provided and network parameters such as R_D, R_S, V_{DD}, and so on, must be determined. In any case, the approach is in many ways the opposite of that described in previous sections. In some cases, it is just a matter of applying Ohm's law in its appropriate form. In particular, if resistive levels are requested, the result is often obtained simply by applying Ohm's law in the following form:

$$R_{\text{unknown}} = \frac{V_R}{I_R} \tag{6.34}$$

where V_R and I_R are often parameters that can be found directly from the specified voltage and current levels.

EXAMPLE 6.15

For the network of Fig. 6.50, the levels of V_{D_Q} and I_{D_Q} are specified. Determine the required values of R_D and R_S. What are the closest standard commercial values?

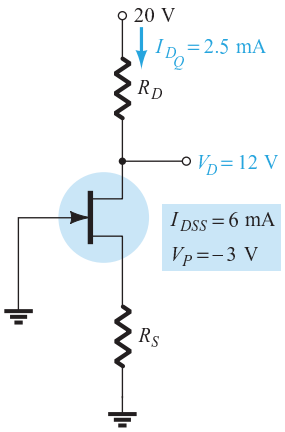


Figure 6.50 Example 6.15.

Solution

As defined by Eq. (6.34),

$$R_D = \frac{V_{R_D}}{I_{D_Q}} = \frac{V_{DD} - V_{D_Q}}{I_{D_Q}}$$

and

$$= \frac{20\text{ V} - 12\text{ V}}{2.5\text{ mA}} = \frac{8\text{ V}}{2.5\text{ mA}} = \mathbf{3.2\ k\Omega}$$

Plotting the transfer curve in Fig. 6.51 and drawing a horizontal line at $I_{D_Q} = 2.5$ mA will result in $V_{GS_Q} = -1$ V, and applying $V_{GS} = -I_D R_S$ will establish the level of R_S:

$$R_S = \frac{-(V_{GS_Q})}{I_{D_Q}} = \frac{-(-1\text{ V})}{2.5\text{ mA}} = \mathbf{0.4\ k\Omega}$$

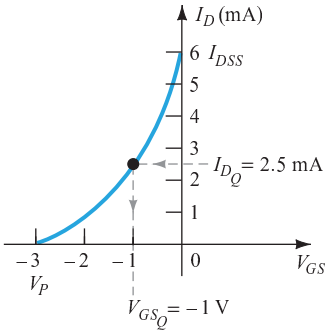


Figure 6.51 Determining V_{GS_Q} for the network of Fig. 6.50.

The nearest standard commercial values are

$$R_D = 3.2\text{ k}\Omega \Rightarrow \mathbf{3.3\ k\Omega}$$

$$R_S = 0.4\text{ k}\Omega \Rightarrow \mathbf{0.39\ k\Omega}$$

EXAMPLE 6.16

For the voltage-divider bias configuration of Fig. 6.52, if $V_D = 12$ V and $V_{GS_Q} = -2$ V, determine the value of R_S.

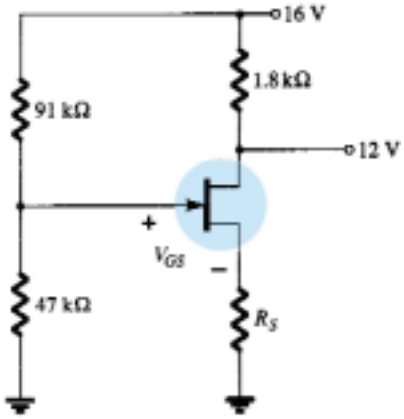


Figure 6.52 Example 6.16.

Solution

The level of V_G is determined as follows:

$$V_G = \frac{47\text{ k}\Omega(16\text{ V})}{47\text{ k}\Omega + 91\text{ k}\Omega} = 5.44\text{ V}$$

with

$$I_D = \frac{V_{DD} - V_D}{R_D}$$

$$= \frac{16\text{ V} - 12\text{ V}}{1.8\text{ k}\Omega} = 2.22\text{ mA}$$

The equation for V_{GS} is then written and the known values substituted:

$$V_{GS} = V_G - I_D R_S$$

$$-2\text{ V} = 5.44\text{ V} - (2.22\text{ mA})R_S$$

$$-7.44\text{ V} = -(2.22\text{ mA})R_S$$

and

$$R_S = \frac{7.44\text{ V}}{2.22\text{ mA}} = \mathbf{3.35\ k\Omega}$$

The nearest standard commercial value is 3.3 kΩ.

EXAMPLE 6.17

The levels of V_{DS} and I_D are specified as $V_{DS} = \frac{1}{2}V_{DD}$ and $I_D = I_{D(\text{on})}$ for the network of Fig. 6.53. Determine the level of V_{DD} and R_D.

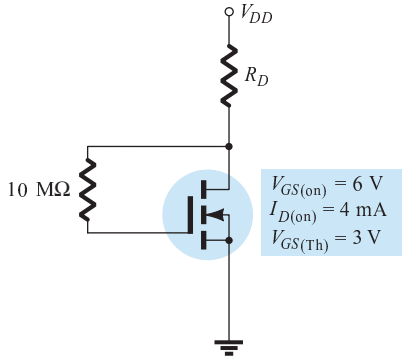


Figure 6.53 Example 6.17.

Solution

Given $I_D = I_{D(\text{on})} = 4$ mA and $V_{GS} = V_{GS(\text{on})} = 6$ V, for this configuration,

$$V_{DS} = V_{GS} = \tfrac{1}{2}V_{DD}$$

and

$$6 \text{ V} = \tfrac{1}{2}V_{DD}$$

so that

$$V_{DD} = \mathbf{12\ V}$$

Applying Eq. (6.34) yields

$$R_D = \frac{V_{R_D}}{I_D} = \frac{V_{DD} - V_{DS}}{I_{D(\text{on})}} = \frac{V_{DD} - \frac{1}{2}V_{DD}}{I_{D(\text{on})}} = \frac{\frac{1}{2}V_{DD}}{I_{D(\text{on})}}$$

and

$$R_D = \frac{6 \text{ V}}{4 \text{ mA}} = \mathbf{1.5\ k\Omega}$$

which is a standard commercial value.

6.10 TROUBLESHOOTING

How often has a network been carefully constructed only to find that when the power is applied, the response is totally unexpected and fails to match the theoretical calculations. What is the next step? Is it a bad connection? A misreading of the color code for a resistive element? An error in the construction process? The range of possibilities seems vast and often frustrating. The troubleshooting process first described in the analysis of BJT transistor configurations should narrow down the list of possibilities and isolate the problem area following a definite plan of attack. In general, the process begins with a rechecking of the network construction and the terminal connections. This is usually followed by the checking of voltage levels between specific terminals and ground or between terminals of the network. Seldom are current levels measured since such maneuvers require disturbing the network structure to insert the meter. Of course, once the voltage levels are obtained, current levels can be calculated using Ohm's law. In any case, some idea of the expected voltage or current level must be known for the measurement to have any importance. In total, therefore, the troubleshooting process can begin with some hope of success only if the basic operation of the network is understood along with some expected levels of voltage

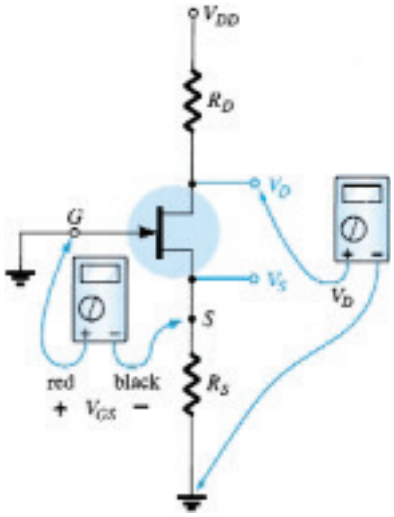


Figure 6.54 Checking the dc operation of the JFET self-bias configuration.

or current. For the *n*-channel JFET amplifier, it is clearly understood that the quiescent value of V_{GS_Q} is limited to 0 V or a negative voltage. For the network of Fig. 6.54, V_{GS_Q} is limited to negative values in the range 0 V to V_P. If a meter is hooked up as shown in Fig. 6.54, with the positive lead (normally red) to the gate and the negative lead (usually black) to the source, the resulting reading should have a negative sign and a magnitude of a few volts. Any other response should be considered suspicious and needs to be investigated.

The level of V_{DS} is typically between 25% and 75% of V_{DD}. A reading of 0 V for V_{DS} clearly indicates that either the output circuit has an "open" or the JFET is internally short-circuited between drain and source. If V_D is V_{DD} volts, there is obviously no drop across R_D due to the lack of current through R_D and the connections should be checked for continuity.

If the level of V_{DS} seems inappropriate, the continuity of the output circuit can easily be checked by grounding the negative lead of the voltmeter and measuring the voltage levels from V_{DD} to ground using the positive lead. If $V_D = V_{DD}$, the current through R_D may be zero, but there is continuity between V_D and V_{DD}. If $V_S = V_{DD}$, the device is not open between drain and source, but it is also not "on." The continuity through to V_S is confirmed, however. In this case, it is possible that there is a poor ground connection between R_S and ground that may not be obvious. The internal connection between the wire of your lead and the terminal connector may have separated. Other possibilities also exist, such as a shorted device from drain to source, but the troubleshooter will simply have to narrow down the possible causes for the malfunction.

The continuity of a network can also be checked simply by measuring the voltage across any resistor of the network (except for R_G in the JFET configuration). An indication of 0 V immediately reveals the lack of current through the element due to an open circuit in the network.

The most sensitive element in the BJT and JFET configurations is the amplifier itself. The application of excessive voltage during the construction or testing phase or the use of incorrect resistor values resulting in high current levels can destroy the device. If you question the condition of the amplifier, the best test for the FET is the curve tracer since it not only reveals whether the device is operable but also its range of current and voltage levels. Some testers may reveal that the device is still fundamentally sound but do not reveal whether its range of operation has been severely reduced.

The development of good troubleshooting techniques comes primarily from experience and a level of confidence in what to expect and why. There are, of course, times when the reasons for a strange response seem to disappear mysteriously when you check a network. In such cases, it is best not to breathe a sigh of relief and continue with the construction. The cause for such a sensitive "make or break" situation should be found and corrected, or it may reoccur at the most inopportune moment.

6.11 *P*-CHANNEL FETS

The analysis thus far has been limited solely to *n*-channel FETs. For *p*-channel FETs, a mirror image of the transfer curves is employed, and the defined current directions are reversed as shown in Fig. 6.55 for the various types of FETs.

Note for each configuration of Fig. 6.55 that each supply voltage is now a negative voltage drawing current in the indicated direction. In particular, note that the double-subscript notation for voltages continues as defined for the *n*-channel device: V_{GS}, V_{DS}, and so on. In this case, however, V_{GS} is positive (positive or negative for the depletion-type MOSFET) and V_{DS} negative.

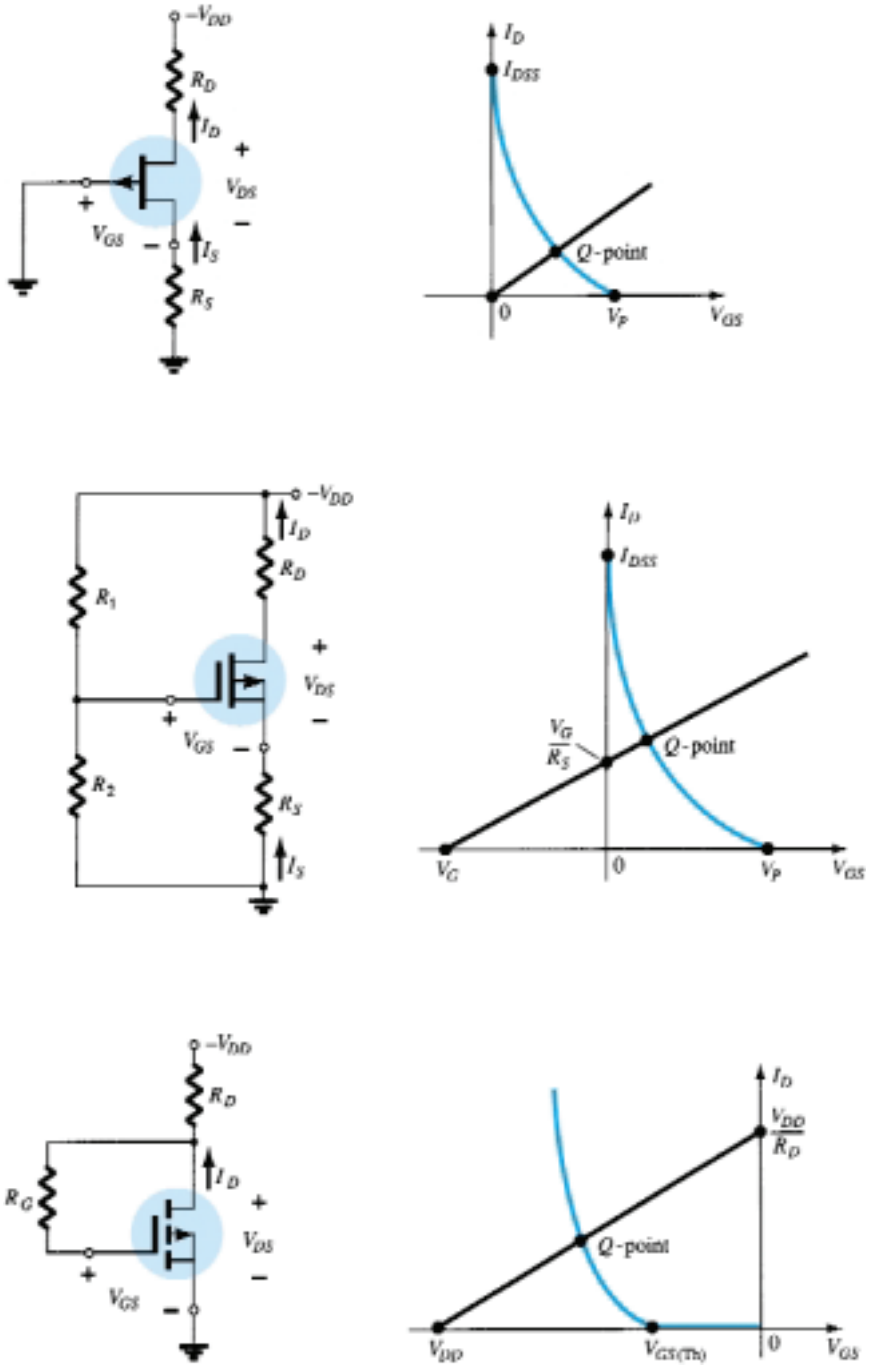


Figure 6.55 *p*-channel configurations.

Due to the similarities between the analysis of *n*-channel and *p*-channel devices, one can actually assume an *n*-channel device and reverse the supply voltage and perform the entire analysis. When the results are obtained, the magnitude of each quantity will be correct, although the current direction and voltage polarities will have to be reversed. However, the next example will demonstrate that with the experience gained through the analysis of *n*-channel devices, the analysis of *p*-channel devices is quite straightforward.