EXAMPLE 6.18

Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the *p*-channel JFET of Fig. 6.56.

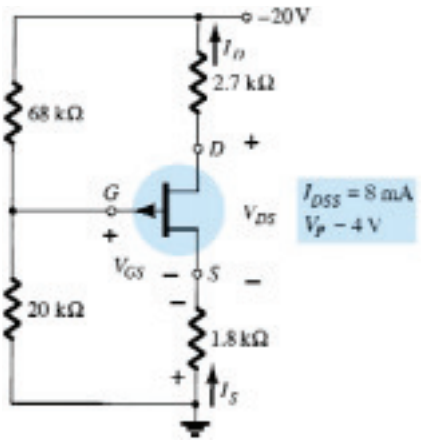


Figure 6.56 Example 6.18.

Solution

$$V_G = \frac{20\ \text{k}\Omega(-20\ \text{V})}{20\ \text{k}\Omega + 68\ \text{k}\Omega} = -4.55\ \text{V}$$

Applying Kirchhoff's voltage law gives

$$V_G - V_{GS} + I_D R_S = 0$$

and

$$V_{GS} = V_G + I_D R_S$$

Choosing $I_D = 0$ mA yields

$$V_{GS} = V_G = -4.55\ \text{V}$$

as appearing in Fig. 6.57.
Choosing $V_{GS} = 0$ V, we obtain

$$I_D = -\frac{V_G}{R_S} = -\frac{-4.55\ \text{V}}{1.8\ \text{k}\Omega} = 2.53\ \text{mA}$$

as also appearing in Fig. 6.57.
The resulting quiescent point from Fig. 6.57:

$$I_{D_Q} = \mathbf{3.4\ mA}$$

$$V_{GS_Q} = \mathbf{1.4\ V}$$

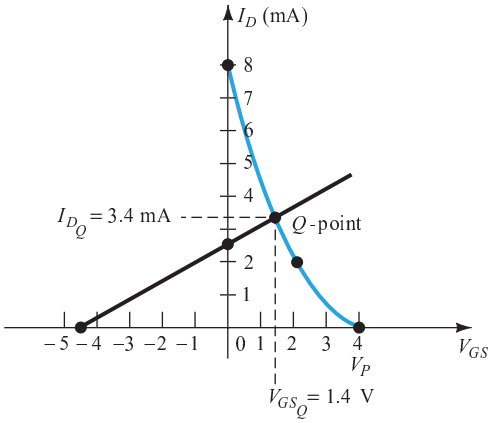


Figure 6.57 Determining the *Q*-point for the JFET configuration of Fig. 6.56.

For V_{DS}, Kirchhoff's voltage law will result in

$$-I_D R_S + V_{DS} - I_D R_D + V_{DD} = 0$$

and

$$\begin{aligned} V_{DS} &= -V_{DD} + I_D(R_D + R_S) \\ &= -20\text{ V} + (3.4\text{ mA})(2.7\text{ k}\Omega + 1.8\text{ k}\Omega) \\ &= -20\text{ V} + 15.3\text{ V} \\ &= \mathbf{-4.7\text{ V}} \end{aligned}$$

6.12 UNIVERSAL JFET BIAS CURVE

Since the dc solution of a FET configuration requires drawing the transfer curve for each analysis, a universal curve was developed that can be used for any level of I_{DSS} and V_P. The universal curve for an *n*-channel JFET or depletion-type MOSFET (for negative values of V_{GSQ}) is provided in Fig. 6.58. Note that the horizontal axis is not that of V_{GS} but of a normalized level defined by $V_{GS}/|V_P|$, the $|V_P|$ indicating that only the magnitude of V_P is to be employed, not its sign. For the vertical axis, the scale is also a normalized level of I_D/I_{DSS}. The result is that when $I_D = I_{DSS}$, the ratio is 1, and when $V_{GS} = V_P$, the ratio $V_{GS}/|V_P|$ is -1. Note also that the scale for I_D/I_{DSS} is on the left rather than on the right as encountered for I_D in past exercises. The additional two scales on the right need an introduction. The vertical scale labeled *m* can in itself be used to find the solution to fixed-bias configurations. The other scale, labeled *M*, is employed along with the *m* scale to find the solution

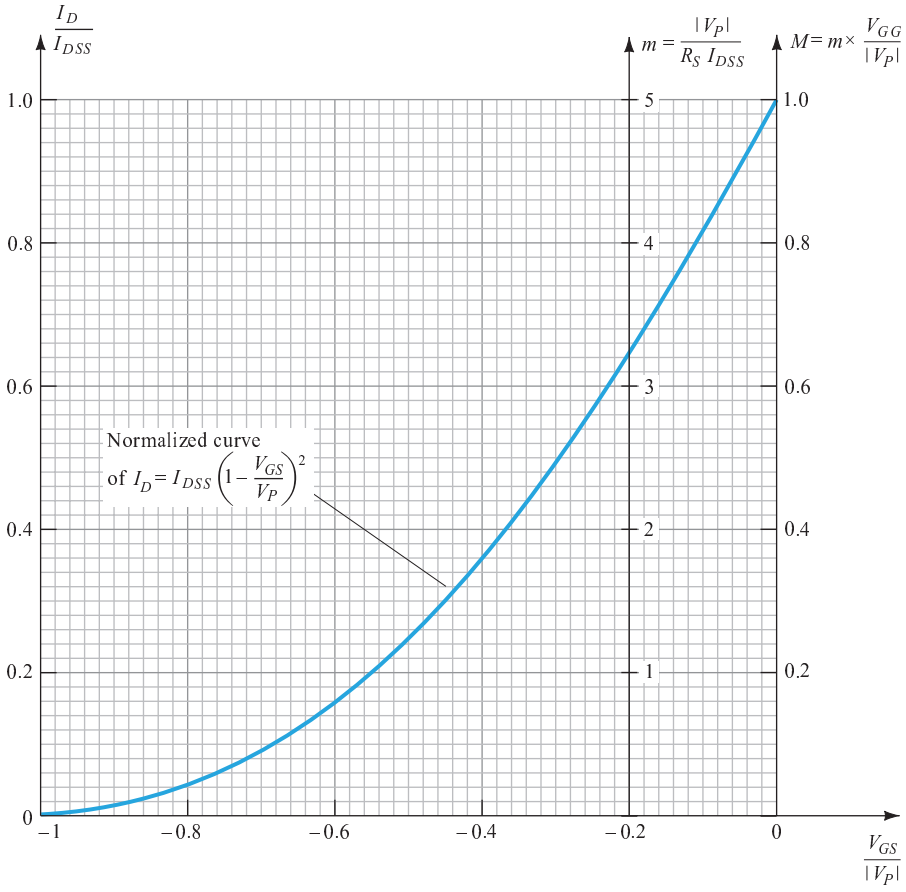


Figure 6.58 Universal JFET bias curve.

to voltage-divider configurations. The scaling for m and M come from a mathematical development involving the network equations and normalized scaling just introduced. The description to follow will not concentrate on why the m scale extends from 0 to 5 at $V_{GS}/|V_P| = -0.2$ and the M scale from 0 to 1 at $V_{GS}/|V_P| = 0$ but rather on how to use the resulting scales to obtain a solution for the configurations. The equations for m and M are the following, with V_G as defind by Eq. (6.15).

$$m = \frac{|V_P|}{I_{DSS}R_S} \tag{6.35}$$

$$M = m \times \frac{V_G}{|V_P|} \tag{6.36}$$

with $$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Keep in mind that the beauty of this approach is the elimination of the need to sketch the transfer curve for each analysis, that the superposition of the bias line is a great deal easier, and that the calculations are fewer. The use of the m and M axes is best described by examples employing the scales. Once the procedure is clearly understood, the analysis can be quite rapid, with a good measure of accuracy.

EXAMPLE 6.19

Determine the quiescent values of I_D and V_{GS} for the network of Fig. 6.59.

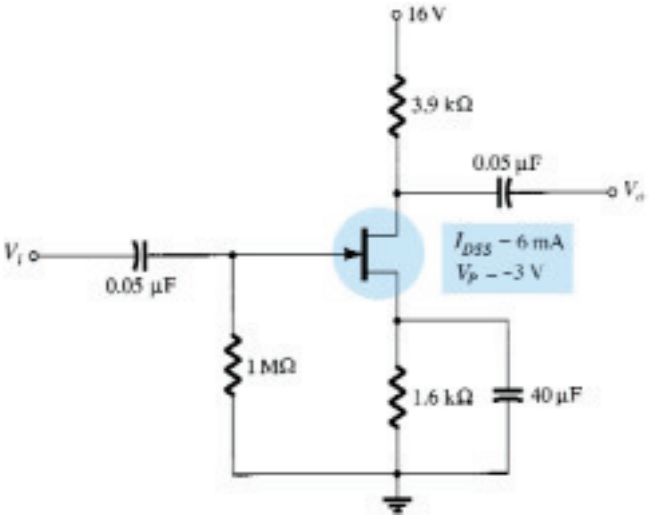


Figure 6.59 Example 6.19.

Solution

Calculating the value of m, we obtain

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-3\text{ V}|}{(6\text{ mA})(1.6\text{ k}\Omega)} = 0.31$$

The self-bias line defined by R_S is plotted by drawing a straight line from the origin through a point defined by $m = 0.31$, as shown in Fig. 6.60.
The resulting Q-point:

$$\frac{I_D}{I_{DSS}} = 0.18 \quad \text{and} \quad \frac{V_{GS}}{|V_P|} = -0.575$$

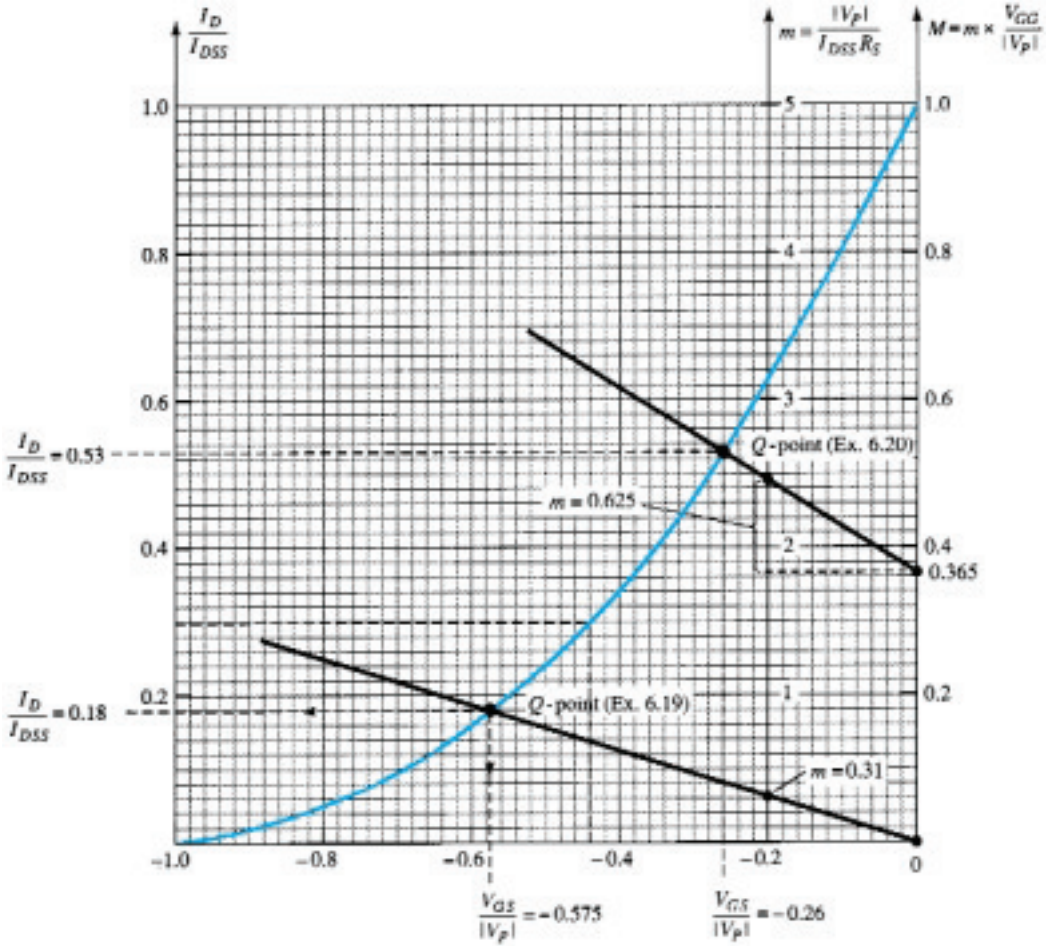


Figure 6.60 Universal curve for Examples 6.19 and 6.20.

The quiescent values of I_D and V_{GS} can then be determined as follows:

$$I_{D_Q} = 0.18I_{DSS} = 0.18(6\text{ mA}) = \mathbf{1.08\text{ mA}}$$

and

$$V_{GS_Q} = -0.575\,|V_P| = -0.575(3\text{ V}) = \mathbf{-1.73\text{ V}}$$

EXAMPLE 6.20

Determine the quiescent values of I_D and V_{GS} for the network of Fig. 6.61.

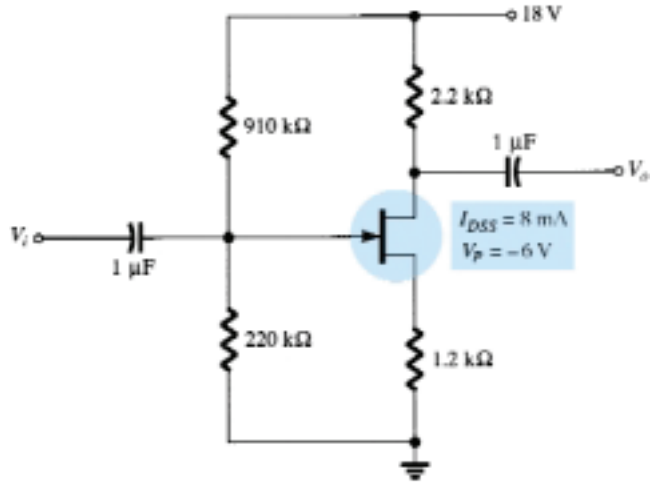


Figure 6.61 Example 6.20.

Solution

Calculating m gives

$$m = \frac{|V_P|}{I_{DSS}R_S} = \frac{|-6\text{ V}|}{(8\text{ mA})(1.2\text{ k}\Omega)} = 0.625$$

Determining V_G yields

$$V_G = \frac{R_2V_{DD}}{R_1 + R_2} = \frac{(220\text{ k}\Omega)(18\text{ V})}{910\text{ k}\Omega + 220\text{ k}\Omega} = 3.5\text{ V}$$

Finding M, we have

$$M = m \times \frac{V_G}{|V_P|} = 0.625\left(\frac{3.5\text{ V}}{6\text{ V}}\right) = 0.365$$

Now that m and M are known, the bias line can be drawn on Fig. 6.60. In particular, note that even though the levels of I_{DSS} and V_P are different for the two networks, the same universal curve can be employed. First find M on the M axis as shown in Fig. 6.60. Then draw a horizontal line over to the m axis and, at the point of intersection, add the magnitude of m as shown in the figure. Using the resulting point on the m axis and the M intersection, draw the straight line to intersect with the transfer curve and define the Q-point:

That is, $$\frac{I_D}{I_{DSS}} = 0.53 \quad \text{and} \quad \frac{V_{GS}}{|V_P|} = -0.26$$

and $$I_{DQ} = 0.53I_{DSS} = 0.53(8\text{ mA}) = \mathbf{4.24\text{ mA}}$$

with $$V_{GSQ} = -0.26|V_P| = -0.26(6\text{ V}) = \mathbf{-1.56\text{ V}}$$

6.13 PSPICE WINDOWS

JFET Voltage-Divider Configuration

The results of Example 6.20 will now be verified using PSpice Windows. The network of Fig. 6.62 is constructed using computer methods described in the previous chapters. The J2N3819 JFET is obtained from the **EVAL.slb** library and, through **Edit-Model-Edit Instance Model (Text), Vto** is set to −6V and **Beta,** as defined by Beta = $I_{DSS}/|V_P|^2$ is set to 0.222 mA/V^2. After an **OK** followed by clicking the **Simulation** icon (the yellow background with the two waveforms) and clearing the **Message Viewer, PSpiceAD** screens will result in Fig. 6.62. The resulting drain cur-

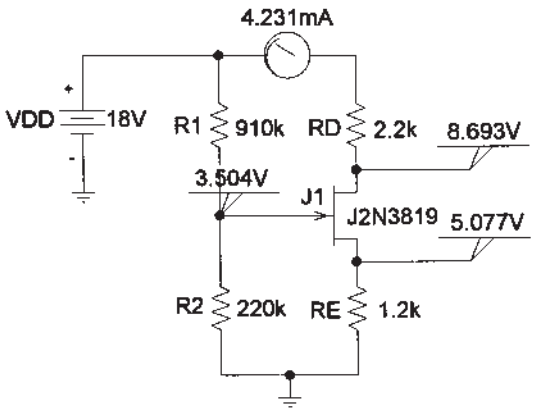


Figure 6.62 JFET voltage-divider configuration with PSpice Windows results for the dc levels.

rent is 4.231 mA compared to the calculated level of 4.24 mA, and V_{GS} is 3.504 V − 5.077 V = −1.573 V versus the calculated value of −1.56 V—both excellent comparisons.

Combination Network

Next, the results of Example 6.13 with both a transistor and JFET will be verified. For the transistor, the **Model** must be altered to have a **Bf**(beta) of 180 to match the example, and for the JFET, **Vto** must be set to −6V and **Beta** to 0.333 mA/V^2. The results appearing in Fig. 6.63 are again an excellent comparison with the hand-written solution. V_D is 11.44 V compared to 11.07 V, V_C is 7.138 V compared to 7.32 V, and V_{GS} is −3.758 V compared to −3.7 V.

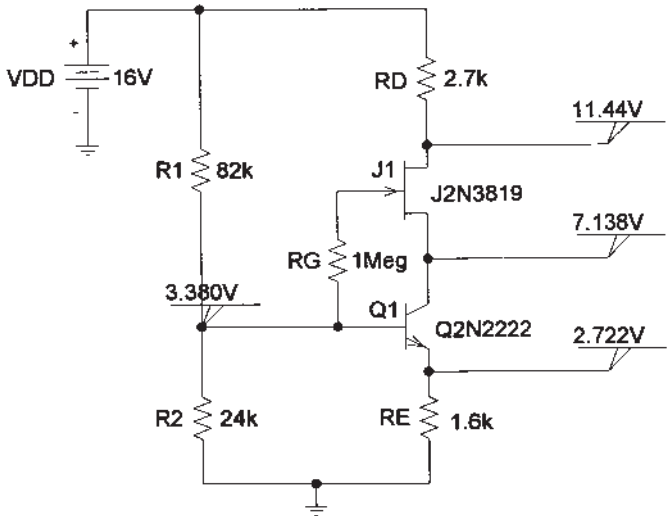


Figure 6.63 Verifying the hand-calculated solution of Example 6.13 using PSpice Windows.

Enhancement MOSFET

Next, the analysis procedure of Section 6.6 will be verified using the IRF150 enhancement-type *n*-channel MOSFET found in the **EVAL.slb** library. First, the device characteristics will be obtained by constructing the network of Fig. 6.64.

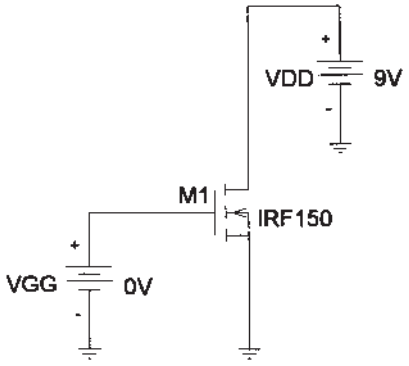


Figure 6.64 Network employed to obtain the characteristics of the IRF150 enhancement-type *n*-channel MOSFET.

Clicking on the **Setup Analysis** icon (with the blue bar at the top in the left-hand corner of the screen), **DC Sweep** is chosen to obtain the **DC Sweep** dialog box. **Voltage Source** is chosen as the **Swept Var. Type,** and **Linear** is chosen for the **Sweep Type.** Since only one curve will be obtained, there is no need for a **Nested Sweep.** The voltage-drain voltage VDD will remain fixed at a value of 9 V (about three times the threshold value (**Vto**) of 2.831 V), while the gate-to-source voltage V_{GS}, which in

this case is VGG, will be swept from 0 to 10 V. The **Name** therefore is VGG and the **Start Value** 0V, the **End Value** 10V, and the **Increment** 0.01V. After an **OK** followed by a **Close** of the **Analysis Setup,** the analysis can be performed through the **Analysis** icon. If **Automatically run Probe after simulation** is chosen under the **Probe Setup Options** of **Analysis,** the **OrCAD-MicroSim Probe** screen will result, with the horizontal axis appearing with VGG as the variable and range from 0 to 10 V. Next, the **Add Traces** dialog box can be obtained by clicking the **Traces** icon (red pointed pattern on an axis) and the **ID(M1)** chosen to obtain the drain current versus the gate-to-source voltage. Click **OK,** and the characteristics will appear on the screen. To expand the scale of the resulting plot to 20 V, simply choose **Plot** followed by **X-Axis Settings** and set the **User Defined** range to 0 to 20 V. After another **OK,** and the plot of Fig. 6.65 will result, revealing a rather high-current device. The labels **ID** and **VGS** were added using the **Text Label** icon with the letters A, B, and C. The hand-drawn load line will be described in the paragraph to follow.

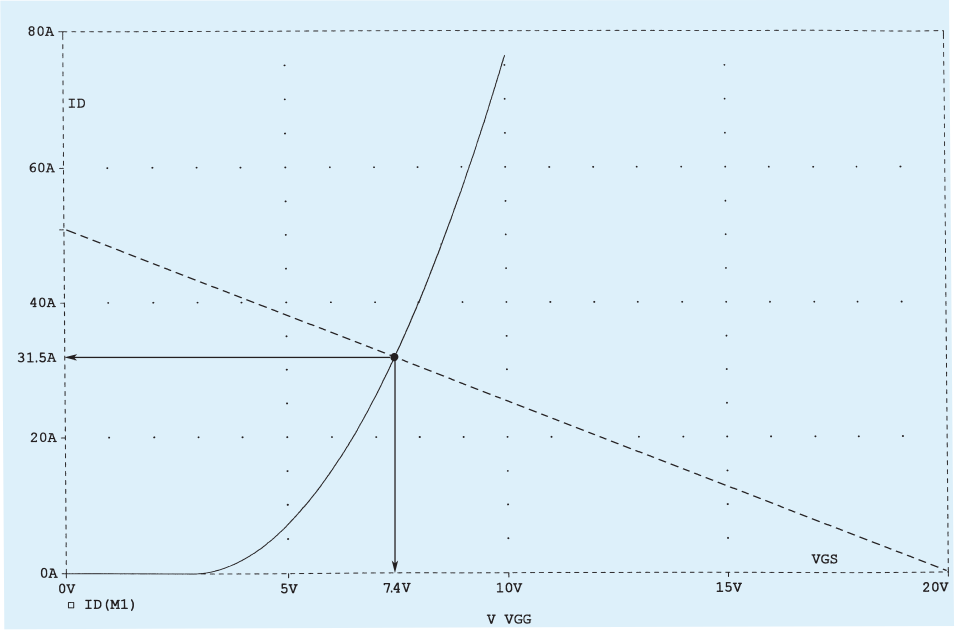


Figure 6.65 Characteristics of the IRF500 MOSFET of Figure 6.64 with a load line defined by the network of Figure 6.66.

The network of Fig. 6.66 was then established to provide a load line extending from I_D equal to 20 V/0.4 Ω = 50 A down to $V_{GS} = V_{GG} = 20$ V as shown in Fig. 6.65. A simulation resulted in the levels shown, which match the solution of Fig. 6.65.

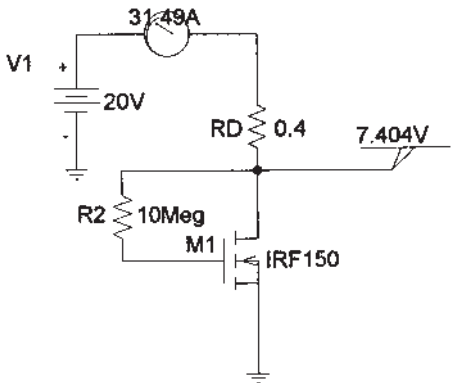


Figure 6.66 Feedback-biasing arrangement employing an IRF150 enhancement-type MOSFET.

§ 6.2 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 6.67:
(a) Sketch the transfer characteristics of the device.
(b) Superimpose the network equation on the same graph.
(c) Determine I_{D_Q} and V_{DS_Q}.
(d) Using Shockley's equation, solve for I_{D_Q} and then find V_{DS_Q}. Compare with the solutions of part (c).

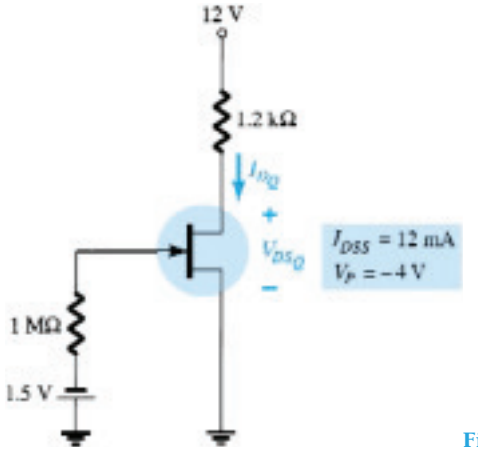


Figure 6.67 Problems 1, 35

2. For the fixed-bias configuration of Fig. 6.68, determine:
(a) I_{D_Q} and V_{GS_Q} using a purely mathematical approach.
(b) Repeat part (a) using a graphical approach and compare results.
(c) Find V_{DS}, V_D, V_G, and V_S using the results of part (a).

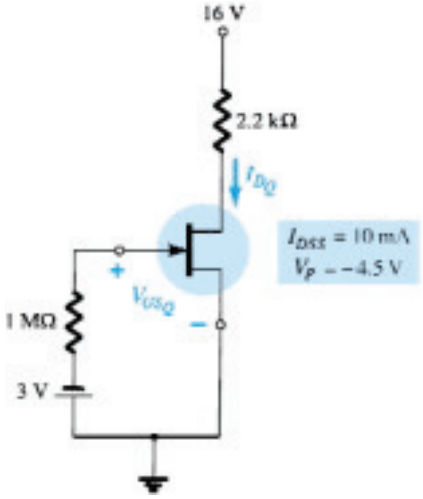


Figure 6.68 Problem 2

3. Given the measured value of V_D in Fig. 6.69, determine:
(a) I_D.
(b) V_{DS}.
(c) V_{GG}.

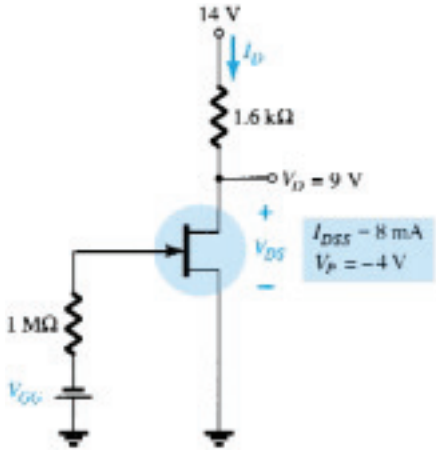


Figure 6.69 Problem 3

4. Determine V_D for the fixed-bias configuration of Fig. 6.70.
5. Determine V_D for the fixed-bias configuration of Fig. 6.71.

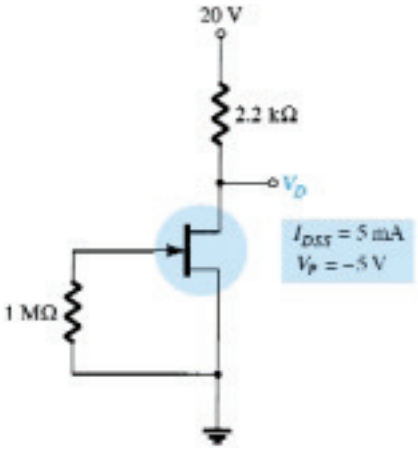


Figure 6.70 Problem 4

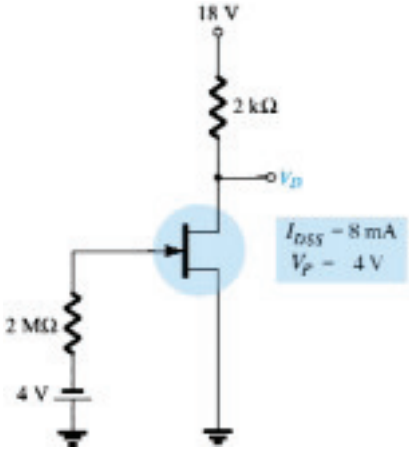


Figure 6.71 Problem 5

§ 6.3 Self-Bias Configuration

6. For the self-bias configuration of Fig. 6.72:
   (a) Sketch the transfer curve for the device.
   (b) Superimpose the network equation on the same graph.
   (c) Determine I_{DQ} and V_{GS_Q}.
   (d) Calculate V_{DS}, V_D, V_G, and V_S.

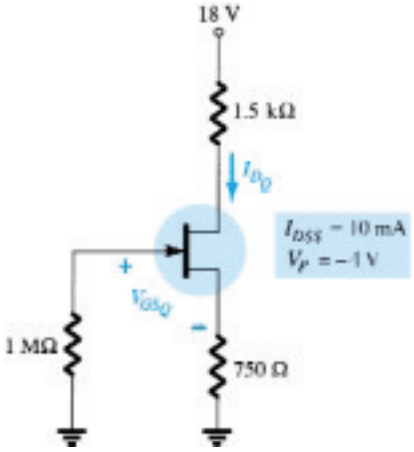


Figure 6.72 Problems 6, 7, 36

* 7. Determine I_{D_Q} for the network of Fig. 6.72 using a purely mathematical approach. That is, establish a quadratic equation for I_D and choose the solution compatible with the network characteristics. Compare to the solution obtained in Problem 6.

8. For the network of Fig. 6.73, determine:
   (a) V_{GS_Q} and I_{D_Q}.
   (b) V_{DS}, V_D, V_G, and V_S.

9. Given the measurement $V_S = 1.7$ V for the network of Fig. 6.74, determine:
   (a) I_{D_Q}.
   (b) V_{GS_Q}.
   (c) I_{DSS}.
   (d) V_D.
   (e) V_{DS}.

* **10.** For the network of Fig. 6.75, determine:
(a) I_D.
(b) V_{DS}.
(c) V_D.
(d) V_S.

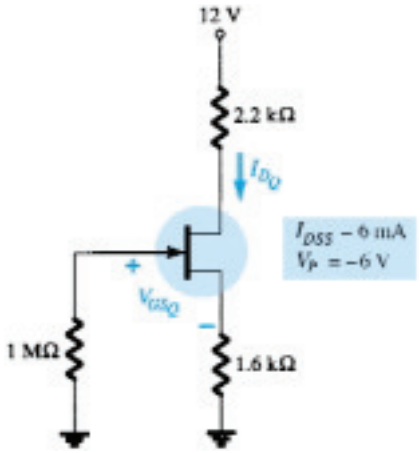


Figure 6.73 Problem 8

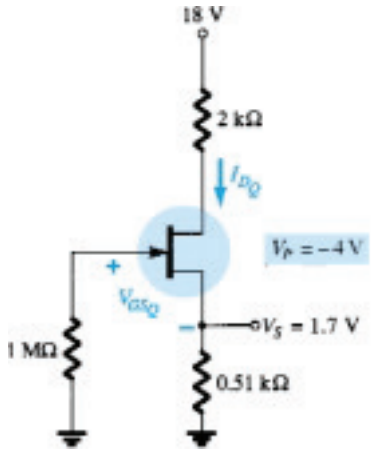


Figure 6.74 Problem 9

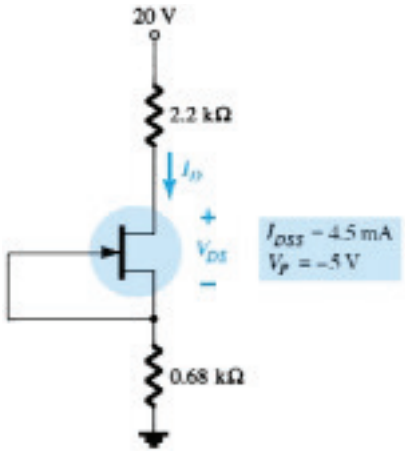


Figure 6.75 Problem 10

* **11.** Find V_S for the network of Fig. 6.76.

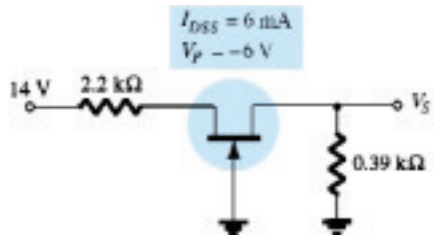


Figure 6.76 Problem 11

§ 6.4 Voltage-Divider Biasing

12. For the network of Fig. 6.77, determine:
(a) V_G.
(b) I_{D_Q} and V_{GS_Q}.
(c) V_D and V_S.
(d) V_{DS_Q}.

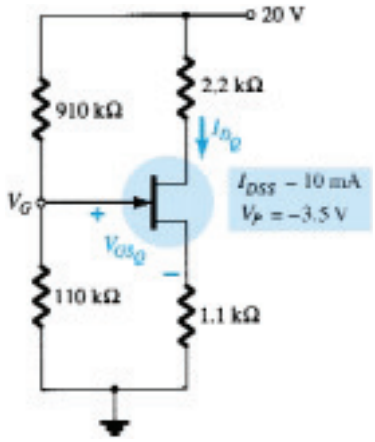


Figure 6.77 Problems 12, 13

13. (a) Repeat Problem 12 with $R_S = 0.51$ kΩ (about 50% of the value of 12). What is the effect of a smaller R_S on I_{D_Q} and V_{GS_Q}?
(b) What is the minimum possible value of R_S for the network of Fig. 6.77?

14. For the network of Fig. 6.78, $V_D = 9$ V. Determine:
(a) I_D.
(b) V_S and V_{DS}.
(c) V_G and V_{GS}.
(d) V_P.

* **15.** For the network of Fig. 6.79, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS} and V_S.

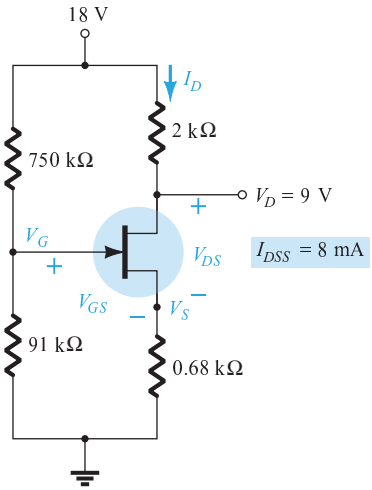


Figure 6.78 Problem 14

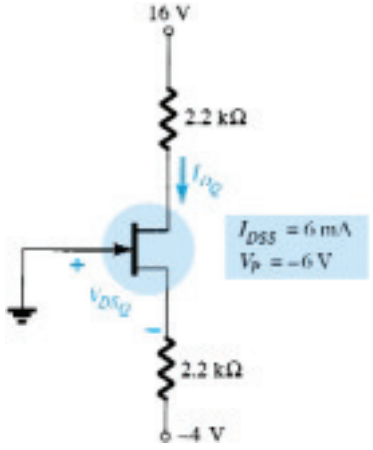


Figure 6.79 Problems 15, 37

* **16.** Given $V_{DS} = 4$ V for the network of Fig. 6.80, determine:
(a) I_D.
(b) V_D and V_S.
(c) V_{GS}.

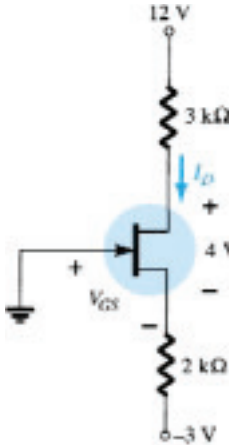


Figure 6.80 Problem 16

§ 6.5 Depletion-Type MOSFETs

17. For the self-bias configuration of Fig. 6.81, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS} and V_D.

* **18.** For the network of Fig. 6.82, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS} and V_S.

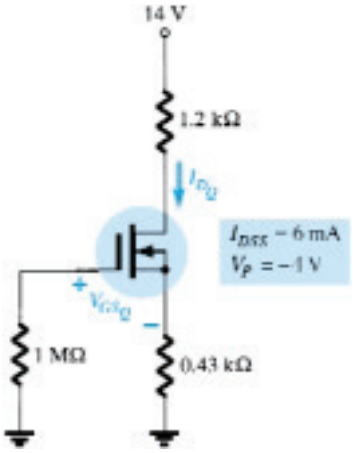


Figure 6.81 Problem 17

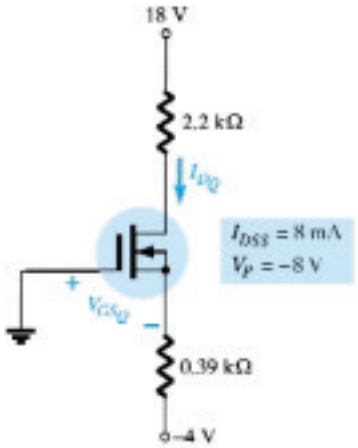


Figure 6.82 Problem 18

§ 6.6 Enhancement-Type MOSFETs

19. For the network of Fig. 6.83, determine:
(a) I_{D_Q}.
(b) V_{GS_Q} and V_{DS_Q}.
(c) V_D and V_S.
(d) V_{DS}.

20. For the voltage-divider configuration of Fig. 6.84, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_D and V_S.

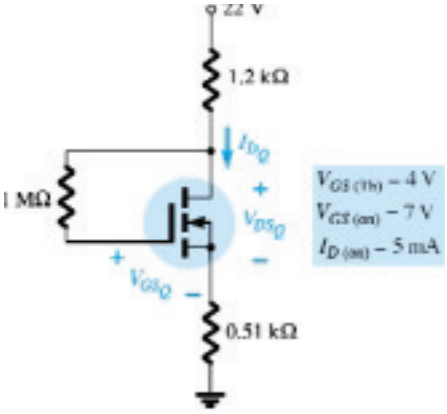


Figure 6.83 Problem 19

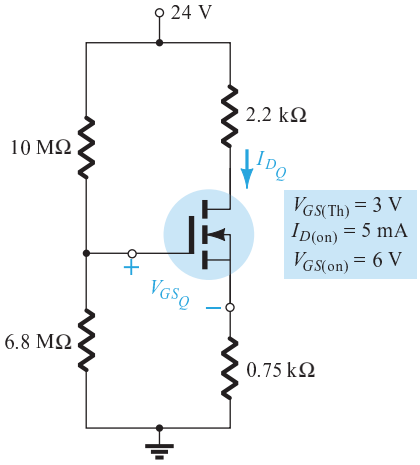


Figure 6.84 Problem 20

§ 6.8 Combination Networks

* **21.** For the network of Fig. 6.85, determine:
(a) V_G.
(b) V_{GS_Q} and I_{D_Q}.
(c) I_E.
(d) I_B.
(e) V_D.
(f) V_C.

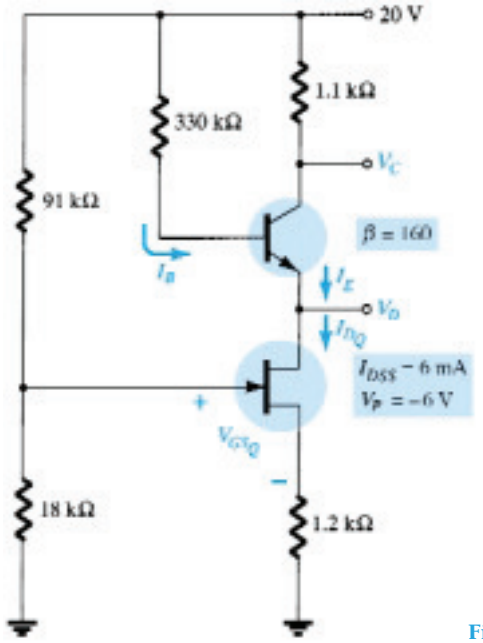


Figure 6.85 Problem 21

* **22.** For the combination network of Fig. 6.86, determine:
  (a) V_B and V_G.
  (b) V_E.
  (c) I_E, I_C, and I_D.
  (d) I_B.
  (e) V_C, V_S, and V_D.
  (f) V_{CE}.
  (g) V_{DS}.

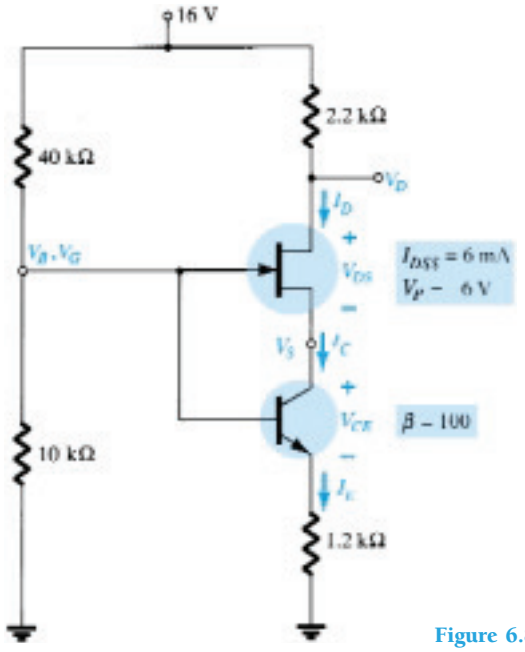


Figure 6.86 Problem 22

§ 6.9 Design

* **23.** Design a self-bias network using a JFET transistor with $I_{DSS} = 8$ mA and $V_P = -6$ V to have a Q-point at $I_{D_Q} = 4$ mA using a supply of 14 V. Assume that $R_D = 3R_S$ and use standard values.

* **24.** Design a voltage-divider bias network using a depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V to have a Q-point at $I_{D_Q} = 2.5$ mA using a supply of 24 V. In addition, set $V_G = 4$ V and use $R_D = 2.5R_S$ with $R_1 = 22$ MΩ. Use standard values.

25. Design a network such as appears in Fig. 6.39 using an enhancement-type MOSFET with $V_{GS(\text{Th})} = 4$ V, $k = 0.5 \times 10^{-3}\text{A/V}^2$ to have a Q-point of $I_{D_Q} = 6$ mA. Use a supply of 16 V and standard values.

§ 6.10 Troubleshooting

* **26.** What do the readings for each configuration of Fig. 6.87 suggest about the operation of the network?

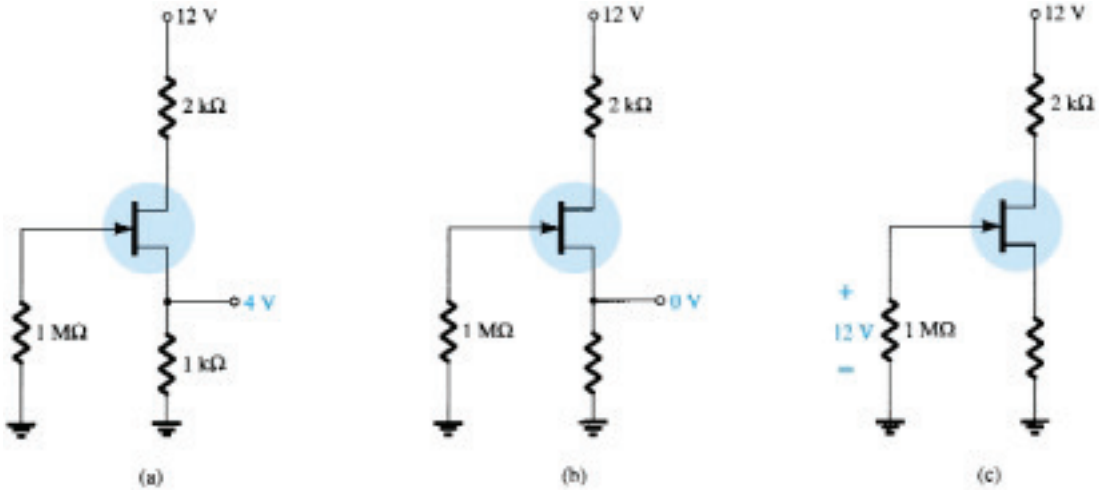


Figure 6.87 Problem 26

* **27.** Although the readings of Fig. 6.88 initially suggest that the network is behaving properly, determine a possible cause for the undesirable state of the network.

* **28.** The network of Fig. 6.89 is not operating properly. What is the specific cause for its failure?

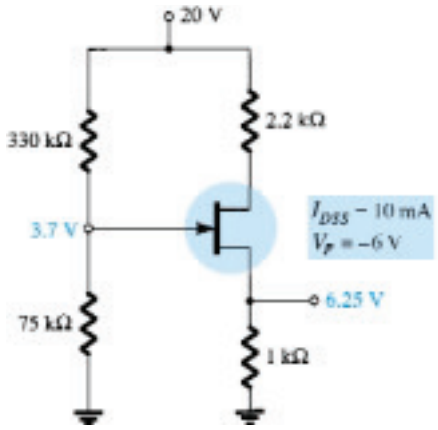


Figure 6.88 Problem 27

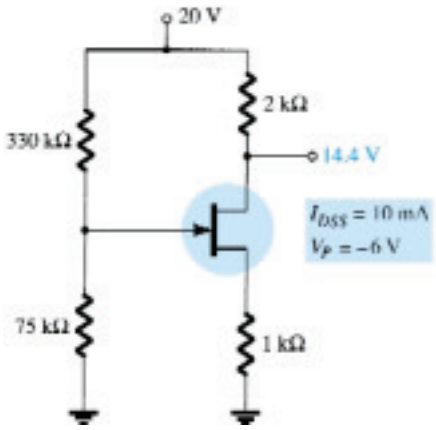


Figure 6.89 Problem 28

§ 6.11 *p*-Channel FETs

29. For the network of Fig. 6.90, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS}.
(c) V_D.

30. For the network of Fig. 6.91, determine:
(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS}.
(c) V_D.

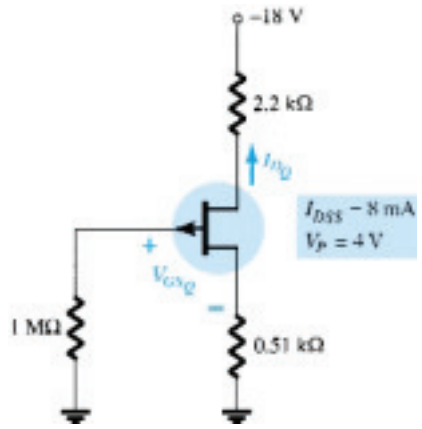


Figure 6.90 Problem 29

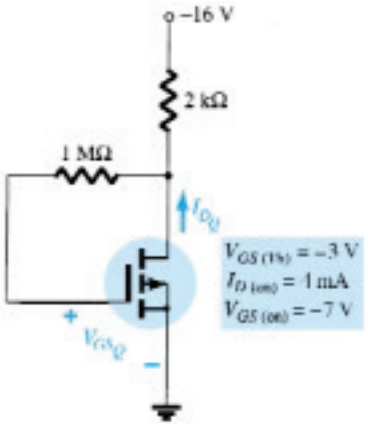


Figure 6.91 Problem 30

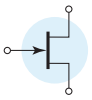
§ 6.12 Universal JFET Bias Curve

31. Repeat Problem 1 using the universal JFET bias curve.

32. Repeat Problem 6 using the universal JFET bias curve.

33. Repeat Problem 12 using the universal JFET bias curve.

34. Repeat Problem 15 using the universal JFET bias curve.



§ 6.13 PSpice Windows

35. Perform a PSpice Windows analysis of the network of Problem 1.

36. Perform a PSpice Windows analysis of the network of Problem 6.

37. Perform a PSpice Windows analysis of the network of Problem 15.

*Please Note: Asterisks indicate more difficult problems.

r_e

CHAPTER

7 BJT Transistor Modeling

7.1 INTRODUCTION

The basic construction, appearance, and characteristics of the transistor were introduced in Chapter 3. The dc biasing of the device was then examined in detail in Chapter 4. We now begin to examine the *small-signal* ac response of the BJT amplifier by reviewing the *models* most frequently used to represent the transistor in the sinusoidal ac domain.

One of our first concerns in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal. It will determine whether *small-signal* or *large-signal* techniques should be applied. There is no set dividing line between the two, but the application—and the magnitude of the variables of interest relative to the scales of the device characteristics—will usually make it quite clear which method is appropriate. The small-signal technique is introduced in this chapter, and large-signal applications are examined in Chapter 16.

There are two models commonly used in the small-signal ac analysis of transistor networks: the r_e model and the *hybrid equivalent* model. This chapter not only introduces both models but defines the role of each and the relationship between the two.

7.2 AMPLIFICATION IN THE AC DOMAIN

It was demonstrated in Chapter 3 that the transistor can be employed as an amplifying device. That is, the output sinusoidal signal is greater than the input signal or, stated another way, the output ac power is greater than the input ac power. The question then arises as to how the ac power output can be greater than the input ac power? Conservation of energy dictates that over time the total power output, P_o, of a system cannot be greater than its power input, P_i, and that the efficiency defined by $\eta = P_o/P_i$ cannot be greater than 1. The factor missing from the discussion above that permits an ac power output greater than the input ac power is the applied dc power. It is a contributor to the total output power even though part of it is dissipated by the device and resistive elements. In other words, there is an "exchange" of dc power to the ac domain that permits establishing a higher output ac power. In fact, a *conversion efficiency* is defined by $\eta = P_{o(\text{ac})}/P_{i(\text{dc})}$, where $P_{o(\text{ac})}$ is the ac power to the load and $P_{i(\text{dc})}$ is the dc power supplied.

Perhaps the role of the dc supply can best be described by first considering the simple dc network of Fig. 7.1. The resulting direction of flow is indicated in the figure with a plot of the current i versus time. Let us now insert a control mechanism

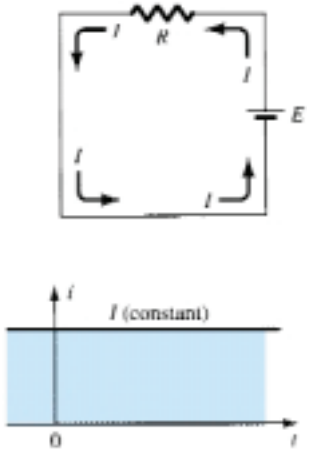


Figure 7.1 Steady current established by a dc supply.

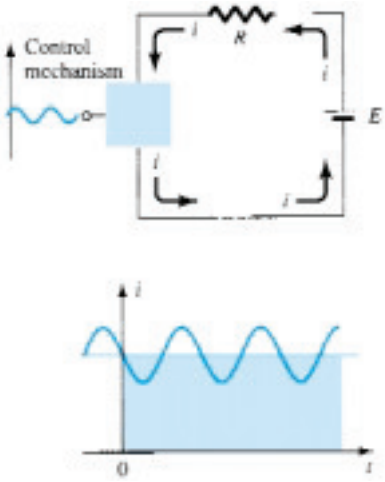


Figure 7.2 Effect of a control element on the steady-state flow of the electrical system of Fig. 7.1.

such as that shown in Fig. 7.2. The control mechanism is such that the application of a relatively small signal to the control mechanism can result in a much larger oscillation in the output circuit. For the system of Fig. 7.2, the peak value of the oscillation is controlled by the established dc level. Any attempt to exceed the limit set by the dc level will result in a "clipping" (flattening) of the peak region of the output signal. In total, therefore, proper amplifier design requires that the dc and ac components be sensitive to each other's requirements and limitations.

However, it is indeed fortunate that transistor small-signal amplifiers can be considered linear for most applications, permitting the use of the superposition theorem to isolate the dc analysis from the ac analysis.

7.3 BJT TRANSISTOR MODELING

The key to transistor small-signal analysis is the use of equivalent circuits (models) to be introduced in this chapter.

A model is the combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

Once the ac equivalent circuit has been determined, the graphical symbol of the device can be replaced in the schematic by this circuit and the basic methods of ac circuit analysis (mesh analysis, nodal analysis, and Thévenin's theorem) can be applied to determine the response of the circuit.

There are two schools of thought in prominence today regarding the equivalent circuit to be substituted for the transistor. For many years the industrial and educational institutions relied heavily on the *hybrid parameters* (to be introduced shortly). The hybrid-parameter equivalent circuit continues to be very popular, although it must now share the spotlight with an equivalent circuit derived directly from the operating conditions of the transistor—the r_e model. Manufacturers continue to specify the hybrid parameters for a particular operating region on their specification sheets. The parameters (or components) of the r_e model can be derived directly from the hybrid parameters in this region. However, the hybrid equivalent circuit suffers from being limited to a particular set of operating conditions if it is to be considered accurate. The parameters of the other equivalent circuit can be determined for any region of operation within the active region and are not limited by the single set of parameters provided by the specification sheet. In turn, however, the r_e model fails to account for the output impedance level of the device and the feedback effect from output to input.

Since both models are used extensively today, they are both examined in detail in this text. In some analysis and examples the hybrid model will be employed, while in others the r_e model will be used exclusively. The text will make every effort, however, to show how closely related the two models are and how a proficiency with one leads to a natural proficiency with the other.

In an effort to demonstrate the effect that the ac equivalent circuit will have on the analysis to follow, consider the circuit of Fig. 7.3. Let us assume for the moment that the small-signal ac equivalent circuit for the transistor has already been determined. Since we are interested only in the ac response of the circuit, all the dc supplies can be replaced by a zero-potential equivalent (short circuit) since they determine only the dc (quiescent level) of the output voltage and not the magnitude of the swing of the ac output. This is clearly demonstrated by Fig. 7.4. The dc levels were simply important for determining the proper Q-point of operation. Once determined, the dc levels can be ignored in the ac analysis of the network. In addition, the coupling capacitors C_1 and C_2 and bypass capacitor C_3 were chosen to have a very small

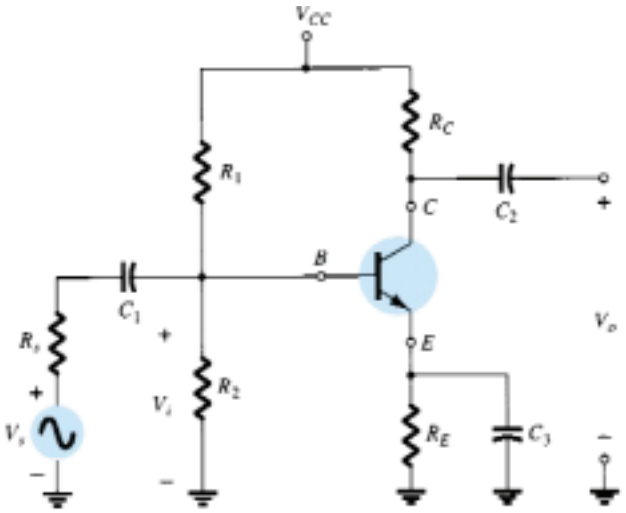


Figure 7.3 Transistor circuit under examination in this introductory discussion.

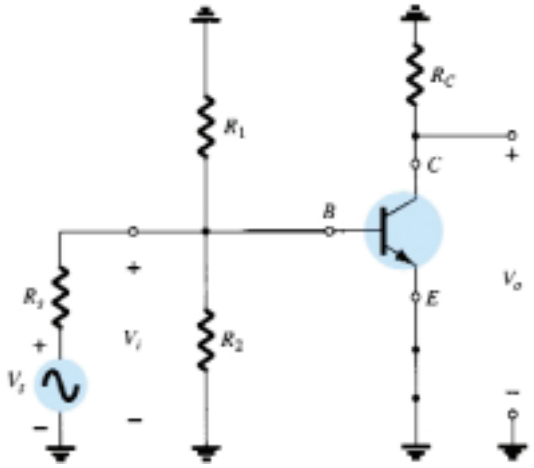


Figure 7.4 The network of Fig. 7.3 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.

reactance at the frequency of application. Therefore, they too may for all practical purposes be replaced by a low-resistance path or a short circuit. Note that this will result in the "shorting out" of the dc biasing resistor R_E. Recall that capacitors assume an "open-circuit" equivalent under dc steady-state conditions, permitting an isolation between stages for the dc levels and quiescent conditions.

If we establish a common ground and rearrange the elements of Fig. 7.4, R_1 and R_2 will be in parallel and R_C will appear from collector to emitter as shown in Fig. 7.5. Since the components of the transistor equivalent circuit appearing in Fig. 7.5 employ familiar components such as resistors and independent controlled sources,

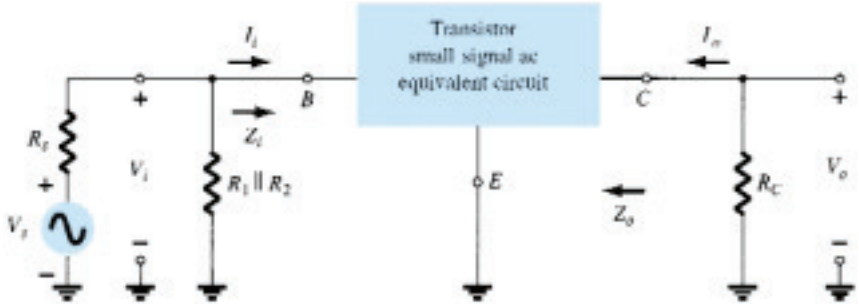


Figure 7.5 Circuit of Fig. 7.4 redrawn for small-signal ac analysis.

analysis techniques such as superposition, Thévenin's theorem, and so on, can be applied to determine the desired quantities.

Let us further examine Fig. 7.5 and identify the important quantities to be determined for the system. Since we know that the transistor is an amplifying device, we would expect some indication of how the output voltage V_o is related to the input voltage V_i—the *voltage gain.* Note in Fig. 7.5 for this configuration that $I_i = I_b$ and $I_o = I_c$, which define the *current gain* $A_i = I_o/I_i$. The input impedance Z_i and output impedance Z_o will prove particularly important in the analysis to follow. A great deal more will be offered about these parameters in the sections to follow.

In summary, therefore, the ac equivalent of a network is obtained by:

1. *Setting all dc sources to zero and replacing them by a short-circuit equivalent*
2. *Replacing all capacitors by a short-circuit equivalent*
3. *Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2*
4. *Redrawing the network in a more convenient and logical form*

In the sections to follow, the r_e and hybrid equivalent circuits will be introduced to complete the ac analysis of the network of Fig. 7.5.

7.4 THE IMPORTANT PARAMETERS: Z_i, Z_o, A_v, A_i

Before investigating the equivalent circuits for BJTs in some detail, let us concentrate on those parameters of a two-port system that are of paramount importance from an analysis and design viewpoint. For the two-port (two pairs of terminals) system of Fig. 7.6, the input side (the side to which the signal is normally applied) is to the left and the output side (where the load is connected) is to the right. In fact, for most electrical and electronic systems, the general flow is usually from the left to the right. For both sets of terminals, the impedance between each pair of terminals under normal operating conditions is quite important.

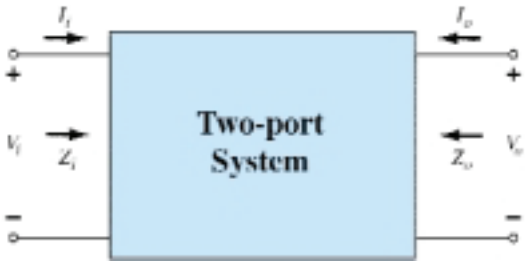


Figure 7.6 Two-port system.

Input Impedance, Z_i

For the input side, the input impedance Z_i is defined by Ohm's law as the following:

$$Z_i = \frac{V_i}{I_i} \tag{7.1}$$

If the input signal V_i is changed, the current I_i can be computed using the same level of input impedance. In other words:

For small-signal analysis, once the input impedance has been determined the same numerical value can be used for changing levels of applied signal.

In fact, we will find in the sections to follow that the input impedance of a transistor can be approximately determined by the dc biasing conditions—conditions that do not change simply because the magnitude of the applied ac signal has changed.

It is particularly noteworthy that for frequencies in the low to mid-range (typically $\leq$100 kHz):

The input impedance of a BJT transistor amplifier is purely resistive in nature and, depending on the manner in which the transistor is employed, can vary from a few ohms to megohms.

In addition:

An ohmmeter cannot be used to measure the small-signal ac input impedance since the ohmmeter operates in the dc mode.

Equation (7.1) is particularly useful in that it provides a method for measuring the input resistance in the ac domain. For instance, in Fig. 7.7 a sensing resistor has been added to the input side to permit a determination of I_i using Ohm's law. An oscilloscope or sensitive digital multimeter (DMM) can be used to measure the voltage V_s and V_i. Both voltages can be the peak-to-peak, peak, or rms values, as long as both levels use the same standard. The input impedance is then determined in the following manner:

$$I_i = \frac{V_s - V_i}{R_{\text{sense}}} \tag{7.2}$$

and

$$Z_i = \frac{V_i}{I_i} \tag{7.3}$$

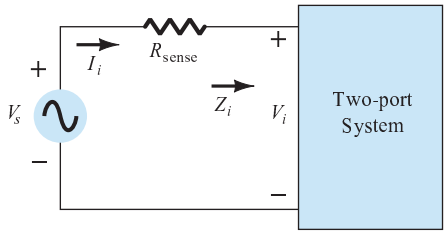


Figure 7.7 Determining Z_i.

The importance of the input impedance of a system can best be demonstrated by the network of Fig. 7.8. The signal source has an internal resistance of 600 Ω, and the system (possibly a transistor amplifier) has an input resistance of 1.2 kΩ. If the source were ideal ($R_s = 0$ Ω), the full 10 mV would be applied to the system, but

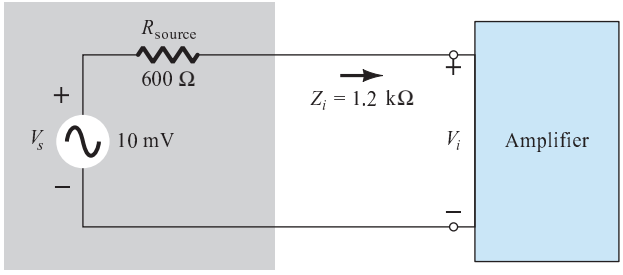


Figure 7.8 Demonstrating the impact of Z_i on an amplifier's response.

with a source impedance, the input voltage must be determined using the voltage-divider rule as follows:

$$V_i = \frac{Z_i V_s}{Z_i + R_{\text{source}}} = \frac{(1.2\ \text{k}\Omega)(10\ \text{mV})}{1.2\ \text{k}\Omega + 0.6\ \text{k}\Omega} = 6.67\ \text{mV}$$

Thus, only 66.7% of the full-input signal is available at the input. If Z_i were only 600 Ω, then $V_i = \frac{1}{2}(10\ \text{mV}) = 5\ \text{mV}$ or 50% of the available signal. Of course, if $Z_i = 8.2\ \text{k}\Omega$, V_i will be 93.2% of the applied signal. The level of input impedance, therefore, can have a significant impact on the level of signal that reaches the system (or amplifier). In the sections and chapters to follow, it will be demonstrated that the ac input resistance is dependent on whether the transistor is in the common-base, common-emitter, or common-collector configuration and on the placement of the resistive elements.

EXAMPLE 7.1

For the system of Fig. 7.9, determine the level of input impedance.

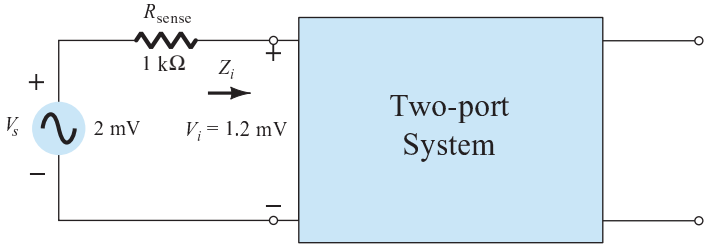


Figure 7.9 Example 7.1

Solution

$$I_i = \frac{V_s - V_i}{R_{\text{sense}}} = \frac{2\ \text{mV} - 1.2\ \text{mV}}{1\ \text{k}\Omega} = \frac{0.8\ \text{mV}}{1\ \text{k}\Omega} = 0.8\ \mu\text{A}$$

and

$$Z_i = \frac{V_i}{I_i} = \frac{1.2\ \text{mV}}{0.8\ \mu\text{A}} = \mathbf{1.5\ k\Omega}$$

Output Impedance, Z_o

The output impedance is naturally defined at the output set of terminals, but the manner in which it is defined is quite different from that of the input impedance. That is:

The output impedance is determined at the output terminals looking back into the system with the applied signal set to zero.

In Fig. 7.10, for example, the applied signal has been set to zero volts. To determine Z_o, a signal, V_s, is applied to the output terminals and the level of V_o is measured with an oscilloscope or sensitive DMM. The output impedance is then determined in the following manner:

$$I_o = \frac{V - V_o}{R_{\text{sense}}} \tag{7.4}$$

and

$$Z_o = \frac{V_o}{I_o} \tag{7.5}$$

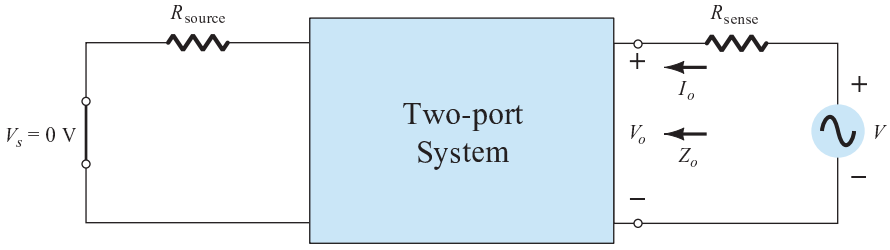


Figure 7.10 Determining Z_o.

In particular, for frequencies in the low to mid-range (typically ≤ 100 kHz):

The output impedance of a BJT transistor amplifier is resistive in nature and, depending on the configuration and the placement of the resistive elements, Z_o, can vary from a few ohms to a level that can exceed 2 MΩ.

In addition:

An ohmmeter cannot be used to measure the small-signal ac output impedance since the ohmmeter operates in the dc mode.

For amplifier configurations where significant gain in current is desired, the level of Z_o should be as large as possible. As demonstrated by Fig. 7.11, if $Z_o \gg R_L$, the majority of the amplifier output current will pass on to the load. It will be demonstrated in the sections and chapters to follow that Z_o is frequently so large compared to R_L that it can be replaced by an open-circuit equivalent.

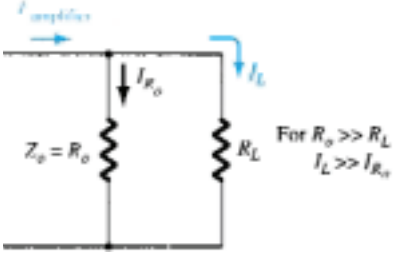


Figure 7.11 Effect of $Z_o = R_o$ on the load or output current I_L.

For the system of Fig. 7.12, determine the level of output impedance. *EXAMPLE 7.2*

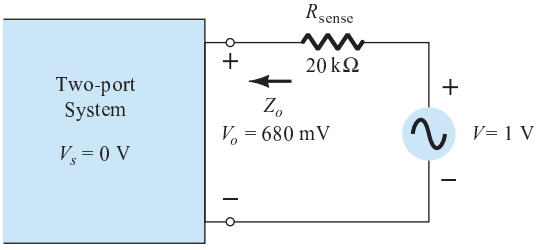


Figure 7.12 Example 7.2.

Solution

$$I_o = \frac{V - V_o}{R_{sense}} = \frac{1\text{ V} - 680\text{ mV}}{20\text{ k}\Omega} = \frac{320\text{ mV}}{20\text{ k}\Omega} = 16\ \mu\text{A}$$

and

$$Z_o = \frac{V_o}{I_o} = \frac{680\text{ mV}}{16\ \mu\text{A}} = \mathbf{42.5\ k\Omega}$$

Voltage Gain, A_v

One of the most important characteristics of an amplifier is the small-signal ac voltage gain as determined by

$$A_v = \frac{V_o}{V_i} \tag{7.6}$$

For the system of Fig. 7.13, a load has not been connected to the output terminals and the level of gain determined by Eq. (7.6) is referred to as the no-load voltage gain. That is,

$$A_{v_{NL}} = \left.\frac{V_o}{V_i}\right|_{R_L = \infty\ \Omega\ \text{(open circuit)}} \tag{7.7}$$

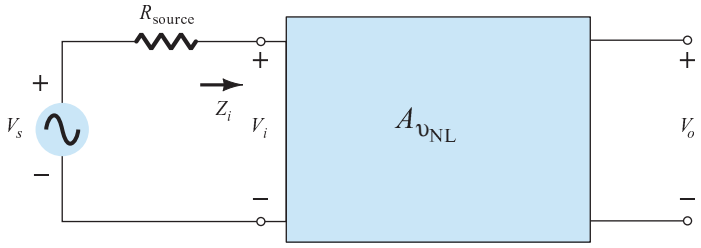


Figure 7.13 Determining the no-load voltage gain.

In Chapter 9 it will be demonstrated that:

For transistor amplifiers, the no-load voltage gain is greater than the loaded voltage gain.

For the system of Fig. 7.13 having a source resistance R_s, the level of V_i would first have to be determined using the voltage-divider rule before the gain V_o/V_s could be calculated. That is,

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

with

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

and

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i}$$

so that

$$A_{v_s} = \frac{V_o}{V_s} = \frac{Z_i}{Z_i + R_s} A_{v_{NL}} \tag{7.8}$$

Experimentally, the voltage gain A_{v_s} or $A_{v_{NL}}$ can be determined simply by measuring the appropriate voltage levels with an oscilloscope or sensitive DMM and substituting into the appropriate equation.

Depending on the configuration, the magnitude of the voltage gain for a loaded single-stage transistor amplifier typically ranges from just less than 1 to a few hundred. A multistage (multiunit) system, however, can have a voltage gain in the thousands.

EXAMPLE 7.3

For the BJT amplifier of Fig. 7.14, determine:
(a) V_i.
(b) I_i.
(c) Z_i.
(d) A_{v_s}.

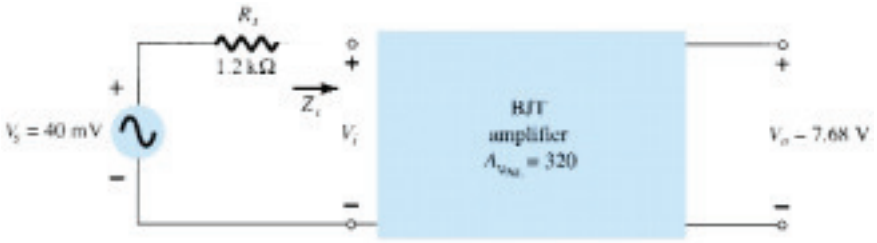


Figure 7.14 Example 7.3.

Solution

(a) $A_{v_{NL}} = \dfrac{V_o}{V_i}$ and $V_i = \dfrac{V_o}{A_{v_{NL}}} = \dfrac{7.68\text{ V}}{320} = \mathbf{24\text{ mV}}$

(b) $I_i = \dfrac{V_s - V_i}{R_s} = \dfrac{40\text{ mV} - 24\text{ mV}}{1.2\text{ k}\Omega} = \mathbf{13.33\ \mu A}$

(c) $Z_i = \dfrac{V_i}{I_i} = \dfrac{24\text{ mV}}{13.33\ \mu\text{A}} = \mathbf{1.8\text{ k}\Omega}$

(d) $A_{v_s} = \dfrac{Z_i}{Z_i + R_s} A_{v_{NL}}$

$= \dfrac{1.8\text{ k}\Omega}{1.8\text{ k}\Omega + 1.2\text{ k}\Omega}(320)$

$= \mathbf{192}$

Current Gain, A_i

The last numerical characteristic to be discussed is the current gain defined by

$$A_i = \frac{I_o}{I_i} \tag{7.9}$$

Although typically the recipient of less attention than the voltage gain, it is, however, an important quantity that can have significant impact on the overall effectiveness of a design. In general:

For BJT amplifiers, the current gain typically ranges from a level just less than 1 to a level that may exceed 100.

For the loaded situation of Fig. 7.15,

$$I_i = \frac{V_i}{Z_i} \quad \text{and} \quad I_o = -\frac{V_o}{R_L}$$

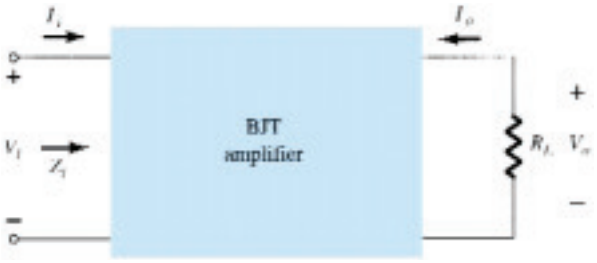


Figure 7.15 Determining the loaded current gain.

with $$A_i = \frac{I_o}{I_i} = -\frac{V_o/R_L}{V_i/Z_i} = -\frac{V_o Z_i}{V_i R_L}$$

and $$\boxed{A_i = -A_v \frac{Z_i}{R_L}} \qquad (7.10)$$

Eq. (7.10) allows the determination of the current gain from the voltage gain and the impedance levels.

Phase Relationship

The phase relationship between input and output sinusoidal signals is important for a variety of practical reasons. Fortunately, however:

For the typical transistor amplifier at frequencies that permit ignoring the effects of the reactive elements, the input and output signals are either 180° out of phase or in phase.

The reason for the either–or situation will become quite clear in the chapters to follow.

Summary

The parameters of primary importance for an amplifier have now been introduced: the input impedance Z_i, the output impedance Z_o, the voltage gain A_v, the current gain A_i, and the resulting phase relationship. Other factors, such as the applied frequency at the low and high ends of the frequency spectrum, will affect some of these parameters, but this will be discussed in Chapter 11. In the sections and chapters to follow, all the parameters will be determined for a variety of transistor networks to permit a comparison of the strengths and weaknesses for each configuration.

7.5 THE r_e TRANSISTOR MODEL

The r_e model employs a diode and controlled current source to duplicate the behavior of a transistor in the region of interest. Recall that a current-controlled current source is one where the parameters of the current source are controlled by a current elsewhere in the network. In fact, in general:

BJT transistor amplifiers are referred to as current-controlled devices.

Common Base Configuration

In Fig. 7.16a, a common-base *pnp* transistor has been inserted within the two-port structure employed in our discussion of the last few sections. In Fig. 7.16b, the r_e model for the transistor has been placed between the same four terminals. As noted in Section 7.3, the model (equivalent circuit) is chosen in such a way as to approximate the behavior of the device it is replacing in the operating region of interest. In other words, the results obtained with the model in place should be relatively close to those obtained with the actual transistor. You will recall from Chapter 3 that one junction of an operating transistor is forward-biased while the other is reverse-biased. The forward-biased junction will behave much like a diode (ignoring the effects of changing levels of V_{CE}) as verified by the curves of Fig. 3.7. For the base-to-emitter junction of the transistor of Fig. 7.16a, the diode equivalence of Fig. 7.16b between the same two terminals seems to be quite appropriate. For the output side, recall that the horizontal curves of Fig. 3.8 revealed that $I_c \cong I_e$ (as derived from $I_c = \alpha I_e$) for the range of values of V_{CE}. The current source of Fig. 7.16b establishes the fact that

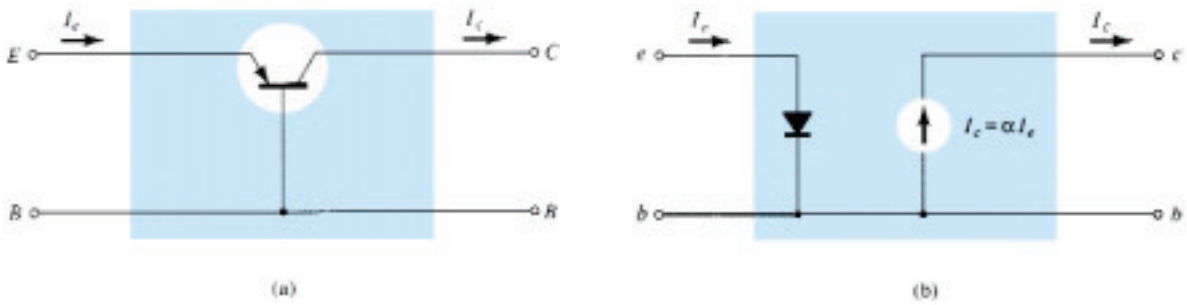


Figure 7.16 (a) Common-base BJT transistor; (b) r_e model for the configuration of Fig. 7.16a.

$I_c = \alpha I_e$, with the controlling current I_e appearing in the input side of the equivalent circuit as dictated by Fig. 7.16a. We have therefore established an equivalence at the input and output terminals with the current-controlled source, providing a link between the two—an initial review would suggest that the model of Fig. 7.16b is a valid model of the actual device.

Recall from Chapter 1 that the ac resistance of a diode can be determined by the equation $r_{ac} = 26\text{ mV}/I_D$, where I_D is the dc current through the diode at the Q (quiescent) point. This same equation can be used to find the ac resistance of the diode of Fig. 7.16b if we simply substitute the emitter current as follows:

$$r_e = \frac{26\text{ mV}}{I_E} \tag{7.11}$$

The subscript e of r_e was chosen to emphasize that it is the dc level of emitter current that determines the ac level of the resistance of the diode of Fig. 7.16b. Substituting the resulting value of r_e in Fig. 7.16b will result in the very useful model of Fig. 7.17.

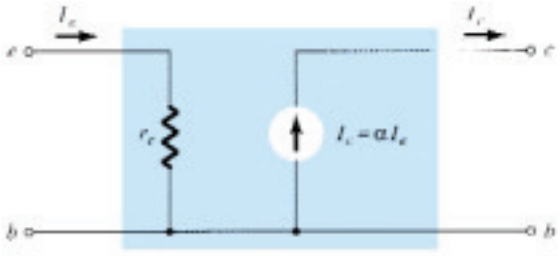


Figure 7.17 Common-base r_e equivalent circuit.

Due to the isolation that exists between input and output circuits of Fig. 7.17, it should be fairly obvious that the input impedance Z_i for the common-base configuration of a transistor is simply r_e. That is,

$$Z_i = r_e \quad (CB) \tag{7.12}$$

For the common-base configuration, typical values of Z_i range from a few ohms to a maximum of about 50 Ω.

For the output impedance, if we set the signal to zero, then $I_e = 0$ A and $I_c = \alpha I_e = \alpha(0\text{ A}) = 0$ A, resulting in an open-circuit equivalence at the output terminals. The result is that for the model of Fig. 7.17,

$$Z_o \cong \infty\ \Omega \quad (CB) \tag{7.13}$$

In actuality:

For the common-base configuration, typical values of Z_o are in the megohm range.

The output resistance of the common-base configuration is determined by the slope of the characteristic lines of the output characteristics as shown in Fig. 7.18. Assuming the lines to be perfectly horizontal (an excellent approximation) would result in the conclusion of Eq. (7.13). If care were taken to measure Z_o graphically or experimentally, levels typically in the range 1- to 2-MΩ would be obtained.

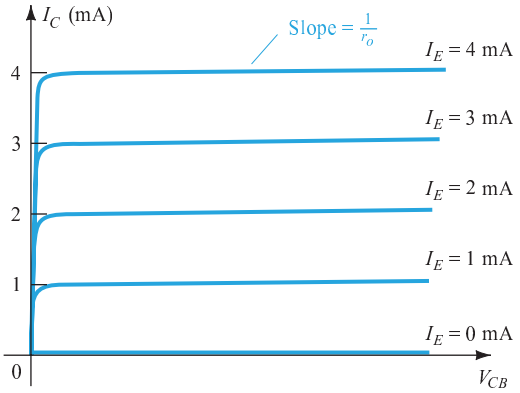


Figure 7.18 Defining Z_o.

In general, for the common-base configuration the input impedance is relatively small and the output impedance quite high.

The voltage gain will now be determined for the network of Fig. 7.19.

$$V_o = -I_o R_L = -(-I_c)R_L = \alpha I_e R_L$$

and

$$V_i = I_e Z_i = I_e r_e$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{\alpha I_e R_L}{I_e r_e}$$

and

$$\boxed{A_v = \frac{\alpha R_L}{r_e} \cong \frac{R_L}{r_e}}_{CB} \tag{7.14}$$

For the current gain,

$$A_i = \frac{I_o}{I_i} = \frac{-I_c}{I_e} = -\frac{\alpha I_e}{I_e}$$

and

$$\boxed{A_i = -\alpha \cong -1}_{CB} \tag{7.15}$$

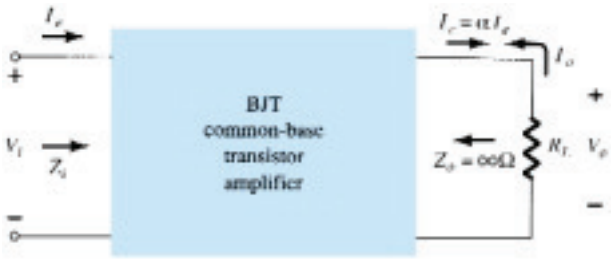


Figure 7.19 Defining $A_v = V_o/V_i$ for the common-base configuration.

The fact that the polarity of the voltage V_o as determined by the current I_c is the same as defined by Fig. 7.19 (i.e., the negative side is at ground potential) reveals that V_o and V_i are *in phase* for the common-base configuration. For an *npn* transistor in the common-base configuration, the equivalence would appear as shown in Fig. 7.20.

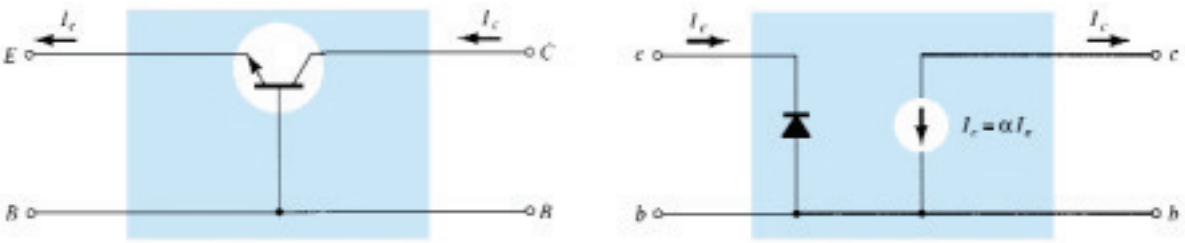


Figure 7.20 Approximate model for a common-base *npn* transistor configuration.

EXAMPLE 7.4

For a common-base configuration of Fig. 7.17 with $I_E = 4$ mA, $\alpha = 0.98$, and an ac signal of 2 mV applied between the base and emitter terminals:

(a) Determine the input impedance.
(b) Calculate the voltage gain if a load of 0.56 kΩ is connected to the output terminals.
(c) Find the output impedance and current gain.

Solution

(a) $r_e = \dfrac{26 \text{ mV}}{I_E} = \dfrac{26 \text{ mV}}{4 \text{ mA}} = \mathbf{6.5\ \Omega}$

(b) $I_i = I_e = \dfrac{V_i}{Z_i} = \dfrac{2 \text{ mV}}{6.5\ \Omega} = 307.69\ \mu\text{A}$

$$V_o = I_c R_L = \alpha I_e R_L = (0.98)(307.69\ \mu\text{A})(0.56\ \text{k}\Omega)$$
$$= 168.86 \text{ mV}$$

and $A_v = \dfrac{V_o}{V_i} = \dfrac{168.86 \text{ mV}}{2 \text{ mV}} = \mathbf{84.43}$

or from Eq. (7.14),

$$A_v = \frac{\alpha R_L}{r_e} = \frac{(0.98)(0.56\ \text{k}\Omega)}{6.5\ \Omega} = \mathbf{84.43}$$

(c) $Z_o \cong \infty\ \Omega$

$A_i = \dfrac{I_o}{I_i} = -\alpha = \mathbf{-0.98}$ as defined by Eq. (7.15)

Common Emitter Configuration

For the common-emitter configuration of Fig. 7.21a, the input terminals are the base and emitter terminals, but the output set is now the collector and emitter terminals. In addition, the emitter terminal is now common between the input and output ports of the amplifier. Substituting the r_e equivalent circuit for the *npn* transistor will result in the configuration of Fig. 7.21b. Note that the controlled-current source is still connected between the collector and base terminals and the diode between the base and

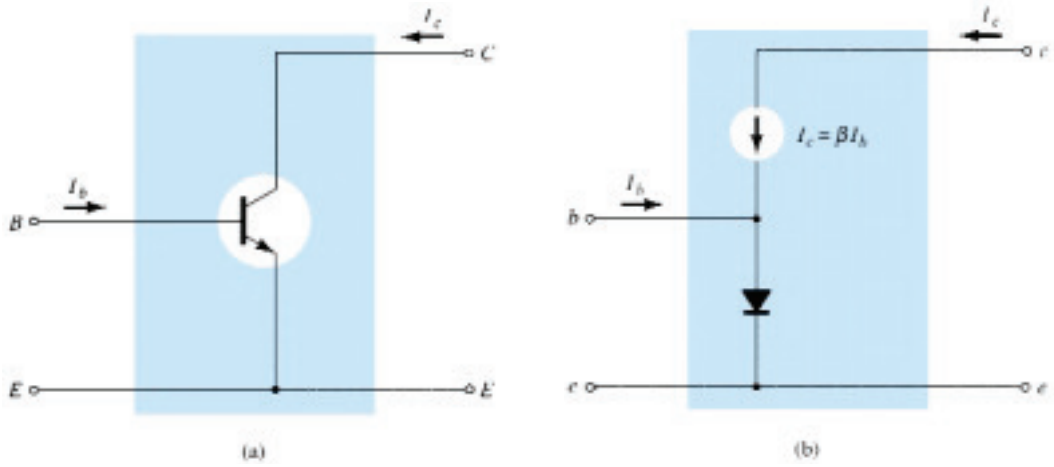


Figure 7.21 (a) Common-emitter BJT transistor; (b) approximate model for the configuration of Fig. 7.21a.

emitter terminals. In this configuration, the base current is the input current while the output current is still I_c. Recall from Chapter 3 that the base and collector currents are related by the following equation:

$$I_c = \beta I_b \tag{7.16}$$

The current through the diode is therefore determined by

$$I_e = I_c + I_b = \beta I_b + I_b$$

and

$$I_e = (\beta + 1) I_b \tag{7.17}$$

However, since the ac beta is typically much greater than 1, we will use the following approximation for the current analysis:

$$I_e \cong \beta I_b \tag{7.18}$$

The input impedance is determined by the following ratio:

$$Z_i = \frac{V_i}{I_i} = \frac{V_{be}}{I_b}$$

The voltage V_{be} is across the diode resistance as shown in Fig. 7.22. The level of r_e is still determined by the dc current I_E. Using Ohm's law gives

$$V_i = V_{be} = I_e r_e \cong \beta I_b r_e$$

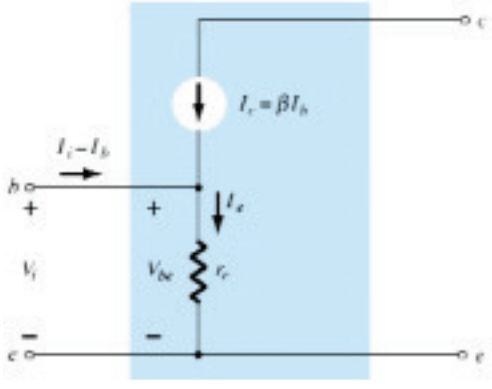


Figure 7.22 Determining Z_i using the approximate model.

Substituting yields

$$Z_i = \frac{V_{be}}{I_b} \cong \frac{\beta I_b r_e}{I_b}$$

and

$$\boxed{Z_i \cong \beta r_e}_{CE} \tag{7.19}$$

In essence, Eq. (7.19) states that the input impedance for a situation such as shown in Fig. 7.23 is beta times the value of r_e. In other words, a resistive element in the emitter leg is reflected into the input circuit by a multiplying factor β. For instance, if $r_e = 6.5\ \Omega$ as in Example 7.4 and $\beta = 160$ (quite typical), the input impedance has increased to a level of

$$Z_i \cong \beta r_e = (160)(6.5\ \Omega) = \mathbf{1.04\ k\Omega}$$

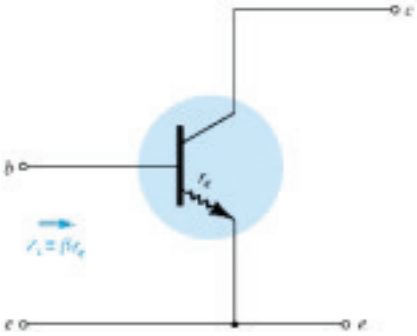


Figure 7.23 Impact of r_e on input impedance.

For the common-emitter configuration, typical values of Z_i defined by βr_e range from a few hundred ohms to the kilohm range, with maximums of about 6–7 kΩ.

For the output impedance, the characteristics of interest are the output set of Fig. 7.24. Note that the slope of the curves increases with increase in collector current. The steeper the slope, the less the level of output impedance (Z_o). The r_e model of Fig. 7.21 does not include an output impedance, but if available from a graphical analysis or from data sheets, it can be included as shown in Fig. 7.25.

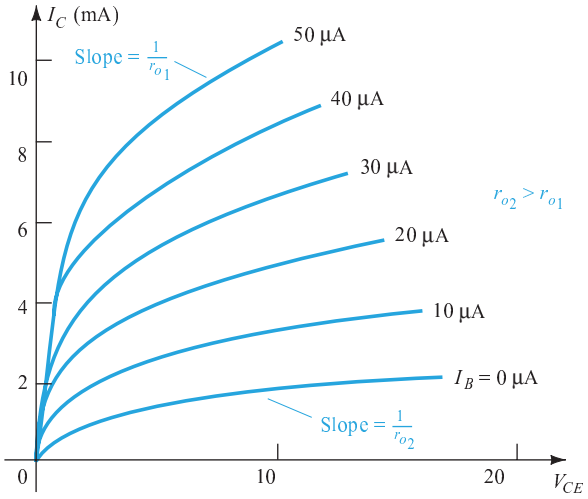


Figure 7.24 Defining r_o for the common-emitter configuration.

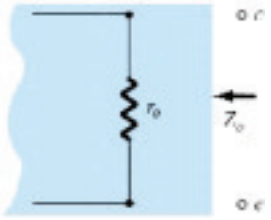


Figure 7.25 Including r_o in the transistor equivalent circuit.

For the common-emitter configuration, typical values of Z_o are in the range of 40 to 50 kΩ.

For the model of Fig. 7.25, if the applied signal is set to zero, the current I_c is 0 A and the output impedance is

$$\boxed{Z_o = r_o}_{CE} \tag{7.20}$$

Of course, if the contribution due to r_o is ignored as in the r_e model, the output impedance is defined by $Z_o = \infty\ \Omega$.

The voltage gain for the common-emitter configuration will now be determined for the configuration of Fig. 7.26 using the assumption that $Z_o = \infty\ \Omega$. The effect of including r_o will be considered in Chapter 8. For the defined direction of I_o and polarity of V_o,

$$V_o = -I_o R_L$$

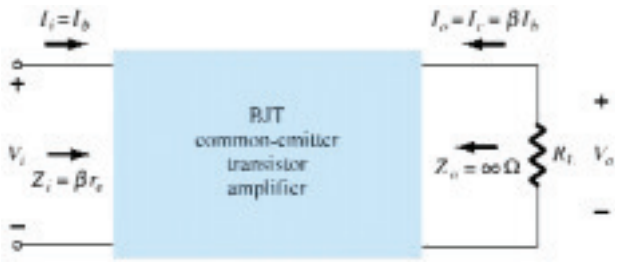


Figure 7.26 Determining the voltage and current gain for the common-emitter transistor amplifier.

The minus sign simply reflects the fact that the direction of I_o in Fig. 7.26 would establish a voltage V_o with the opposite polarity. Continuing gives

$$V_o = -I_o R_L = -I_c R_L = -\beta I_b R_L$$

and

$$V_i = I_i Z_i = I_b \beta r_e$$

so that

$$A_v = \frac{V_o}{V_i} = -\frac{\beta I_b R_L}{I_b \beta r_e}$$

and

$$\boxed{A_v = -\frac{R_L}{r_e}}_{CE, r_o = \infty \Omega} \tag{7.21}$$

The resulting minus sign for the voltage gain reveals that the output and input voltages are 180° out of phase.

The current gain for the configuration of Fig. 7.26:

$$A_i = \frac{I_o}{I_i} = \frac{I_c}{I_b} = \frac{\beta I_b}{I_b}$$

and

$$\boxed{A_i = \beta}_{CE, r_o = \infty\ \Omega} \tag{7.22}$$

Using the facts that the input impedance is βr_e, the collector current is βI_b, and the output impedance is r_o, the equivalent model of Fig. 7.27 can be an effective tool in the analysis to follow. For typical parameter values, the common-emitter configuration can be considered one that has a moderate level of input impedance, a high voltage and current gain, and an output impedance that may have to be included in the network analysis.

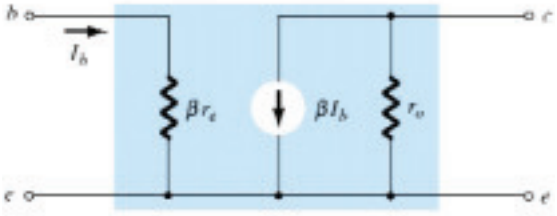


Figure 7.27 r_e model for the common-emitter transistor configuration.

EXAMPLE 7.5

Given $\beta = 120$ and $I_E = 3.2$ mA for a common-emitter configuration with $r_o = \infty\ \Omega$, determine:

(a) Z_i.

(b) A_v if a load of 2 kΩ is applied.

(c) A_i with the 2 kΩ load.

Solution

(a) $r_e = \dfrac{26\text{ mV}}{I_E} = \dfrac{26\text{ mV}}{3.2\text{ mA}} = 8.125\ \Omega$

and $Z_i = \beta r_e = (120)(8.125\ \Omega) = \mathbf{975\ \Omega}$

(b) Eq. (7.21): $A_v = -\dfrac{R_L}{r_e} = -\dfrac{2\text{ k}\Omega}{8.125\ \Omega} = \mathbf{-246.15}$

(c) $A_i = \dfrac{I_o}{I_i} = \beta = \mathbf{120}$

Common Collector Configuration

For the common-collector configuration, the model defined for the common-emitter configuration of Fig. 7.21 is normally applied rather than defining a model for the common-collector configuration. In subsequent chapters, a number of common-collector configurations will be investigated and the impact of using the same model will become quite apparent.

7.6 THE HYBRID EQUIVALENT MODEL

It was pointed out in Section 7.5 that the r_e model for a transistor is sensitive to the dc level of operation of the amplifier. The result is an input resistance that will vary with the dc operating point. For the hybrid equivalent model to be described in this section, the parameters are defined at an operating point that may or may not reflect the actual operating conditions of the amplifier. This is due to the fact that specification sheets cannot provide parameters for an equivalent circuit at every possible operating point. They must choose operating conditions that they believe reflect the general characteristics of the device. The hybrid parameters as shown in Fig. 7.28 are drawn from the specification sheet for the 2N4400 transistor described in Chapter 3. The values are provided at a dc collector current of 1 mA and a collector-to-emitter voltage of 10 V. In addition, a range of values is provided for each parameter for guidance in the initial design or analysis of a system. One obvious advantage of the specification sheet listing is the immediate knowledge of typical levels for the parameters of the device as compared to other transistors.

The quantities h_{ie}, h_{re}, h_{fe}, and h_{oe} of Fig. 7.28 are called the hybrid parameters and are the components of a small-signal equivalent circuit to be described shortly. For years, the hybrid model with all its parameters was the chosen model for the educational and industrial communities. Presently, however, the r_e model is applied more frequently, but often with the h_{oe} parameter of the hybrid equivalent model to provide

		Min.	Max.	
Input impedance (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz) 2N4400	h_{ie}	0.5	7.5	kΩ
Voltage feedback ratio (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz)	h_{re}	0.1	8.0	$\times 10^{-4}$
Small-signal current gain (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz) 2N4400	h_{fe}	20	250	—
Output admittance (I_C = 1 mA dc, V_{CE} = 10 V dc, f = 1 kHz)	h_{oe}	1.0	30	1μS

Figure 7.28 Hybrid parameters for the 2N4400 transistor.

some measure for the output impedance. Since specification sheets do provide the hybrid parameters and the hybrid model continues to receive a good measure of attention, it is quite important that the hybrid model be covered in some detail in this book. Once developed, the similarities between the r_e and hybrid models will be quite apparent. In fact, once the components of one are defined for a particular operating point, the parameters of the other model are immediately available.

Our description of the hybrid equivalent model will begin with the general two-port system of Fig. 7.29. The following set of equations (7.23) is only one of a number of ways in which the four variables of Fig. 7.29 can be related. It is the most frequently employed in transistor circuit analysis, however, and therefore is discussed in detail in this chapter.

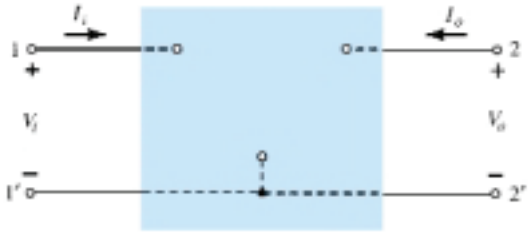


Figure 7.29 Two-port system.

$$V_i = h_{11}I_i + h_{12}V_o \tag{7.23a}$$

$$I_o = h_{21}I_i + h_{22}V_o \tag{7.23b}$$

The parameters relating the four variables are called *h-parameters* from the word "hybrid." The term *hybrid* was chosen because the mixture of variables (V and I) in each equation results in a "hybrid" set of units of measurement for the h-parameters. A clearer understanding of what the various h-parameters represent and how we can determine their magnitude can be developed by isolating each and examining the resulting relationship.

If we arbitrarily set $V_o = 0$ (short circuit the output terminals) and solve for h_{11} in Eq. (7.23a), the following will result:

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o = 0} \quad \text{ohms} \tag{7.24}$$

The ratio indicates that the parameter h_{11} is an impedance parameter with the units of ohms. Since it is the ratio of the *input* voltage to the *input* current with the output terminals *shorted,* it is called the *short-circuit input-impedance parameter.* The subscript 11 of h_{11} defines the fact that the parameter is determined by a ratio of quantities measured at the input terminals.

If I_i is set equal to zero by opening the input leads, the following will result for h_{12}:

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i = 0} \quad \text{unitless} \tag{7.25}$$

The parameter h_{12}, therefore, is the ratio of the input voltage to the output voltage with the input current equal to zero. It has no units since it is a ratio of voltage levels and is called the *open-circuit reverse transfer voltage ratio parameter.* The subscript 12 of h_{12} reveals that the parameter is a transfer quantity determined by a ratio of input to output measurements. The first integer of the subscript defines the

measured quantity to appear in the numerator; the second integer defines the source of the quantity to appear in the denominator. The term *reverse* is included because the ratio is an input voltage over an output voltage rather than the reverse ratio typically of interest.

If in Eq. (7.23b) V_o is equal to zero by again shorting the output terminals, the following will result for h_{21}:

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0} \qquad \text{unitless} \qquad (7.26)$$

Note that we now have the ratio of an output quantity to an input quantity. The term *forward* will now be used rather than *reverse* as indicated for h_{12}. The parameter h_{21} is the ratio of the output current to the input current with the output terminals shorted. This parameter, like h_{12}, has no units since it is the ratio of current levels. It is formally called the *short-circuit forward transfer current ratio parameter.* The subscript 21 again indicates that it is a transfer parameter with the output quantity in the numerator and the input quantity in the denominator.

The last parameter, h_{22}, can be found by again opening the input leads to set $I_1 = 0$ and solving for h_{22} in Eq. (7.23b):

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0} \qquad \text{siemens} \qquad (7.27)$$

Since it is the ratio of the output current to the output voltage, it is the output conductance parameter and is measured in siemens (S). It is called the *open-circuit output admittance parameter.* The subscript 22 reveals that it is determined by a ratio of output quantities.

Since each term of Eq. (7.23a) has the unit volt, let us apply Kirchhoff's voltage law "in reverse" to find a circuit that "fits" the equation. Performing this operation will result in the circuit of Fig. 7.30. Since the parameter h_{11} has the unit ohm, it is represented by a resistor in Fig. 7.30. The quantity h_{12} is dimensionless and therefore simply appears as a multiplying factor of the "feedback" term in the input circuit.

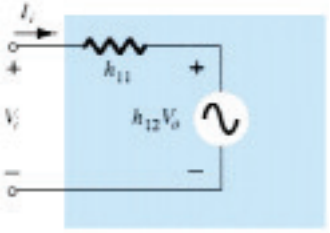


Figure 7.30 Hybrid input equivalent circuit.

Since each term of Eq. (7.23b) has the units of current, let us now apply Kirchhoff's current law "in reverse" to obtain the circuit of Fig. 7.31. Since h_{22} has the units of admittance, which for the transistor model is conductance, it is represented by the resistor symbol. Keep in mind, however, that the resistance in ohms of this resistor is equal to the reciprocal of conductance ($1/h_{22}$).

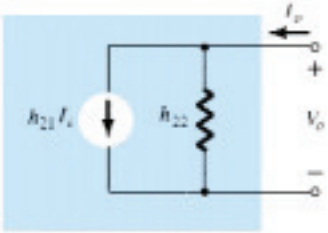


Figure 7.31 Hybrid output equivalent circuit.

The complete "ac" equivalent circuit for the basic three-terminal linear device is indicated in Fig. 7.32 with a new set of subscripts for the *h*-parameters. The notation of Fig. 7.32 is of a more practical nature since it relates the *h*-parameters to the resulting ratio obtained in the last few paragraphs. The choice of letters is obvious from the following listing:

$h_{11} \rightarrow$ *i*nput resistance $\rightarrow h_i$

$h_{12} \rightarrow$ *r*everse transfer voltage ratio $\rightarrow h_r$

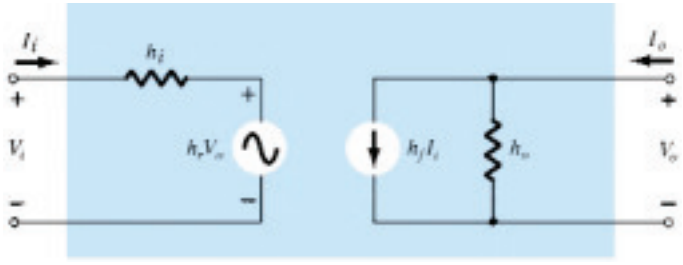


Figure 7.32 Complete hybrid equivalent circuit.

$h_{21} \rightarrow$ *f*orward transfer current ratio $\rightarrow h_f$

$h_{22} \rightarrow$ *o*utput conductance $\rightarrow h_o$

The circuit of Fig. 7.32 is applicable to any linear three-terminal electronic device or system with no internal independent sources. For the transistor, therefore, even though it has three basic configurations, *they are all three-terminal configurations,* so that the resulting equivalent circuit will have the same format as shown in Fig. 7.32. In each case, the bottom of the input and output sections of the network of Fig. 7.32 can be connected as shown in Fig. 7.33 since the potential level is the same. Essentially, therefore, the transistor model is a three-terminal two-port system. The *h*-parameters, however, will change with each configuration. To distinguish which parameter has been used or which is available, a second subscript has been added to the *h*-parameter notation. For the common-base configuration, the lowercase letter *b* was added, while for the common-emitter and common-collector configurations, the letters *e* and *c* were added, respectively. The hybrid equivalent network for the common-emitter configuration appears with the standard notation in Fig. 7.33. Note that $I_i = I_b$, $I_o = I_c$, and through an application of Kirchhoff's current law, $I_e = I_b + I_c$. The input voltage is now V_{be}, with the output voltage V_{ce}. For the common-base configuration of Fig. 7.34, $I_i = I_e$, $I_o = I_c$ with $V_{eb} = V_i$ and $V_{cb} = V_o$. The networks of Figs. 7.33 and 7.34 are applicable for *pnp* or *npn* transistors.

The fact that both a Thévenin and Norton circuit appear in the circuit of Fig. 7.32 was further impetus for calling the resultant circuit a *hybrid* equivalent circuit. Two additional transistor equivalent circuits, not to be discussed in this text, called the

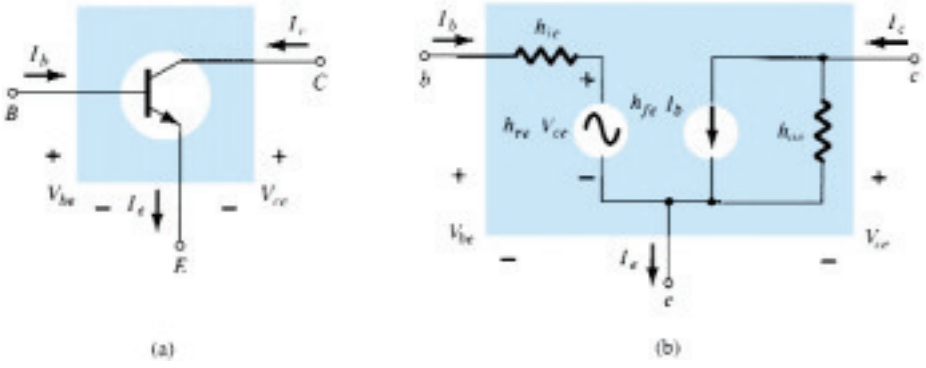


Figure 7.33 Common-emitter configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

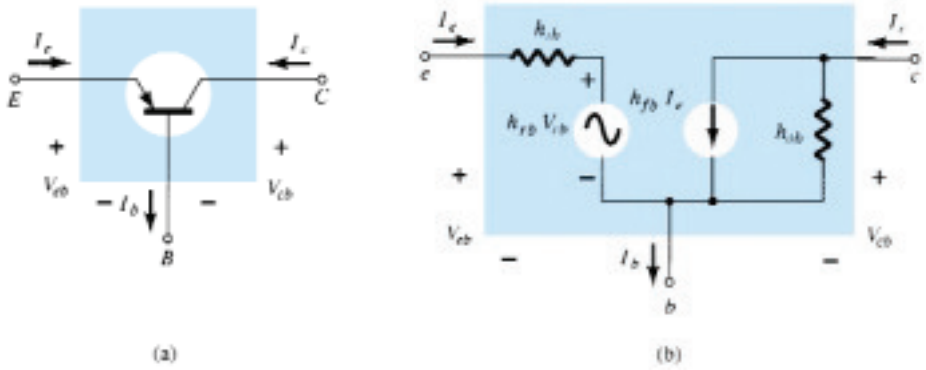


Figure 7.34 Common-base configuration: (a) graphical symbol; (b) hybrid equivalent circuit.

z-parameter and **y**-parameter equivalent circuits, use either the voltage source or the current source, but not both, in the same equivalent circuit. In Section 7.7, the magnitudes of the various parameters will be found from the transistor characteristics in the region of operation resulting in the desired *small-signal equivalent network* for the transistor.

For the common-emitter and common-base configurations, the magnitude of h_r and h_o is often such that the results obtained for the important parameters such as Z_i, Z_o, A_v, and A_i are only slightly affected if they (h_r and h_o) are not included in the model.

Since h_r is normally a relatively small quantity, its removal is approximated by $h_r \cong 0$ and $h_r V_o = 0$, resulting in a short-circuit equivalent for the feedback element as shown in Fig. 7.35. The resistance determined by $1/h_o$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open-circuit equivalent for the CE and CB models, as shown in Fig. 7.35.

The resulting equivalent of Fig. 7.36 is quite similar to the general structure of the common-base and common-emitter equivalent circuits obtained with the r_e model. In fact, the hybrid equivalent and the r_e models for each configuration have been repeated in Fig. 7.37 for comparison. It should be reasonably clear from Fig. 7.37a that

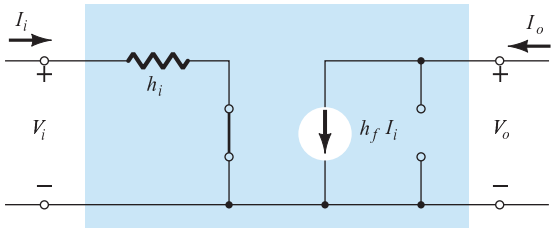


Figure 7.35 Effect of removing h_{re} and h_{oe} from the hybrid equivalent circuit.

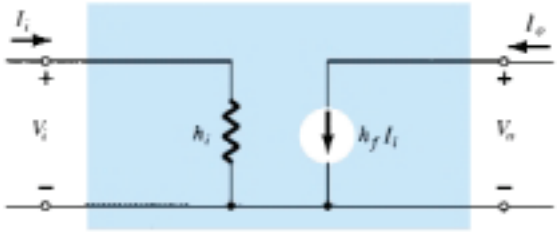


Figure 7.36 Approximate hybrid equivalent model.

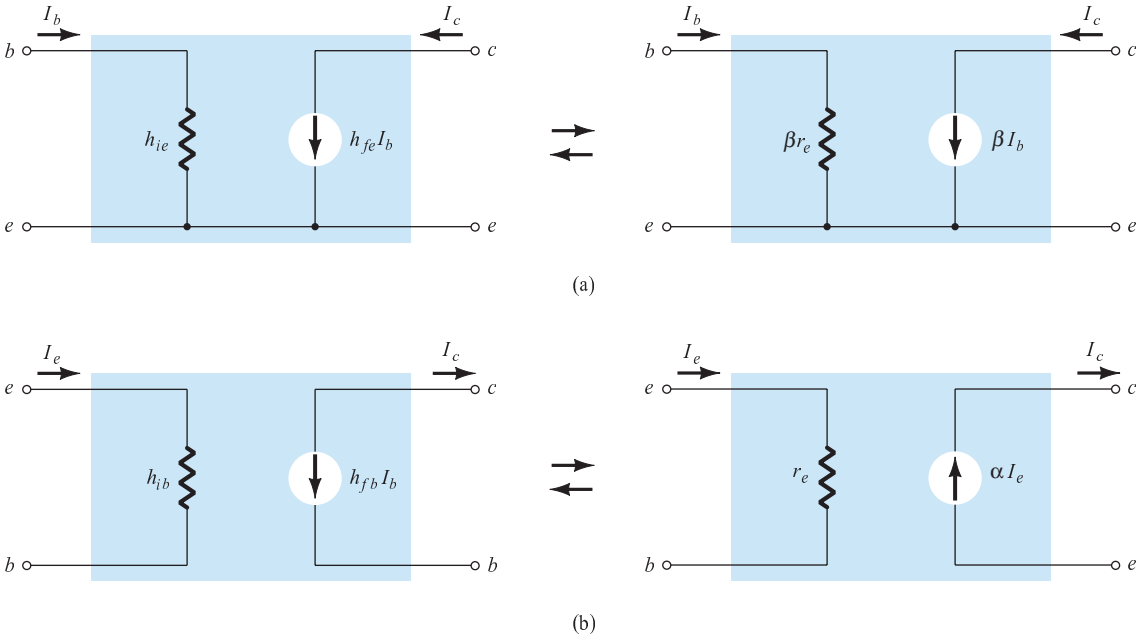


Figure 7.37 Hybrid versus r_e model: (a) common-emitter configuration; (b) common-base configuration.

$$h_{ie} = \beta r_e \tag{7.28}$$

and

$$h_{fe} = \beta_{ac} \tag{7.29}$$

From Fig. 7.37b,

$$h_{ib} = r_e \tag{7.30}$$

and

$$h_{fb} = -\alpha \cong -1 \tag{7.31}$$

In particular, note that the minus sign in Eq. (7.31) accounts for the fact that the current source of the standard hybrid equivalent circuit is pointing down rather than in the actual direction as shown in the r_e model of Fig. 7.37b.

EXAMPLE 7.6

Given $I_E = 2.5$ mA, $h_{fe} = 140$, $h_{oe} = 20$ μS (μmho), and $h_{ob} = 0.5$ μS, determine:
(a) The common-emitter hybrid equivalent circuit.
(b) The common-base r_e model.

Solution

(a) $$r_e = \frac{26 \text{ mV}}{I_E} = \frac{26 \text{ mV}}{2.5 \text{ mA}} = 10.4\ \Omega$$

$$h_{ie} = \beta r_e = (140)(10.4\ \Omega) = \mathbf{1.456\ k\Omega}$$

$$r_o = \frac{1}{h_{oe}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

Note Fig. 7.38.

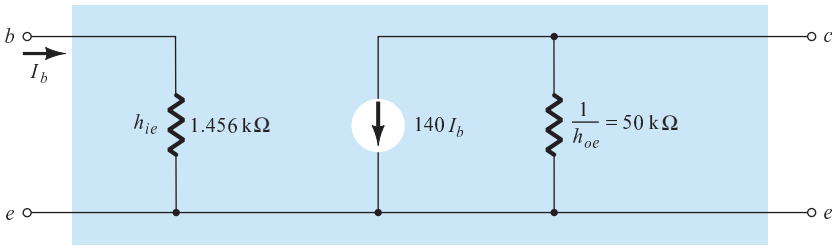


Figure 7.38 Common-emitter hybrid equivalent circuit for the parameters of example 7.6.

(b) $r_e = \mathbf{10.4\ \Omega}$

$$\alpha \cong 1, \qquad r_o = \frac{1}{h_{ob}} = \frac{1}{0.5\ \mu\text{S}} = \mathbf{2\ M\Omega}$$

Note Fig. 7.39.

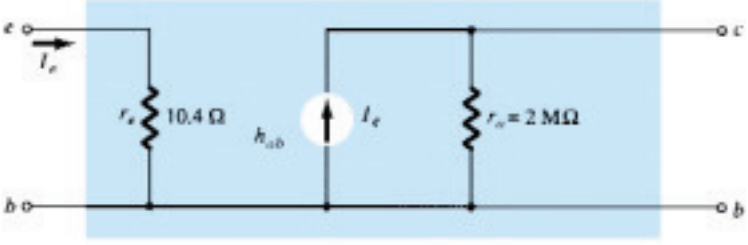


Figure 7.39 Common-base r_e model for the parameters of example 7.6.

A series of equations relating the parameters of each configuration for the hybrid equivalent circuit is provided in Appendix A. In Section 7.8, we demonstrate that the hybrid parameter h_{fe} (β_{ac}) is the least sensitive of the hybrid parameters to a change in collector current. Assuming, therefore, that $h_{fe} = \beta$ is a constant for the range of interest, is a fairly good approximation. It is $h_{ie} = \beta r_e$ that will vary significantly with I_C and should be determined at operating levels, since it can have a real impact on the gain levels of a transistor amplifier.

7.7 GRAPHICAL DETERMINATION OF THE *h*-PARAMETERS

Using partial derivatives (calculus), it can be shown that the magnitude of the *h*-parameters for the small-signal transistor equivalent circuit in the region of operation for the common-emitter configuration can be found using the following equations:*

$$h_{ie} = \frac{\partial v_i}{\partial i_i} = \frac{\partial v_{be}}{\partial i_b} \cong \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{CE} = \text{ constant}} \quad \text{(ohms)} \tag{7.32}$$

$$h_{re} = \frac{\partial v_i}{\partial v_o} = \frac{\partial v_{be}}{\partial v_{ce}} \cong \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_B = \text{ constant}} \quad \text{(unitless)} \tag{7.33}$$

$$h_{fe} = \frac{\partial i_o}{\partial i_i} = \frac{\partial i_c}{\partial i_b} \cong \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{CE} = \text{ constant}} \quad \text{(unitless)} \tag{7.34}$$

$$h_{oe} = \frac{\partial i_o}{\partial v_o} = \frac{\partial i_c}{\partial v_{ce}} \cong \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{I_B = \text{ constant}} \quad \text{(siemens)} \tag{7.35}$$

In each case, the symbol Δ refers to a small change in that quantity around the quiescent point of operation. In other words, the *h*-parameters are determined in the region of operation for the applied signal so that the equivalent circuit will be the most accurate available. The constant values of V_{CE} and I_B in each case refer to a condition that must be met when the various parameters are determined from the characteristics of the transistor. For the common-base and common-collector configurations, the proper equation can be obtained by simply substituting the proper values of v_i, v_o, i_i, and i_o.

The parameters h_{ie} and h_{re} are determined from the input or base characteristics, while the parameters h_{fe} and h_{oe} are obtained from the output or collector characteristics. Since h_{fe} is usually the parameter of greatest interest, we shall discuss the operations involved with equations, such as Eqs. (7.32) through (7.35), for this parameter first. The first step in determining any of the four hybrid parameters is to find the quiescent point of operation as indicated in Fig. 7.40. In Eq. (7.34) the condition $V_{CE} =$ constant requires that the changes in base current and collector current be taken along a vertical straight line drawn through the *Q*-point representing a fixed collector-to-emitter voltage. Equation (7.34) then requires that a small change in collector current be divided by the corresponding change in base current. For the greatest accuracy, these changes should be made as small as possible.

*The partial derivative $\partial v_i/\partial i_i$ provides a measure of the instantaneous change in v_i due to an instantaneous change in i_i.

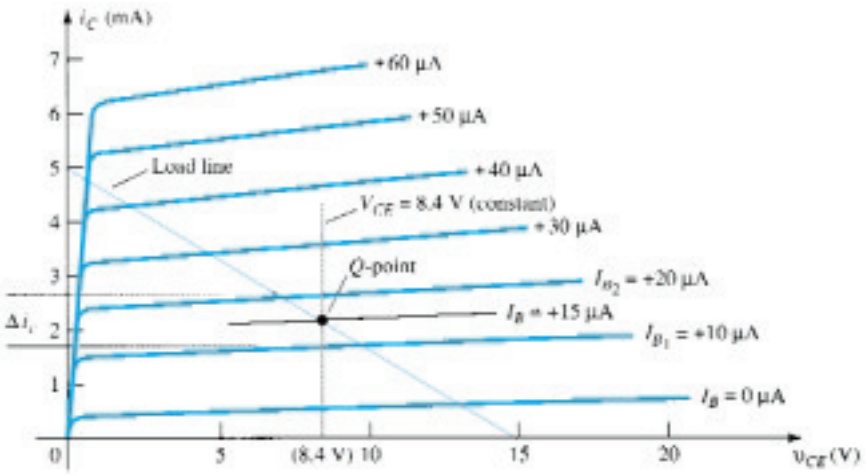


Figure 7.40 h_{fe} determination.

In Fig. 7.40, the change in i_b was chosen to extend from I_{B_1} to I_{B_2} along the perpendicular straight line at V_{CE}. The corresponding change in i_c is then found by drawing the horizontal lines from the intersections of I_{B_1} and I_{B_2} with V_{CE} = constant to the vertical axis. All that remains is to substitute the resultant changes of i_b and i_c into Eq. (7.34). That is,

$$|h_{fe}| = \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{CE}\ =\ \text{constant}} = \left.\frac{(2.7 - 1.7)\ \text{mA}}{(20 - 10)\ \mu\text{A}}\right|_{V_{CE}\ =\ 8.4\ \text{V}}$$

$$= \frac{10^{-3}}{10 \times 10^{-6}} = \mathbf{100}$$

In Fig. 7.41, a straight line is drawn tangent to the curve I_B through the Q-point to establish a line I_B = constant as required by Eq. (7.35) for h_{oe}. A change in v_{CE} was then chosen and the corresponding change in i_C determined by drawing the horizontal lines to the vertical axis at the intersections on the I_B = constant line. Substituting into Eq. (7.35), we get

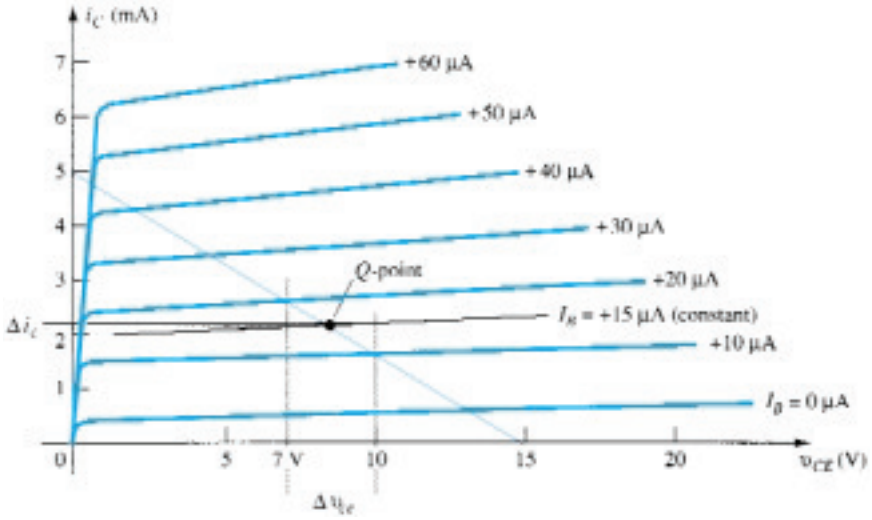


Figure 7.41 h_{oe} determination.

$$|h_{oe}| = \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{I_B = \text{ constant}} = \left.\frac{(2.2 - 2.1)\text{ mA}}{(10 - 7)\text{ V}}\right|_{I_B = +15\ \mu\text{A}}$$

$$= \frac{0.1 \times 10^{-3}}{3} = \mathbf{33\ \mu A/V = 33 \times 10^{-6}\ S = 33\ \mu S}$$

To determine the parameters h_{ie} and h_{re} the Q-point must first be found on the input or base characteristics as indicated in Fig. 7.42. For h_{ie}, a line is drawn tangent to the curve $V_{CE} = 8.4$ V through the Q-point to establish a line $V_{CE} =$ constant as required by Eq. (7.32). A small change in v_{be} was then chosen, resulting in a corresponding change in i_b. Substituting into Eq. (7.32), we get

$$|h_{ie}| = \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{CE} = \text{ constant}} = \left.\frac{(733 - 718)\text{ mV}}{(20 - 10)\ \mu\text{A}}\right|_{V_{CE} = 8.4\text{ V}}$$

$$= \frac{15 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{1.5\ k\Omega}$$

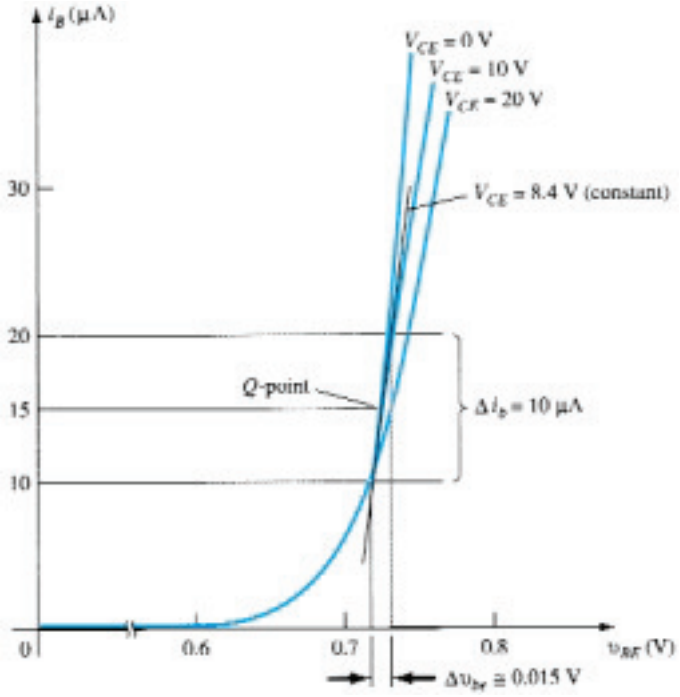


Figure 7.42 h_{ie} determination.

The last parameter, h_{re}, can be found by first drawing a horizontal line through the Q-point at $I_B = 15\ \mu$A. The natural choice then is to pick a change in v_{CE} and find the resulting change in v_{BE} as shown in Fig. 7.43.

Substituting into Eq. (7.33), we get

$$|h_{re}| = \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_B = \text{ constant}} = \frac{(733 - 725)\text{ mV}}{(20 - 0)\text{ V}} = \frac{8 \times 10^{-3}}{20} = \mathbf{4 \times 10^{-4}}$$

For the transistor whose characteristics have appeared in Figs. 7.40 through 7.43, the resulting hybrid small-signal equivalent circuit is shown in Fig. 7.44.

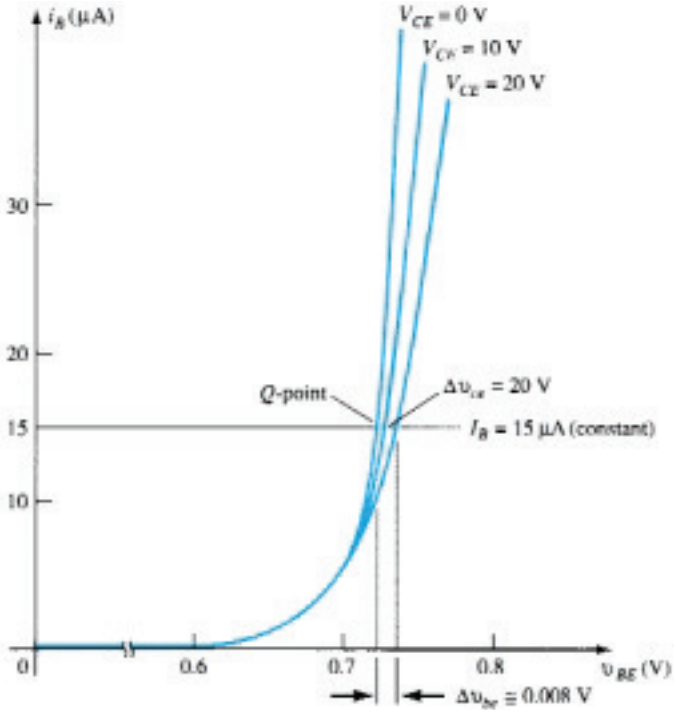


Figure 7.43 h_{re} determination.

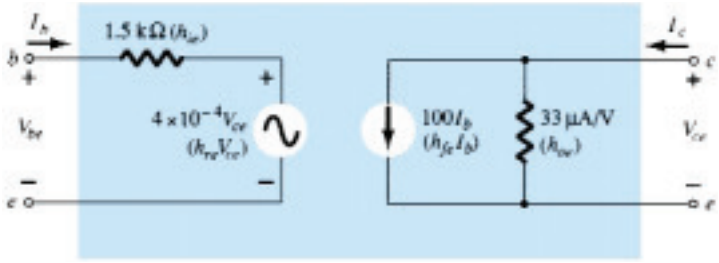


Figure 7.44 Complete hybrid equivalent circuit for a transistor having the characteristics that appear in Figs. 7.40 through 7.43.

As mentioned earlier, the hybrid parameters for the common-base and common-collector configurations can be found using the same basic equations with the proper variables and characteristics.

Table 7.1 lists typical parameter values in each of the three configurations for the broad range of transistors available today. The minus sign indicates that in Eq. (7.34) as one quantity increased in magnitude, within the change chosen, the other decreased in magnitude.

TABLE 7.1 Typical Parameter Values for the CE, CC, and CB Transistor Configurations

Parameter	*CE*	*CC*	*CB*
h_i	1 kΩ	1 kΩ	20 Ω
h_r	2.5×10^{-4}	≅1	3.0×10^{-4}
h_f	50	−50	−0.98
h_o	25 μA/V	25 μA/V	0.5 μA/V
$1/h_o$	40 kΩ	40 kΩ	2 MΩ

Note in retrospect (Section 3.5: Transistor Amplifying Action) that the input resistance of the common-base configuration is low, while the output resistance is high. Consider also that the short-circuit current gain is very close to 1. For the common-emitter and common-collector configurations, note that the input resistance is much higher than that of the common-base configuration and that the ratio of output to input resistance is about 40 : 1. Consider also for the common-emitter and common-base configurations that h_r is very small in magnitude. Transistors are available today with values of h_{fe} that vary from 20 to 600. For any transistor, the region of operation and conditions under which it is being used will have an effect on the various h-parameters. The effect of temperature and collector current and voltage on the h-parameters is discussed in Section 7.8.

7.8 VARIATIONS OF TRANSISTOR PARAMETERS

There are a large number of curves that can be drawn to show the variations of the h-parameters with temperature, frequency, voltage, and current. The most interesting and useful at this stage of the development include the h-parameter variations with junction temperature and collector voltage and current.

In Fig. 7.45, the effect of the collector current on the h-parameter has been indicated. Take careful note of the logarithmic scale on the vertical and horizontal axes. Logarithmic scales will be examined in Chapter 11. The parameters have all been normalized to unity so that the relative change in magnitude with collector current can easily be determined. On every set of curves, such as in Fig. 7.46, the operating point at which the parameters were found is always indicated. For this particular situation, the quiescent point is at the intersection of $V_{CE} = 5.0$ V and $I_C = 1.0$ mA. Since the frequency and temperature of operation will also affect the h-parameters, these quantities are also indicated on the curves. At 0.1 mA, h_{fe} is about 0.5 or 50% of its value at 1.0 mA, while at 3 mA, it is 1.5 or 150% of that value. In other words, if $h_{fe} = 50$ at $I_C = 1.0$ mA, h_{fe} has changed from a value of 0.5(50) = 25 to 1.5(50) = 75, with

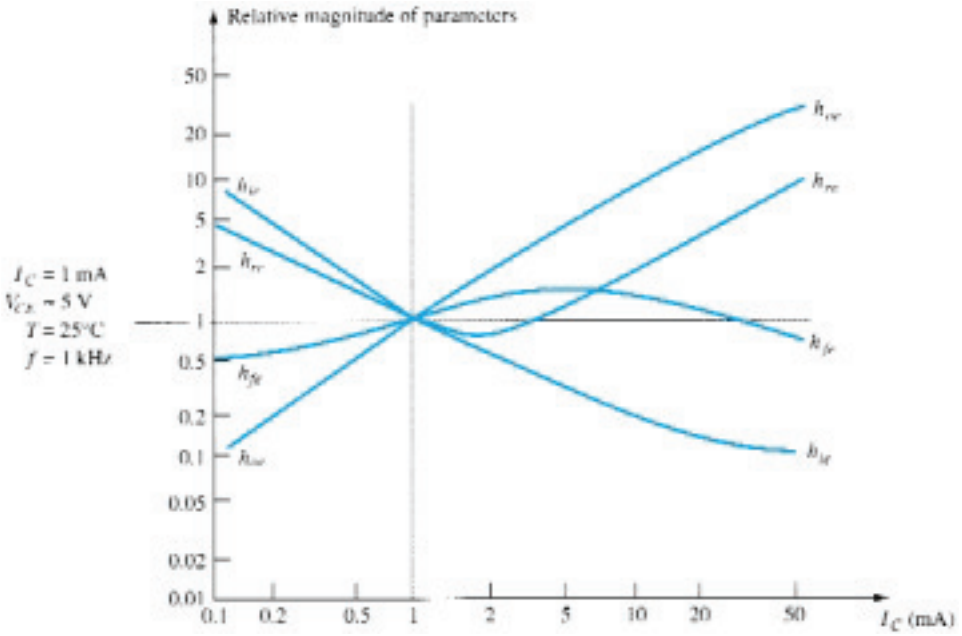


Figure 7.45 Hybrid parameter variations with collector current.

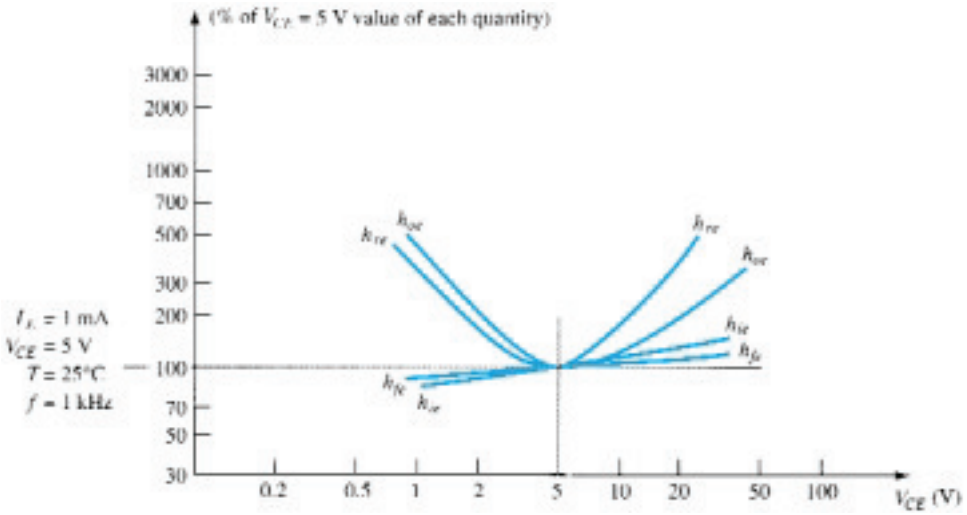


Figure 7.46 Hybrid parameter variations with collector–emitter potential.

a change of I_C from 0.1 to 3 mA. Consider, however, the point of operation at $I_C = 50$ mA. The magnitude of h_{re} is now approximately 11 times that at the defined Q-point, a magnitude that may not permit eliminating this parameter from the equivalent circuit. The parameter h_{oe} is approximately 35 times the normalized value. This increase in h_{oe} will decrease the magnitude of the output resistance of the transistor to a point where it may approach the magnitude of the load resistor. There would then be no justification in eliminating h_{oe} from the equivalent circuit on an approximate basis.

In Fig. 7.46, the variation in magnitude of the h-parameters on a normalized basis has been indicated with changes in collector voltage. This set of curves was normalized at the same operating point of the transistor discussed in Fig. 7.45 so that a comparison between the two sets of curves can be made. Note that h_{ie} and h_{fe} are relatively steady in magnitude while h_{oe} and h_{re} are much larger to the left and right of the chosen operating point. In other words, h_{oe} and h_{re} are much more sensitive to changes in collector voltage than are h_{ie} and h_{fe}.

It is interesting to note from Figs. 7.45 and 7.46 that the value of h_{fe} appears to change the least. Therefore, the specific value of current gain, whether h_{fe} or β, can, on an approximate and relative basis, be considered fairly constant for the range of collector current and voltage.

The value of $h_{ie} = \beta r_e$ does vary considerably with collector current as one might expect due to the sensitivity of r_e to emitter ($I_E \cong I_C$) current. It is therefore a quantity that should be determined as close to operating conditions as possible. For values below the specified V_{CE}, h_{re} is fairly constant, but it does increase measurably for higher values. It is indeed fortunate that for most applications the magnitude of h_{re} and h_{oe} are such that they can usually be ignored. They are quite sensitive to collector current and collector-to-emitter voltage.

In Fig. 7.47, the variation in h-parameters has been plotted for changes in junction temperature. The normalization value is taken to be room temperature: $T = 25°C$. The horizontal scale is a linear scale rather than a logarithmic scale as was employed for Figs. 7.45 and 7.46. In general, all the parameters increase in magnitude with temperature. The parameter least affected, however, is h_{oe}, while the input impedance h_{ie} changes at the greatest rate. The fact that h_{fe} will change from 50% of its normalized value at $-50°C$ to 150% of its normalized value at $+150°C$ indicates clearly that the operating temperature must be carefully considered in the design of transistor circuits.

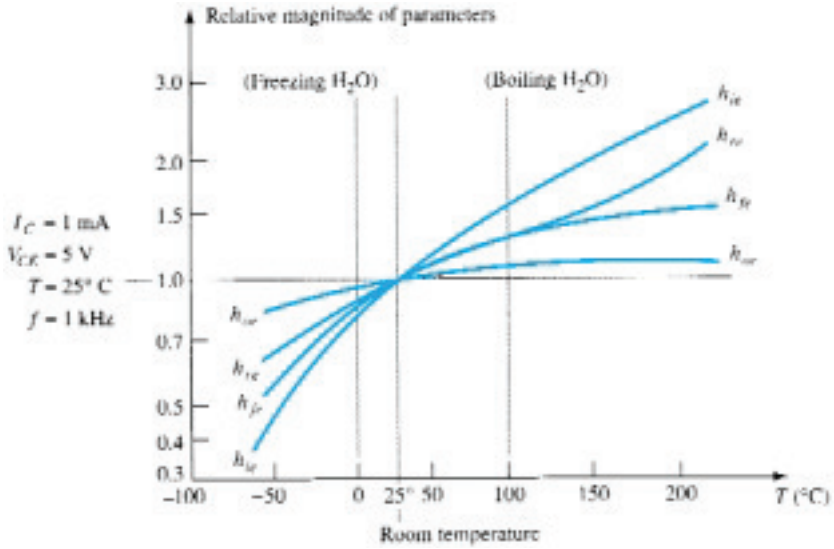


Figure 7.47 Hybrid parameter variations with temperature.

PROBLEMS

§ 7.2 Amplification in the AC Domain

1. (a) What is the expected amplification of a BJT transistor amplifier if the dc supply is set to zero volts?
(b) What will happen to the output ac signal if the dc level is insufficient? Sketch the effect on the waveform.
(c) What is the conversion efficiency of an amplifier in which the effective value of the current through a 2.2-kΩ load is 5 mA and the drain on the 18-V dc supply is 3.8 mA?

2. Can you think of an analogy that would explain the importance of the dc level on the resulting ac gain?

§ 7.3 BJT Transistor Modeling

3. What is the reactance of a 10-μF capacitor at a frequency of 1 kHz? For networks in which the resistor levels are typically in the kilohm range, is it a good assumption to use the short-circuit equivalence for the conditions just described? How about at 100 kHz?

4. Given the common-base configuration of Fig. 7.48, sketch the ac equivalent using the notation for the transistor model appearing in Fig. 7.5.

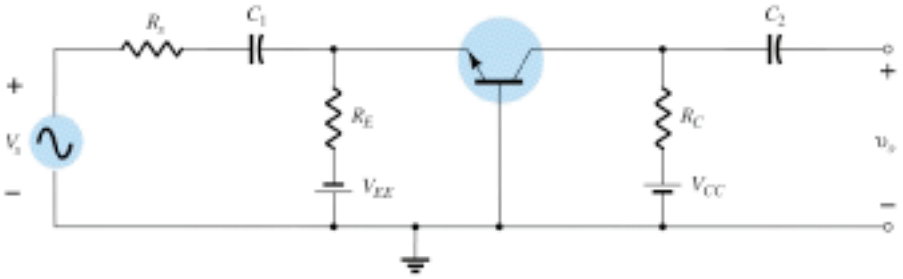


Figure 7.48 Problem 4

5. (a) Describe the differences between the r_e and hybrid equivalent models for a BJT transistor.
(b) For each model, list the conditions under which it should be applied.

§ 7.4 The Important Parameters: Z_i, Z_o, A_v, A_i

6. (a) For the configuration of Fig. 7.7, determine Z_i if $V_s = 40$ mV, $R_{\text{sense}} = 0.5$ kΩ, and $I_i = 20\ \mu$A.
(b) Using the results of part (a), determine V_i if the applied source is changed to 12 mV with an internal resistance of 0.4 kΩ.

7. (a) For the network of Fig. 7.10, determine Z_o if $V = 600$ mV, $R_{\text{sense}} = 10$ kΩ, and $I_o = 10\ \mu$A.
(b) Using the Z_o obtained in part (a), determine I_L for the configuration of Fig. 7.11 if $R_L = 2.2$ kΩ and $I_{\text{amplifier}} = 6$ mA.

8. Given the BJT configuration of Fig. 7.49, determine:
(a) V_i.
(b) Z_i.
(c) $A_{v_{\text{NL}}}$.
(d) A_{v_s}.

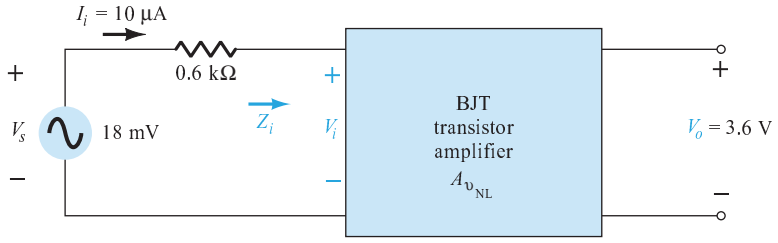


Figure 7.49 Problem 8

9. For the BJT amplifier of Fig. 7.50, determine:
(a) I_i.
(b) Z_i.
(c) V_o.
(d) I_o.
(e) A_i using the results of parts (a) and (d).
(f) A_i using Eq. (7.10).

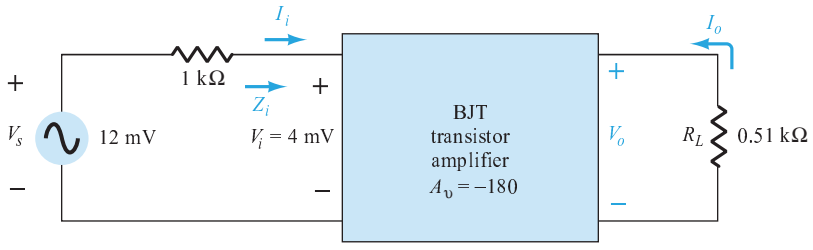


Figure 7.50 Problem 9

§ 7.5 The r_e Transistor Model

10. For the common-base configuration of Fig. 7.17, an ac signal of 10 mV is applied, resulting in an emitter current of 0.5 mA. If $\alpha = 0.980$, determine:
(a) Z_i.
(b) V_o if $R_L = 1.2$ kΩ.
(c) $A_v = V_o/V_i$.
(d) Z_o with $r_o = \infty$ Ω.
(e) $A_i = I_o/I_i$.
(f) I_b.

11. For the common-base configuration of Fig. 7.17, the emitter current is 3.2 mA and α is 0.99. Determine the following if the applied voltage is 48 mV and the load is 2.2 kΩ.
(a) r_e.
(b) Z_i.
(c) I_c.
(d) V_o.
(e) A_v.
(f) I_b.

12. Using the model of Fig. 7.27, determine the following for a common-emitter amplifier if $\beta = 80$, I_E (dc) = 2 mA, and $r_o = 40$ kΩ.
(a) Z_i.
(b) I_b.
(c) $A_i = I_o/I_i = I_L/I_b$ if $R_L = 1.2$ kΩ.
(d) A_v if $R_L = 1.2$ kΩ.

13. The input impedance to a common-emitter transistor amplifier is 1.2 kΩ with $\beta = 140$, $r_o = 50$ kΩ, and $R_L = 2.7$ kΩ. Determine:
(a) r_e.
(b) I_b if $V_i = 30$ mV.
(c) I_c.
(d) $A_i = I_o/I_i = I_L/I_b$.
(e) $A_v = V_o/V_i$.

§ 7.6 The Hybrid Equivalent Model

14. Given I_E (dc) = 1.2 mA, $\beta = 120$, and $r_o = 40$ kΩ, sketch the:
(a) Common-emitter hybrid equivalent model.
(b) Common-emitter r_e equivalent model.
(c) Common-base hybrid equivalent model.
(d) Common-base r_e equivalent model.

15. Given $h_{ie} = 2.4$ kΩ, $h_{fe} = 100$, $h_{re} = 4\times10^{-4}$, and $h_{oe} = 25$ μS, sketch the:
(a) Common-emitter hybrid equivalent model.
(b) Common-emitter r_e equivalent model.
(c) Common-base hybrid equivalent model.
(d) Common-base r_e equivalent model.

16. Redraw the common-emitter network of Fig. 7.3 for the ac response with the approximate hybrid equivalent model substituted between the appropriate terminals.

17. Redraw the network of Fig. 7.51 for the ac response with the r_e model inserted between the appropriate terminals. Include r_o.

18. Redraw the network of Fig. 7.52 for the ac response with the r_e model inserted between the appropriate terminals. Include r_o.

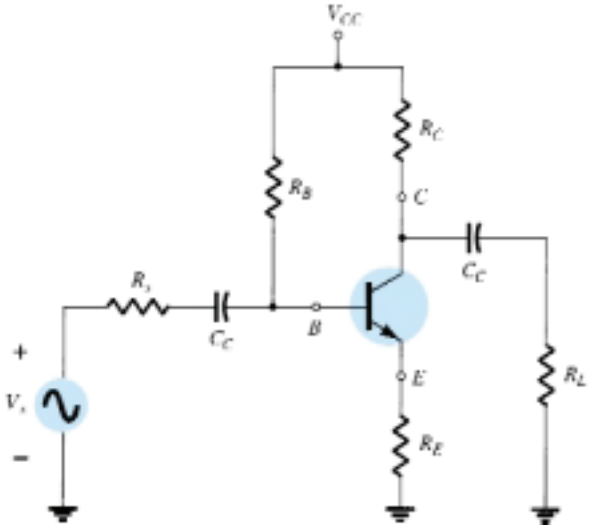


Figure 7.51 Problem 17

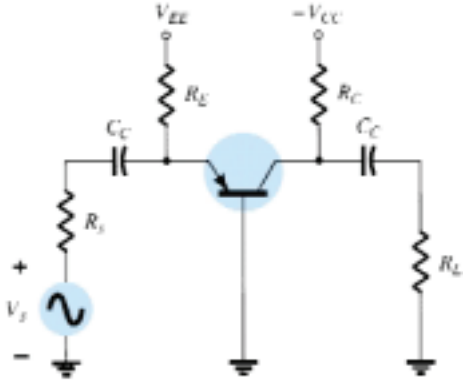


Figure 7.52 Problem 18

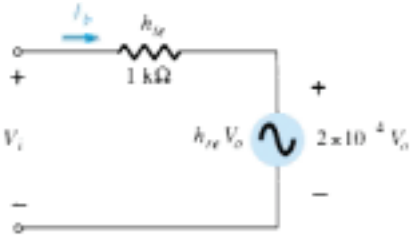


Figure 7.53 Problems 19, 21

19. Given the typical values of $h_{ie} = 1$ kΩ, $h_{re} = 2 \times 10^{-4}$, and $A_v = -160$ for the input configuration of Fig. 7.53:

(a) Determine V_o in terms of V_i.

(b) Calculate I_b in terms of V_i.

(c) Calculate I_b if $h_{re}V_o$ is ignored.

(d) Determine the percent difference in I_b using the following equation:

$$\%\ \text{difference in } I_b = \frac{I_b(\text{without } h_{re}) - I_b(\text{with } h_{re})}{I_b(\text{without } h_{re})} \times 100\%$$

(e) Is it a valid approach to ignore the effects of $h_{re}V_o$ for the typical values employed in this example?

20. Given the typical values of $R_L = 2.2$ kΩ and $h_{oe} = 20\ \mu$S, is it a good approximation to ignore the effects of $1/h_{oe}$ on the total load impedance? What is the percent difference in total loading on the transistor using the following equation?

$$\%\ \text{difference in total load} = \frac{R_L - R_L \| (1/h_{oe})}{R_L} \times 100\%$$

21. Repeat Problem 19 using the average values of the parameters of Fig. 7.28 with $A_v = -180$.

22. Repeat Problem 20 for $R_L = 3.3$ kΩ and the average value of h_{oe} in Fig. 7.28.

§ 7.7 Graphical Determination of the *h*-Parameters

23. (a) Using the characteristics of Fig. 7.40, determine h_{fe} at $I_C = 6$ mA and $V_{CE} = 5$ V.

(b) Repeat part (a) at $I_C = 1$ mA and $V_{CE} = 15$ V.

24. (a) Using the characteristics of Fig. 7.41, determine h_{oe} at $I_C = 6$ mA and $V_{CE} = 5$ V.
(b) Repeat part (a) at $I_C = 1$ mA and $V_{CE} = 15$ V.

25. (a) Using the characteristics of Fig. 7.42, determine h_{ie} at $I_B = 20\ \mu$A and $V_{CE} = 20$ V.
(b) Repeat part (a) at $I_B = 5\ \mu$A and $V_{CE} = 10$ V.

26. (a) Using the characteristics of Fig. 7.43, determine h_{re} at $I_B = 20\ \mu$A.
(b) Repeat part (a) at $I_B = 30\ \mu$A.

* **27.** Using the characteristics of Figs. 7.40 and 7.42, determine the approximate CE hybrid equivalent model at $I_B = 25\ \mu$A and $V_{CE} = 12.5$ V.

* **28.** Determine the CE r_e model at $I_B = 25\ \mu$A and $V_{CE} = 12.5$ V using the characteristics of Figs. 7.40 and 7.42.

* **29.** Using the results of Fig. 7.44, sketch the r_e equivalent model for the transistor having the characteristics appearing in Figs. 7.40 through 7.43. Include r_o.

§ 7.8 Variations of Transistor Parameters

For Problems 30 through 34, use Figs. 7.45 through 7.47.

30. (a) Using Fig. 7.45, determine the magnitude of the percent change in h_{fe} for an I_C change from 0.2 mA to 1 mA using the equation

$$\%\ \text{change} = \left| \frac{h_{fe}(0.2\ \text{mA}) - h_{fe}(1\ \text{mA})}{h_{fe}(0.2\ \text{mA})} \right| \times 100\%$$

(b) Repeat part (a) for an I_C change from 1 mA to 5 mA.

31. Repeat Problem 30 for h_{ie} (same changes in I_C).

32. (a) If $h_{oe} = 20\ \mu$S at $I_C = 1$ mA on Fig. 7.45, what is the approximate value of h_{oe} at $I_C = 0.2$ mA?
(b) Determine its resistive value at 0.2 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

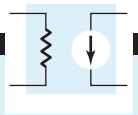
33. (a) If $h_{oe} = 20\ \mu$S at $I_C = 1$ mA on Fig. 7.45, what is the approximate value of h_{oe} at $I_C = 10$ mA?
(b) Determine its resistive value at 10 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

34. (a) If $h_{re} = 2 \times 10^{-4}$ at $I_C = 1$ mA on Fig. 7.45, determine the approximate value of h_{re} at 0.1 mA.
(b) Using the value of h_{re} determined in part (a), can h_{re} be ignored as a good approximation if $A_v = 210$?

* **35.** (a) Reviewing the characteristics of Fig. 7.45, which parameter changed the least for the full range of collector current?
(b) Which parameter changed the most?
(c) What are the maximum and minimum values of $1/h_{oe}$? Is the approximation $1/h_{oe} \| R_L \cong R_L$ more appropriate at high or low levels of collector current?
(d) In which region of current spectrum is the approximation $h_{re}V_{ce} \cong 0$ the most appropriate?

36. (a) Reviewing the characteristics of Fig. 7.47, which parameter changed the most with increase in temperature?
(b) Which changed the least?
(c) What are the maximum and minimum values of h_{fe}? Is the change in magnitude significant? Was it expected?
(d) How does r_e vary with increase in temperature? Simply calculate its level at three or four points and compare their magnitudes.
(e) In which temperature range do the parameters change the least?

*Please Note: Asterisks indicate more difficult problems.



CHAPTER

8 BJT Small-Signal Analysis

8.1 INTRODUCTION

The transistor models introduced in Chapter 7 will now be used to perform a small-signal ac analysis of a number of standard transistor network configurations. The networks analyzed represent the majority of those appearing in practice today. Modifications of the standard configurations will be relatively easy to examine once the content of this chapter is reviewed and understood.

Since the r_e model is sensitive to the actual point of operation, it will be our primary model for the analysis to be performed. For each configuration, however, the effect of an output impedance is examined as provided by the h_{oe} parameter of the hybrid equivalent model. To demonstrate the similarities in analysis that exist between models, a section is devoted to the small-signal analysis of BJT networks using solely the hybrid equivalent model. The analysis of this chapter does not include a load resistance R_L or source resistance R_s. The effect of both parameters is reserved for a systems approach in Chapter 10.

The computer analysis section includes a brief description of the transistor model employed in the PSpice software package. It demonstrates the range and depth of the computer analysis systems available today and how relatively easy it is to enter a complex network and print out the desired results.

8.2 COMMON-EMITTER FIXED-BIAS CONFIGURATION

The first configuration to be analyzed in detail is the common-emitter *fixed-bias* network of Fig. 8.1. Note that the input signal V_i is applied to the base of the transistor while the output V_o is off the collector. In addition, recognize that the input current I_i is not the base current but the source current, while the output current I_o is the collector current. The small-signal ac analysis begins by removing the dc effects of V_{CC} and replacing the dc blocking capacitors C_1 and C_2 by short-circuit equivalents, resulting in the network of Fig. 8.2.

Note in Fig. 8.2 that the common ground of the dc supply and the transistor emitter terminal permits the relocation of R_B and R_C in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network parameters Z_i, Z_o, I_i, and I_o on the redrawn network. Substituting the r_e model for the common-emitter configuration of Fig. 8.2 will result in the network of Fig. 8.3.

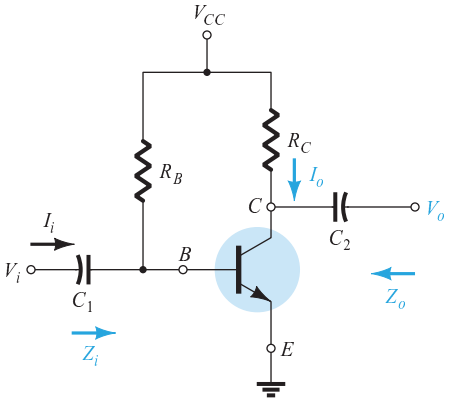


Figure 8.1 Common-emitter fixed-bias configuration.

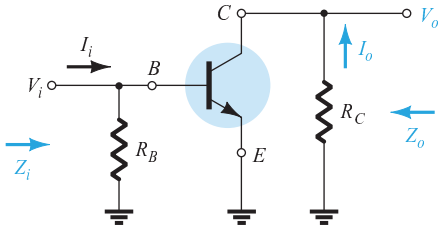


Figure 8.2 Network of Figure 8.1 following the removal of the effects of V_{CC}, C_1, and C_2.

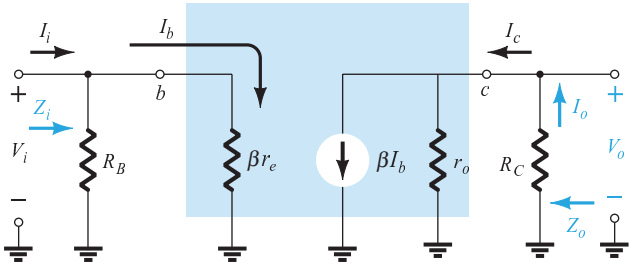


Figure 8.3 Substituting the r_e model into the network of Fig. 8.2.

The next step is to determine β, r_e, and r_o. The magnitude of β is typically obtained from a specification sheet or by direct measurement using a curve tracer or transistor testing instrument. The value of r_e must be determined from a dc analysis of the system, and the magnitude of r_o is typically obtained from the specification sheet or characteristics. Assuming that β, r_e, and r_o have been determined will result in the following equations for the important two-port characteristics of the system.

***Z_i*:** Figure 8.3 clearly reveals that

$$Z_i = R_B \| \beta r_e \quad \text{ohms} \tag{8.1}$$

For the majority of situations R_B is greater than βr_e by more than a factor of 10 (recall from the analysis of parallel elements that the total resistance of two parallel resistors is always less than the smallest and very close to the smallest if one is much larger than the other), permitting the following approximation:

$$Z_i \cong \beta r_e \quad \text{ohms} \tag{8.2}$$
$$R_B \geq 10\beta r_e$$

***Z_o*:** Recall that the output impedance of any system is defined as the impedance Z_o determined when $V_i = 0$. For Fig. 8.3, when $V_i = 0$, $I_i = I_b = 0$, resulting in an open-circuit equivalence for the current source. The result is the configuration of Fig. 8.4.

$$Z_o = R_C \| r_o \quad \text{ohms} \tag{8.3}$$

If $r_o \geq 10\ R_D$, the approximation $R_C \| r_o \cong R_C$ is frequently applied and

$$Z_o \cong R_C \tag{8.4}$$
$$r_o \geq 10R_C$$

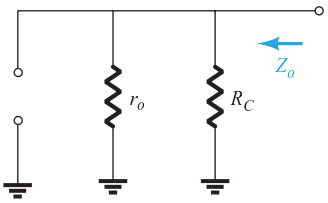


Figure 8.4 Determining Z_o for the network of Fig. 8.3.

A_v: The resistors r_o and R_C are in parallel,

and
$$V_o = -\beta I_b(R_C \| r_o)$$

but
$$I_b = \frac{V_i}{\beta r_c}$$

so that
$$V_o = -\beta\left(\frac{V_i}{\beta_{r_e}}\right)(R_C \| r_o)$$

and
$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}} \tag{8.5}$$

If $r_o \geq 10R_C$,

$$\boxed{A_v = -\frac{R_C}{r_e}}_{r_o \geq 10R_C} \tag{8.6}$$

Note the explicit absence of β in Eqs. (8.5 and 8.6), although we recognize that β must be utilized to determine r_e.

A_i: The current gain is determined in the following manner: Applying the current-divider rule to the input and output circuits,

$$I_o = \frac{(r_o)(\beta I_b)}{r_o + R_C} \quad \text{and} \quad \frac{I_o}{I_b} = \frac{r_o\beta}{r_o + R_C}$$

with
$$I_b = \frac{(R_B)(I_i)}{R_B + \beta r_e} \quad \text{or} \quad \frac{I_b}{I_i} = \frac{R_B}{R_B + \beta r_e}$$

The result is

$$A_i = \frac{I_o}{I_i} = \left(\frac{I_o}{I_b}\right)\left(\frac{I_b}{I_i}\right) = \left(\frac{r_o\beta}{r_o + R_C}\right)\left(\frac{R_B}{R_B + \beta r_e}\right)$$

and
$$\boxed{A_i = \frac{I_o}{I_i} = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}} \tag{8.7}$$

which is certainly an unwieldy, complex expression.

However, if $r_o \geq 10R_C$ and $R_B \geq 10\beta r_e$, which is often the case,

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R_B r_o}{(r_o)(R_B)}$$

and
$$\boxed{A_i \cong \beta}_{r_o \geq 10R_C,\ R_B \geq 10\beta r_e} \tag{8.8}$$

The complexity of Eq. (8.7) suggests that we may want to return to an equation such as Eq. (7.10), which utilizes A_o and Z_i. That is,

$$\boxed{A_i = -A_v\frac{Z_i}{R_C}} \tag{8.9}$$

Phase Relationship: The negative sign in the resulting equation for A_v reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 8.5.

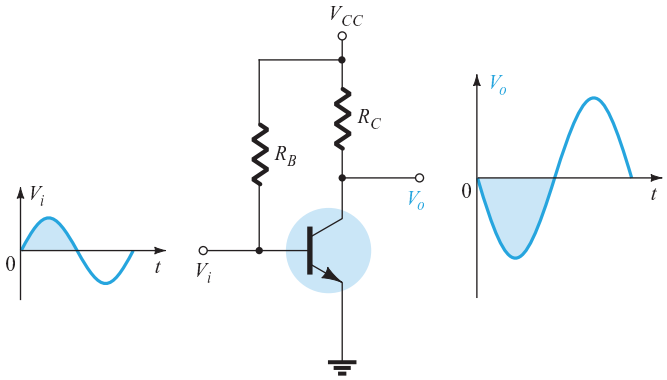


Figure 8.5 Demonstrating the 180° phase shift between input and output waveforms.

EXAMPLE 8.1

For the network of Fig. 8.6:

(a) Determine r_e.
(b) Find Z_i (with $r_o = \infty\ \Omega$).
(c) Calculate Z_o (with $r_o = \infty\ \Omega$).
(d) Determine A_v (with $r_o = \infty\ \Omega$).
(e) Find A_i (with $r_o = \infty\ \Omega$).
(f) Repeat parts (c) through (e) including $r_o = 50\ \text{k}\Omega$ in all calculations and compare results.

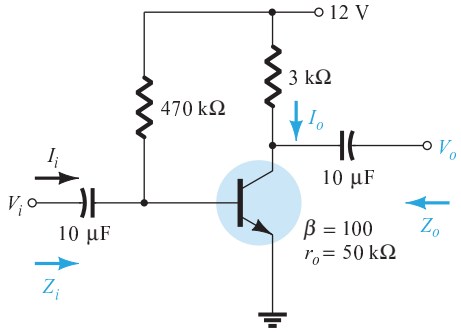


Figure 8.6 Example 8.1.

Solution

(a) DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.428\ \text{mA}} = \mathbf{10.71\ \Omega}$$

(b) $\beta r_e = (100)(10.71\ \Omega) = 1.071\ \text{k}\Omega$

$Z_i = R_B \| \beta r_e = 470\ \text{k}\Omega \| 1.071\ \text{k}\Omega = \mathbf{1.069\ k\Omega}$

(c) $Z_o = R_C = \mathbf{3\ k\Omega}$

(d) $A_v = -\dfrac{R_C}{r_e} = -\dfrac{3\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$

(e) Since $R_B \geq 10\beta r_e (470\ \text{k}\Omega > 10.71\ \text{k}\Omega)$

$A_i \cong \beta = \mathbf{100}$

(f) $Z_o = r_o \| R_C = 50\ \text{k}\Omega \| 3\ \text{k}\Omega = \mathbf{2.83\ k\Omega}$ vs. 3 kΩ

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-264.24}\ \text{vs.}\ -280.11$$

$$A_i = \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)} = \frac{(100)(470\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 3\ \text{k}\Omega)(470\ \text{k}\Omega + 1.071\ \text{k}\Omega)}$$

$$= \mathbf{94.13}\ \text{vs.}\ 100$$

As a check:

$$A_i = -A_v \frac{Z_i}{R_C} = \frac{-(-264.24)(1.069\ \text{k}\Omega)}{3\ \text{k}\Omega} = \mathbf{94.16}$$

which differs slightly only due to the accuracy carried through the calculations.

8.3 VOLTAGE-DIVIDER BIAS

The next configuration to be analyzed is the *voltage-divider* bias network of Fig. 8.7. Recall that the name of the configuration is a result of the voltage-divider bias at the input side to determine the dc level of V_B.

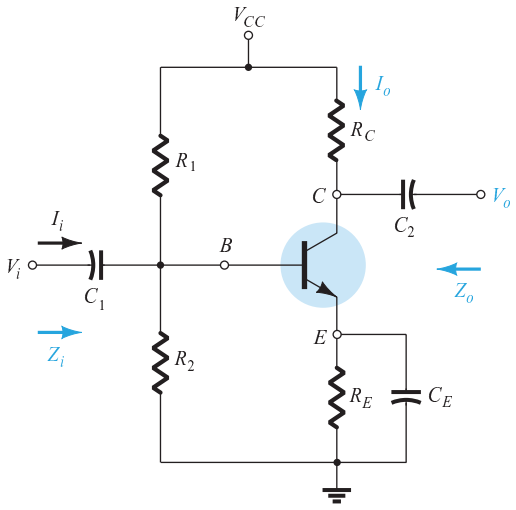


Figure 8.7 Voltage-divider bias configuration.

Substituting the r_e equivalent circuit will result in the network of Fig. 8.8. Note the absence of R_E due to the low-impedance shorting effect of the bypass capacitor, C_E. That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to R_E that it is treated as a short circuit across R_E. When

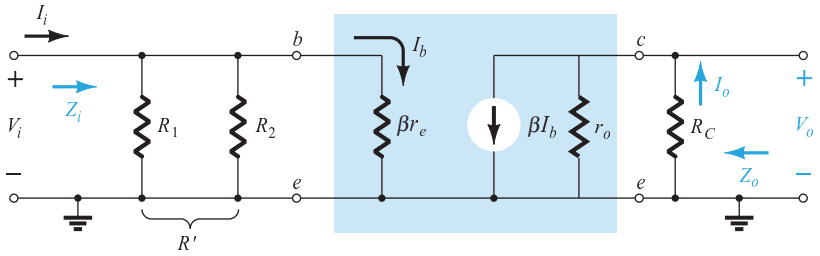


Figure 8.8 Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 8.7.

V_{CC} is set to zero, it places one end of R_1 and R_C at ground potential as shown in Fig. 8.8. In addition, note that R_1 and R_2 remain part of the input circuit while R_C is part of the output circuit. The parallel combination of R_1 and R_2 is defined by

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{8.10}$$

Z_i: From Fig. 8.8,

$$Z_i = R' \| \beta r_e \tag{8.11}$$

Z_o: From Fig. 8.8 with V_i set to 0 V resulting in $I_b = 0$ μA and $\beta I_b = 0$ mA,

$$Z_o = R_C \| r_o \tag{8.12}$$

If $r_o \geq 10R_C$,

$$Z_o \cong R_C \Big|_{r_o \geq 10R_C} \tag{8.13}$$

A_v: Since R_C and r_o are in parallel,

$$V_o = -(\beta I_b)(R_C \| r_o)$$

and

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right)(R_C \| r_o)$$

and

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e} \tag{8.14}$$

which you will note is an exact duplicate of the equation obtained for the fixed-bias configuration.

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \Big|_{r_o \geq 10R_C} \tag{8.15}$$

A_i: Since the network of Fig. 8.8 is so similar to that of Fig. 8.3 except for the fact that $R' = R_1 \| R_2 = R_B$, the equation for the current gain will have the same format as Eq. (8.7). That is,

$$A_i = \frac{I_o}{I_i} = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)} \tag{8.16}$$

For $r_o \geq 10R_C$,

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R' r_o}{r_o (R' + \beta r_e)}$$

and

$$A_i = \frac{I_o}{I_i} \cong \frac{\beta R'}{R' + \beta r_e} \Big|_{r_o \geq 10R_C} \tag{8.17}$$

And if $R' \geq 10\beta r_e$,

$$A_i = \frac{I_o}{I_i} = \frac{\beta R'}{R'}$$

and

$$\boxed{A_i = \frac{I_o}{I_i} \cong \beta} \qquad r_o \geq 10R_C,\ R' \geq 10\beta r_e \tag{8.18}$$

As an option,

$$\boxed{A_i = -A_v \frac{Z_i}{R_C}} \tag{8.19}$$

Phase relationship: The negative sign of Eq. (8.14) reveals a 180° phase shift between V_o and V_i.

EXAMPLE 8.2

For the network of Fig. 8.9, determine:
(a) r_e.
(b) Z_i.
(c) Z_o ($r_o = \infty\ \Omega$).
(d) A_v ($r_o = \infty\ \Omega$).
(e) A_i ($r_o = \infty\ \Omega$).
(f) The parameters of parts (b) through (e) if $r_o = 1/h_{oe} = 50\ \text{k}\Omega$ and compare results.

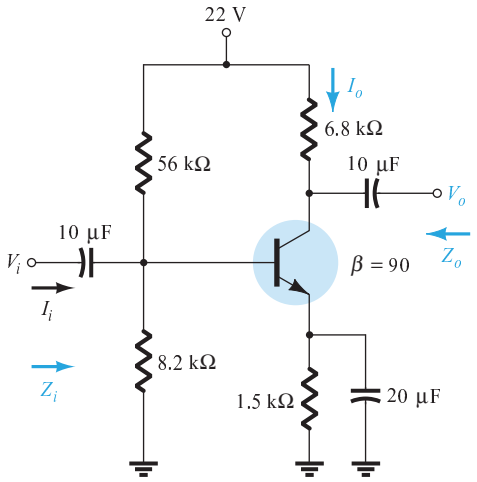


Figure 8.9 Example 8.2.

Solution

(a) DC: Testing $\beta R_E > 10R_2$

$$(90)(1.5\ \text{k}\Omega) > 10(8.2\ \text{k}\Omega)$$

$$135\ \text{k}\Omega > 82\ \text{k}\Omega\ (\textit{satisfied})$$

Using the approximate approach,

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\ \text{k}\Omega)(22\ \text{V})}{56\ \text{k}\Omega + 8.2\ \text{k}\Omega} = 2.81\ \text{V}$$

$$V_E = V_B - V_{BE} = 2.81\ \text{V} - 0.7\ \text{V} = 2.11\ \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11\ \text{V}}{1.5\ \text{k}\Omega} = 1.41\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.41\ \text{mA}} = \mathbf{18.44\ \Omega}$$

(b) $R' = R_1 \| R_2 = (56\ \text{k}\Omega) \| (8.2\ \text{k}\Omega) = 7.15\ \text{k}\Omega$

$Z_i = R' \| \beta r_e = 7.15\ \text{k}\Omega \| (90)(18.44\ \Omega) = 7.15\ \text{k}\Omega \| 1.66\ \text{k}\Omega$

$= \mathbf{1.35\ k\Omega}$

(c) $Z_o = R_C = \mathbf{6.8\ k\Omega}$

(d) $A_v = -\frac{R_C}{r_e} = -\frac{6.8\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

(e) The condition $R' \geq 10\beta r_e$ ($7.15\ \text{k}\Omega \geq 10(1.66\ \text{k}\Omega) = 16.6\ \text{k}\Omega$ is *not* satisfied. Therefore,

$$A_i \cong \frac{\beta R'}{R' + \beta r_e} = \frac{(90)(7.15\ \text{k}\Omega)}{7.15\ \text{k}\Omega + 1.66\ \text{k}\Omega} = \mathbf{73.04}$$

(f) $Z_i = \mathbf{1.35\ k\Omega}$

$Z_o = R_C \| r_o = 6.8\ \text{k}\Omega \| 50\ \text{k}\Omega = \mathbf{5.98\ k\Omega}$ vs. $6.8\ \text{k}\Omega$

$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}$ vs. -368.76

The condition

$$r_o \geq 10R_C\ (50\ \text{k}\Omega \geq 10(6.8\ \text{k}\Omega) = 68\ \text{k}\Omega)$$

is *not* satisfied. Therefore,

$$A_i = \frac{\beta R' r_o}{(r_o + R_C)(R' + \beta r_e)} = \frac{(90)(7.15\ \text{k}\Omega)(50\ \text{k}\Omega)}{(50\ \text{k}\Omega + 6.8\ \text{k}\Omega)(7.15\ \text{k}\Omega + 1.66\ \text{k}\Omega)}$$

$= \mathbf{64.3}$ vs. 73.04

There was a measurable difference in the results for Z_o, A_v, and A_i because the condition $r_o \geq 10R_C$ was *not* satisfied.

8.4 CE EMITTER-BIAS CONFIGURATION

The networks examined in this section include an emitter resistor that may or may not be bypassed in the ac domain. We will first consider the unbypassed situation and then modify the resulting equations for the bypassed configuration.

Unbypassed

The most fundamental of unbypassed configurations appears in Fig. 8.10. The r_e equivalent model is substituted in Fig. 8.11, but note the absence of the resistance r_o. The effect of r_o is to make the analysis a great deal more complicated, and considering the fact that in most situations its effect can be ignored, it will not be included in the current analysis. However, the effect of r_o will be discussed later in this section.

Applying Kirchhoff's voltage law to the input side of Fig. 8.11 will result in

$$V_i = I_b \beta r_e + I_e R_E$$

or

$$V_i = I_b \beta r_e + (\beta + 1) I_b R_E$$

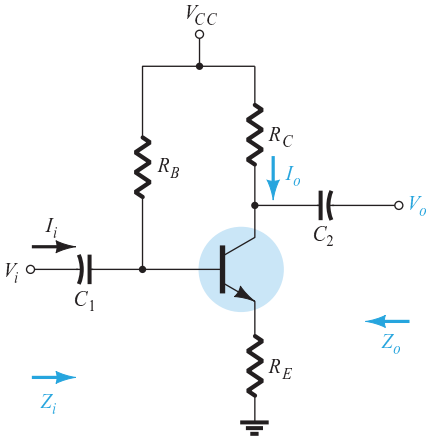


Figure 8.10 CE emitter-bias configuration.

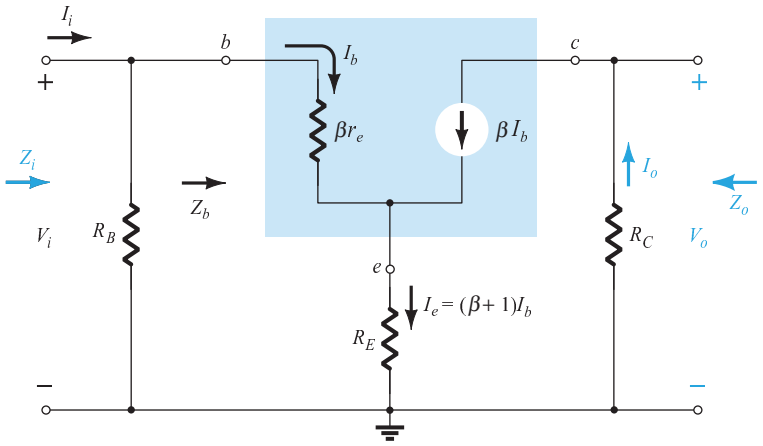


Figure 8.11 Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 8.10.

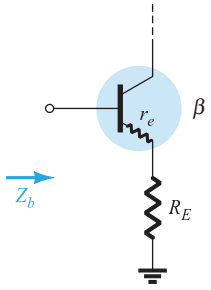


Figure 8.12 Defining the input impedance of a transistor with an unbypassed emitter resistor.

and the input impedance looking into the network to the right of R_B *is*

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

The result as displayed in Fig. 8.12 reveals that the input impedance of a transistor with an unbypassed resistor R_E is determined by

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E} \tag{8.20}$$

Since β is normally much greater than 1, the approximate equation is the following:

$$Z_b \cong \beta r_e + \beta R_E$$

and

$$\boxed{Z_b \cong \beta(r_e + R_E)} \tag{8.21}$$

Since R_E is often much greater than r_e, Eq. (8.21) can be further reduced to

$$\boxed{Z_b \cong \beta R_E} \tag{8.22}$$

***Z*$_i$:** Returning to Fig. 8.11, we have

$$\boxed{Z_i = R_B \| Z_b} \tag{8.23}$$

***Z*$_o$:** With V_i set to zero, $I_b = 0$ and βI_b can be replaced by an open-circuit equivalent. The result is

$$\boxed{Z_o = R_C} \tag{8.24}$$

***A*$_v$:**

$$I_b = \frac{V_i}{Z_b}$$

and

$$V_o = -I_o R_C = -\beta I_b R_C$$

$$= -\beta\left(\frac{V_i}{Z_b}\right) R_C$$

with

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}} \tag{8.25}$$

Substituting $Z_b = \beta(r_e + R_E)$ gives

$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e + R_E} \tag{8.26}$$

and for the approximation $Z_b \cong \beta R_E$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E} \tag{8.27}$$

Note again the absence of β from the equation for A_v.

***A_i*:** The magnitude of R_B is often too close to Z_b to permit the approximation $I_b = I_i$. Applying the current-divider rule to the input circuit will result in

$$I_b = \frac{R_B I_i}{R_B + Z_b}$$

and

$$\frac{I_b}{I_i} = \frac{R_B}{R_B + Z_b}$$

In addition,

$$I_o = \beta I_b$$

and

$$\frac{I_o}{I_b} = \beta$$

so that

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b}\frac{I_b}{I_i}$$

$$= \beta \frac{R_B}{R_B + Z_b}$$

and

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_B}{R_B + Z_b} \tag{8.28}$$

or

$$A_i = -A_v \frac{Z_i}{R_C} \tag{8.29}$$

Phase relationship: The negative sign in Eq. (8.25) again reveals a 180° phase shift between V_o and V_i.

Effect of r_o: The equations appearing below will clearly reveal the additional complexity resulting from including r_o in the analysis. Note in each case, however, that when certain conditions are met, the equations return to the form just derived. The derivation of each equation is beyond the needs of this text and is left as an exercise for the reader. Each equation can be derived through *careful* application of the basic laws of circuit analysis such as Kirchhoff's voltage and current laws, source conversions, Thévenin's theorem, and so on. The equations were included to remove the nagging question of the effect of r_o on the important parameters of a transistor configuration.

***Z_i*:**

$$Z_b = \beta r_e + \left[\frac{(\beta + 1) + R_C/r_o}{1 + (R_C + R_E)/r_o}\right] R_E \tag{8.30}$$

Since the ratio R_C/r_o is always much less than $(\beta + 1)$,

$$Z_b \cong \beta r_e + \frac{(\beta + 1)R_E}{1 + (R_C + R_E)/r_o}$$

For $r_o \geq 10(R_C + R_E)$,

$$Z_b \cong \beta r_e + (\beta + 1)R_E$$

which compares directly with Eq. (8.20).

In other words, if $r_o \geq 10(R_C + R_E)$, all the equations derived earlier will result.

Since $\beta + 1 \cong \beta$, the following equation is an excellent one for most applications:

$$\boxed{Z_b \cong \beta(r_e + R_E)}_{r_o \geq 10(R_C + R_E)} \tag{8.31}$$

***Z_o*:**

$$\boxed{Z_o = R_C \| \left[r_o + \frac{\beta(r_o + r_e)}{1 + \dfrac{\beta r_e}{R_E}} \right]} \tag{8.32}$$

However, $r_o \gg r_e$, and

$$Z_o \cong R_C \| r_o \left[1 + \frac{\beta}{1 + \dfrac{\beta r_e}{R_E}} \right]$$

which can be written as

$$Z_o \cong R_C \| r_o \left[1 + \frac{1}{\dfrac{1}{\beta} + \dfrac{r_e}{R_E}} \right]$$

Typically $1/\beta$ and r_e/R_E are less than one with a sum usually less than one. The result is a multiplying factor for r_o greater than one. For $\beta = 100$, $r_e = 10\ \Omega$, and $R_E = 1\ \text{k}\Omega$:

$$\frac{1}{\dfrac{1}{\beta} + \dfrac{r_e}{R_E}} = \frac{1}{\dfrac{1}{100} + \dfrac{10\ \Omega}{1000\ \Omega}} = \frac{1}{0.02} = 50$$

and

$$Z_o = R_C \| 51 r_o$$

which is certainly simply R_C. Therefore,

$$\boxed{Z_o = R_C}_{\text{Any level of } r_o} \tag{8.33}$$

which was obtained earlier.

***A_v*:**

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-\dfrac{\beta R_C}{Z_b}\left[1 + \dfrac{r_e}{r_o}\right] + \dfrac{R_C}{r_o}}{1 + \dfrac{R_C}{r_o}}} \tag{8.34}$$

The ratio $\frac{r_e}{r_o} \ll 1$

and
$$A_v = \frac{V_o}{V_i} \cong \frac{-\frac{\beta R_C}{Z_b} + \frac{R_C}{r_o}}{1 + \frac{R_C}{r_o}}$$

For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b}}_{r_o \geq 10R_C} \tag{8.35}$$

as obtained earlier.

A_i: The determination of A_i will be left to the equation

$$\boxed{A_i = -A_v \frac{Z_i}{R_C}} \tag{8.36}$$

using the above equations.

Bypassed

If R_E of Fig. 8.10 is bypassed by an emitter capacitor C_E, the complete r_e equivalent model can be substituted resulting in the same equivalent network as Fig. 8.3. Eqs. (8.1 through 8.9) are therefore applicable.

EXAMPLE 8.3

For the network of Fig. 8.13, without C_E (unbypassed), determine:
(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.

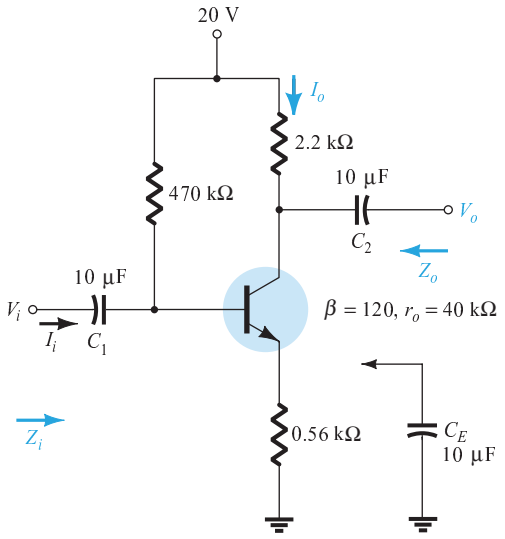


Figure 8.13 Example 8.3.

Solution

(a) DC: $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$

$I_E = (\beta + 1)I_B = (121)(46.5\ \mu\text{A}) = 4.34\text{ mA}$

and $r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$

(b) Testing the condition $r_o \geq 10(R_C + R_E)$,

$$40\ \text{k}\Omega \geq 10(2.2\ \text{k}\Omega + 0.56\ \text{k}\Omega)$$

$$40\ \text{k}\Omega \geq 10(2.76\ \text{k}\Omega) = 27.6\ \text{k}\Omega\ (\textit{satisfied})$$

Therefore,

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\ \Omega + 560\ \Omega)$$
$$= 67.92\ \text{k}\Omega$$

and

$$Z_i = R_B \| Z_b = 470\ \text{k}\Omega \| 67.92\ \text{k}\Omega$$
$$= \mathbf{59.34\ k\Omega}$$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\ \text{k}\Omega)}{67.92\ \text{k}\Omega}$$
$$= \mathbf{-3.89}$$

compared to -3.93 using Eq. (8.27): $A_v \cong -R_C/R_E$.

(e) $$A_i = -A_v \frac{Z_i}{R_C} = -(-3.89)\left(\frac{59.34\ \text{k}\Omega}{2.2\ \text{k}\Omega}\right)$$
$$= \mathbf{104.92}$$

compared to 104.85 using Eq. (8.28): $A_i \cong \beta R_B/(R_B + Z_b)$.

EXAMPLE 8.4 Repeat the analysis of Example 8.3 with C_E in place.

Solution

(a) The dc analysis is the same, and $r_e = 5.99\ \Omega$.

(b) R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\ \text{k}\Omega \| (120)(5.99\ \Omega)$$
$$= 470\ \text{k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $$A_v = -\frac{R_C}{r_e}$$
$$= -\frac{2.2\ \text{k}\Omega}{5.99\ \Omega} = \mathbf{-367.28}$$ (a significant increase)

(e) $$A_i = \frac{\beta R_B}{R_B + Z_b} = \frac{(120)(470\ \text{k}\Omega)}{470\ \text{k}\Omega + 718.8\ \Omega}$$
$$= \mathbf{119.82}$$

EXAMPLE 8.5 For the network of Fig. 8.14, determine (using appropriate approximations):

(a) r_e.

(b) Z_i.

(c) Z_o.

(d) A_v.

(e) A_i.

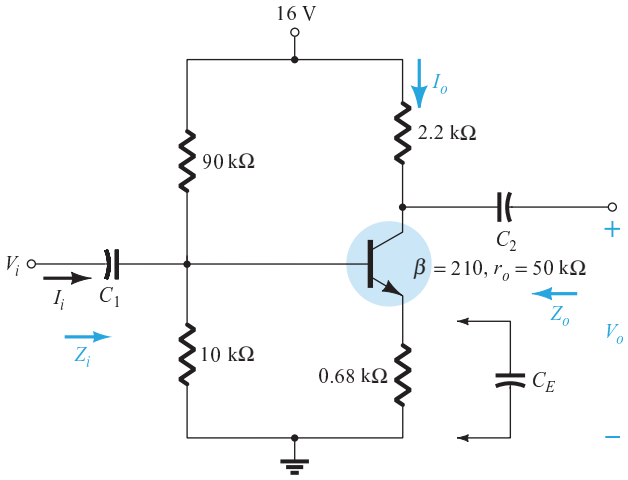


Figure 8.14 Example 8.5.

Solution

(a) Testing $\beta R_E > 10R_2$

$$(210)(0.68\ \text{k}\Omega) > 10(10\ \text{k}\Omega)$$

$$142.8\ \text{k}\Omega > 100\ \text{k}\Omega\ (\textit{satisfied})$$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10\ \text{k}\Omega}{90\ \text{k}\Omega + 10\ \text{k}\Omega}(16\ \text{V}) = 1.6\ \text{V}$$

$$V_E = V_B - V_{BE} = 1.6\ \text{V} - 0.7\ \text{V} = 0.9\ \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{0.9\ \text{V}}{0.68\ \text{k}\Omega} = 1.324\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.324\ \text{mA}} = \mathbf{19.64\ \Omega}$$

(b) The ac equivalent circuit is provided in Fig. 8.15. The resulting configuration is now different from Fig. 8.11 only by the fact that now

$$R_B = R' = R_1 \| R_2 = 9\ \text{k}\Omega$$

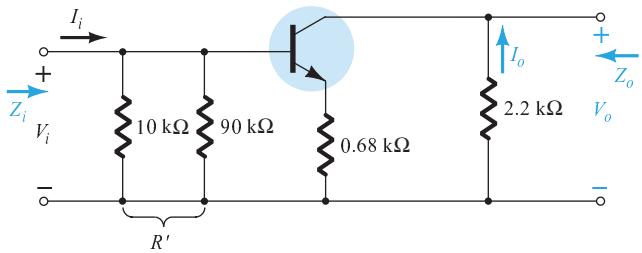


Figure 8.15 The ac equivalent circuit of Fig. 8.14.

The testing conditions of $r_o \geq 10(R_C + R_E)$ and $r_o \geq 10R_C$ are both satisfied. Using the appropriate approximations yields

$$Z_b \cong \beta R_E = 142.8\ \text{k}\Omega$$

$$Z_i = R_B \| Z_b = 9\ \text{k}\Omega \| 142.8\ \text{k}\Omega$$

$$= \mathbf{8.47\ k\Omega}$$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $A_v = -\dfrac{R_C}{R_E} = -\dfrac{2.2\ \text{k}\Omega}{0.68\ \text{k}\Omega} = \mathbf{-3.24}$

(e) $A_i = -A_v\dfrac{Z_i}{R_C} = -(-3.24)\left(\dfrac{8.47\ \text{k}\Omega}{2.2\ \text{k}\Omega}\right)$

$= \mathbf{12.47}$

EXAMPLE 8.6 Repeat Example 8.5 with C_E in place.

Solution

(a) The dc analysis is the same, and $r_e = \mathbf{19.64\ \Omega}$.

(b) $Z_b = \beta r_e = (210)(19.64\ \Omega) \cong 4.12\ \text{k}\Omega$

$Z_i = R_B \| Z_b = 9\ \text{k}\Omega \| 4.12\ \text{k}\Omega$

$= \mathbf{2.83\ k\Omega}$

(c) $Z_o = R_C = \mathbf{2.2\ k\Omega}$

(d) $A_v = -\dfrac{R_C}{r_e} = -\dfrac{2.2\ \text{k}\Omega}{19.64\ \text{k}\Omega} = \mathbf{-112.02}$ (a significant increase)

(e) $A_i = -A_v\dfrac{Z_i}{R_L} = -(-112.02)\left(\dfrac{2.83\ \text{k}\Omega}{2.2\ \text{k}\Omega}\right)$

$= \mathbf{144.1}$

Another variation of an emitter-bias configuration appears in Fig. 8.16. For the dc analysis, the emitter resistance is $R_{E_1} + R_{E_2}$, while for the ac analysis, the resistor R_E in the equations above is simply R_{E_1} with R_{E_2} bypassed by C_E.

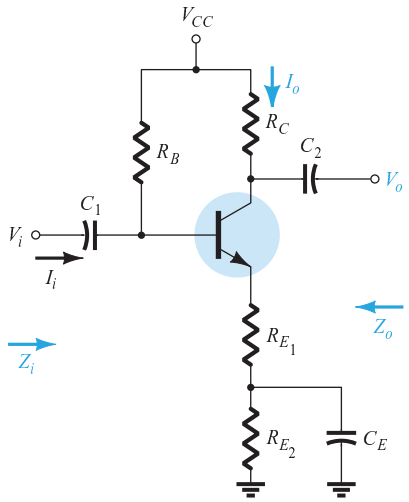


Figure 8.16 An emitter-bias configuration with a portion of the emitter-bias resistance bypassed in the ac domain.

8.5 EMITTER-FOLLOWER CONFIGURATION

When the output is taken from the emitter terminal of the transistor as shown in Fig. 8.17, the network is referred to as an *emitter-follower*. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the ap-

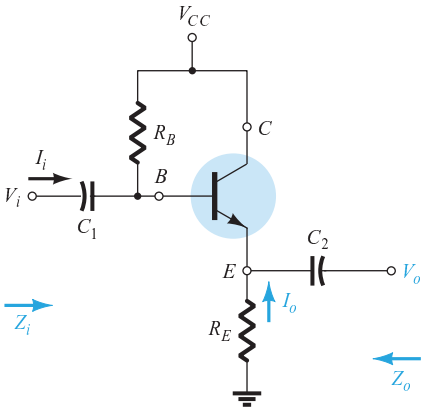


Figure 8.17 Emitter-follower configuration.

proximation $A_v \cong 1$ is usually a good one. Unlike the collector voltage, the emitter voltage is in phase with the signal V_i. That is, both V_o and V_i will attain their positive and negative peak values at the same time. The fact that V_o "follows" the magnitude of V_i with an in-phase relationship accounts for the terminology emitter-follower.

The most common emitter-follower configuration appears in Fig. 8.17. In fact, because the collector is grounded for ac analysis, it is actually a *common-collector* configuration. Other variations of Fig. 8.17 that draw the output off the emitter with $V_o \cong V_i$ will appear later in this section.

The emitter-follower configuration is frequently used for impedance-matching purposes. It presents a high impedance at the input and a low impedance at the output, which is the direct opposite of the standard fixed-bias configuration. The resulting effect is much the same as that obtained with a transformer, where a load is matched to the source impedance for maximum power transfer through the system.

Substituting the r_e equivalent circuit into the network of Fig. 8.17 will result in the network of Fig. 8.18. The effect of r_o will be examined later in the section.

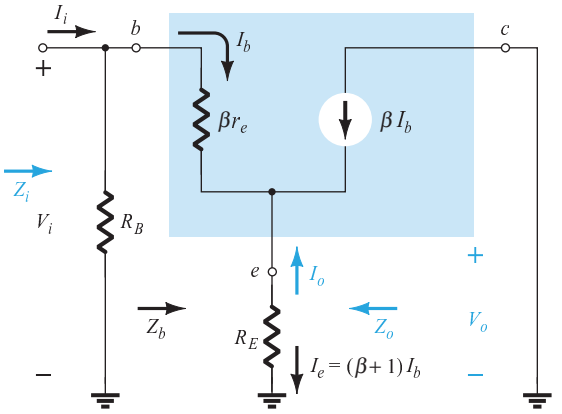


Figure 8.18 Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 8.17.

Z_i: The input impedance is determined in the same manner as described in the preceding section:

$$Z_i = R_B \| Z_b \tag{8.37}$$

with

$$Z_b = \beta r_e + (\beta + 1) R_E \tag{8.38}$$

or
$$\boxed{Z_b \cong \beta(r_e + R_E)} \tag{8.39}$$

and
$$\boxed{Z_b \cong \beta R_E} \tag{8.40}$$

Z_o: The output impedance is best described by first writing the equation for the current I_b:

$$I_b = \frac{V_i}{Z_b}$$

and then multiplying by $(\beta + 1)$ to establish I_e. That is,

$$I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b}$$

Substituting for Z_b gives

$$I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

or
$$I_e = \frac{V_i}{[\beta r_e/(\beta + 1)] + R_E}$$

but
$$(\beta + 1) \cong \beta$$

and
$$\frac{\beta r_e}{\beta + 1} \cong \frac{\beta r_e}{\beta} = r_e$$

so that
$$\boxed{I_e \cong \frac{V_i}{r_e + R_E}} \tag{8.41}$$

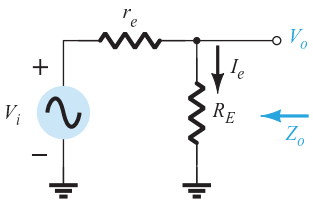


Figure 8.19 Defining the output impedance for the emitter-follower configuration.

If we now construct the network defined by Eq. (8.41), the configuration of Fig. 8.19 will result.

To determine Z_o, V_i is set to zero and

$$\boxed{Z_o = R_E \| r_e} \tag{8.42}$$

Since R_E is typically much greater than r_e, the following approximation is often applied:

$$\boxed{Z_o \cong r_e} \tag{8.43}$$

A_v: Figure 8.19 can be utilized to determine the voltage gain through an application of the voltage-divider rule:

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

and
$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}} \tag{8.44}$$

Since R_E is usually much greater than r_e, $R_E + r_e \cong R_E$ and

$$\boxed{A_v = \frac{V_o}{V_i} \cong 1} \tag{8.45}$$

A_i: From Fig. 8.18,

$$I_b = \frac{R_B I_i}{R_B + Z_b}$$

or

$$\frac{I_b}{I_i} = \frac{R_B}{R_B + Z_b}$$

and

$$I_o = -I_e = -(\beta + 1)I_b$$

or

$$\frac{I_o}{I_b} = -(\beta + 1)$$

so that

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b}\frac{I_b}{I_i}$$

$$= -(\beta + 1)\frac{R_B}{R_B + Z_b}$$

and since

$$(\beta + 1) \cong \beta,$$

$$\boxed{A_i \cong -\frac{\beta R_B}{R_B + Z_b}} \tag{8.46}$$

or

$$\boxed{A_i = -A_v \frac{Z_i}{R_E}} \tag{8.47}$$

Phase relationship: As revealed by Eq. (8.44) and earlier discussions of this section, V_o and V_i are in phase for the emitter-follower configuration.

Effect of r_o:

Z_i:

$$\boxed{Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \dfrac{R_E}{r_o}}} \tag{8.48}$$

If the condition $r_o \geq 10R_E$ is satisfied,

$$Z_b = \beta r_e + (\beta + 1)R_E$$

which matches earlier conclusions with

$$\boxed{Z_b \cong \beta(r_e + R_E)}_{r_o \geq 10R_E} \tag{8.49}$$

Z_o:

$$\boxed{Z_o = r_o \| R_E \| \frac{\beta r_e}{(\beta + 1)}} \tag{8.50}$$

Using $\beta + 1 \cong \beta$,

$$Z_o = r_o \| R_E \| r_e$$

and since $r_o \gg r_e$,

$$\boxed{Z_o \cong R_E \| r_e}_{\text{Any } r_o} \tag{8.51}$$

A_v:

$$A_v = \frac{(\beta + 1)R_E/Z_b}{1 + \frac{R_E}{r_o}} \tag{8.52}$$

If the condition $r_o \geq 10R_E$ is satisfied and we use the approximation $\beta + 1 \cong \beta$,

$$A_v \cong \frac{\beta R_E}{Z_b}$$

But $$Z_b \cong \beta(r_e + R_E)$$

so that $$A_v \cong \frac{\beta R_E}{\beta(r_e + R_E)}$$

and

$$A_v \cong \frac{R_E}{r_e + R_E}_{r_o \geq 10R_E} \tag{8.53}$$

EXAMPLE 8.7

For the emitter-follower network of Fig. 8.20, determine:
(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.
(f) Repeat parts (b) through (e) with $r_o = 25\ \text{k}\Omega$ and compare results.

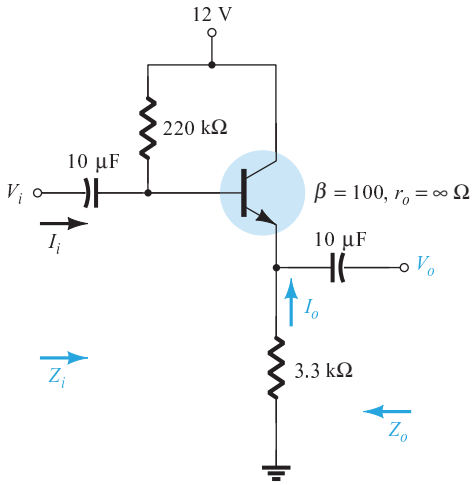


Figure 8.20 Example 8.7.

Solution

(a) $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$= \frac{12\ \text{V} - 0.7\ \text{V}}{220\ \text{k}\Omega + (101)3.3\ \text{k}\Omega} = 20.42\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B$$

$$= (101)(20.42\ \mu\text{A}) = 2.062\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.062\ \text{mA}} = \mathbf{12.61\ \Omega}$$

(b) $Z_b = \beta r_e + (\beta + 1)R_E$

$= (100)(12.61\ \Omega) + (101)(3.3\ \text{k}\Omega)$

$= 1.261\ \text{k}\Omega + 333.3\ \text{k}\Omega$

$= 334.56\ \text{k}\Omega \cong \beta R_E$

$Z_i = R_B \| Z_b = 220\ \text{k}\Omega \| 334.56\ \text{k}\Omega$

$= \mathbf{132.72\ k\Omega}$

(c) $Z_o = R_E \| r_e = 3.3\ \text{k}\Omega \| 12.61\ \Omega$

$= \mathbf{12.56\ \Omega} \cong r_e$

(d) $A_v = \dfrac{V_o}{V_i} = \dfrac{R_E}{R_E + r_e} = \dfrac{3.3\ \text{k}\Omega}{3.3\ \text{k}\Omega + 12.61\ \Omega}$

$= \mathbf{0.996} \cong 1$

(e) $A_i \cong -\dfrac{\beta R_B}{R_B + Z_b} = -\dfrac{(100)(220\ \text{k}\Omega)}{220\ \text{k}\Omega + 334.56\ \text{k}\Omega} = \mathbf{-39.67}$

versus

$$A_i = -A_v \frac{Z_i}{R_E} = -(0.996)\left(\frac{132.72\ \text{k}\Omega}{3.3\ \text{k}\Omega}\right) = \mathbf{-40.06}$$

(f) Checking the condition $r_o \geq 10R_E$, we have

$$25\ \text{k}\Omega \geq 10(3.3\ \text{k}\Omega) = 33\ \text{k}\Omega$$

which is *not* satisfied. Therefore,

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \dfrac{R_E}{r_o}} = (100)(12.61\ \Omega) + \frac{(100 + 1)3.3\ \text{k}\Omega}{1 + \dfrac{3.3\ \text{k}\Omega}{25\ \text{k}\Omega}}$$

$= 1.261\ \text{k}\Omega + 294.43\ \text{k}\Omega$

$= 295.7\ \text{k}\Omega$

with $Z_i = R_B \| Z_b = 220\ \text{k}\Omega \| 295.7\ \text{k}\Omega$

$= \mathbf{126.15\ k\Omega}$ vs. $132.72\ \text{k}\Omega$ obtained earlier

$Z_o = R_E \| r_e = \mathbf{12.56\ \Omega}$ as obtained earlier

$$A_v = \frac{(\beta + 1)R_E / Z_b}{\left[1 + \dfrac{R_E}{r_o}\right]} = \frac{(100 + 1)(3.3\ \text{k}\Omega)/295.7\ \text{k}\Omega}{\left[1 + \dfrac{3.3\ \text{k}\Omega}{25\ \text{k}\Omega}\right]}$$

$= \mathbf{0.996} \cong 1$

matching the earlier result.

In general, therefore, even though the condition $r_o \geq 10R_E$ was not satisfied, the results for Z_o and A_v are the same, with Z_i only slightly less. The results suggest that for most applications a good approximation for the actual results can be obtained by simply ignoring the effects of r_o for this configuration.

The network of Fig. 8.21 is a variation of the network of Fig. 8.17, which employs a voltage-divider input section to set the bias conditions. Equations (8.37) through (8.47) are changed only by replacing R_B by $R' = R_1 \| R_2$.

The network of Fig. 8.22 will also provide the input/output characteristics of an emitter-follower but includes a collector resistor R_C. In this case R_B is again replaced by the parallel combination of R_1 and R_2. The input impedance Z_i and output impedance Z_o are unaffected by R_C since it is not reflected into the base or emitter equiv-

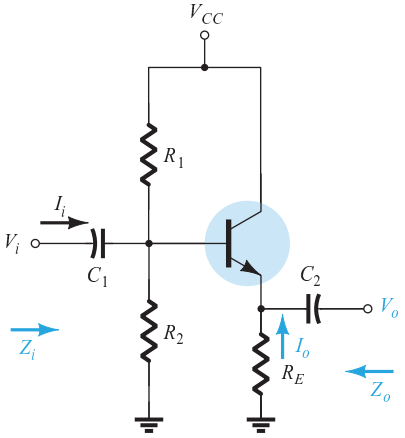


Figure 8.21 Emitter-follower configuration with a voltage-divider biasing arrangement.

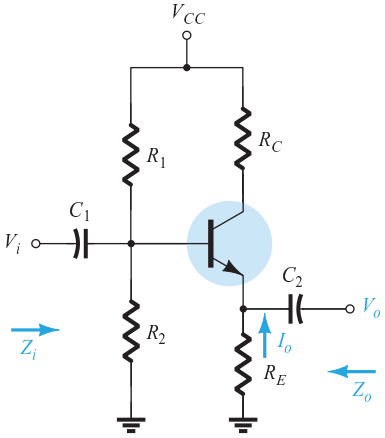


Figure 8.22 Emitter-follower configuration with a collector resistor R_C.

alent networks. In fact, the only effect of R_C will be to determine the Q-point of operation.

8.6 COMMON-BASE CONFIGURATION

The common-base configuration is characterized as having a relatively low input and a high output impedance and a current gain less than 1. The voltage gain, however, can be quite large. The standard configuration appears in Fig. 8.23, with the common-base r_e equivalent model substituted in Fig. 8.24. The transistor output impedance r_o is not included for the common-base configuration because it is typically in the megohm range and can be ignored in parallel with the resistor R_C.

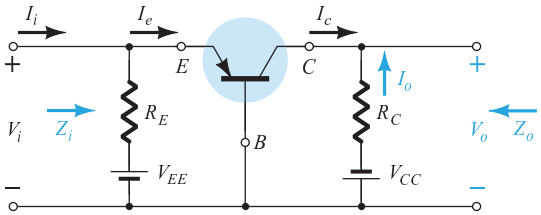


Figure 8.23 Common-base configuration.

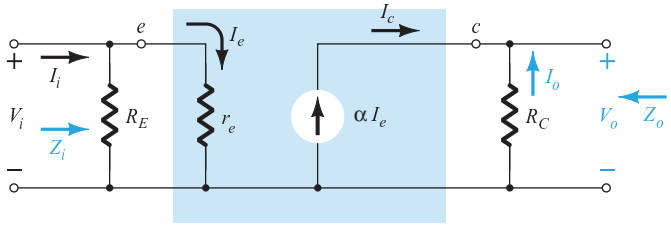


Figure 8.24 Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 8.23.

Z_i:

$$Z_i = R_E \| r_e \tag{8.54}$$

Z_o:

$$Z_o = R_C \tag{8.55}$$

A_v:

$$V_o = -I_o R_C = -(-I_c)R_C = \alpha I_e R_C$$

with $$I_e = \frac{V_i}{r_e}$$

so that $$V_o = \alpha\left(\frac{V_i}{r_e}\right) R_C$$

and $$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e} \tag{8.56}$$

***A_i*:** Assuming that $R_E \gg r_e$ yields

$$I_e = I_i$$

and $$I_o = -\alpha I_e = -\alpha I_i$$

with $$A_i = \frac{I_o}{I_i} = -\alpha \cong -1 \tag{8.57}$$

Phase relationship: The fact that A_v is a positive number reveals that V_o and V_i are in phase for the common-base configuration.

Effect of r_o: For the common-base configuration, $r_o = 1/h_{ob}$ is typically in the megohm range and sufficiently larger than the parallel resistance R_C to permit the approximation $r_o \| R_C \cong R_C$.

EXAMPLE 8.8

For the network of Fig. 8.25, determine:
(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.

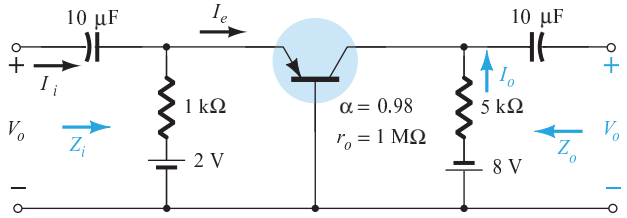


Figure 8.25 Example 8.8.

Solution

(a) $$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \frac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$$

(b) $$Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\ \Omega$$
$$= \mathbf{19.61\ \Omega} \cong r_e$$

(c) $$Z_o = R_C = \mathbf{5\text{ k}\Omega}$$

(d) $$A_v \cong \frac{R_C}{r_e} = \frac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$$

(e) $$A_i = \mathbf{-0.98} \cong -1$$

8.7 COLLECTOR FEEDBACK CONFIGURATION

The collector feedback network of Fig. 8.26 employs a feedback path from collector to base to increase the stability of the system as discussed in Section 4.12. However, the simple maneuver of connecting a resistor from base to collector rather than base to dc supply has a significant impact on the level of difficulty encountered when analyzing the network.

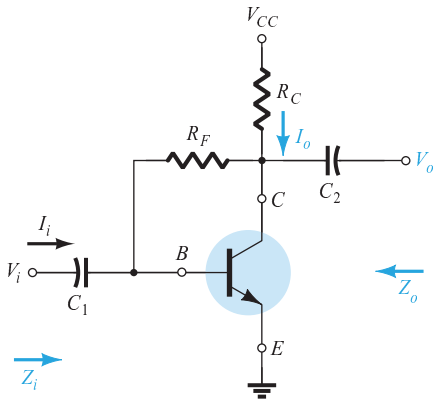


Figure 8.26 Collector feedback configuration.

Some of the steps to be performed below are the result of experience working with such configurations. It is not expected that a new student of the subject would choose the sequence of steps described below without taking a wrong step or two. Substituting the equivalent circuit and redrawing the network will result in the configuration of Fig. 8.27. The effects of a transistor output resistance r_o will be discussed later in the section.

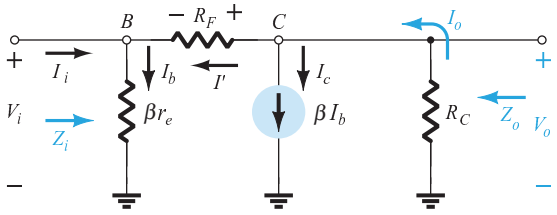


Figure 8.27 Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 8.26.

Z_i:
$$I' = \frac{V_o - V_i}{R_F}$$

with
$$V_o = -I_o R_C$$

and
$$I_o = \beta I_b + I'$$

Since βI_b is normally much larger than I',

$$I_o \cong \beta I_b$$

and
$$V_o = -(\beta I_b)R_C = -\beta I_b R_C$$

but
$$I_b = \frac{V_i}{\beta r_e}$$

and
$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)R_C = -\frac{R_C}{r_e}V_i$$

Therefore,

$$I' = \frac{V_o - V_i}{R_F} = \frac{V_o}{R_F} - \frac{V_i}{R_F} = -\frac{R_C V_i}{r_e R_F} - \frac{V_i}{R_F} = -\frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right]V_i$$

The result is

$$V_i = I_b\beta r_e = (I_i + I')\beta r_e = I_i\beta r_e + I'\beta r_e$$

$$V_i = I_i\beta r_e - \frac{1}{R_F}\left[1 + \frac{R_C}{r_e}\right]\beta r_e V_i$$

or

$$V_i\left[1 + \frac{\beta r_e}{R_F}\left[1 + \frac{R_C}{r_e}\right]\right] = I_i\beta r_e$$

and

$$Z_i = \frac{V_i}{I_i} = \frac{\beta r_e}{1 + \dfrac{\beta r_e}{R_F}\left[1 + \dfrac{R_C}{r_e}\right]}$$

but R_C is usually much greater than r_e and $1 + \dfrac{R_C}{r_e} \cong \dfrac{R_C}{r_e}$

so that

$$Z_i = \frac{\beta r_e}{1 + \dfrac{\beta R_C}{R_F}}$$

or

$$Z_i = \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}} \tag{8.58}$$

Z_o: If we set V_i to zero as required to define Z_o, the network will appear as shown in Fig. 8.28. The effect of βr_e is removed and R_F appears in parallel with R_C and

$$Z_o \cong R_C \| R_F \tag{8.59}$$

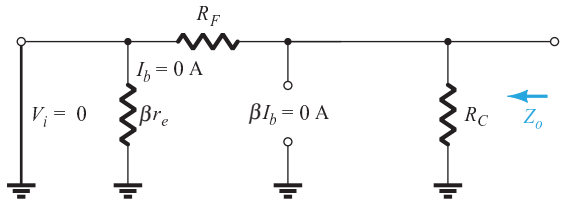


Figure 8.28 Defining Z_o for the collector feedback configuration.

A_v: At node C of Fig. 8.27,

$$I_o = \beta I_b + I'$$

For typical values, $\beta I_b \gg I'$ and $I_o \cong \beta I_b$.

$$V_o = -I_o R_C = -(\beta I_b)R_C$$

Substituting $I_b = V_i/\beta r_e$ gives us

$$V_o = -\beta\frac{V_i}{\beta r_e} R_C$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{R_C}{r_e} \tag{8.60}$$

A_i: Applying Kirchhoff's voltage law around the outside network loop yields

$$V_i + V_{R_F} - V_o = 0$$

and

$$I_b\beta r_e + (I_b - I_i)R_F + I_oR_C = 0$$

Using $I_o \cong \beta I_b$, we have

$$I_b\beta r_e + I_bR_F - I_iR_F + \beta I_bR_C = 0$$

and

$$I_b(\beta r_e + R_F + \beta R_C) = I_iR_F$$

Substituting $I_b = I_o/\beta$ from $I_o \cong \beta I_b$ yields

$$\frac{I_o}{\beta}(\beta r_e + R_F + \beta R_C) = I_iR_F$$

and

$$I_o = \frac{\beta R_F I_i}{\beta r_e + R_F + \beta R_C}$$

Ignoring βr_e compared to R_F and βR_C gives us

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{\beta R_F}{R_F + \beta R_C}} \tag{8.61}$$

For $\beta R_C \gg R_F$,

$$A_i = \frac{I_o}{I_i} = \frac{\beta R_F}{\beta R_C}$$

and

$$\boxed{A_i = \frac{I_o}{I_i} \cong \frac{R_F}{R_C}} \tag{8.62}$$

Phase relationship: The negative sign of Eq. (8.60) reveals a 180° phase shift between V_o and V_i.

Effect of r_o:

Z_i: A complete analysis without applying approximations will result in

$$\boxed{Z_i = \frac{1 + \dfrac{R_C \| r_o}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C \| r_o}{R_F r_e}}} \tag{8.63}$$

Recognizing that $1/R_F \cong 0$ and applying the condition $r_o \geq 10R_C$,

$$Z_i = \frac{1 + \dfrac{R_C}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{R_C}{R_F r_e}}$$

but typically $R_C/R_F \ll 1$ and

$$Z_i = \frac{1}{\dfrac{1}{\beta r_e} + \dfrac{R_C}{R_F r_e}}$$

or
$$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}} \qquad r_o \geq 10R_C \tag{8.64}$$

as obtained earlier.

***Z*$_o$:** Including r_o in parallel with R_C in Fig. 8.28 will result in

$$Z_o = r_o \| R_C \| R_F \tag{8.65}$$

For $r_o \geq 10R_C$,

$$Z_o \cong R_C \| R_F \qquad r_o \geq 10R_C \tag{8.66}$$

as obtained earlier. For the common condition of $R_F \gg R_C$,

$$Z_o \cong R_C \qquad r_o \geq 10R_C,\ R_F \gg R_C \tag{8.67}$$

***A*$_v$:**

$$A_v = -\frac{\left[\frac{1}{R_F} + \frac{1}{r_e}\right](r_o \| R_C)}{1 + \frac{r_o \| R_C}{R_F}} \tag{8.68}$$

Since $R_F \gg r_e$,

$$A_v \cong -\frac{\frac{r_o \| R_C}{r_e}}{1 + \frac{r_o \| R_C}{R_F}}$$

For $r_o \geq 10R_C$,

$$A_v \cong -\frac{\frac{R_C}{r_e}}{1 + \frac{R_C}{R_F}} \qquad r_o \geq 10R_C \tag{8.69}$$

and since R_C/R_F is typically much less than one,

$$A_v \cong -\frac{R_C}{r_e} \qquad r_o \geq 10R_C,\ R_F \gg R_C \tag{8.70}$$

as obtained earlier.

EXAMPLE 8.9

For the network of Fig. 8.29, determine:
(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.
(f) Repeat parts (b) through (e) with $r_o = 20\ \text{k}\Omega$ and compare results.

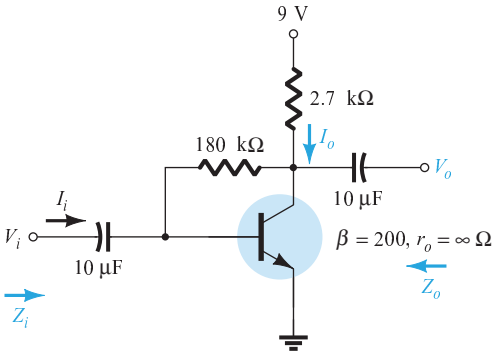


Figure 8.29 Example 8.9.

Solution

(a) $$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{9\text{ V} - 0.7\text{ V}}{180\text{ k}\Omega + (200)2.7\text{ k}\Omega}$$

$$= 11.53\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (201)(11.53\ \mu\text{A}) = 2.32\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.32\text{ mA}} = \mathbf{11.21\ \Omega}$$

(b) $$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}} = \frac{11.21\ \Omega}{\frac{1}{200} + \frac{2.7\text{ k}\Omega}{180\text{ k}\Omega}} = \frac{11.21\ \Omega}{0.005 + 0.015}$$

$$= \frac{11.21\ \Omega}{0.02} = 50(11.21\ \Omega) = \mathbf{560.5\ \Omega}$$

(c) $$Z_o = R_C \| R_F = 2.7\text{ k}\Omega \| 180\text{ k}\Omega = \mathbf{2.66\ k\Omega}$$

(d) $$A_v = -\frac{R_C}{r_e} = -\frac{27\text{ k}\Omega}{11.21\ \Omega} = \mathbf{-240.86}$$

(e) $$A_i = \frac{\beta R_F}{R_F + \beta R_C} = \frac{(200)(180\text{ k}\Omega)}{180\text{ k}\Omega + (200)(2.7\text{ k}\Omega)}$$

$$= \mathbf{50}$$

(f) Z_i: The condition $r_o \geq 10R_C$ is *not* satisfied. Therefore,

$$Z_i = \frac{1 + \frac{R_C \| r_o}{R_F}}{\frac{1}{\beta r_e} + \frac{1}{R_F} + \frac{R_C \| r_o}{R_F r_e}} = \frac{1 + \frac{2.7\text{ k}\Omega \| 20\text{ k}\Omega}{180\text{ k}\Omega}}{\frac{1}{(200)(11.21)} + \frac{1}{180\text{ k}\Omega} + \frac{2.7\text{ k}\Omega \| 20\text{ k}\Omega}{(180\text{ k}\Omega)(11.21\ \Omega)}}$$

$$= \frac{1 + \frac{2.38\text{ k}\Omega}{180\text{ k}\Omega}}{0.45 \times 10^{-3} + 0.006 \times 10^{-3} + 1.18 \times 10^{-3}} = \frac{1 + 0.013}{1.64 \times 10^{-3}}$$

$$= \mathbf{617.7\ \Omega}\text{ vs. } 560.5\ \Omega \text{ above}$$

Z_o:

$$Z_o = r_o \| R_C \| R_F = 20\text{ k}\Omega \| 2.7\text{ k}\Omega \| 180\text{ k}\Omega$$

$$= \mathbf{2.35\ k\Omega}\text{ vs. } 2.66\text{ k}\Omega \text{ above}$$

A_v:

$$A_v = \frac{-\left[\frac{1}{R_F} + \frac{1}{r_e}\right](r_o \| R_C)}{1 + \frac{r_o \| R_C}{R_F}} = \frac{-\left[\frac{1}{180\,\text{k}\Omega} + \frac{1}{11.21\Omega}\right](2.38\,\text{k}\Omega)}{1 + \frac{2.38\,\text{k}\Omega}{180\,\text{k}\Omega}}$$

$$= \frac{-[5.56 \times 10^{-6} - 8.92 \times 10^{-2}](2.38\,\text{k}\Omega)}{1 + 0.013}$$

$$= \mathbf{-209.56} \text{ vs. } -240.86 \text{ above}$$

A_i:

$$A_i = -A_v \frac{Z_i}{R_C}$$

$$= -(-209.56)\frac{617.7\ \Omega}{2.7\ \text{k}\Omega}$$

$$= \mathbf{47.94} \text{ vs. } 50 \text{ above}$$

For the configuration of Fig. 8.30, Eqs. (8.71) through (8.74) will determine the variables of interest. The derivations are left as an exercise at the end of the chapter.

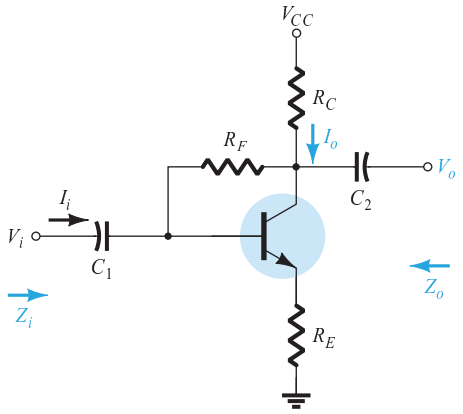


Figure 8.30 Collector feedback configuration with an emitter resistor R_E.

Z_i:

$$Z_i \cong \frac{R_E}{\left[\frac{1}{\beta} + \frac{(R_E + R_C)}{R_F}\right]} \tag{8.71}$$

Z_o:

$$Z_o \cong R_C \| R_F \tag{8.72}$$

A_v:

$$A_v \cong -\frac{R_C}{R_E} \tag{8.73}$$

A_i:

$$A_i \cong \frac{1}{\frac{1}{\beta} + \frac{(R_E + R_C)}{R_F}} \tag{8.74}$$

8.8 COLLECTOR DC FEEDBACK CONFIGURATION

The network of Fig. 8.31 has a dc feedback resistor for increased stability, yet the capacitor C_3 will shift portions of the feedback resistance to the input and output sections of the network in the ac domain. The portion of R_F shifted to the input or output side will be determined by the desired ac input and output resistance levels.

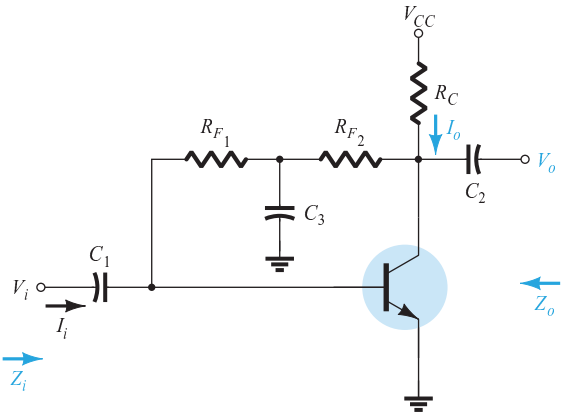


Figure 8.31 Collector dc feedback configuration.

At the frequency or frequencies of operation, the capacitor will assume a short-circuit equivalent to ground due to its low impedance level compared to the other elements of the network. The small-signal ac equivalent circuit will then appear as shown in Fig. 8.32.

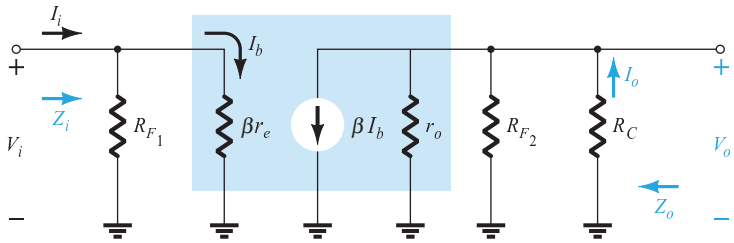


Figure 8.32 Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 8.31.

***Z_i*:**

$$Z_i = R_{F_1} \| \beta r_e \tag{8.75}$$

***Z_o*:**

$$Z_o = R_C \| R_{F_2} \| r_o \tag{8.76}$$

For $r_o \geq 10R_C$,

$$Z_o \cong R_C \| R_{F_2} \qquad r_o \geq 10R_C \tag{8.77}$$

***A_v*:**

$$R' = r_o \| R_{F_2} \| R_C$$

and

$$V_o = -\beta I_b R'$$

but $$I_b = \frac{V_i}{\beta r_e}$$

and $$V_o = -\beta \frac{V_i}{\beta r_e} R'$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{r_o \| R_{F_2} \| R_C}{r_e}} \tag{8.78}$$

For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_{F_2} \| R_C}{r_e}}_{r_o \geq 10R_C} \tag{8.79}$$

A_i: For the input side,

$$I_b = \frac{R_{F_1} I_i}{R_{F_1} + \beta r_e} \qquad \text{or} \qquad \frac{I_b}{I_i} = \frac{R_{F_1}}{R_{F_1} + \beta r_e}$$

and for the output side using $R' = r_o \| R_{F_2}$

$$I_o = \frac{R' \beta I_b}{R' + R_C} \qquad \text{or} \qquad \frac{I_o}{I_b} = \frac{R' \beta}{R' + R_C}$$

The current gain,

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b} \cdot \frac{I_b}{I_i}$$
$$= \frac{R' \beta}{R' + R_C} \cdot \frac{R_{F_1}}{R_{F_1} + \beta r_e}$$

and

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{\beta R_{F_1} R'}{(R_{F_1} + \beta r_e)(R' + R_C)}}_{R' = r_o \| R_{F_2}} \tag{8.80}$$

Since R_{F_1} is usually much larger than βr_e, $R_{F_1} + \beta r_e \cong R_{F_1}$

and $$A_i = \frac{I_o}{I_i} \cong \frac{\beta R_{F_1} (r_o \| R_{F_2})}{R_{F_1} (r_o \| R_{F_2} + R_C)}$$

so that

$$\boxed{A_i = \frac{I_o}{I_i} \cong \frac{\beta}{1 + \dfrac{R_C}{r_o \| R_{F_2}}}}_{R_{F_1} \geq 10\beta r_e} \tag{8.81}$$

or

$$\boxed{A_i = \frac{I_o}{I_i} = -A_v \frac{Z_i}{R_C}} \tag{8.82}$$

Phase relationship: The negative sign in Eq. (8.78) clearly reveals a 180° phase shift between input and output voltages.

EXAMPLE 8.10

For the network of Fig. 8.33, determine:

(a) r_e.
(b) Z_i.
(c) Z_o.
(d) A_v.
(e) A_i.

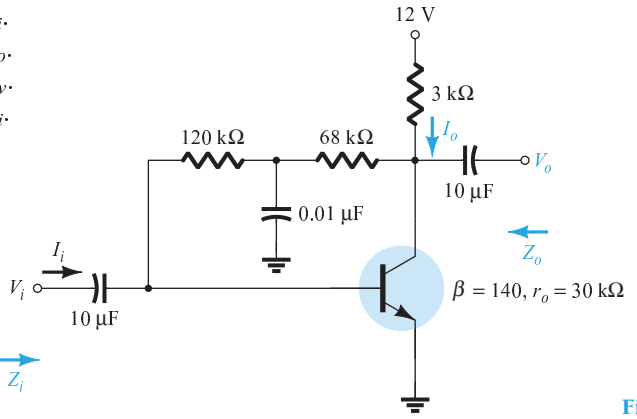


Figure 8.33 Example 8.10.

Solution

(a) DC: $$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C}$$

$$= \frac{12\text{ V} - 0.7\text{ V}}{(120\text{ k}\Omega + 68\text{ k}\Omega) + (140)3\text{ k}\Omega}$$

$$= \frac{11.3\text{V}}{608\text{ k}\Omega} = 18.6\mu\text{A}$$

$$I_E = (\beta + 1)I_B = (141)(18.6\mu A)$$

$$= 2.62\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.62\text{ mA}} = \mathbf{9.92\ \Omega}$$

(b) $\beta r_e = (140)(9.92\ \Omega) = 1.39\text{ k}\Omega$

The ac equivalent network appears in Fig. 8.34.

$$Z_i = R_{F_1} \| \beta r_e = 120\text{ k}\Omega \| 1.39\text{ k}\Omega$$

$$\cong \mathbf{1.37\ k\Omega}$$

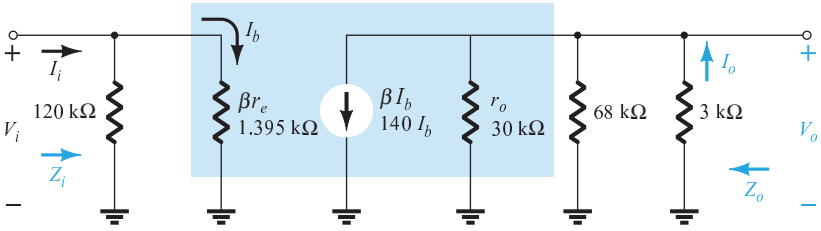


Figure 8.34 Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 8.33.

(c) Testing the condition $r_o \geq 10R_C$, we find

$$30\text{ k}\Omega \geq 10(3\text{ k}\Omega) = 30\text{ k}\Omega$$

which is satisfied through the equals sign in the condition. Therefore,

$$Z_o \cong R_C \| R_{F_2} = 3\text{ k}\Omega \| 68\text{ k}\Omega$$

$$= \mathbf{2.87\ k\Omega}$$

(d) $r_o \geq 10R_C$, therefore,

$$A_v \cong -\frac{R_{F_2} \| R_C}{r_e} = -\frac{68\ \text{k}\Omega \| 3\ \text{k}\Omega}{9.92\ \Omega}$$

$$\cong -\frac{2.87\ \text{k}\Omega}{9.92\ \Omega}$$

$$\cong \mathbf{-289.3}$$

(e) Since the condition $R_{F_1} \gg \beta r_e$ is satisfied,

$$A_i \cong \frac{\beta}{1 + \dfrac{R_C}{r_o \| R_{F_2}}} = \frac{140}{1 + \dfrac{3\ \text{k}\Omega}{30\ \text{k}\Omega \| 68\ \text{k}\Omega}} = \frac{140}{1 + 0.14} = \frac{140}{1.14}$$

$$\cong \mathbf{122.8}$$

8.9 APPROXIMATE HYBRID EQUIVALENT CIRCUIT

The analysis using the approximate hybrid equivalent circuit of Fig. 8.35 for the common-emitter configuration and of Fig. 8.36 for the common-base configuration is very similar to that just performed using the r_e model. Although time and priorities do not permit a detailed analysis of all the configurations discussed thus far, a brief overview of some of the most important will be included in this section to demonstrate the similarities in approach and the resulting equations.

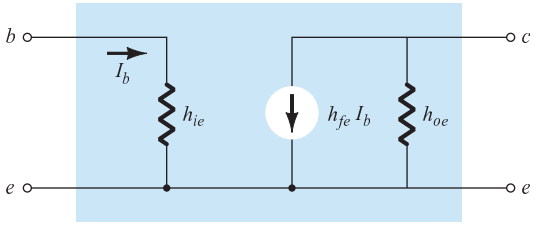


Figure 8.35 Approximate common-emitter hybrid equivalent circuit.

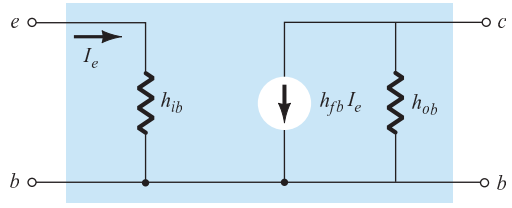


Figure 8.36 Approximate common-base hybrid equivalent circuit.

Since the various parameters of the hybrid model are specified by a data sheet or experimental analysis, the dc analysis associated with use of the r_e model is not an integral part of the use of the hybrid parameters. In other words, when the problem is presented, the parameters such as h_{ie}, h_{fe}, h_{ib}, and so on, are specified. Keep in mind, however, that the hybrid parameters and components of the r_e model are related by the following equations as discussed in detail in Chapter 7: $h_{ie} = \beta r_e$, $h_{fe} = \beta$, $h_{oe} = 1/r_o$, $h_{fb} = -\alpha$, and $h_{ib} = r_e$ (note Appendix A).

Fixed-Bias Configuration

For the fixed-bias configuration of Fig. 8.37, the small-signal ac equivalent network will appear as shown in Fig. 8.38 using the approximate common-emitter hybrid equiv-

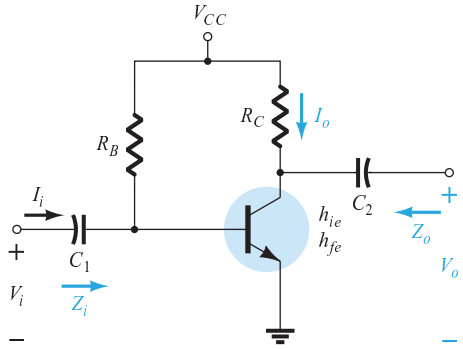


Figure 8.37 Fixed-bias configuration.

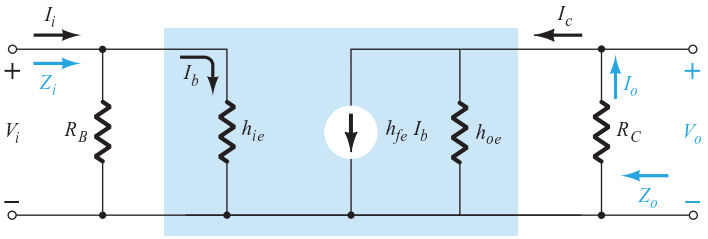


Figure 8.38 Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 8.37.

alent model. Compare the similarities in appearance with Fig. 8.3 and the r_e model analysis. The similarities suggest that the analysis will be quite similar, and the results of one can be directly related to the other.

***Z_i*:** From Fig. 8.38,

$$\boxed{Z_i = R_B \| h_{ie}} \tag{8.83}$$

***Z_o*:** From Fig. 8.38,

$$\boxed{Z_o = R_C \| 1/h_{oe}} \tag{8.84}$$

***A_v*:** Using $R' = 1/h_{oe} \| R_C$,

$$V_o = -I_o R' = -I_C R'$$
$$= -h_{fe} I_b R'$$

and

$$I_b = \frac{V_i}{h_{ie}}$$

with

$$V_o = -h_{fe}\frac{V_i}{h_{ie}} R'$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}}} \tag{8.85}$$

***A_i*:** Assuming that $R_B \gg h_{ie}$ and $1/h_{oe} \geq 10R_C$, then $I_b \cong I_i$ and $I_o = I_c = h_{fe}I_b = h_{fe} I_i$ with

$$\boxed{A_i = \frac{I_o}{I_i} \cong h_{fe}} \tag{8.86}$$

For the network of Fig. 8.39, determine:

EXAMPLE 8.11

(a) Z_i.
(b) Z_o.
(c) A_v.
(d) A_i.

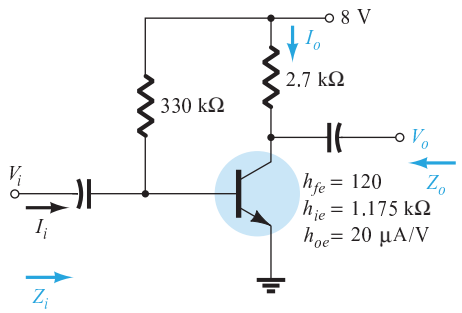


Figure 8.39 Example 8.11.

Solution

(a) $Z_i = R_B \| h_{ie} = 330\ \text{k}\Omega \| 1.175\ \text{k}\Omega$

$\cong h_{ie} = \mathbf{1.171\ k\Omega}$

(b) $r_o = \dfrac{1}{h_{oe}} = \dfrac{1}{20\ \mu\text{A/V}} = 50\ \text{k}\Omega$

$Z_o = \dfrac{1}{h_{oe}} \| R_C = 50\ \text{k}\Omega \| 2.7\ \text{k}\Omega = \mathbf{2.56\ k\Omega} \cong R_C$

(c) $Av = -\dfrac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} = -\dfrac{(120)(2.7\ \text{k}\Omega \| 50\ \text{k}\Omega)}{1.171\ \text{k}\Omega} = \mathbf{-262.34}$

(d) $A_i \cong h_{fe} = 120$

Voltage-Divider Configuration

For the voltage-divider bias configuration of Fig. 8.40, the resulting small-signal ac equivalent network will have the same appearance as Fig. 8.38, with R_B replaced by $R' = R_1 \| R_2$.

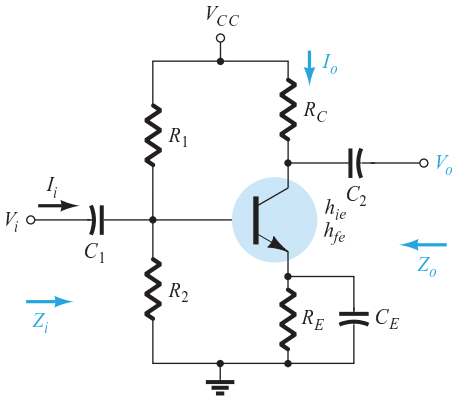


Figure 8.40 Voltage-divider bias configuration.

Z_i: From Fig. 8.38 with $R_B = R'$,

$$Z_i = R' \| h_{ie} \tag{8.87}$$

Z_o: From Fig. 8.38,

$$Z_o \cong R_C \tag{8.88}$$

A_v:

$$A_v = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} \tag{8.89}$$

A_i:

$$A_i = -\frac{h_{fe}R'}{R' + h_{ie}} \tag{8.90}$$

Unbypassed Emitter-Bias Configuration

For the CE unbypassed emitter-bias configuration of Fig. 8.41, the small-signal ac model will be the same as Fig. 8.11, with βr_e replaced by h_{ie} and βI_b by $h_{fe}I_b$. The analysis will proceed in the same manner.

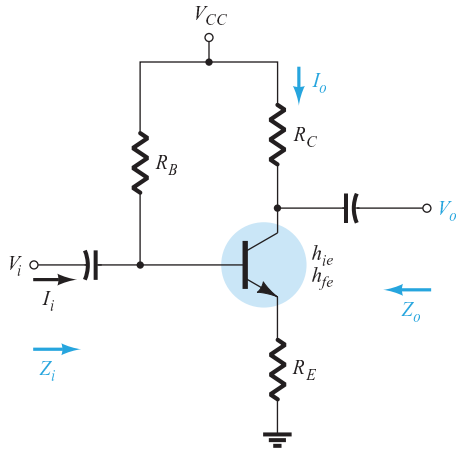


Figure 8.41 CE unbypassed emitter-bias configuration.

Z_i:

$$Z_b \cong h_{fe}\, R_E \tag{8.91}$$

and

$$Z_i = R_B \| Z_b \tag{8.92}$$

Z_o:

$$Z_o = R_C \tag{8.93}$$

A_v:

$$A_v = -\frac{h_{fe}\, R_C}{Z_b} \cong -\frac{h_{fe}R_C}{h_{fe}\, R_E}$$

and

$$A_v \cong -\frac{R_C}{R_E} \tag{8.94}$$

A_i:

$$A_i = \frac{h_{fe}R_B}{R_B + Z_b} \tag{8.95}$$

or
$$A_i = -A_v \frac{Z_i}{R_C} \tag{8.96}$$

Emitter-Follower Configuration

For the emitter-follower of Fig. 8.42, the small-signal ac model will match Fig. 8.18, with $\beta r_e = h_{ie}$ and $\beta = h_{fe}$. The resulting equations will therefore be quite similar.

***Z_i*:**

$$Z_b \cong h_{fe} R_E \tag{8.97}$$

$$Z_i = R_B \| Z_b \tag{8.98}$$

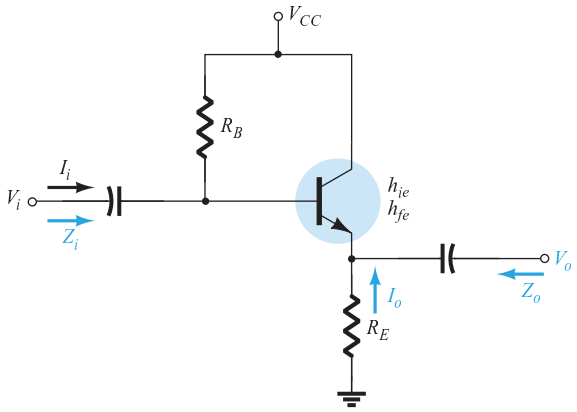


Figure 8.42 Emitter-follower configuration.

***Z_o*:** For Z_o, the output network defined by the resulting equations will appear as shown in Fig. 8.43. Review the development of the equations in Section 8.5 and

$$Z_o = R_E \| \frac{h_{ie}}{1 + h_{fe}}$$

or since $1 + h_{fe} \cong h_{fe}$,

$$Z_o \cong R_E \| \frac{h_{ie}}{h_{fe}} \tag{8.99}$$

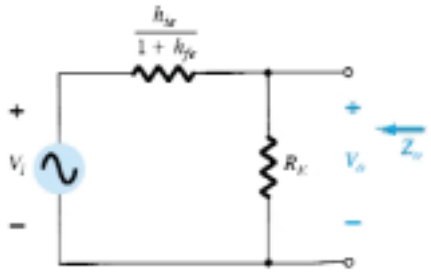


Figure 8.43 Defining Z_o for the emitter-follower configuration.

***A_v*:** For the voltage gain, the voltage-divider rule can be applied to Fig. 8.43 as follows:

$$V_o = \frac{R_E (V_i)}{R_E + h_{ie}/(1 + h_{fe})}$$

but since $1 + h_{fe} \cong h_{fe}$,

$$A_v = \frac{V_o}{V_i} \cong \frac{R_E}{R_E + h_{ie}/h_{fe}} \tag{8.100}$$

A_i:

$$A_i = \frac{h_{fe} R_B}{R_B + Z_b} \tag{8.101}$$

or

$$A_i = -A_v \frac{Z_i}{R_E} \tag{8.102}$$

Common-Base Configuration

The last configuration to be examined with the approximate hybrid equivalent circuit will be the common-base amplifier of Fig. 8.44. Substituting the approximate common-base hybrid equivalent model will result in the network of Fig. 8.45, which is very similar to Fig. 8.24. From Fig. 8.45,

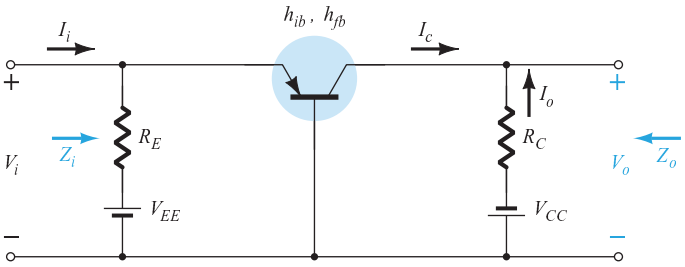


Figure 8.44 Common-base configuration.

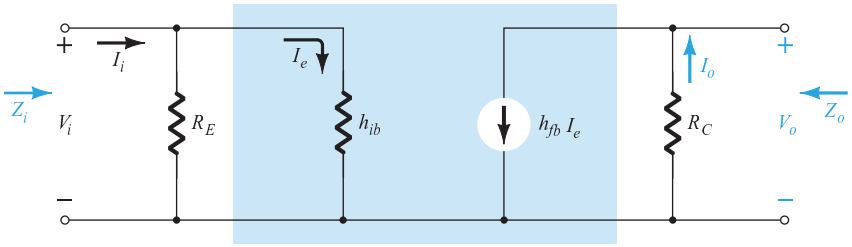


Figure 8.45 Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 8.44.

Z_i:

$$Z_i = R_E \| h_{ib} \tag{8.103}$$

Z_o:

$$Z_o = R_C \tag{8.104}$$

A_v:

$$V_o = -I_o R_C = -(h_{fb} I_e) R_C$$

with $I_e = \dfrac{V_i}{h_{ib}}$ and $V_o = -h_{fb}\dfrac{V_i}{h_{ib}}R_C$

so that

$$A_v = \frac{V_o}{V_i} = -\frac{h_{fb}R_C}{h_{ib}} \tag{8.105}$$

A_i:

$$A_i = \frac{I_o}{I_i} = h_{fb} \cong -1 \tag{8.106}$$

EXAMPLE 8.12

For the network of Fig. 8.46, determine:
(a) Z_i.
(b) Z_o.
(c) A_v.
(d) A_i.

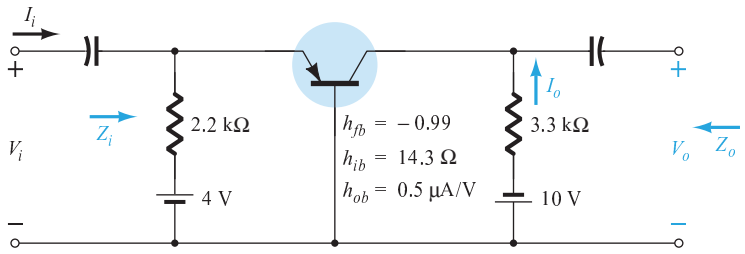


Figure 8.46 Example 8.12.

Solution

(a) $Z_i = R_E \| h_{ib} = 2.2\ \text{k}\Omega \| 14.3\ \Omega = \mathbf{14.21\ \Omega} \cong h_{ib}$

(b) $r_o = \dfrac{1}{h_{ob}} = \dfrac{1}{0.5\ \mu\text{A/V}} = 2\ \text{M}\Omega$

$$Z_o = \frac{1}{h_{ob}} \| R_C \cong R_C = \mathbf{3.3\ k\Omega}$$

(c) $A_v = -\dfrac{h_{fb}R_C}{h_{ib}} = -\dfrac{(-0.99)(3.3\ \text{k}\Omega)}{14.21} = \mathbf{229.91}$

(d) $A_i \cong h_{fb} = \mathbf{-1}$

The remaining configurations of Sections 8.1 through 8.8 that were not analyzed in this section are left as an exercise in the problem section of this chapter. It is assumed that the analysis above clearly reveals the similarities in approach using the r_e or approximate hybrid equivalent models, thereby removing any real difficulty with analyzing the remaining networks of the earlier sections.

8.10 COMPLETE HYBRID EQUIVALENT MODEL

The analysis of Section 8.9 was limited to the approximate hybrid equivalent circuit with some discussion about the output impedance. In this section, we employ the complete equivalent circuit to show the impact of h_r and define in more specific terms the

impact of h_o. It is important to realize that since the hybrid equivalent model has the same appearance for the common-base, common-emitter, and common-collector configurations, the equations developed in this section can be applied to each configuration. It is only necessary to insert the parameters defined for each configuration. That is, for a common-base configuration, h_{fb}, h_{ib}, and so on, are employed, while for a common-emitter configuration, h_{fe}, h_{ie}, and so on, are utilized. Recall that Appendix A permits a conversion from one set to the other if one set is provided and the other is required.

Consider the general configuration of Fig. 8.47 with the two-port parameters of particular interest. The complete hybrid equivalent model is then substituted in Fig. 8.48 using parameters that do not specify the type of configuration. In other words, the solutions will be in terms of h_i, h_r, h_f, and h_o. Unlike the analysis of previous sections of this chapter, the current gain A_i will be determined first since the equations developed will prove useful in the determination of the other parameters.

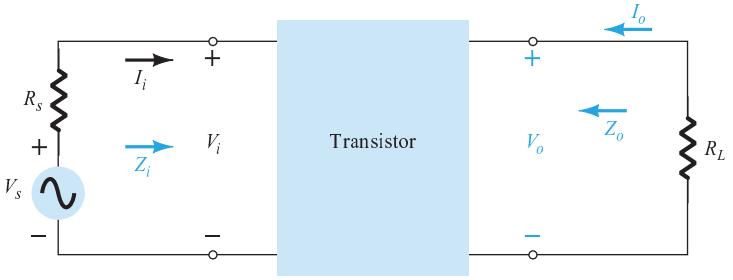


Figure 8.47 Two-port system.

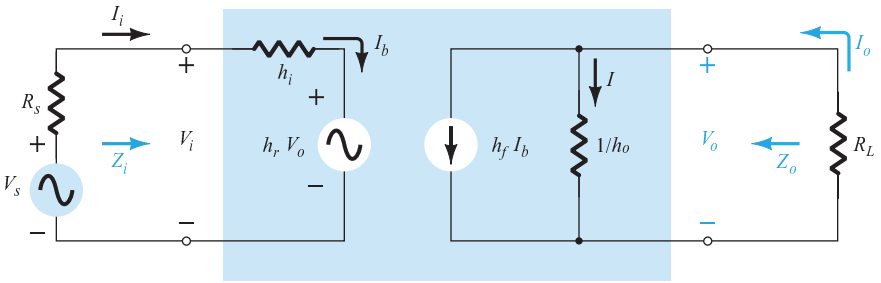


Figure 8.48 Substituting the complete hybrid equivalent circuit into the two-port system of Fig. 8.47.

Current Gain, $A_i = I_o/I_i$

Applying Kirchhoff's current law to the output circuit yields

$$I_o = h_f I_b + I = h_f I_i + \frac{V_o}{1/h_o} = h_f I_i + h_o V_o$$

Substituting $V_o = -I_o R_L$ gives us

$$I_o = h_f I_i - h_o R_L I_o$$

Rewriting the equation above, we have

$$I_o + h_o R_L I_o = h_f I_i$$

and

$$I_o(1 + h_o R_L) = h_f I_i$$

so that
$$A_i = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L} \tag{8.107}$$

Note that the current gain will reduce to the familiar result of $A_i = h_f$ if the factor $h_o R_L$ is sufficiently small compared to 1.

Voltage Gain, $A_v = V_o/V_i$

Applying Kirchhoff's voltage law to the input circuit results in

$$V_i = I_i h_i + h_r V_o$$

Substituting $I_i = (1 + h_o R_L) I_o / h_f$ from Eq. (8.107) and $I_o = -V_o/R_L$ from above results in

$$V_i = \frac{-(1 + h_o R_L) h_i}{h_f R_L} V_o + h_r V_o$$

Solving for the ratio V_o/V_i yields

$$A_v = \frac{V_o}{V_i} = \frac{-h_f R_L}{h_i + (h_i h_o - h_f h_r) R_L} \tag{8.108}$$

In this case, the familiar form of $A_v = -h_f R_L / h_i$ will return if the factor $(h_i h_o - h_f h_r) R_L$ is sufficiently small compared to h_i.

Input Impedance, $Z_i = V_i/I_i$

For the input circuit,

$$V_i = h_i I_i + h_r V_o$$

Substituting $V_o = -I_o R_L$

we have
$$V_i = h_i I_i - h_r R_L I_o$$

Since
$$A_i = \frac{I_o}{I_i}$$

$$I_o = A_i I_i$$

so that the equation above becomes

$$V_i = h_i I_i - h_r R_L A_i I_i$$

Solving for the ratio V_i/I_i, we obtain

$$Z_i = \frac{V_i}{I_i} = h_i - h_r R_L A_i$$

and substituting

$$A_i = \frac{h_f}{1 + h_o R_L}$$

yields
$$Z_i = \frac{V_i}{I_i} = h_i \frac{-h_f h_r R_L}{1 + h_o R_L} \tag{8.109}$$

The familiar form of $Z_i = h_i$ will be obtained if the second factor is sufficiently smaller than the first.

Output Impedance, $Z_o = V_o/I_o$

The output impedance of an amplifier is defined to be the ratio of the output voltage to the output current with the signal V_s set to zero. For the input circuit with $V_s = 0$,

$$I_i = \frac{-h_r V_o}{R_s + h_i}$$

Substituting this relationship into the following equation obtained from the output circuit yields

$$I_o = h_f I_i + h_o V_o$$

$$= \frac{-h_f h_r V_o}{R_s + h_i} + h_o V_o$$

and

$$\boxed{Z_o = \frac{V_o}{I_o} = \frac{1}{h_o - [h_f h_r/(h_i + R_s)]}} \tag{8.110}$$

In this case, the output impedance will reduce to the familiar form $Z_o = 1/h_o$ for the transistor when the second factor in the denominator is sufficiently smaller than the first.

EXAMPLE 8.13

For the network of Fig. 8.49, determine the following parameters using the complete hybrid equivalent model and compare to the results obtained using the approximate model.

(a) Z_i and Z_i'.
(b) A_v.
(c) $A_i = I_o/I_i$ and $A_i' = I_o/I_i'$.
(d) Z_o (within R_C) and Z_o' (including R_C).

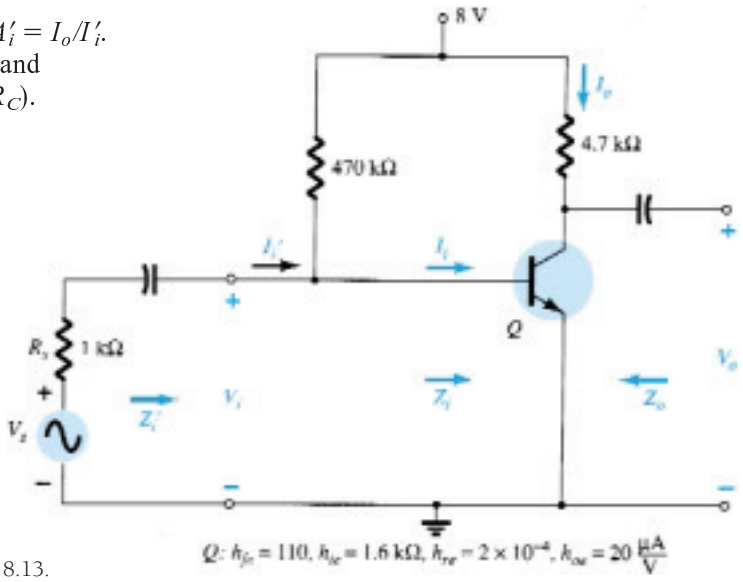


Figure 8.49 Example 8.13.

Solution

Now that the basic equations for each quantity have been derived, the order in which they are calculated is arbitrary. However, the input impedance is often a useful quantity to know and therefore will be calculated first. The complete common-emitter hybrid equivalent circuit has been substituted and the network redrawn as shown in Fig. 8.50. A Thévenin equivalent circuit for the input section of Fig. 8.50 will result in the input equivalent of Fig. 8.51 since $E_{\text{Th}} \cong V_s$ and $R_{\text{Th}} \cong R_s = 1$ kΩ (a result of $R_B = 470$ kΩ being much greater than $R_s = 1$ kΩ). In this example, $R_L = R_C$ and I_o is de-

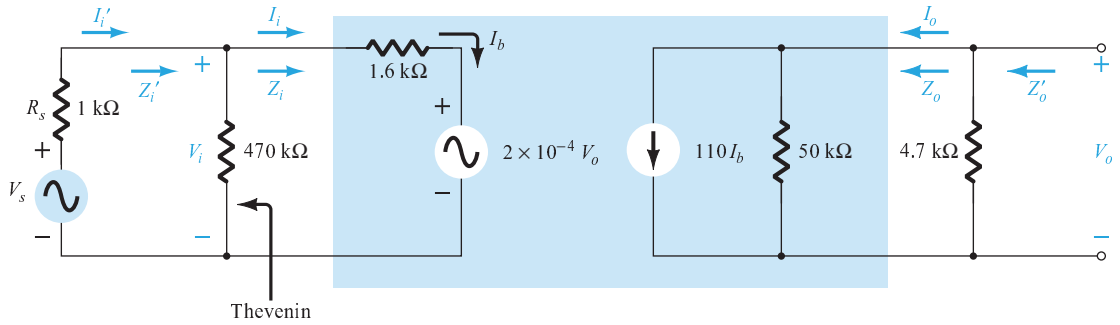


Figure 8.50 Substituting the complete hybrid equivalent circuit into the ac equivalent network of Fig. 8.49.

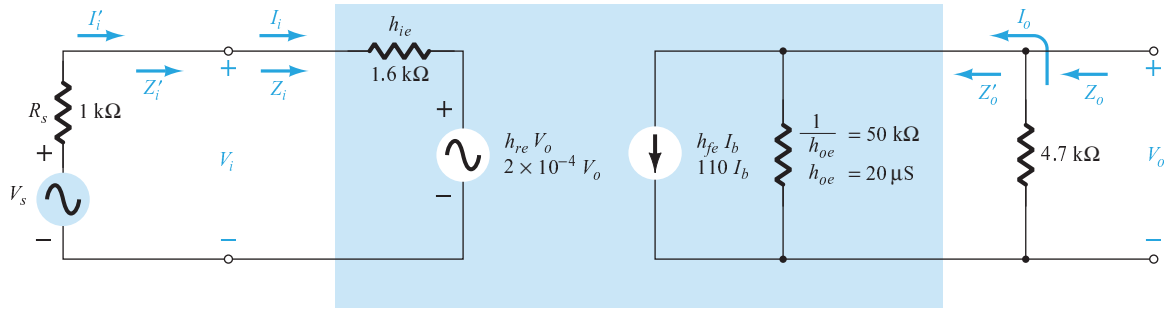


Figure 8.51 Replacing the input section of Fig. 8.50 with a Thévenin equivalent circuit.

fined as the current through R_C as in previous examples of this chapter. The output impedance Z_o as defined by Eq. (8.110) is for the output transistor terminals only. It does not include the effects of R_C. Z'_o is simply the parallel combination of Z_o and R_L. The resulting configuration of Fig. 8.51 is then an exact duplicate of the defining network of Fig. 8.48, and the equations derived above can be applied.

(a) Eq. (8.109): $$Z_i = \frac{V_i}{I_i} = h_{ie} - \frac{h_{fe}h_{re}R_L}{1 + h_{oe}R_L}$$

$$= 1.6\ \text{k}\Omega - \frac{(110)(2 \times 10^{-4})(4.7\ \text{k}\Omega)}{1 + (20\ \mu\text{S})(4.7\ \text{k}\Omega)}$$

$$= 1.6\ \text{k}\Omega - 94.52\ \Omega$$

$$= \mathbf{1.51\ k\Omega}$$

versus 1.6 kΩ using simply h_{ie}.

$$Z'_i = 470\ \text{k}\Omega \| Z_i \cong Z_i = \mathbf{1.51\ k\Omega}$$

(b) Eq. (8.108): $$A_v = \frac{V_o}{V_i} = \frac{-h_{fe}R_L}{h_{ie} + (h_{ie}h_{oe} - h_{fe}h_{re})R_L}$$

$$= \frac{-(110)(4.7\ \text{k}\Omega)}{1.6\ \text{k}\Omega + [(1.6\ \text{k}\Omega)(20\ \mu\text{S}) - (110)(2 \times 10^{-4})]4.7\ \text{k}\Omega}$$

$$= \frac{-517 \times 10^3\ \Omega}{1.6\ \text{k}\Omega + (0.032 - 0.022)4.7\ \text{k}\Omega}$$

$$= \frac{-517 \times 10^3\ \Omega}{1.6\ \text{k}\Omega + 47\ \Omega}$$

$$= \mathbf{-313.9}$$

versus -323.125 using $A_v \cong -h_{fe}R_L/h_{ie}$.

(c) Eq. (8.107): $$A_i = \frac{I_o}{I_i} = \frac{h_{fe}}{1 + h_{oe}R_L} = \frac{110}{1 + (20\ \mu\text{S})(4.7\ \text{k}\Omega)}$$

$$= \frac{110}{1 + 0.094} = \mathbf{100.55}$$

versus 110 using simply h_{fe}. Since $470\ \text{k}\Omega \gg Z_i$, $I'_i \cong I_i$ and $A'_i \cong \mathbf{100.55}$ also.

(d) Eq. (8.110): $$Z_o = \frac{V_o}{I_o} = \frac{1}{h_{oe} - [h_{fe}h_{re}/(h_{ie} + R_s)]}$$

$$= \frac{1}{20\ \mu\text{S} - [(110)(2 \times 10^{-4})/(1.6\ \text{k}\Omega + 1\ \text{k}\Omega)]}$$

$$= \frac{1}{20\ \mu\text{S} - 8.46\ \mu\text{S}}$$

$$= \frac{1}{11.54\ \mu\text{S}}$$

$$= \mathbf{86.66\ k\Omega}$$

which is greater than the value determined from $1/h_{oe} = 50\ \text{k}\Omega$.

$$Z'_o = R_C \| Z_o = 4.7\ \text{k}\Omega \| 86.66\ \text{k}\Omega = \mathbf{4.46\ k\Omega}$$

versus $4.7\ \text{k}\Omega$ using only R_C.

Note from the results above that the approximate solutions for A_v and Z_i were very close to those calculated with the complete equivalent model. In fact, even A_i was off by less than 10%. The higher value of Z_o only contributed to our earlier conclusion that Z_o is often so high that it can be ignored compared to the applied load. However, keep in mind that when there is a need to determine the impact of h_{re} and h_{oe}, the complete hybrid equivalent model must be used, as described above.

The specification sheet for a particular transistor typically provides the common-emitter parameters as noted in Fig. 7.28. The next example will employ the same transistor parameters appearing in Fig. 8.49 in a *pnp* common-base configuration to introduce the parameter conversion procedure and emphasize the fact that the hybrid equivalent model maintains the same layout.

EXAMPLE 8.14

For the common-base amplifier of Fig. 8.52, determine the following parameters using the complete hybrid equivalent model and compare the results to those obtained using the approximate model.

(a) Z_i and Z'_i.

(b) A_i and A'_i.

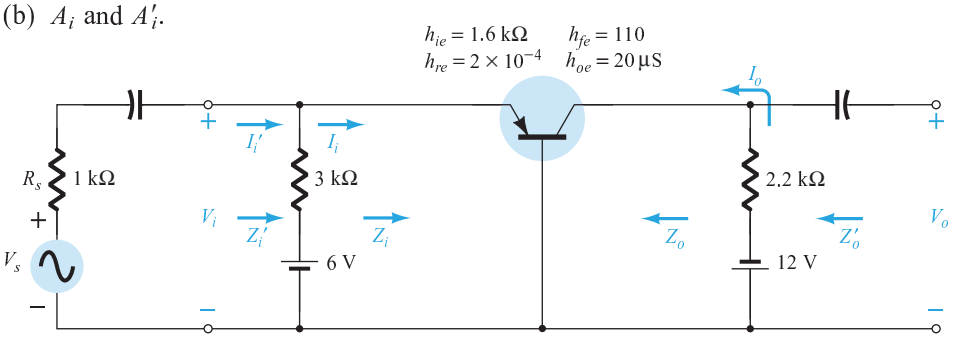


Figure 8.52 Example 8.14.

(c) A_v.
(d) Z_o and Z'_o.

Solution

The common-base hybrid parameters are derived from the common-emitter parameters using the approximate equations of Appendix A:

$$h_{ib} \cong \frac{h_{ie}}{1 + h_{fe}} = \frac{1.6\ \text{k}\Omega}{1 + 110} = \mathbf{14.41\ \Omega}$$

Note how closely the magnitude compares with the value determined from

$$h_{ib} = r_e = \frac{h_{ie}}{\beta} = \frac{1.6\ \text{k}\Omega}{110} = 14.55\ \Omega$$

$$h_{rb} \cong \frac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re} = \frac{(1.6\ \text{k}\Omega)(20\ \mu\text{S})}{1 + 110} - 2 \times 10^{-4}$$

$$= \mathbf{0.883 \times 10^{-4}}$$

$$h_{fb} \cong \frac{-h_{fe}}{1 + h_{fe}} = \frac{-110}{1 + 110} = \mathbf{-0.991}$$

$$h_{ob} \cong \frac{h_{oe}}{1 + h_{fe}} = \frac{20\ \mu\text{S}}{1 + 110} = \mathbf{0.18\ \mu S}$$

Substituting the common-base hybrid equivalent circuit into the network of Fig.

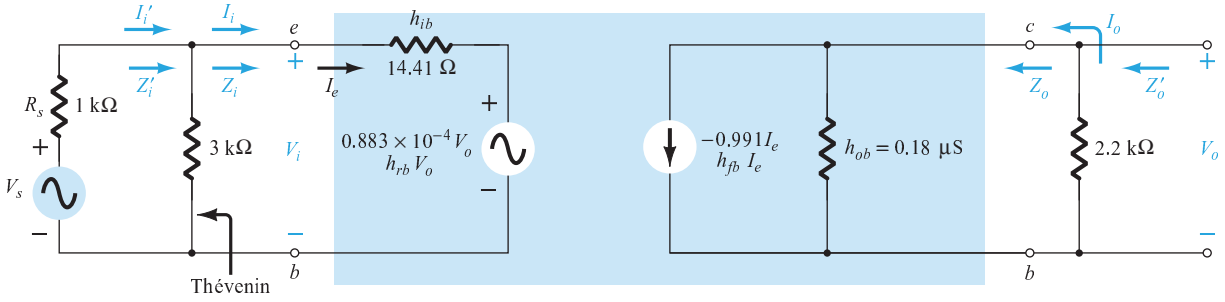


Figure 8.53 Small-signal equivalent for the network of Fig. 8.52.

8.52 will then result in the small-signal equivalent network of Fig. 8.53. The Thévenin network for the input circuit will result in $R_{\text{Th}} = 3\ \text{k}\Omega \| 1\ \text{k}\Omega = 0.75\ \text{k}\Omega$ for R_s in the equation for Z_o.

(a) Eq. (8.109): $$Z_i = \frac{V_i}{I_i} = h_{ib} - \frac{h_{fb}h_{rb}R_L}{1 + h_{ob}R_L}$$

$$= 14.41\ \Omega - \frac{(-0.991)(0.883 \times 10^{-4})(2.2\ \text{k}\Omega)}{1 + (0.18\ \mu\text{S})(2.2\ \text{k}\Omega)}$$

$$= 14.41\ \Omega + 0.19\ \Omega$$

$$= \mathbf{14.60\ \Omega}$$

versus 14.41 Ω using $Z_i \cong h_{ib}$.

$$Z'_i = 3\ \text{k}\Omega \| Z_i \cong Z_i = \mathbf{14.60\ \Omega}$$

(b) Eq. (8.107): $$A_i = \frac{I_o}{I_i} = \frac{h_{fb}}{1 + h_{ob}R_L}$$

$$= \frac{-0.991}{1 + (0.18\ \mu\text{S})(2.2\ \text{k}\Omega)}$$

$$= \mathbf{-0.991} = h_{fb}$$

Since $3\ \text{k}\Omega \gg Z_i$, $I'_i \cong I_i$ and $A'_i = I_o/I'_i \cong -1$ also.

(c) Eq. (8.108): $$A_v = \frac{V_o}{V_i} = \frac{-h_{fb}R_L}{h_{ib} + (h_{ib}h_{ob} - h_{fb}h_{rb})R_L}$$

$$= \frac{-(-0.991)(2.2\ \text{k}\Omega)}{14.41\ \Omega + [(14.41\ \Omega)(0.18\ \mu\text{S}) - (-0.991)(0.883 \times 10^{-4})]2.2\ \text{k}\Omega}$$

$$= \mathbf{149.25}$$

versus 151.3 using $A_v \cong -h_{fb}R_L/h_{ib}$.

(d) Eq. (8.110): $$Z_o = \frac{1}{h_{ob} - [h_{fb}h_{rb}/(h_{ib} + R_s)]}$$

$$= \frac{1}{0.18\ \mu\text{S} - [(-0.991)(0.883 \times 10^{-4})/(14.41\ \Omega + 0.75\ \text{k}\Omega)]}$$

$$= \frac{1}{0.295\ \mu\text{S}}$$

$$= \mathbf{3.39\ M\Omega}$$

versus 5.56 MΩ using $Z_o \cong 1/h_{ob}$. For Z'_o as defined by Fig. 8.53:

$$Z'_o = R_C \| Z_o = 2.2\ \text{k}\Omega \| 3.39\ \text{M}\Omega = \mathbf{2.199\ k\Omega}$$

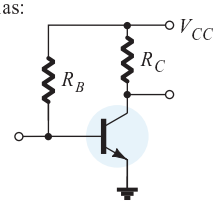
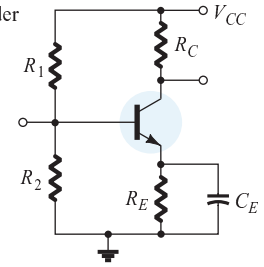
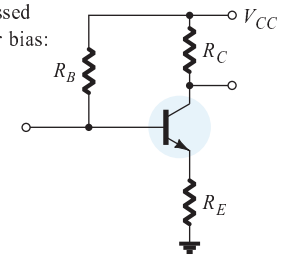
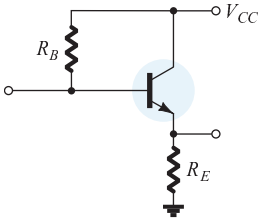
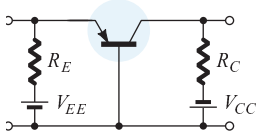
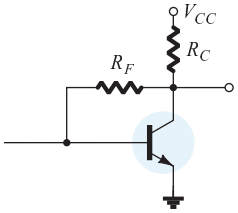
versus 2.2 kΩ using $Z'_o \cong R_C$.

8.11 SUMMARY TABLE

Now that the most familiar configurations of the small-signal transistor amplifiers have been introduced, Table 8.1 is presented to review the general characteristics of each for immediate recall. It must be absolutely clear that the values listed are simply typical values to establish a basis for comparison. The levels obtained in an actual analysis will most likely be different, and certainly different from one configuration to another. Being able to repeat most of the information in the table is an important first step in developing a general familiarity with the subject matter. For instance, one should now be able to state with some assurance that the emitter-follower configuration typically has a high input impedance, low output impedance, and a voltage gain slightly less than 1. There should be no need to perform a variety of calculations to recall salient facts such as those above. For the future, it will permit the study of a network or system without becoming mathematically involved. The function of each component of a design will become increasingly familiar as general facts such as those above become part of your background.

One obvious advantage of being able to recall general facts like the above is an ability to check the results of a mathematical analysis. If the input impedance of a common-base configuration is in the kilohm range, there is good reason to recheck the analysis. However, on the other side of the coin, a result of 22 Ω suggests that the analysis may be correct.

TABLE 8.1 Relative Levels for the Important Parameters of the CE, CB, and CC Transistor Amplifiers

Configuration	Z_i	Z_o	A_v	A_i
Fixed-bias: 	Medium (1 kΩ) $= R_B \| \beta r_e$ $\cong \beta r_e$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= R_C \| r_o$ $\cong R_C$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{(R_C \| r_o)}{r_e}$ $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$	High (100) $= \frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}$ $\cong \beta$ $(r_o \geq 10R_C, R_B \geq 10\beta r_e)$
Voltage-divider bias: 	Medium (1 kΩ) $= R_1 \| R_2 \| \beta r_e$	Medium (2 kΩ) $= R_C \| r_o$ $\cong R_C$ $(r_o \geq 10R_C)$	High (−200) $= -\frac{R_C \| r_o}{r_e}$ $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$	High (50) $= \frac{\beta(R_1 \| R_2) r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}$ $\cong \frac{\beta \| (R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}$ $(r_o \geq 10R_C)$
Unbypassed emitter bias: 	High (100 kΩ) $= R_B \| Z_b$ $Z_b \cong \beta(r_e + R_E)$ $\cong R_B \| \beta R_E$ $(R_E \gg r_e)$	Medium (2 kΩ) $= R_C$ (any level of r_o)	Low (−5) $= -\frac{R_C}{r_e + R_E}$ $\cong -\frac{R_C}{R_E}$ $(R_E \gg r_e)$	High (50) $\cong -\frac{\beta R_B}{R_B + Z_b}$
Emitter-follower: 	High (100 kΩ) $= R_B \| Z_b$ $Z_b \cong \beta(r_e + R_E)$ $\cong R_B \| \beta R_E$ $(R_E \gg r_e)$	Low (20 Ω) $= R_E \| r_e$ $\cong r_e$ $(R_E \gg r_e)$	Low ($\cong 1$) $= \frac{R_E}{R_E + r_e}$ $\cong 1$	High (−50) $\cong -\frac{\beta R_B}{R_B + Z_b}$
Common-base: 	Low (20 Ω) $= R_E \| r_e$ $\cong r_e$ $(R_E \gg r_e)$	Medium (2 kΩ) $= R_C$	High (200) $\cong \frac{R_C}{r_e}$	Low (−1) $\cong -1$
Collector feedback: 	Medium (1 kΩ) $= \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_E}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong R_C \| R_F$ $(r_o \geq 10R_C)$	High (−200) $\cong -\frac{R_C}{r_e}$ $(r_o \geq 10R_C)$ $R_F \gg R_C)$	High (50) $= \frac{\beta R_F}{R_F + \beta R_C}$ $\cong \frac{R_F}{R_C}$

8.12 TROUBLESHOOTING

Although the terminology *troubleshooting* suggests that the procedures to be described are designed simply to isolate a malfunction, it is important to realize that the same techniques can be applied to ensure that a system is operating properly. In any case, the testing, checking, or isolating procedures require an understanding of what to expect at various points in the network in both the dc and ac domains. In most cases, a network operating correctly in the dc mode will also behave properly in the ac domain. In addition, a network providing the expected ac response is most likely biased as planned. In a typical laboratory setting, both the dc and ac supplies are applied and the ac response at various points in the network is checked with an oscilloscope as shown in Fig. 8.54. Note that the black (gnd) lead of the oscilloscope is connected directly to ground and the red lead is moved from point to point in the network, providing the patterns appearing in Fig. 8.54. The vertical channels are set in the ac mode to remove any dc component associated with the voltage at a particular point. The small ac signal applied to the base is amplified to the level appearing from collector to ground. Note the difference in vertical scales for the two voltages. There is no ac

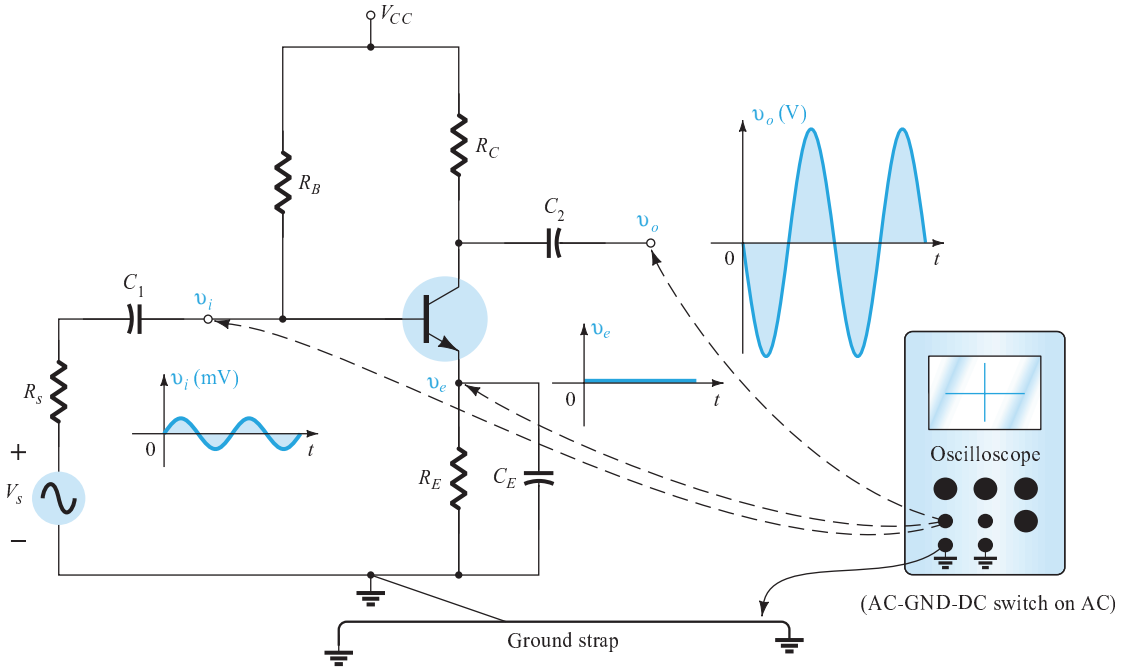


Figure 8.54 Using the oscilloscope to measure and display various voltages of a BJT amplifier.

response at the emitter terminal due to the short-circuit characteristics of the capacitor at the applied frequency. The fact that v_o is measured in volts and v_i in millivolts suggests a sizable gain for the amplifier. In general, the network appears to be operating properly. If desired, the dc mode of the multimeter could be used to check V_{BE} and the levels of V_B, V_{CE}, and V_E to review whether they lie in the expected range. Of course, the oscilloscope can also be used to compare dc levels simply by switching to the dc mode for each channel.

Needless to say, a poor ac response can be due to a variety of reasons. In fact, there may be more than one problem area in the same system. Fortunately, however, with time and experience, the probability of malfunctions in some areas can be predicted and an experienced person can isolate problem areas fairly quickly.

In general, there is nothing mysterious about the general troubleshooting process. If you decide to follow the ac response, it is good procedure to start with the applied

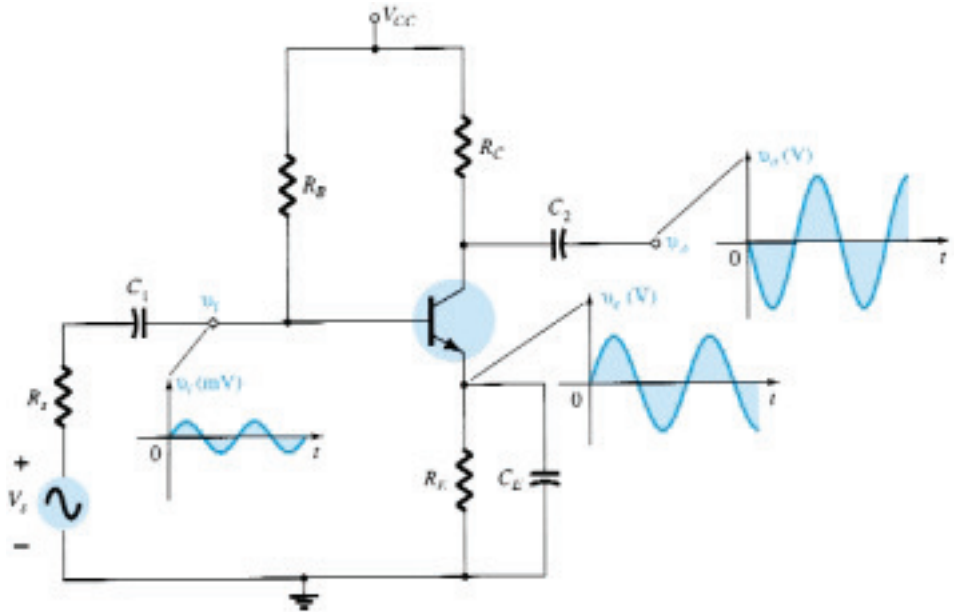


Figure 8.55 The waveforms resulting from a malfunction in the emitter area.

signal and progress through the system toward the load, checking critical points along the way. An unexpected response at some point suggests that the network is fine up to that area, thereby defining the region that must be investigated further. The waveform obtained on the oscilloscope will certainly help in defining the possible problems with the system.

If the response for the network of Fig. 8.54 is as appears in Fig. 8.55, the network has a malfunction that is probably in the emitter area. An ac response across the emitter is unexpected, and the gain of the system as revealed by v_o is much lower. Recall for this configuration that the gain is much greater if R_E is bypassed. The response obtained suggests that R_E is not bypassed by the capacitor and the terminal connections of the capacitor and the capacitor itself should be checked. In this case, a checking of the dc levels will probably not isolate the problem area since the capacitor has an "open-circuit" equivalent for dc. In general, a prior knowledge of what to expect, a familiarity with the instrumentation, and most important, experience are all factors that contribute to the development of an effective approach to the art of troubleshooting.

8.13 PSPICE WINDOWS

Voltage-Divider Configuration Using the Software Transistor Parameters

Now that the basic maneuvers for developing the network on the schematics grid have been introduced, the current description will concentrate on the variations introduced by the ac analysis.

Using schematics, the network of Fig. 8.9 (Example 8.2) is developed as shown in Fig. 8.56. Note the ac source of 1 mV and the printer symbol at the output terminal of the network.

The sinusoidal ac source is listed in the **SOURCE.slb** library as **VSIN.** Once

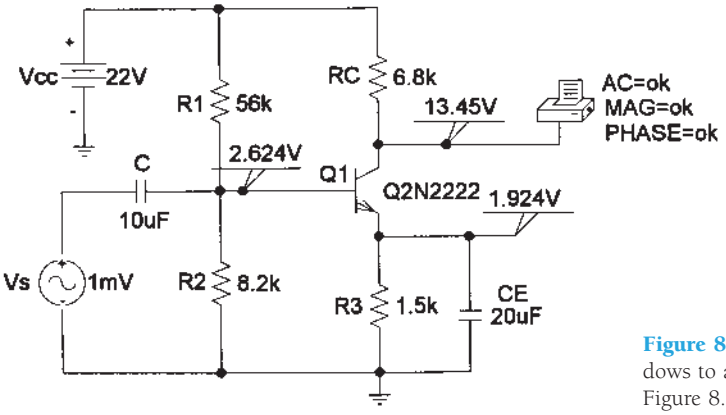


Figure 8.56 Using PSpice Windows to analyze the network of Figure 8.9 (Example 8.2).

placed on the diagram, double-clicking the symbol will result in the **PartName: VSIN** dialog box with a list of options. Each choice can be made by double-clicking the desired quantity, which will then appear in the **Name** and **Value** rectangles at the top of the box. The cursor appears in the **Value** box, and the desired value can be entered. After each entry, be sure to **Save Attr** to save the entered attribute. If done properly, the assigned value will appear in the listing.

For our analysis, the following choices will be made:

VAMPL = 1mV (the peak value of the sinusoidal signal).

FREQ = 10kHz (the frequency of interest).

PHASE = 0 (no initial phase angle for the sinusoidal signal).

VOFF = 0 (no dc offset voltage for the sinusoidal signal).

AC = 1mV.

If you want to display the value of the ac signal, simply click on **Change Display** after saving the attribute. For instance, if AC = 1mV was just saved and **Change Display** was chosen, a **Change Attribute** dialog box would appear. Since AC is the name and 1mV the value, choose **Value Only,** and only the 1mV will be displayed after the sequence **OK-OK.**

The printer symbol on the collector of the transistor is listed as **VPRINT1** under the **SPECIAL.slb** library. When placed on the schematic, it dictates that the ac voltage at that point will be printed in the output file (*.out). Double-clicking on the printer symbol will result in a **PRINT1** dialog box, within which the following choices should be made:

AC = ok.

MAG = ok.

PHASE = ok.

After each entry, be sure to **Save Attr** or the computer will remind you. The above choices can be listed next to the printer symbol on the schematic by simply clicking the **Change Display** option and choosing the **Display Value and Name** for each item.

The transistor is obtained through the sequence **Get New Part** icon-**Libraries-EVAL.slb-Q2N2222-OK-Place & Close.** Since we will want the parameters of the transistor to match those of the example as closely as possible, one must first click on the transistor to put it in the active mode (red) and then choose **Edit-Model-Edit Instance Model (Text).** Next, the beta (**Bf**) is set to 90 and **Is** is set to 2E-15A to result in a base-to-emitter voltage close to 0.7 V. This value of *I* is the result of nu-

merous runs of the network to find that value of I_S that provided a level of V_{BE} closest to 0.7 V. For the remainder of this text, however, this chosen level of I_S will remain the same. In most cases, it provides the desired results.

VIEWPOINTs have been inserted to display the three dc voltages of interest. Since it has been used recently, **VIEWPOINT** can be found in the scroll listing at the top right of the menu bar rather than by returning to the library listing.

Choosing the **Setup Analysis** icon will result in the **Analysis Setup** dialog box, in which the **AC Sweep** must be chosen because of the applied ac source. Clicking on **AC Sweep** will result in an **AC Sweep and Noise Analysis** dialog box, in which **Linear** is chosen along with **Total Pts:** 1, **Start Freq:** 10kHz, and **End Freq:** 10kHz. The result will be an analysis at only one frequency. Our initial interest will simply be in the magnitude of the quantities of interest and not their shape or appearance. Therefore, we should turn to **Analysis-Probe Setup** and choose **Do not auto-run Probe** to save time getting to the desired results.

Clicking the **Analysis** icon will result in a **PSpiceAD** dialog box that will indicate the **AC Analysis** is finished. Note also the listing of the frequency applied at the bottom of the dialog box. Within this box, if we choose **File** followed by **Examine Output,** we will obtain a lengthy listing of input and output data on the analyzed network. Specific headings are duplicated in Fig. 8.57. Under **Schematics Netlist,** the nodes assigned to the network are revealed. Note that ground is always defined as the 0 node and the assumed node of higher potential listed first. The transistor is listed in the order Collector-Base-Emitter. Under **BJT MODEL PARAMETERS,** the defining parameters of the device are listed with the set values of I_S = 2E-15A and β = 90. Under **SMALL-SIGNAL BIAS SOLUTION,** the dc levels at the various nodes are revealed, which compare directly with the **VIEWPOINT** values. In particular, note that V_{BE} is exactly 0.7 V.

The next listing, **OPERATING POINT INFORMATION,** reveals that even though beta of the **BJT MODEL PARAMETERS** listing was set at 90, the operating conditions of the network resulted in a dc beta of 48.3 and an ac beta of 55. Fortunately, however, the voltage-divider configuration is less sensitive to changes in beta in the dc mode, and the dc results are excellent. However, the drop in ac beta had an effect on the resulting level of V_o: 296.1 mV versus the hand-written solution (with r_o = 50 kΩ) of 324.3 mV—a 9% difference. The results are certainly close, but probably not as close as one would like. A closer result (within 7%) could be obtained by setting all the parameters of the device except I_S and beta to zero. However, for the moment, the impact of the remaining parameters has been demonstrated, and the results will be accepted as sufficiently close to the hand-written levels. Later in this chapter, an ac model for the transistor will be introduced with results that will be an exact match with the hand-written solution. The phase angle is −178° versus the ideal of −180°—a very close match.

A plot of the output waveform can be obtained using the **Probe** option. The sequence **Analysis-Probe Setup-Automatically run Probe after simulation-OK** will result in a **MicroSim Probe** screen when the **Analysis** icon is chosen. However, if we follow this procedure without setting the horizontal scale, we will simply end up with a plot point of 296 mV at a frequency of 10 kHz. The horizontal scale is set by the sequence **Analysis-Setup-Transient** with the **AC Sweep** disabled. Clicking the **Transient** option will result in a **Transient** dialog box, in which a number of choices have to be made based on the waveform to be viewed. The period of the applied signal of 10 kHz is 0.1 ms = 100 μs. The **Print Step** option refers to the time interval between printing or plotting the results of the transient analysis. For our example, we will choose 1 μs to provide 100 plot points per cycle. The **Final Time** is the last instant the network's response will be determined. Our choice is 500 μs or 0.5 ms to provide five full cycles of the waveform. The **No-Print Delay** was chosen as 0 since all the capacitors are essentially short cir-

```
 ****     CIRCUIT DESCRIPTION
******************************************************************************
* Schematics Netlist *

V_V1         $N_0001 0 22
R_R1         $N_0001 $N_0002  56k
R_R4         $N_0002 0  8.2k
R_R2         $N_0001 $N_0003  6.8k
R_R3         $N_0004 0  1.5k
C_C1         $N_0004 0  20u
C_C2         $N_0005 $N_0002  10u
V_V2         $N_0005 0  AC 1m
+SIN 0 1m 10k 0 0 0

.PRINT         AC
+ VM([$N_0003])
+ VP([$N_0003])
Q_Q1         $N_0003 $N_0002 $N_0004 Q2N2222-X

**** RESUMING edc8a.cir ****

 ****     BJT MODEL PARAMETERS
******************************************************************************
               Q2N2222-X
               NPN
         IS    2.000000E-15
         BF    90
         NF    1
        VAF    74.03
        IKF      .2847
        ISE    14.340000E-15
         NE    1.307
         BR    6.092
         NR    1
         RB    10
         RC    1
        CJE    22.010000E-12
        MJE      .377
        CJC    7.306000E-12
        MJC      .3416
         TF  411.100000E-12
        XTF    3
        VTF    1.7
        ITF      .6
         TR   46.910000E-09
        XTB    1.5

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
******************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

($N_0001)   22.0000                  ($N_0002)    2.6239

($N_0003)   13.4530                  ($N_0004)    1.9244

($N_0005)    0.0000


    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_V1        -1.603E-03
    V_V2         0.000E+00

    TOTAL POWER DISSIPATION   3.53E-02  WATTS

 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
******************************************************************************
**** BIPOLAR JUNCTION TRANSISTORS


NAME         Q_Q1
MODEL        Q2N2222-X
IB           2.60E-05
IC           1.26E-03
VBE          6.99E-01
VBC         -1.08E+01
VCE          1.15E+01
BETADC       4.83E+01
GM           4.84E-02
RPI          1.14E+03
RX           1.00E+01
RO           6.75E+04
CBE          5.78E-11
CBC          2.87E-12
CJS          0.00E+00
BETAAC       5.50E+01
CBX          0.00E+00
FT           1.27E+08

 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C
******************************************************************************
  FREQ        VM($N_0003) VP($N_0003)

   1.000E+04   2.961E-01  -1.780E+02
```

Figure 8.57 Output file for the network of Figure 8.56.

cuits at 10 kHz. If we felt there was a transient phase between energizing the network and reaching a steady-state response, the **No-Print Delay** could be used to effectively eliminate this period of time. The last choice of **Step Ceiling** sets a maximum time period between response calculations for the system, which we will set at 1 μs. The time between calculations will be adjusted internally by the software package to ensure sufficient data at times when the response may change faster than usual. However, they will never be separated by a time period greater than that set by the **Step Ceiling.**

After **Simulation,** a **MicroSim Probe** screen will appear showing only the horizontal scale from 0 to 500 μs as specified in the **Transient** dialog box. To obtain a waveform, one can either choose **Trace** on the menu bar or the **Trace** icon (red pattern on a black axis). If the **Trace** on the menu bar is chosen, one must follow with **Add,** and the **Add Traces** dialog box will appear. Using the icon results in the dialog box immediately. Now one must choose the waveform to be displayed from the list of **Simulation Output Variables.** Since we want the collector-to-emitter voltage of the transistor, **V(Q1:c)**—an option under **Alias** names—will be chosen, followed by an **OK.** The result is the waveform of Fig. 8.58, with the waveform riding on the

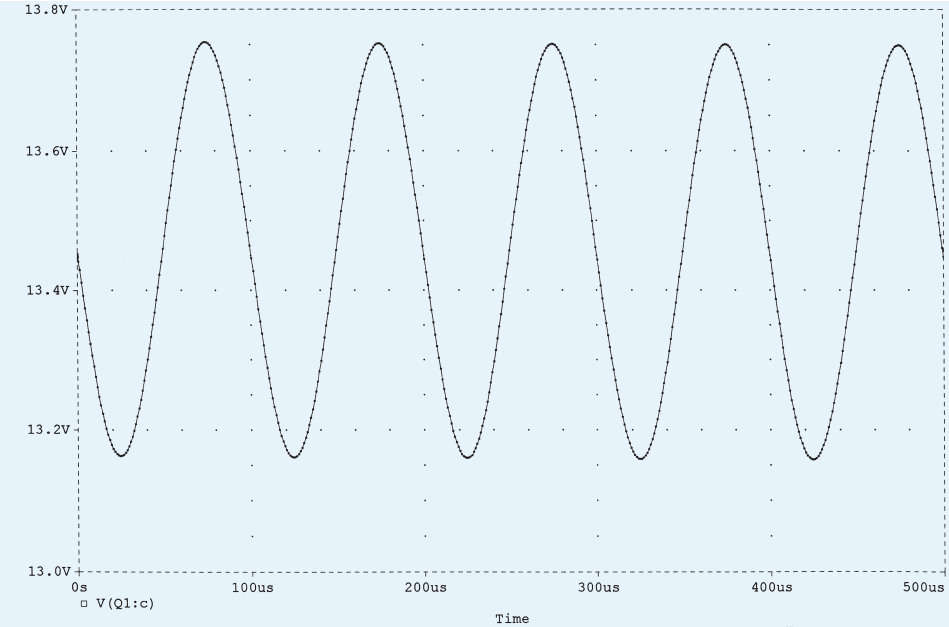


Figure 8.58 Voltage v_c for the network of Figure 8.56.

dc level of 13.45 V. The range of the vertical axis was automatically chosen by the computer. Five full cycles of the output waveform are displayed (as we expected) with 100 data points for each cycle. If you would like to see the data points (as shown in Fig. 8.58), simply turn to **Tools-Options-Probe Options** and choose **Mark Data Points.** Click **OK,** and the data points will appear. Using the scale of the graph, the peak-to-peak value of the curve is approximately 13.76 V − 13.16 V = 0.6 V = 600 mV, resulting in a peak value of 300 mV. Since a 1-mV signal was applied, the gain is 300, or very close to the values displayed above.

If a comparison is to be made between the input and output voltages on the same graph, the **Add Y-Axis** option under **Plot** can be chosen. After it is triggered, choose

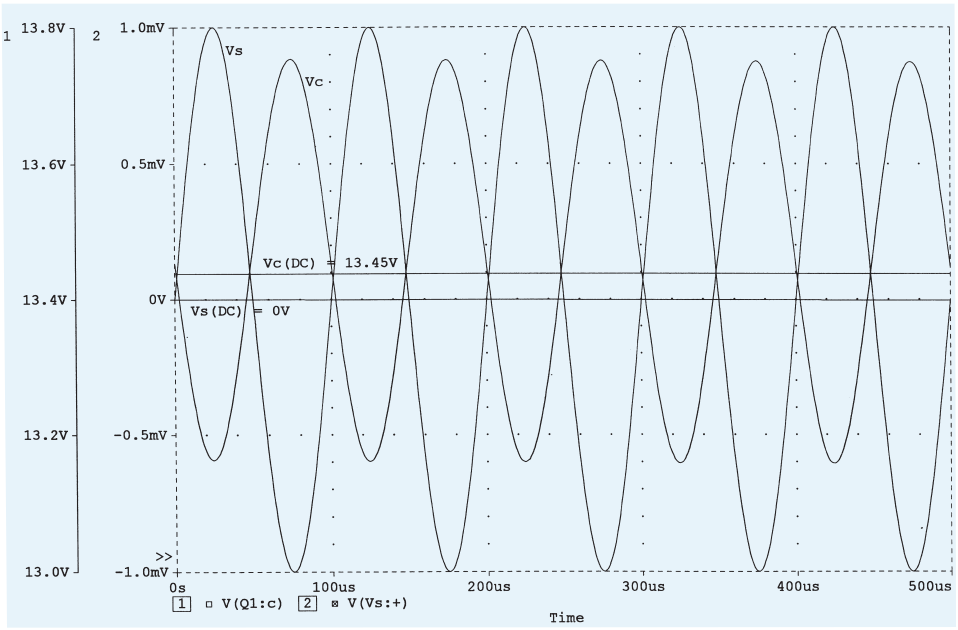


Figure 8.59 The voltages v_c and v_s for the network of Figure 8.56.

the **Add Trace** icon and select **V(Vs:+).** The result is that both waveforms will appear on the same screen, each with their own vertical scale. Labels can be added to the waveforms as shown in Fig. 8.59 using **Tools-Label-Text.** A **Text Label** dialog box will appear, in which the desired text can be entered. Click **OK,** and it can be placed with the mouse in any location on the graph. Lines can also be added with **Tools-Label-Line.** A pencil will appear, which can be used to draw the line with a left-click at the starting point and another click when the line is in place. Each plot

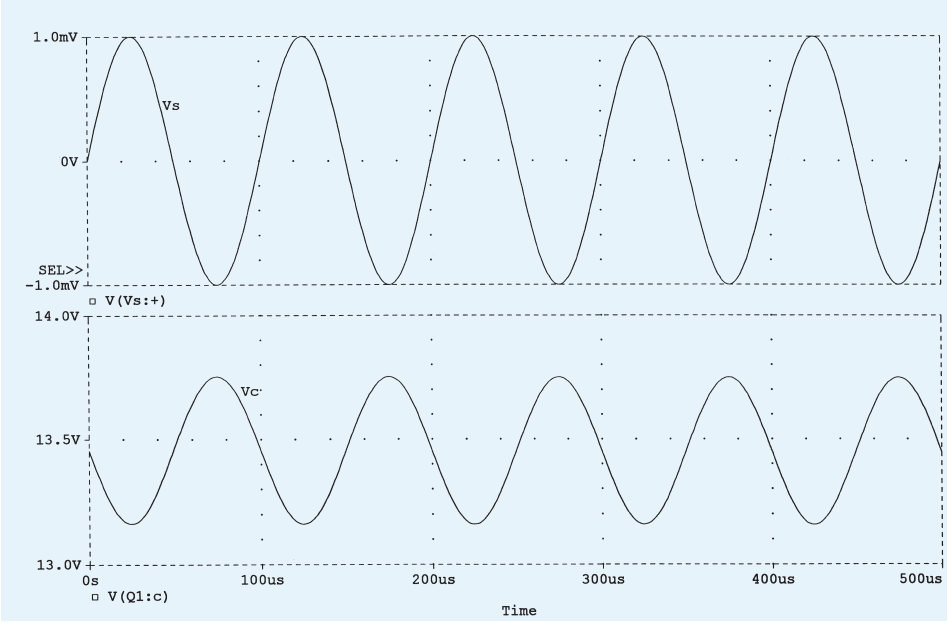


Figure 8.60 Two separate plots of v_c and v_s in Figure 8.56.

can be printed with **File-Print-Copies-OK.**

If two separate graphs are preferred, we can choose the **Plot** option and select **Add Plot** after **V** has been displayed. Upon selection, another graph will appear, waiting for the next choice. The sequence **Trace-Add-V(Vs:+)** will then result in the graphs of Fig. 8.60. The labels **Vs** and **Vc** were added using the **Tools** option. If further operations are to be performed on either graph, the **SEL′+** defines the active plot.

The last waveform of this section will demonstrate the use of the **Cursor** option that can be called up using the **Tools** menu choice or the **Cursor Point** icon (having a graph with an arrow drawn from the graph to the vertical axis). The sequence **Tools-Cursor-Display** will result in a line at the dc level of 13.453 V, as shown in the dialog box at the bottom right of the graph of Fig. 8.61. Left-clicking on the mouse once will result in a horizontal and vertical line intersecting at some point on the curve. By clicking on the vertical line and holding it down, the vertical line and corresponding horizontal line (on the graph) can be moved across the waveform. At each point, the vertical and horizontal intersections will appear in the dialog box. If moved to the first peak value, **A1** will be at 13.754 V and 74.825 μs. By right-clicking on the mouse, a second intersection, defined by **A2,** appears, which also has its location registered in the dialog box. These intersecting lines are moved by holding down

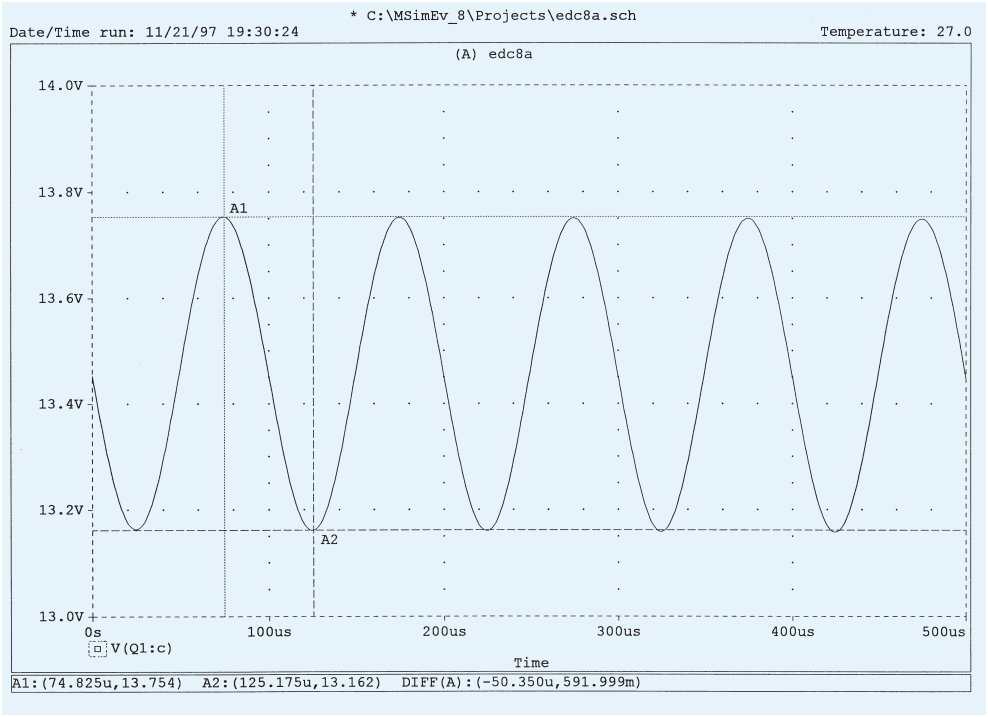


Figure 8.61 Demonstrating the use of cursors to read specific points on a plot.

the right side of the mouse. The remaining information on the third line of the box is the difference between the two intersections on the two axis. If **A2** is set at the bottom of the waveform as shown in Fig. 8.61, it will read 13.162 V at 125.17 μs, resulting in a difference between the two of 591.999 mV, or 0.592 V vertically and 50.35 μs horizontally. This is as expected, because the peak-to-peak value matches the 2×0.296 V = 0.592 V obtained earlier. The time interval is essentially 1/4 of the total period (200 μs) of the waveform. The labels **A1** and **A2** were added using the **Tools-Label-Text** sequence or the **ABC** text icon.

The peak and minimum values for the graph of Fig. 8.61 can also be found using the icons appearing in the top right region of the menu bar. Once the desired wave-

form is obtained and the sequence **Tools-Cursor-Display** applied or the **Toggle cursor** icon (the icon in the center region of the menu bar with the black dashed axis and red curve passing through the origin) is chosen, the six icons to the right of the **Toggle cursor** icon will change to a color pattern indicating they are ready for use. Clicking on the icon with the intersection at the top will automatically place the **A1** intersection at the top of the curve. Clicking the next icon to the right will place the intersection at the bottom (trough) of the curve. The next icon will place the intersection at the steepest slope and the next at the minimum value (matching the trough value).

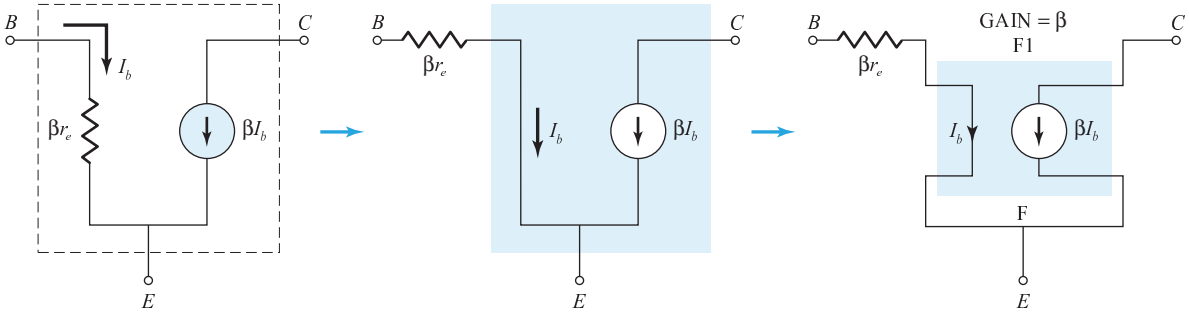


Figure 8.62 Using a controlled source to represent the transistor of Figure 8.56.

Voltage-Divider Configuration—Controlled Source Substitution

The results obtained for any analysis using the transistors provided in the software package will always be different from those obtained with an equivalent model that only includes the effect of beta and r_e. This was demonstrated for the network of Fig. 8.56. If a solution is desired that is limited to the approximate model, then the transistor must be represented by a model such as appearing in Fig. 8.62.

For Example 8.2, β is 90, with $\beta r_e = 1.66\ \text{k}\Omega$. The current controlled current source (**CCCS**) is found in the **ANALOG.slb** library as **Part F.** When you click on **F,** the **Description** above will read **Current-controlled current source.** After **OK-Place & Close,** the graphical symbol for the **CCCS** will appear on the screen as shown in Fig. 8.63. Since βr_e does not appear within the basic structure of the **CCCS,** it must be added in series with the controlling current indicated by the arrow on the

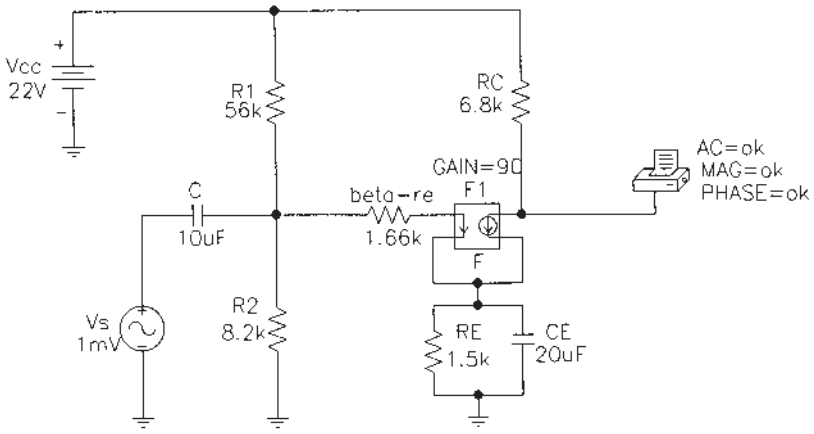


Figure 8.63 Substituting the controlled source of Figure 8.62 for the transistor of Figure 8.56.

§ 8.2 Common-Emitter Fixed-Bias Configuration

1. For the network of Fig. 8.64:
(a) Determine Z_i and Z_o.
(b) Find A_v and A_i.
(c) Repeat part (a) with $r_o = 20\ \text{k}\Omega$.
(d) Repeat part (b) with $r_o = 20\ \text{k}\Omega$.

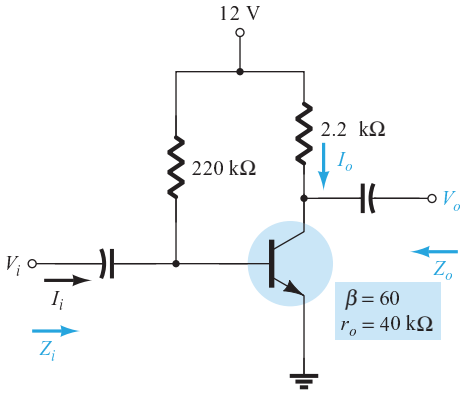


Figure 8.64 Problems 1 and 21

2. For the network of Fig. 8.65, determine V_{CC} for a voltage gain of $A_v = -200$.

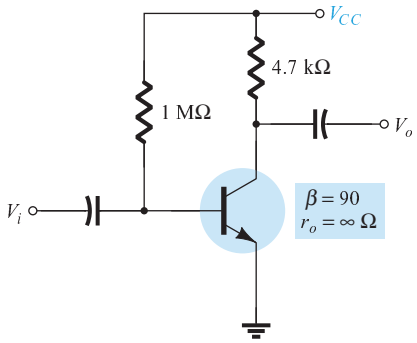


Figure 8.65 Problem 2

* **3.** For the network of Fig. 8.66:
(a) Calculate I_B, I_C, and r_e.
(b) Determine Z_i and Z_o.
(c) Calculate A_v and A_i.
(d) Determine the effect of $r_o = 30\ \text{k}\Omega$ on A_v and A_i.

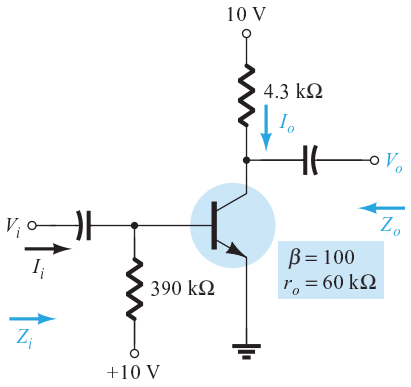


Figure 8.66 Problem 3

§ 8.3 Voltage-Divider Bias

4. For the network of Fig. 8.67:
(a) Determine r_e.
(b) Calculate Z_i and Z_o.
(c) Find A_v and A_i.
(d) Repeat parts (b) and (c) with $r_o = 25\ \text{k}\Omega$.

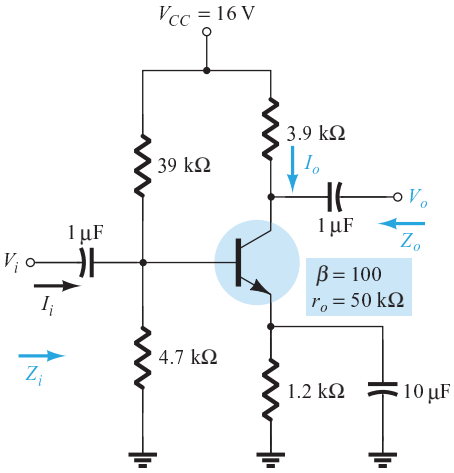


Figure 8.67 Problem 4

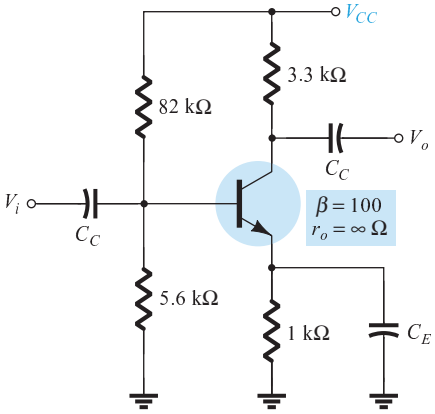


Figure 8.68 Problem 5

5. Determine V_{CC} for the network of Fig. 8.68 if $A_v = -160$ and $r_o = 100\ \text{k}\Omega$.

6. For the network of Fig. 8.69:
(a) Determine r_e.
(b) Calculate V_B and V_C.
(c) Determine Z_i and $A_v = V_o/V_i$.

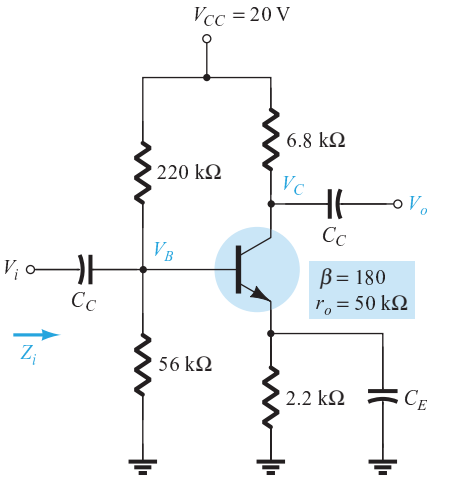


Figure 8.69 Problem 6

§ 8.4 CE Emitter-Bias Configuration

7. For the network of Fig. 8.70:
(a) Determine r_e.
(b) Find Z_i and Z_o.
(c) Calculate A_v and A_i.
(d) Repeat parts (b) and (c) with $r_o = 20\ \text{k}\Omega$.

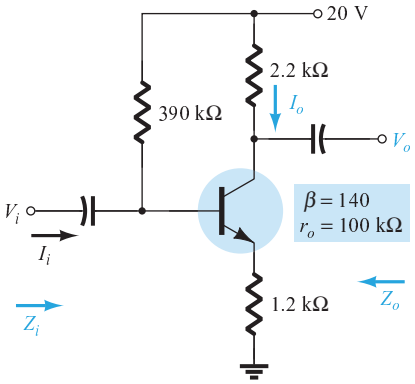


Figure 8.70 Problems 7 and 9

8. For the network of Fig. 8.71, determine R_E and R_B if $A_v = -10$ and $r_e = 3.8\ \Omega$. Assume that $Z_b = \beta R_E$.

9. Repeat Problem 7 with R_E bypassed. Compare results.

* 10. For the network of Fig. 8.72:
   (a) Determine r_e.
   (b) Find Z_i and A_v.
   (c) Calculate A_i.

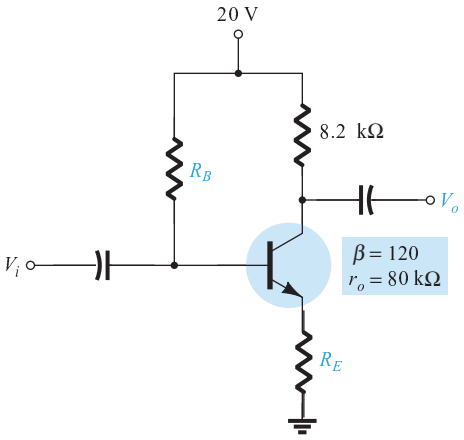


Figure 8.71 Problem 8

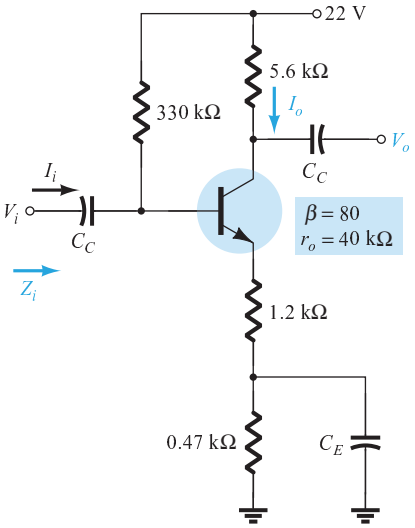


Figure 8.72 Problem 10

§ 8.5 Emitter-Follower Configuration

11. For the network of Fig. 8.73:
   (a) Determine r_e and βr_e.
   (b) Find Z_i and Z_o.
   (c) Calculate A_v and A_i.

* 12. For the network of Fig. 8.74:
   (a) Determine Z_i and Z_o.
   (b) Find A_v.
   (c) Calculate V_o if $V_i = 1$ mV.

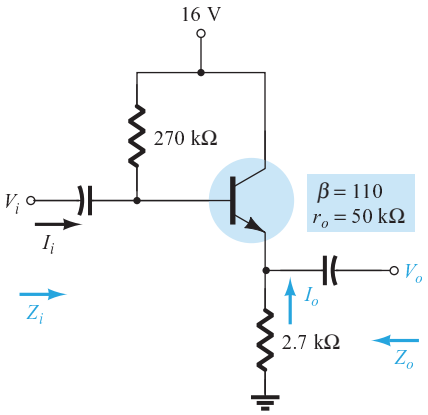


Figure 8.73 Problem 11

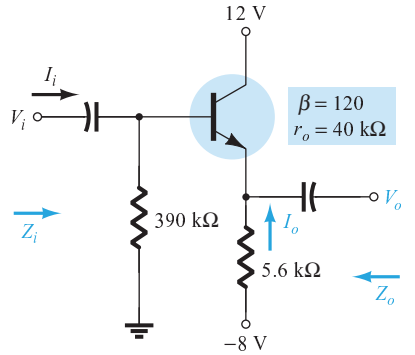


Figure 8.74 Problem 12

* **13.** For the network of Fig. 8.75:
(a) Calculate I_B and I_C.
(b) Determine r_e.
(c) Determine Z_i and Z_o.
(d) Find A_v and A_i.

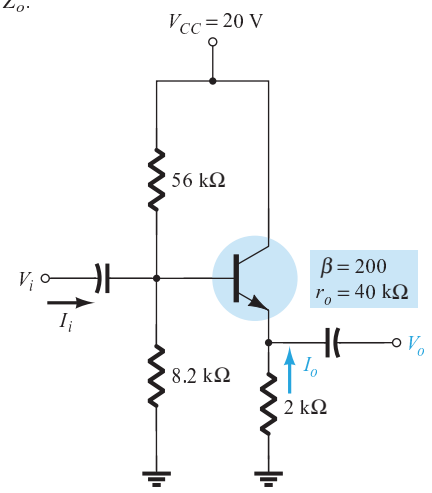


Figure 8.75 Problem 13

§ 8.6 Common-Base Configuration

14. For the common-base configuration of Fig. 8.76:
(a) Determine r_e.
(b) Find Z_i and Z_o.
(c) Calculate A_v and A_i.

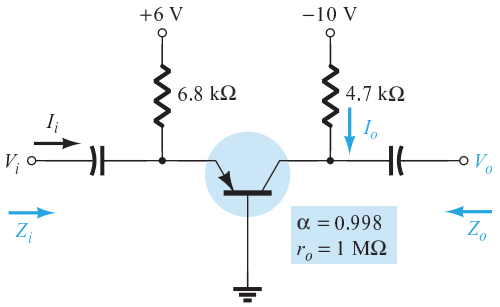


Figure 8.76 Problem 14

* **15.** For the network of Fig. 8.77, determine A_v and A_i.

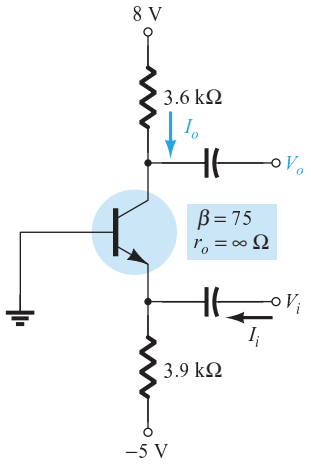


Figure 8.77 Problem 15

§ 8.7 Collector Feedback Configuration

16. For the collector FB configuration of Fig. 8.78:
(a) Determine r_e.
(b) Find Z_i and Z_o.
(c) Calculate A_v and A_i.

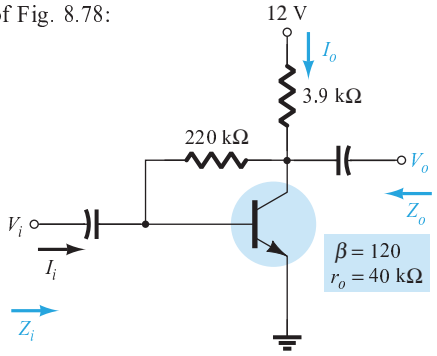


Figure 8.78 Problem 16

* **17.** Given $r_e = 10\ \Omega$, $\beta = 200$, $A_v = -160$, and $A_i = 19$ for the network of Fig. 8.79, determine R_C, R_F, and V_{CC}.

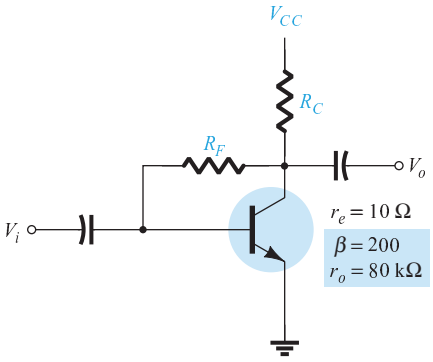


Figure 8.79 Problem 17

* **18.** For the network of Fig. 8.30:
(a) Derive the approximate equation for A_v.
(b) Derive the approximate equation for A_i.
(c) Derive the approximate equations for Z_i and Z_o.
(d) Given $R_C = 2.2$ kΩ, $R_F = 120$ kΩ, $R_E = 1.2$ kΩ, $\beta = 90$, and $V_{CC} = 10$ V, calculate the magnitudes of A_v, A_i, Z_i, and Z_o using the equations of parts (a) through (c).

§ 8.8 Collector DC Feedback Configuration

19. For the network of Fig. 8.80:
(a) Determine Z_i and Z_o.
(b) Find A_v and A_i.

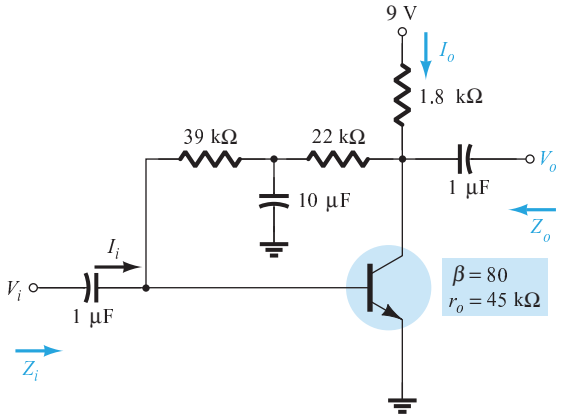


Figure 8.80 Problem 19

§ 8.9 Approximate Hybrid Equivalent Circuit

20. (a) Given $\beta = 120$, $r_e = 4.5\ \Omega$, and $r_o = 40\ \text{k}\Omega$, sketch the approximate hybrid equivalent circuit.

(b) Given $h_{ie} = 1\ \text{k}\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 90$, and $h_{oe} = 20\ \mu\text{S}$, sketch the r_e model.

21. For the network of Problem 1:

(a) Determine r_e.

(b) Find h_{fe} and h_{ie}.

(c) Find Z_i and Z_o using the hybrid parameters.

(d) Calculate A_v and A_i using the hybrid parameters.

(e) Determine Z_i and Z_o if $h_{oe} = 50\ \mu\text{S}$.

(f) Determine A_v and A_i if $h_{oe} = 50\ \mu\text{S}$.

(g) Compare the solutions above with those of Problem 1. (Note: The solutions are available in Appendix E if Problem 1 was not performed.)

22. For the network of Fig. 8.81:

(a) Determine Z_i and Z_o.

(b) Calculate A_v and A_i.

(c) Determine r_e and compare βr_e to h_{ie}.

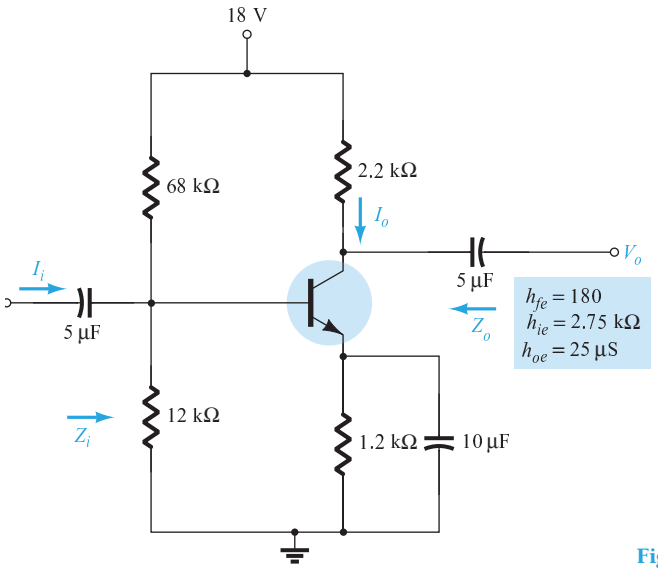


Figure 8.81 Problems 22 and 24

* **23.** For the common-base network of Fig. 8.82:

(a) Determine Z_i and Z_o.

(b) Calculate A_v and A_i.

(c) Determine α, β, r_e, and r_o.

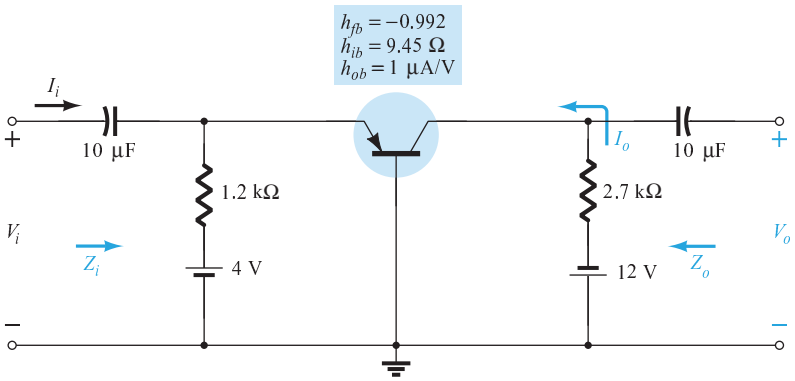


Figure 8.82 Problem 23

§ 8.10 Complete Hybrid Equivalent Model

* **24.** Repeat parts (a) and (b) of Problem 22 with $h_{re} = 2 \times 10^{-4}$ and compare results.

* **25.** For the network of Fig. 8.83, determine:
  (a) Z_i.
  (b) A_v.
  (c) $A_i = I_o/I_i$.
  (d) Z_o.

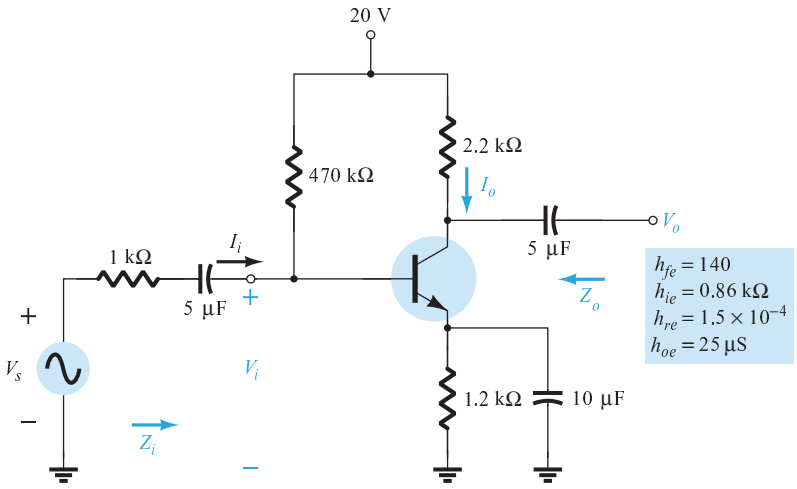


Figure 8.83 Problem 25

* **26.** For the common-base amplifier of Fig. 8.84, determine:
  (a) Z_i.
  (b) A_i.
  (c) A_v.
  (d) Z_o.

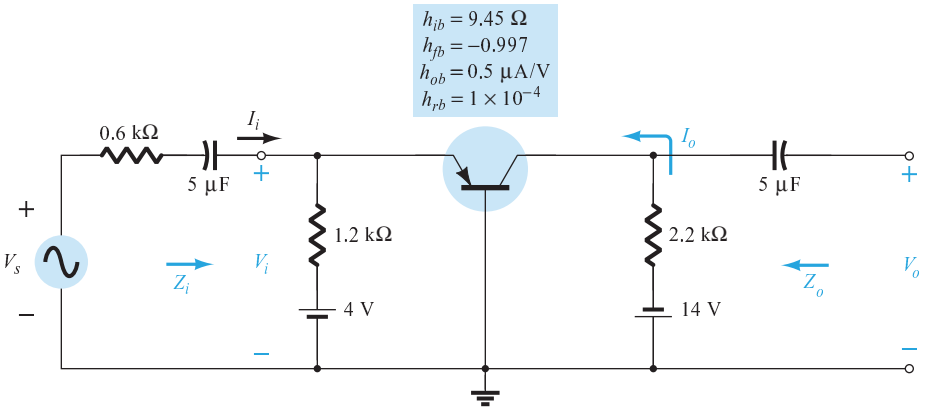


Figure 8.84 Problem 26

§ 8.12 Troubleshooting

* **27.** Given the network of Fig. 8.85:
  (a) Determine if the system is operating properly based on the voltage-divider bias levels and expected waveforms for v_o and v_E.
  (b) Determine the reason for the dc levels obtained and why the waveform for v_o was obtained.

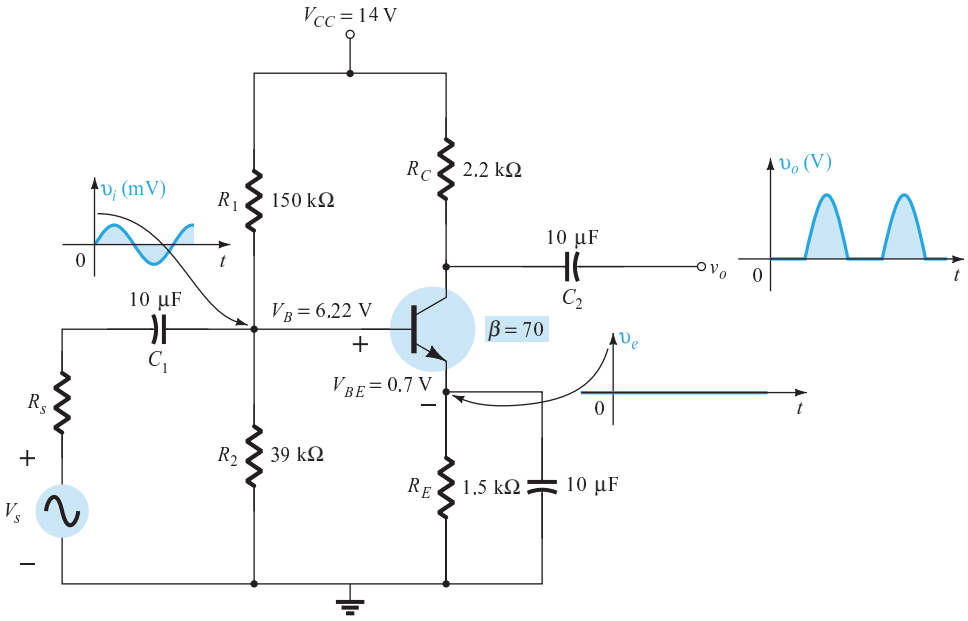


Figure 8.85 Problem 27

§ 8.13 PSpice Windows

28. Using PSpice Windows, determine the gain for the network of Fig. 8.6. Use Probe to display the input and output waveforms.

29. Using PSpice Windows, determine the gain for the network of Fig. 8.13. Use Probe to display the input and output waveforms.

30. Using PSpice Windows, determine the gain for the network of Fig. 8.25. Use Probe to display the input and output waveforms.

*Please Note: Asterisks indicate more difficult problems.

g_m

CHAPTER

9 FET Small-Signal Analysis

9.1 INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has a much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor β (beta), the FET has a transconductance factor, g_m.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications. Table 9.1, located at the end of the chapter, provides a summary of FET small-signal amplifier circuits and related formulas.

While the common-source configuration is the most popular providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity. While the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

FET ac amplifier networks can also be analyzed using computer software. Using PSpice, one can perform a dc analysis to obtain the circuit bias conditions and an ac analysis to determine the small-signal voltage gain. Using PSpice transistor models,

one can analyze the circuit using specific transistor models. On the other hand, one can develop a program using a language such as BASIC that can perform both the dc and ac analyses and provide the results in a very special format.

9.2 FET SMALL-SIGNAL MODEL

The ac analysis of an FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of an FET.

Recall from Chapter 6 that a dc gate-to-source voltage controlled the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$. The *change* in collector current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m \, \Delta V_{GS} \tag{9.1}$$

The prefix *trans-* in the terminology applied to g_m reveals that it establishes a relationship between an output and input quantity. The root word *conductance* was chosen because g_m is determined by a voltage-to-current ratio similar to the ratio that defines the conductance of a resistor $G = 1/R = I/V$.

Solving for g_m in Eq. (9.1), we have:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \tag{9.2}$$

Graphical Determination of g_m

If we now examine the transfer characteristics of Fig. 9.1, we find that g_m is actually the slope of the characteristics at the point of operation. That is,

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \tag{9.3}$$

Following the curvature of the transfer characteristics, it is reasonably clear that the slope and, therefore, g_m increase as we progress from V_P to I_{DSS}. Or, in other words, as V_{GS} approaches 0 V, the magnitude of g_m increases.

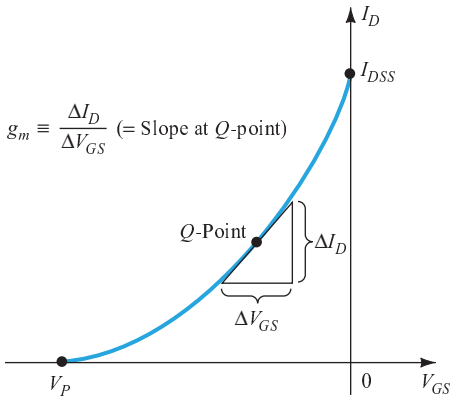


Figure 9.1 Definition of g_m using transfer characteristic.

Equation (9.2) reveals that g_m can be determined at any Q-point on the transfer characteristics by simply choosing a finite increment in V_{GS} (or in I_D) about the Q-point and then finding the corresponding change in I_D (or V_{GS}, respectively). The resulting changes in each quantity are then substituted in Eq. (9.2) to determine g_m.

EXAMPLE 9.1

Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V at the following dc bias points:
(a) $V_{GS} = -0.5$ V.
(b) $V_{GS} = -1.5$ V.
(c) $V_{GS} = -2.5$ V.

Solution

The transfer characteristics are generated as Fig. 9.2 using the procedure defined in Chapter 6. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for V_{GS} to reflect a variation to either side of each Q-point. Equation (9.2) is then applied to determine g_m.

(a) $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{2.1 \text{ mA}}{0.6 \text{ V}} = \mathbf{3.5\ mS}$$

(b) $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8 \text{ mA}}{0.7 \text{ V}} \cong \mathbf{2.57\ mS}$$

(c) $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5 \text{ mA}}{1.0 \text{ V}} = \mathbf{1.5\ mS}$$

Note the decrease in g_m as V_{GS} approaches V_P.

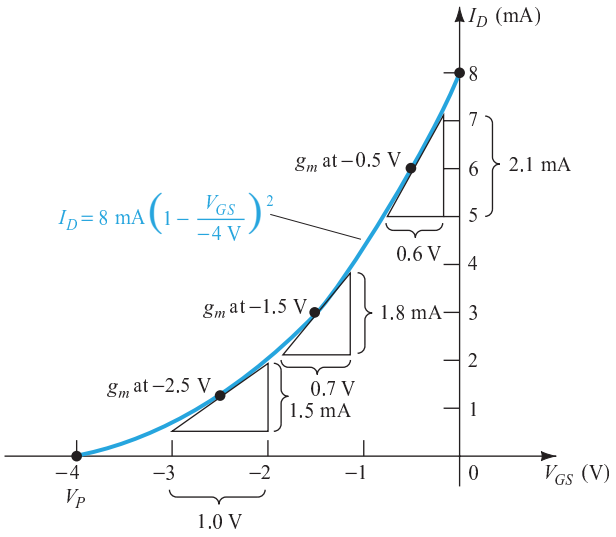


Figure 9.2 Calculating g_m at various bias points.

Mathematical Definition of g_m

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined. Naturally, the larger the graph the better the accuracy, but this can then become a cumbersome

problem. An alternative approach to determining g_m employs the approach used to find the ac resistance of a diode in Chapter 1, where it was stated that:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, an equation for g_m can be derived as follows:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{Q\text{-pt.}} = \frac{dI_D}{dV_{GS}}\bigg|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{9.4}$$

where $|V_P|$ denotes magnitude only to ensure a positive value for g_m.

It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into Eq. (9.4) will result in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}} \tag{9.5}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (9.4) then becomes

$$\boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{9.6}$$

EXAMPLE 9.2

For the JFET having the transfer characteristics of Example 9.1:
(a) Find the maximum value of g_m.
(b) Find the value of g_m at each operating point of Example 9.1 using Eq. (9.6) and compare with the graphical results.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\text{ mS}}$ (maximum possible value of g_m)

(b) At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\text{ mS}}$$ (versus 3.5 mS graphically)

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\ mS} \quad \text{(versus 2.57 mS graphically)}$$

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\ mS} \quad \text{(versus 1.5 mS graphically)}$$

The results of Example 9.2 are certainly sufficiently close to validate Eq. (9.4) through (9.6) for future use when g_m is required.

On specification sheets, g_m is provided as y_{fs} where y indicates it is part of an admittance equivalent circuit. The f signifies *f*orward transfer parameter, and the s reveals that it is connected to the source terminal.

In equation form,

$$\boxed{g_m = y_{fs}} \tag{9.7}$$

For the JFET of Fig. 5.18, y_{fs} ranges from 1000 to 5000 μS or 1 to 5 mS.

Plotting g_m vs. V_{GS}

Since the factor $\left(1 - \frac{V_{GS}}{V_P}\right)$ of Eq. (9.6) is less than 1 for any value of V_{GS} other than 0 V, the magnitude of g_m will decrease as V_{GS} approaches V_P and the ratio $\frac{V_{GS}}{V_P}$ increases in magnitude. At $V_{GS} = V_P$, $g_m = g_{m0}(1 - 1) = 0$. Equation (9.6) defines a straight line with a minimum value of 0 and a maximum value of g_m as shown by the plot of Fig. 9.3.

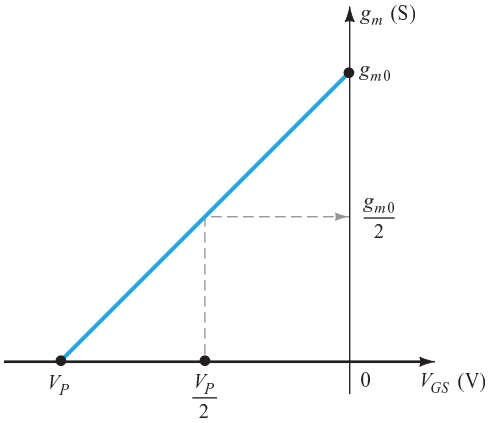


Figure 9.3 Plot of g_m vs. V_{GS}.

Figure 9.3 also reveals that when V_{GS} is one-half the pinch-off value, g_m will be one-half the maximum value.

EXAMPLE 9.3

Plot g_m vs. V_{GS} for the JFET of examples 9.1 and 9.2.

Solution

Note Fig. 9.4.

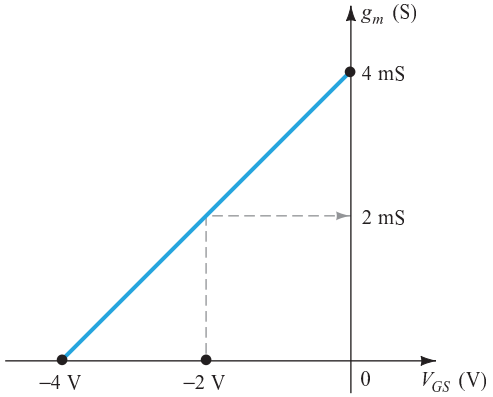


Figure 9.4 Plot of g_m vs. V_{GS} for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ V.

Impact of I_D on g_m

A mathematical relationship between g_m and the dc bias current I_D can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \tag{9.8}$$

Substituting Eq. (9.8) into Eq. (9.6) will result in

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \tag{9.9}$$

Using Eq. (9.9) to determine g_m for a few specific values of I_D, the results are

(a) If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = \boldsymbol{g_{m0}}$$

(b) If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = \mathbf{0.707}\boldsymbol{g_{m0}}$$

(c) If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = \mathbf{0.5}\boldsymbol{g_{m0}}$$

EXAMPLE 9.4

Plot g_m vs. I_D for the JFET of Examples 9.1 through 9.3.

Solution

See Fig. 9.5.

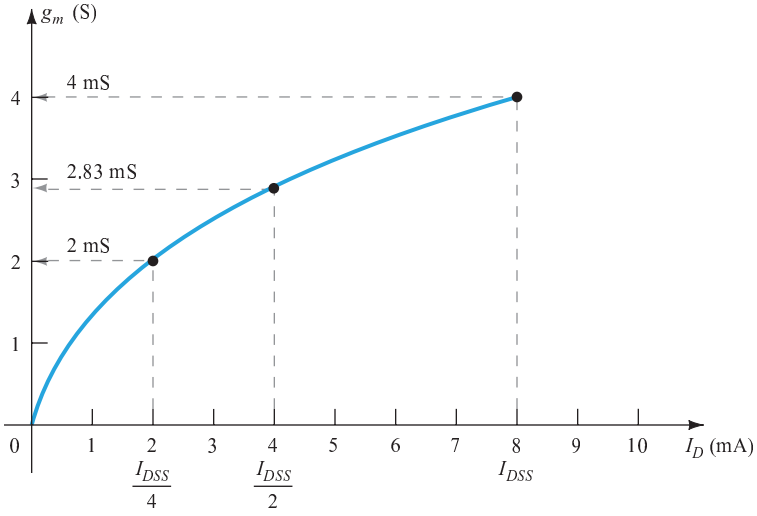


Figure 9.5 Plot of g_m vs. I_D for a JFET with $I_{DSS} = 8$ mA and $V_{GS} = -4$ V.

The plots of Examples 9.3 and 9.4 clearly reveal that the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D its maximum value of I_{DSS}.

FET Input Impedance Z_i

The input impedance of all commercially available FETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i \text{ (FET)} = \infty\ \Omega \tag{9.10}$$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, while a value of 10^{12} to $10^{15}\ \Omega$ is typical for MOSFETs.

FET Output Impedance Z_o

The output impedance of FETs is similar in magnitude to that of conventional BJTs. On FET specification sheets, the output impedance will typically appear as y_{os} with the units of μS. The parameter y_{os} is a component of an *admittance equivalent circuit,* with the subscript o signifying an *o*utput network parameter and s the terminal (source) to which it is attached in the model. For the JFET of Fig. 5.18, y_{os} has a range of 10 to 50 μS or 20 kΩ ($R = 1/G = 1/50\ \mu$S) to 100 kΩ ($R = 1/G = 1/10\ \mu$S).

In equation form,

$$Z_o \text{ (FET)} = r_d = \frac{1}{y_{os}} \tag{9.11}$$

The output impedance is defined on the characteristics of Fig. 9.6 as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater the output impedance. If perfectly horizontal, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

In equation form,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}} \tag{9.12}$$

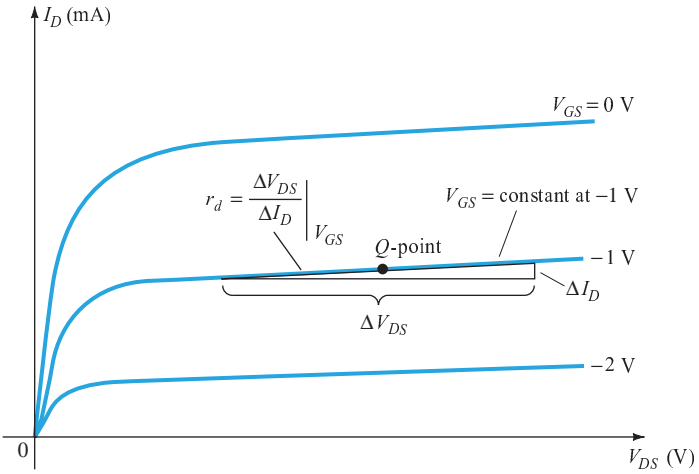


Figure 9.6 Definition of r_d using FET drain characteristics.

Note the requirement when applying Eq. (9.12) that the voltage V_{GS} remain constant when r_d is determined. This is accomplished by drawing a straight line approximating the V_{GS} line at the point of operation. A ΔV_{DS} or ΔI_D is then chosen and the other quantity measured off for use in the equation.

EXAMPLE 9.5

Determine the output impedance for the FET of Fig. 9.7 for $V_{GS} = 0$ V and $V_{GS} = -2$ V at $V_{DS} = 8$ V.

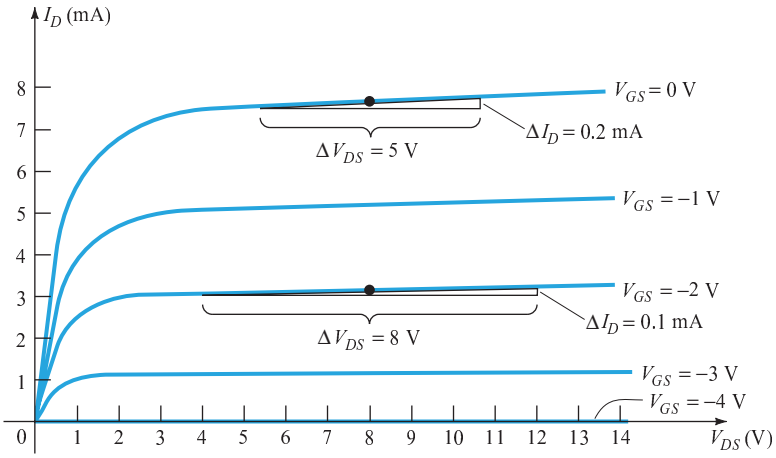


Figure 9.7 Drain characteristics used to calculate r_d in Example 9.5.

Solution

For $V_{GS} = 0$ V, a tangent line is drawn and ΔV_{DS} is chosen as 5 V, resulting in a ΔI_D of 0.2 mA. Substituting into Eq. (9.12),

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = \mathbf{25\ k\Omega}$$

For $V_{GS} = -2$ V, a tangent line is drawn and ΔV_{DS} is chosen as 8 V, resulting in a ΔI_D of 0.1 mA. Substituting into Eq. (9.12),

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = \mathbf{80\ k\Omega}$$

revealing that r_d does change from one operating region to another, with lower values typically occurring at lower levels of V_{GS} (closer to 0 V).

FET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the FET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 9.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

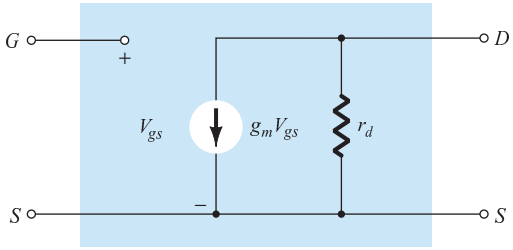


Figure 9.8 FET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate to source voltage is now represented by V_{gs} (lower-case subscripts) to distinguish it from dc levels. In addition, take note of the fact that the source is common to both input and output circuits while the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

In situations where r_d is ignored (assumed sufficiently large to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled device.

EXAMPLE 9.6

Given $y_{fs} = 3.8$ mS and $y_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution

$$g_m = y_{fs} = 3.8\text{ mS} \quad \text{and} \quad r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

resulting in the ac equivalent model of Fig. 9.9.

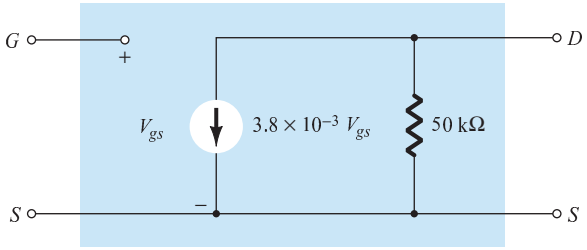


Figure 9.9 FET ac equivalent model for Example 9.6.

9.3 JFET FIXED-BIAS CONFIGURATION

Now that the FET equivalent circuit has been defined, a number of fundamental FET small-signal configurations will be investigated. The approach will parallel the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

The *fixed-bias* configuration of Fig. 9.10 includes the coupling capacitors C_1 and C_2 that isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

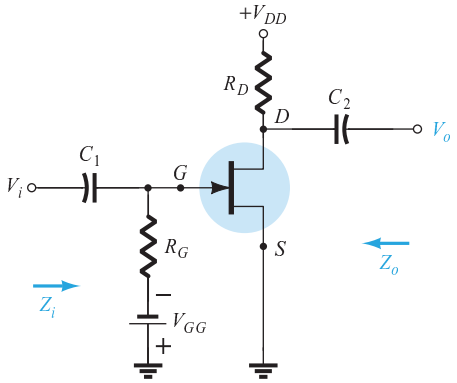


Figure 9.10 JFET fixed-bias configuration.

Once the level of g_m and r_d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 9.11. Note that both capacitors have the short-circuit equivalent because the reactance $X_C = 1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to zero volts by a short-circuit equivalent.

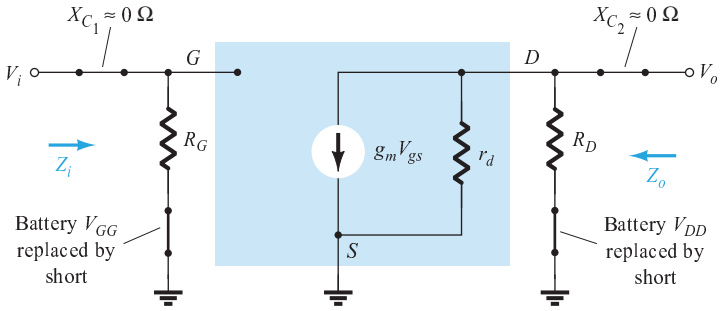


Figure 9.11 Substituting the JFET ac equivalent circuit unit into the network of Fig. 9.10.

The network of Fig. 9.11 is then carefully redrawn as shown in Fig. 9.12. Note the defined polarity of V_{gs}, which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across R_D by V_o.

***Z_i*:** Figure 9.12 clearly reveals that

$$Z_i = R_G \tag{9.13}$$

because of the open-circuit equivalence at the input terminals of the JFET.

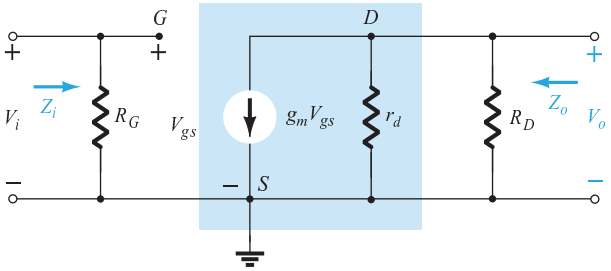


Figure 9.12 Redrawn network of Fig. 9.11.

Z_o: Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 9.13. The output impedance is

$$\boxed{Z_o = R_D \| r_d} \tag{9.14}$$

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{9.15}$$

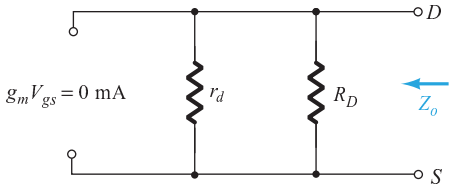


Figure 9.13 Determining Z_o.

A_v: Solving for V_o in Fig. 9.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i(r_d \| R_D)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{9.16}$$

If $r_d \geq 10R_D$:

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m R_D}_{r_d \geq 10R_D} \tag{9.17}$$

Phase Relationship: The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.

EXAMPLE 9.7

The fixed-bias configuration of Example 6.1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 9.14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

(a) Determine g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o.
(e) Determine the voltage gain A_v.
(f) Determine A_v ignoring the effects of r_d.

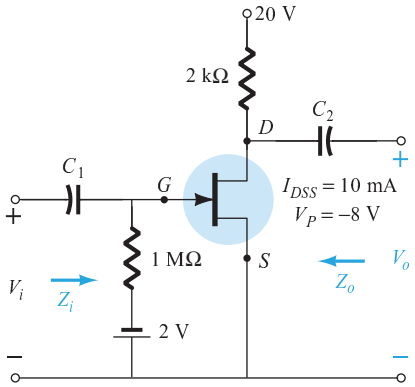


Figure 9.14 JFET configuration for Example 9.7.

Solution

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\ mS}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

(e) $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

(f) $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D resulted in a difference of 8% in solution.

9.4 JFET SELF-BIAS CONFIGURATION

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 9.15 requires only one dc supply to establish the desired operating point.

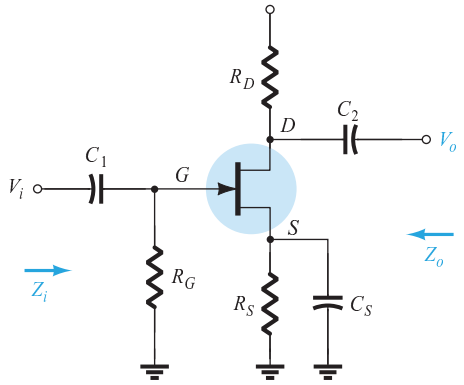


Figure 9.15 Self-bias JFET configuration.

The capacitor C_S across the source resistance assumes its short-circuit equivalence for dc, allowing R_S to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and "short circuits" the effects of R_S. If left in the ac, gain will be reduced as will be shown in the paragraphs to follow.

The JFET equivalent circuit is established in Fig. 9.16 and carefully redrawn in Fig. 9.17.

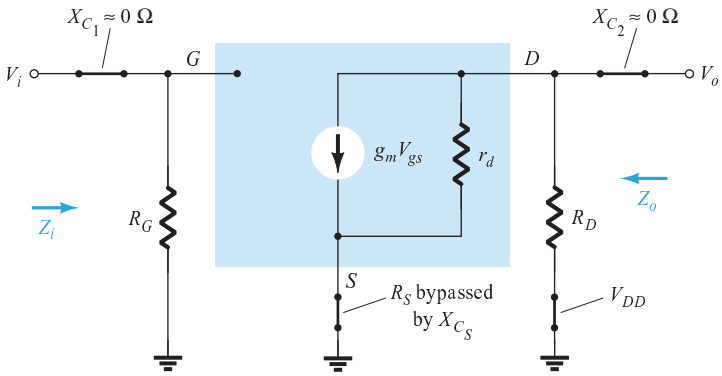


Figure 9.16 Network of Fig. 9.15 following the substitution of the JFET ac equivalent circuit.

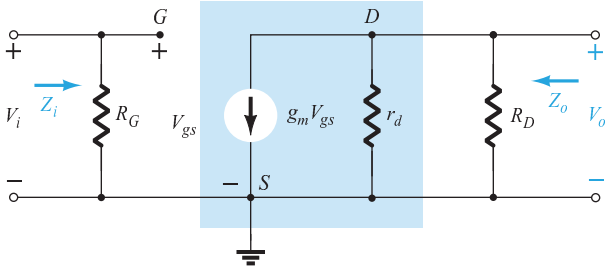


Figure 9.17 Redrawn network of Fig. 9.16.

Since the resulting configuration is the same as appearing in Fig. 9.12, the resulting equations Z_i, Z_o, and A_v will be the same.

Z_i:

$$Z_i = R_G \tag{9.18}$$

$\boldsymbol{Z_o}$:

$$Z_o = r_d \| R_D \tag{9.19}$$

If $r_d \geq 10R_D$,

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D} \tag{9.20}$$

$\boldsymbol{A_v}$:

$$A_v = -g_m(r_d \| R_D) \tag{9.21}$$

If $r_d \geq 10R_D$,

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D} \tag{9.22}$$

Phase relationship: The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

Unbypassed R_S

If C_S is removed from Fig 9.15, the resistor R_S will be part of the ac equivalent circuit as shown in Fig. 9.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Z_i, Z_o, and A_v, one must simply be very careful with notation and defined polarities and direction. Initially, the resistance r_d will be left out of the analysis to form a basis for comparison.

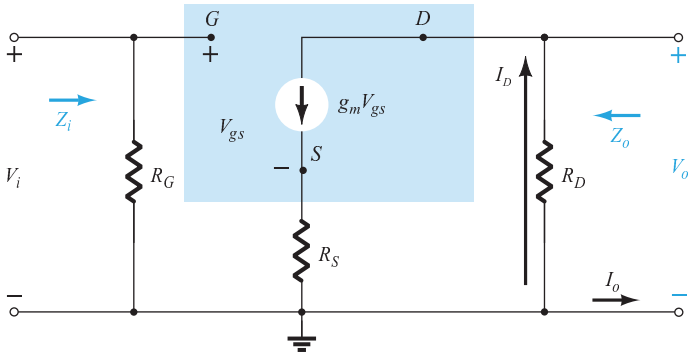


Figure 9.18 Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

$\boldsymbol{Z_i}$: Due to the open-circuit condition between the gate and output network, the input remains the following:

$$Z_i = R_G \tag{9.23}$$

$\boldsymbol{Z_o}$: The output impedance is defined by

$$Z_o = \frac{V_o}{I_o}\bigg|_{V_i = 0}$$

Setting $V_i = 0$ V in Fig. 9.18 will result in the gate terminal being at ground potential (0 V). The voltage across R_G is then 0 V, and R_G has been effectively "shorted out" of the picture.

Applying Kirchhoff's current law will result in:

$$I_o + I_D = g_m V_{gs}$$

with $$V_{gs} = -(I_o + I_D)R_S$$

so that $$I_o + I_D = -g_m\,(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

or $$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

and $$I_o = -I_D$$ (the controlled current source $g_m V_{gs} = 0$ A for the applied conditions)

Since $$V_o = -I_D R_D$$

then $$V_o = -(-I_o)R_D = I_o R_D$$

and $$\boxed{Z_o = \frac{V_o}{I_o} = R_D}\Big|_{r_d = \infty\Omega} \qquad (9.24)$$

If r_d is included in the network, the equivalent will appear as shown in Fig. 9.19.

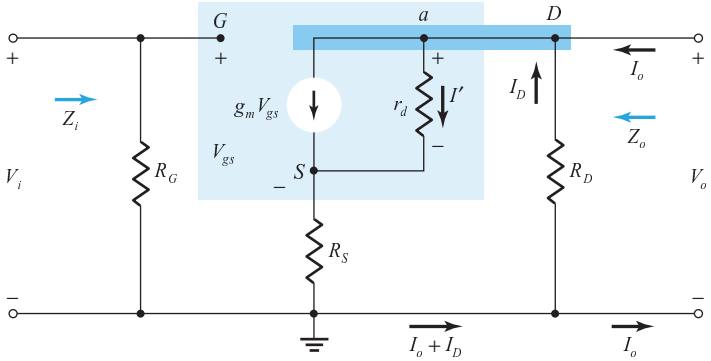


Figure 9.19 Including the effects of r_d in the self-bias JFET configuration.

Since $$Z_o = \frac{V_o}{I_o}\bigg|_{V_i = 0\text{ V}} = -\frac{I_D R_D}{I_o}$$

we should try to find an expression for I_o in terms of I_D.

Applying Kirchhoff's current law:

$$I_o = g_m V_{gs} + I_{r_d} - I_D$$

but $$V_{r_d} = V_o + V_{gs}$$

and $$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

or $$I_o = \left(g_m + \frac{1}{r_d}\right) V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

Now, $$V_{gs} = -(I_D + I_o)\,R_S$$

so that $$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o)\,R_S - \frac{I_D R_D}{r_d} - I_D$$

with the result that $$I_o\left[1 + g_m R_s + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

or $$I_o = \frac{-I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_S + \frac{R_S}{r_d}}$$

and
$$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{\dfrac{-I_D\left(1 + g_m R_s + \dfrac{R_s}{r_d} + \dfrac{R_D}{r_d}\right)}{1 + g_m R_S + \dfrac{R_S}{r_d}}}$$

and finally,
$$\boxed{Z_o = \frac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]} R_D} \qquad (9.25a)$$

For $r_d \geq 10\, R_D$, $\left(1 + g_m R_S + \dfrac{R_S}{r_d}\right) >> \dfrac{R_D}{r_d}$ and $1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}$ $\cong 1 + g_m R_S + \dfrac{R_S}{r_d}$ and

$$\boxed{Z_o = R_D}_{r_d \geq 10R_D} \qquad (9.25b)$$

A_v: For the network of Fig. 9.19, an application of Kirchhoff's voltage law on the input circuit will result in

$$V_i - V_{gs} - V_{R_S} = 0$$
$$V_{gs} = V_i - I_D R_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_o - V_{R_S}$$

and
$$I' = \frac{V_o - V_{R_S}}{r_d}$$

so that an application of Kirchhoff's current law will result in

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{R_S} we have

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

so that
$$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

or
$$I_D = \frac{g_m V_i}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

and
$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}} \qquad (9.26)$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S} \qquad (9.27)$$

$r_d \geq 10(R_D + R_S)$

Phase Relationship: The negative sign in Eq. (9.26) again reveals that a 180° phase shift will exist between V_i and V_o.

EXAMPLE 9.8

The self-bias configuration of Example 6.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 9.20 with an applied signal V_i. The value of y_{os} is given as 20 μS.

(a) Determine g_m.
(b) Find r_d.
(c) Find Z_i.
(d) Calculate Z_o with and without the effects of r_d. Compare the results.
(e) Calculate A_v with and without the effects of r_d. Compare the results.

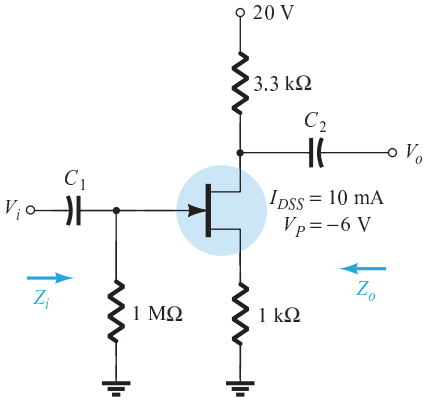


Figure 9.20 Network for Example 9.8.

Solution

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\ mS}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) With r_d:

$$r_d = 50\text{ k}\Omega > 10\ R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\ \Omega$

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

(e) With r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

Without r_d:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\ \text{mS})(3.3\ \text{k}\Omega)}{1 + (1.51\ \text{mS})(1\ \text{k}\Omega)} = \mathbf{-1.98}$$

As above, the effect of r_d was minimal because the condition $r_d \geq 10(R_D + R_S)$ was satisfied.

Note also that the typical gain of a JFET amplifier is less than that generally encountered for BJTs of similar configurations. Keep in mind, however, that Z_i is magnitudes greater than the typical Z_i of a BJT, which will have a very positive effect on the overall gain of a system.

9.5 JFET VOLTAGE-DIVIDER CONFIGURATION

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 9.21.

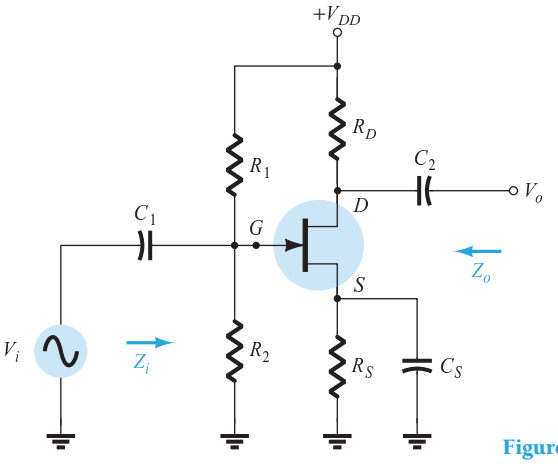


Figure 9.21 JFET voltage-divider configuration.

Substituting the ac equivalent model for the JFET will result in the configuration of Fig. 9.22. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D. Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 9.23. R_D can also be brought down to ground but in the output circuit across r_d. The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

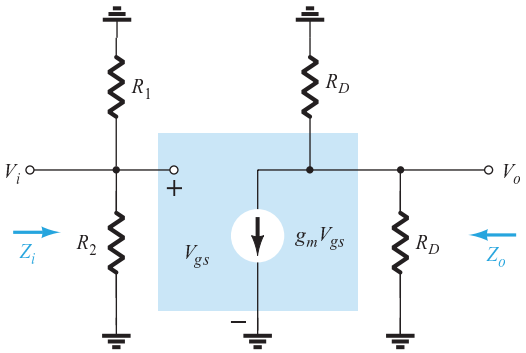


Figure 9.22 Network of Fig. 9.21 under ac conditions.

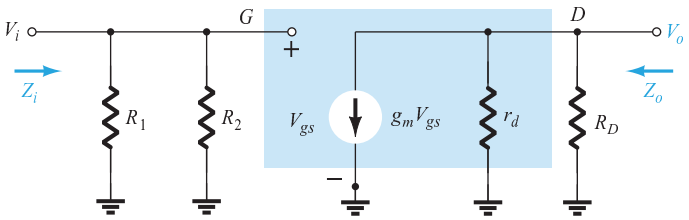


Figure 9.23 Redrawn network of Fig. 9.22.

Z_i: R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET resulting in

$$\boxed{Z_i = R_1 \| R_2} \tag{9.28}$$

Z_o: Setting $V_i = 0$ V will set V_{gs} and $g_m V_{gs}$ to zero and

$$\boxed{Z_o = r_d \| R_D} \tag{9.29}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{9.30}$$

A_v:

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{9.31}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}_{r_d \geq 10R_D} \tag{9.32}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

9.6 JFET SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of Fig. 9.24. Note that the output is taken off the source terminal and, when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology common-drain).

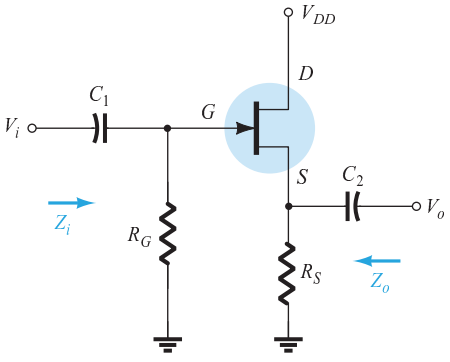


Figure 9.24 JFET source-follower configuration.

Substituting the JFET equivalent circuit will result in the configuration of Fig. 9.25. The controlled source and internal output impedance of the JFET are tied to ground at one end and R_S on the other, with V_o across R_S. Since $g_m V_{gs}$, r_d, and R_S are connected to the same terminal and ground, they can all be placed in parallel as shown in Fig. 9.26. The current source reversed direction but V_{gs} is still defined between the gate and source terminals.

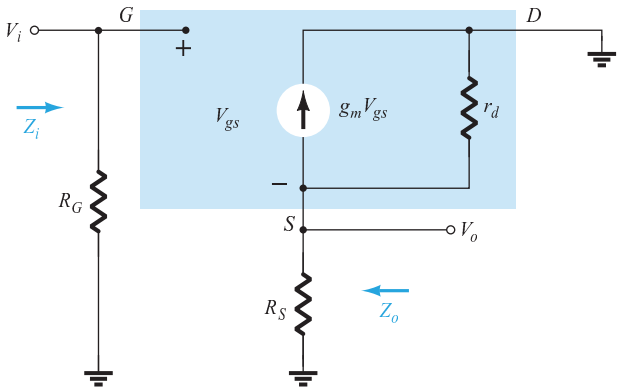


Figure 9.25 Network of Fig. 9.24 following the substitution of the JFET ac equivalent model.

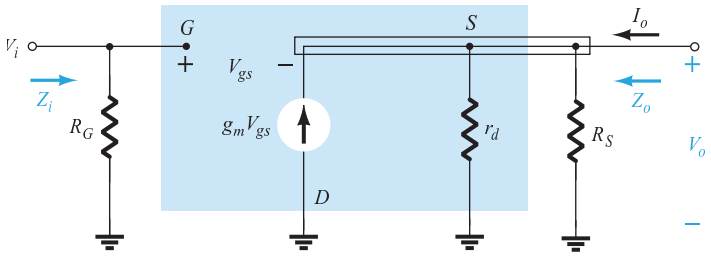


Figure 9.26 Network of Fig. 9.25 redrawn.

***Z_i*:** Figure 9.26 clearly reveals that Z_i is defined by

$$Z_i = R_G \tag{9.33}$$

***Z_o*:** Setting $V_i = 0$ V will result in the gate terminal being connected directly to ground as shown in Fig. 9.27. The fact that V_{gs} and V_o are across the same parallel network results in $V_o = -V_{gs}$.

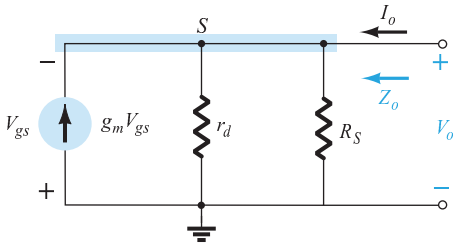


Figure 9.27 Determining Z_o for the network of Fig. 9.24.

Applying Kirchhoff's current law at node s,

$$I_o + g_m V_{gs} = I_{r_d} + I_{R_S}$$
$$= \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

The result is

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$
$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$
$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and $$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$\boxed{Z_o = r_d \| R_S \| 1/g_m} \tag{9.34}$$

For $r_d \geq 10R_S$,

$$\boxed{Z_o \cong R_S \| 1/g_m}_{r_d \geq 10R_S} \tag{9.35}$$

A_v: The output voltage V_o is determined by

$$V_o = g_m V_{gs}(r_d \| R_S)$$

and applying Kirchhoff's voltage law around the perimeter of the network of Fig. 9.26 will result in

$$V_i = V_{gs} + V_o$$

and $$V_{gs} = V_i - V_o$$

so that $$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

or $$V_o = g_m V_i(r_d \| R_S) - g_m V_o(r_d \| R_S)$$

and $$V_o[1 + g_m(r_d \| R_S)] = g_m V_i(r_d \| R_S)$$

so that $$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}} \tag{9.36}$$

In the absence of r_d or if $r_d \geq 10R_S$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S}}_{r_d \geq 10R_S} \tag{9.37}$$

Since the bottom of Eq. (9.36) is larger than the numerator by a factor of one, the gain can never be equal to or greater than one (as encountered for the emitter-follower BJT network).

Phase Relationship: Since A_v of Eq. (9.36) is a positive quantity, V_o and V_i are in phase for the JFET source-follower configuration.

EXAMPLE 9.9

A dc analysis of the source-follower network of Fig. 9.28 will result in $V_{GS_Q} = -2.86$ V and $I_{D_Q} = 4.56$ mA.

(a) Determining g_m.
(b) Find r_d.
(c) Determine Z_i.
(d) Calculate Z_o with and without r_d. Compare results.
(e) Determine A_v with and without r_d. Compare results.

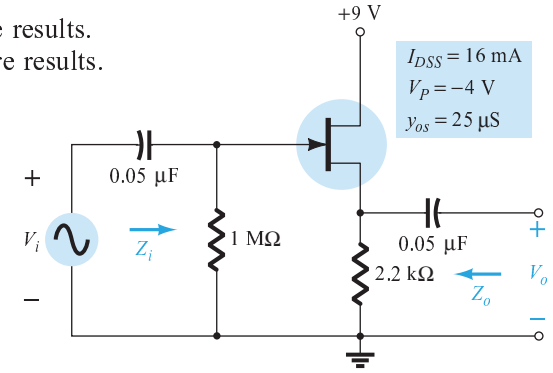


Figure 9.28 Network to be analyzed in Example 9.9.

Solution

(a) $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \frac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\ mS}$$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{25\ \mu\text{S}} = \mathbf{40\ k\Omega}$

(c) $Z_i = R_G = \mathbf{1\ M\Omega}$

(d) With r_d:

$$\begin{aligned} Z_o = r_d \| R_S \| 1/g_m &= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS} \\ &= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega \\ &= \mathbf{362.52\ \Omega} \end{aligned}$$

revealing that Z_o is often relatively small and determined primarily by $1/g_m$. Without r_d:

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

revealing that r_d typically has little impact on Z_o.

(e) With r_d:

$$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}$$

$$\frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83}$$

which is less than 1 as predicted above.

Without r_d:

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28\text{ mS})(2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.2\text{ k}\Omega)}$$

$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

revealing that r_d usually has little impact on the gain of the configuration.

9.7 JFET COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the common-gate configuration of Fig. 9.29, which parallels the common-base configuration employed with BJT transistors.

Substituting the JFET equivalent circuit will result in Fig. 9.30. Note the continuing requirement that the controlled source $g_m V_{gs}$ be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network. In addition, the resistor connected between input terminals is no longer R_G but the resistor R_S connected from source to ground. Note also the location of the controlling voltage V_{gs} and the fact that it appears directly across the resistor R_S.

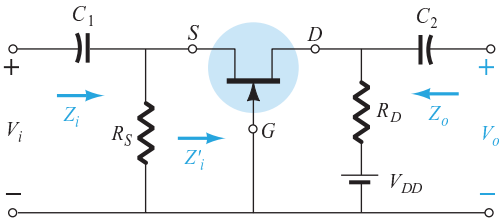


Figure 9.29 JFET common-gate configuration.

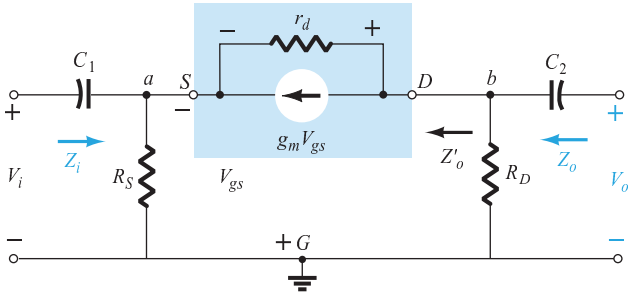


Figure 9.30 Network of Fig. 9.29 following substitution of JFET ac equivalent model.

***Z_i*:** The resistor R_S is directly across the terminals defining Z_i. Let us therefore find the impedance Z'_i of Fig. 9.29, which will simply be in parallel with R_S when Z_i is defined.

The network of interest is redrawn as Fig. 9.31. The voltage $V' = -V_{gs}$. Applying Kirchhoff's voltage law around the output perimeter of the network will result in

$$V' - V_{r_d} - V_{R_D} = 0$$

and

$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

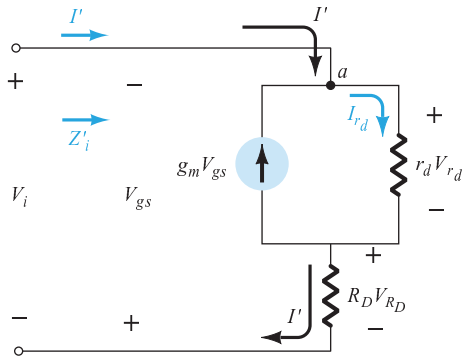


Figure 9.31 Determining Z'_i for the network of Fig. 9.29.

Applying Kirchhoff's current law at node *a* results in

$$I' + g_m V_{gs} = I_{r_d}$$

and

$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I'R_D)}{r_d} - g_m V_{gs}$$

or

$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

so that

$$I'\left[1 + \frac{R_D}{r_d}\right] = V'\left[\frac{1}{r_d} + g_m\right]$$

and

$$Z'_i = \frac{V'}{I'} = \frac{\left[1 + \dfrac{R_D}{r_d}\right]}{\left[g_m + \dfrac{1}{r_d}\right]} \tag{9.38}$$

or

$$Z'_i = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_m r_d}$$

and $$Z_i = R_S \| Z_i'$$

results in $$\boxed{Z_i = R_S \left\| \left[\frac{r_d + R_D}{1 + g_m r_d} \right] \right.} \tag{9.39}$$

If $r_d \geq 10R_D$, Eq. (9.38) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

$$Z_i' = \frac{\left[1 + \dfrac{R_D}{r_d} \right]}{\left[g_m + \dfrac{1}{r_d} \right]} \cong \frac{1}{g_m}$$

and $$\boxed{Z_i \cong R_S \| 1/g_m}_{r_d \geq 10R_D} \tag{9.40}$$

Z_o: Substituting $V_i = 0$ V in Fig. 9.30 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_m V_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D \| r_d} \tag{9.41}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D} \tag{9.42}$$

A_v: Figure 9.30 reveals that

$$V_i = -V_{gs}$$

and $$V_o = I_D R_D$$

The voltage across r_d is

$$V_{r_d} = V_o - V_i$$

and $$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node b in Fig. 9.30 results in

$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and $$I_D = -I_{rd} - g_m V_{gs}$$

$$= -\left[\frac{V_o - V_i}{r_d} \right] - g_m[-V_i]$$

$$I_D = \frac{V_i - V_o}{r_d} + g_m V_i$$

so that $$V_o = I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i \right] R_D$$

$$= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m$$

and $$V_o \left[1 + \frac{R_D}{r_d} \right] = V_i \left[\frac{R_D}{r_d} + g_m R_D \right]$$

with
$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} \tag{9.43}$$

For $r_d \geq 10R_D$, the factor R_D/r_d of Eq. (9.43) can be dropped as a good approximation and

$$A_v = g_m R_D \quad r_d \geq 10R_D \tag{9.44}$$

Phase Relationship: The fact that A_v is a positive number will result in an *in-phase* relationship between V_o and V_i for the common-gate configuration.

EXAMPLE 9.10

Although the network of Fig. 9.32 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 9.29. If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:
(a) Determine g_m.
(b) Find r_d.
(c) Calculate Z_i with and without r_d. Compare results.
(d) Find Z_o with and without r_d. Compare results.
(e) Determine V_o with and without r_d. Compare results.

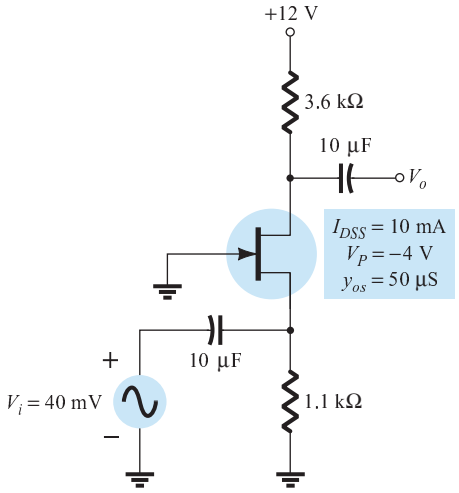


Figure 9.32 Network for Example 9.10.

Solution

(a) $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 5\text{ mS}\left(1 - \frac{(-2.2\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.25\ mS}$$

(b) $r_d = \frac{1}{y_{os}} = \frac{1}{50\ \mu\text{S}} = \mathbf{20\ k\Omega}$

(c) With r_d:

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{ k}\Omega \| \left[\frac{20\text{ k}\Omega + 3.6\text{ k}\Omega}{1 + (2.25\text{ ms})(20\text{ k}\Omega)}\right]$$
$$= 1.1\text{ k}\Omega \| 0.51\text{ k}\Omega = \mathbf{0.35\ k\Omega}$$

Without r_d:

$$Z_i = R_S\|1/g_m = 1.1\ \text{k}\Omega\|1/2.25\ \text{ms} = 1.1\ \text{k}\Omega\|0.44\ \text{k}\Omega$$
$$= \mathbf{0.31\ k\Omega}$$

Even though the condition,

$$r_d \geq 10R_D = > 20\ \text{k}\Omega \geq 10(3.6\ \text{k}\Omega) = > 20\ \text{k}\Omega \geq 36\ \text{k}\Omega$$

is *not* satisfied, both equations result in essentially the same level of impedance. In this case, $1/g_m$ was the predominant factor.

(d) With r_d:

$$Z_o = R_D\|r_d = 3.6\ \text{k}\Omega\|20\ \text{k}\Omega = \mathbf{3.05\ k\Omega}$$

Without r_d:

$$Z_o = R_D = \mathbf{3.6\ k\Omega}$$

Again the condition $r_d \geq 10R_D$ is *not* satisfied, but both results are reasonably close. R_D is certainly the predominant factor in this example.

(e) With r_d:

$$A_v = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]} = \frac{\left[(2.25\ \text{mS})(3.6\ \text{k}\Omega) + \dfrac{3.6\ \text{k}\Omega}{20\ \text{k}\Omega}\right]}{\left[1 + \dfrac{3.6\ \text{k}\Omega}{20\ \text{k}\Omega}\right]}$$
$$= \frac{8.1 + 0.18}{1 + 0.18} = \mathbf{7.02}$$

and $$A_v = \frac{V_o}{V_i} = \blacktriangleright\ V_o = A_v V_i = (7.02)(40\ \text{mV}) = \mathbf{280.8\ mV}$$

Without r_d:

$$A_v = g_m R_D = (2.25\ \text{mS})(3.6\ \text{k}\Omega) = \mathbf{8.1}$$

with $$V_o = A_v V_i = (8.1)(40\ \text{mV}) = \mathbf{324\ mV}$$

In this case, the difference is a little more noticeable but not dramatically so.

Example 9.10 demonstrates that even though the condition $r_d \geq 10R_D$ was not satisfied, the results for the parameters given were not significantly different using the exact and approximate equations. In fact, in most cases, the approximate equations can be used to find a reasonable idea of particular levels with a reduced amount of effort.

9.8 DEPLETION-TYPE MOSFETs

The fact that Shockley's equation is also applicable to depletion-type MOSFETs results in the same equation for g_m. In fact, the ac equivalent model for D-MOSFETs is exactly the same as that employed for JFETs as shown in Fig. 9.33.

The only difference offered by D-MOSFETs is that V_{GS_Q} can be positive for *n*-channel devices and negative for *p*-channel units. The result is that g_m can be greater than g_{m0} as demonstrated by the example to follow. The range of r_d is very similar to that encountered for JFETs.

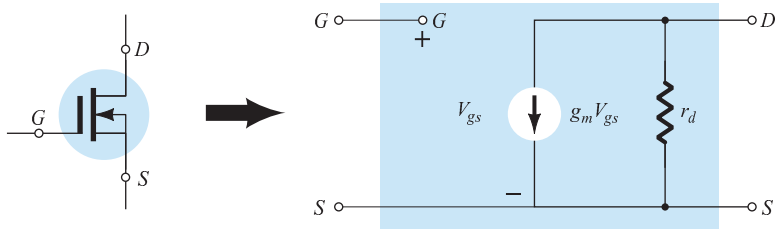


Figure 9.33 D-MOSFET ac equivalent model.

EXAMPLE 9.11

The network of Fig. 9.34 was analyzed as Example 6.8, resulting in $V_{GS_Q} = 0.35$ V and $I_{D_Q} = 7.6$ mA.

(a) Determine g_m and compare to g_{m0}.
(b) Find r_d.
(c) Sketch the ac equivalent network for Fig. 9.34.
(d) Find Z_i.
(e) Calculate Z_o.
(f) Find A_v.

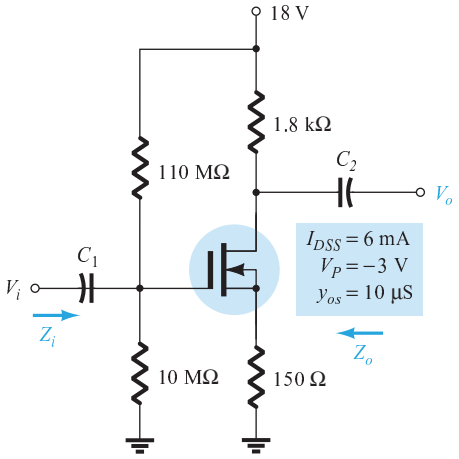


Figure 9.34 Network for Example 9.11.

Solution

(a) $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(6\text{ mA})}{3\text{ V}} = 4\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{(+0.35\text{ V})}{(-3\text{ V})}\right) = 4\text{ mS}(1 + 0.117) = \mathbf{4.47\text{ mS}}$$

(b) $$r_d = \frac{1}{y_{os}} = \frac{1}{10\ \mu S} = \mathbf{100\ k\Omega}$$

(c) See Fig. 9.35. Note the similarities with the network of Fig. 9.23. Equations (9.28) through (9.32) are therefore applicable.

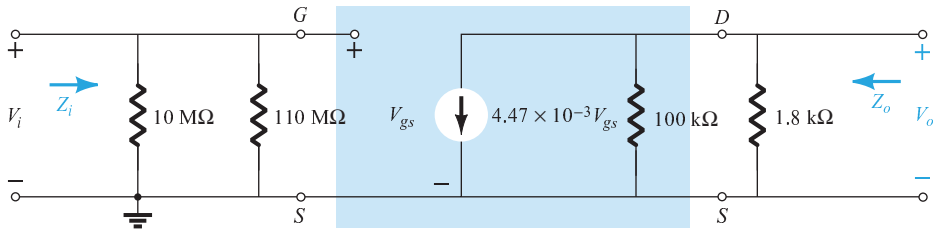


Figure 9.35 AC equivalent circuit for Fig. 9.34.

(d) Eq. (9.28): $Z_i = R_1 \| R_2 = 10\ \text{M}\Omega \| 110\ \text{M}\Omega = \mathbf{9.17\ M\Omega}$
(e) Eq. (9.29): $Z_o = r_d \| R_D = 100\ \text{k}\Omega \| 1.8\ \text{k}\Omega = \mathbf{1.77\ k\Omega} \cong R_D = \mathbf{1.8\ k\Omega}$
(f) $r_d \geq 10R_D \rightarrow 100\ \text{k}\Omega \geq 18\ \text{k}\Omega$
Eq. (9.32): $A_v = -g_m R_D = -(4.47\ \text{mS})(1.8\ \text{k}\Omega) = \mathbf{8.05}$

9.9 ENHANCEMENT-TYPE MOSFETs

The enhancement-type MOSFET can be either an *n*-channel (*n*MOS) or *p*-channel (*p*MOS) device, as shown in Fig. 9.36. The ac small-signal equivalent circuit of either device is shown in Fig. 9.36, revealing an open-circuit between gate and drain-source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source r_d, which is usually provided on specification sheets as an admittance y_{os}. The device transconductance, g_m, is provided on specification sheets as the forward transfer admittance, y_{fs}.

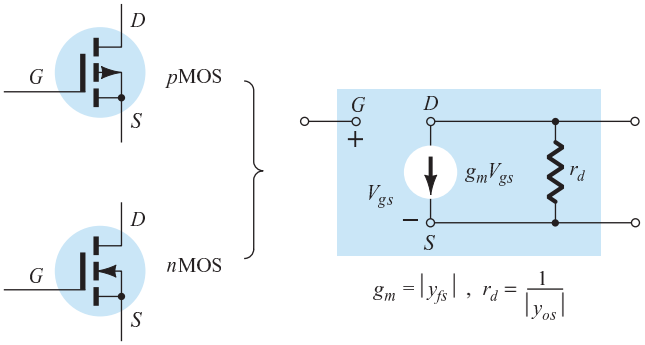


Figure 9.36 Enhancement MOSFET ac small-signal model.

In our analysis of JFETs, an equation for g_m was derived from Shockley's equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

and

$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})} \qquad (9.45)$$

Recall that the constant k can be determined from a given typical operating point on a specification sheet. In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs. Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

9.10 E-MOSFET DRAIN-FEEDBACK CONFIGURATION

The E-MOSFET drain-feedback configuration appears in Fig. 9.37. Recall from dc calculations that R_G could be replaced by a short-circuit equivalent since $I_G = 0$ A and therefore $V_{R_G} = 0$ V. However, for ac situations it provides an important high impedance between V_o and V_i. Otherwise, the input and output terminals would be connected directly and $V_o = V_i$.

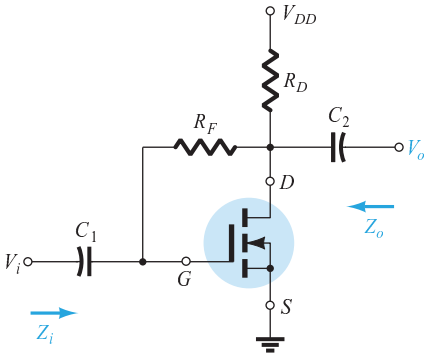


Figure 9.37 E-MOSFET drain-feedback configuration.

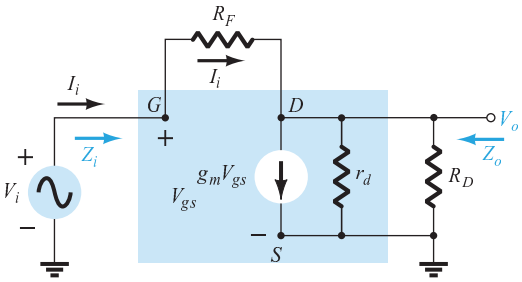


Figure 9.38 AC equivalent of the network of Fig. 9.37.

Substituting the ac equivalent model for the device will result in the network of Fig. 9.38. Note that R_F is not within the shaded area defining the equivalent model of the device but does provide a direct connection between input and output circuits.

Z_i: Applying Kirchhoff's current law to the output circuit (at node D in Fig. 9.38) results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

and

$$V_{gs} = V_i$$

so that

$$I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

or

$$I_i - g_m V_i = \frac{V_o}{r_d \| R_D}$$

Therefore,

$$V_o = (r_d \| R_D)(I_i - g_m V_i)$$

with

$$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \| R_D)(I_i - g_m V_i)}{R_F}$$

and

$$I_i R_F = V_i - (r_d \| R_D) I_i + (r_d \| R_D) g_m V_i$$

so that

$$V_i[1 + g_m(r_d \| R_D)] = I_i[R_F + r_d \| R_D]$$

and finally,

$$\boxed{Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}} \qquad (9.46)$$

Typically, $R_F \gg r_d \| R_D$, so that

$$Z_i \cong \frac{R_F}{1 + g_m(r_d \| R_D)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_i \cong \frac{R_F}{1 + g_m R_D}} \quad R_F \gg r_d \| R_D,\ r_d \geq 10R_D \tag{9.47}$$

***Z_o*:** Substituting $V_i = 0$ V will result in $V_{gs} = 0$ V and $g_m V_{gs} = 0$, with a short-circuit path from gate to ground as shown in Fig. 9.39. R_F, r_d, and R_D are then in parallel and

$$\boxed{Z_o = R_F \| r_d \| R_D} \tag{9.48}$$

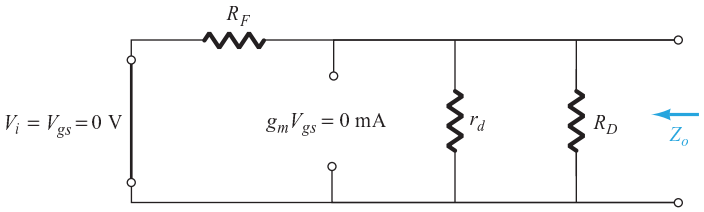


Figure 9.39 Determining Z_o for the network of Fig. 9.37.

Normally, R_F is so much larger than $r_d \| R_D$ that

$$Z_o \cong r_d \| R_D$$

and with $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D} \quad R_F \gg r_d \| R_D,\ r_d \geq 10R_D \tag{9.49}$$

***A_v*:** Applying Kirchhoff's current law at node D of Fig. 9.38 will result in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

but

$$V_{gs} = V_i \text{ and } I_i = \frac{V_i - V_o}{R_F}$$

so that

$$\frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

and

$$\frac{V_i}{R_F} - \frac{V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

so that

$$V_o\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right] = V_i\left[\frac{1}{R_F} - g_m\right]$$

and

$$A_v = \frac{V_o}{V_i} = \frac{\left[\frac{1}{R_F} - g_m\right]}{\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right]}$$

but
$$\frac{1}{r_d \| R_D} + \frac{1}{R_F} = \frac{1}{R_F \| r_d \| R_D}$$

and
$$g_m \gg \frac{1}{R_F}$$

so that
$$A_v = -g_m(R_F \| r_d \| R_D) \tag{9.50}$$

Since R_F is usually $>>$ $r_d \| R_D$ and if $r_d \geq 10R_D$,

$$A_v \cong -g_m R_D \quad R_F \gg r_d \| R_D,\ r_d \geq 10R_D \tag{9.51}$$

Phase Relationship: The negative sign for A_v reveals that V_o and V_i are out of phase by 180°.

EXAMPLE 9.12

The E-MOSFET of Fig. 9.40 was analyzed in Example 6.11, with the result that $k = 0.24 \times 10^{-3}$ A/V^2, $V_{GS_Q} = 6.4$ V, and $I_{D_Q} = 2.75$ mA.
(a) Determine g_m.
(b) Find r_d.
(c) Calculate Z_i with and without r_d. Compare results.
(d) Find Z_o with and without r_d. Compare results.
(e) Find A_v with and without r_d. Compare results.

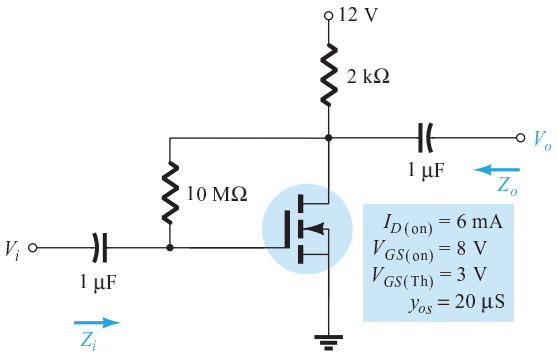


Figure 9.40 Drain-feedback amplifier from Example 6.11.

Solution

(a) $g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})}) = 2(0.24 \times 10^{-3}\ \text{A/V}^2)(6.4\ \text{V} - 3\ \text{V})$
$= \mathbf{1.63\ mS}$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

(c) With r_d:

$$Z_i = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)} = \frac{10\ \text{M}\Omega + 50\ \text{k}\Omega \| 2\ \text{k}\Omega}{1 + (1.63\ \text{mS})(50\ \text{k}\Omega \| 2\ \text{k}\Omega)}$$
$$= \frac{10\ \text{M}\Omega + 1.92\ \text{k}\Omega}{1 + 3.13} = \mathbf{2.42\ M\Omega}$$

Without r_d:

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10\ \text{M}\Omega}{1 + (1.63\ \text{mS})(2\ \text{k}\Omega)} = \mathbf{2.53\ M\Omega}$$

revealing that since the condition $r_d \geq 10R_D = 50\ \text{k}\Omega \geq 40\ \text{k}\Omega$ is satisfied, the results for Z_o with or without r_d will be quite close.

(d) With r_d:

$$Z_o = R_F \| r_d \| R_D = 10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega = 49.75\ \text{k}\Omega \| 2\ \text{k}\Omega$$
$$= \mathbf{1.92\ k\Omega}$$

Without r_d:

$$Z_o \cong R_D = \mathbf{2\ k\Omega}$$

again providing very close results.

(e) With r_d:

$$A_v = -g_m(R_F \| r_d \| R_D)$$
$$= -(1.63\ \text{mS})(10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega)$$
$$= -(1.63\ \text{mS})(1.92\ \text{k}\Omega)$$
$$= \mathbf{-3.21}$$

Without r_d:

$$A_v = -g_m R_D = -(1.63\ \text{mS})(2\ \text{k}\Omega)$$
$$= \mathbf{-3.26}$$

which is very close to the above result.

9.11 E-MOSFET VOLTAGE-DIVIDER CONFIGURATION

The last E-MOSFET configuration to be examined in detail is the voltage-divider network of Fig. 9.41. The format is exactly the same as appearing in a number of earlier discussions.

Substituting the ac equivalent network for the E-MOSFET will result in the configuration of Fig. 9.42, which is exactly the same as Fig. 9.23. The result is that Eqs. (9.28) through (9.32) are applicable as listed below for the E-MOSFET.

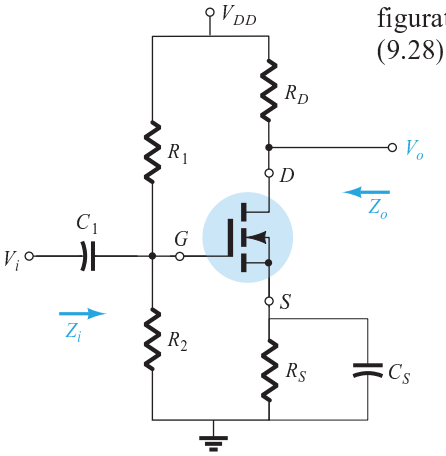


Figure 9.41 E-MOSFET voltage-divider configuration.

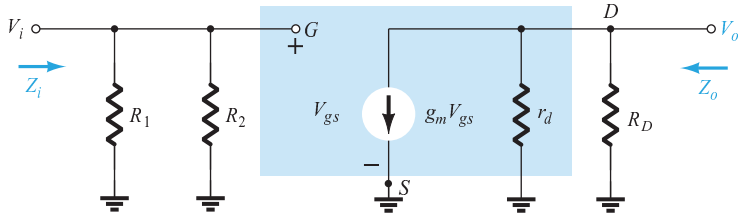


Figure 9.42 AC equivalent network for the configuration of Fig. 9.41.

Z_i:

$$Z_i = R_1 \| R_2 \tag{9.52}$$

Z_o:

$$Z_o = r_d \| R_D \tag{9.53}$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D} \tag{9.54}$$

A_v:

$$A_v = \frac{V_o}{V_i} = -g_m(r_D \| R_D) \tag{9.55}$$

and if $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \tag{9.56}$$

9.12 DESIGNING FET AMPLIFIER NETWORKS

Design problems at this stage are limited to obtaining a desired dc bias condition or ac voltage gain. In most cases, the various equations developed are used "in reverse" to define the parameters necessary to obtain the desired gain, input impedance, or output impedance. To avoid unnecessary complexity during the initial stages of the design, the approximate equations are often employed because some variation will occur when calculated resistors are replaced by standard values. Once the initial design is completed, the results can be tested and refinements made using the complete equations.

Throughout the design procedure be aware that although superposition permits a separate analysis and design of the network from a dc and an ac viewpoint, a parameter chosen in the dc environment will often play an important role in the ac response. In particular, recall that the resistance R_G could be replaced by a short-circuit equivalent in the feedback configuration because $I_G \cong 0$ A for dc conditions, but for the ac analysis, it presents an important high impedance path between V_o and V_i. In addition, recall that g_m is larger for operating points closer to the I_D axis ($V_{GS} = 0$ V), requiring that R_S be relatively small. In the unbypassed R_S network, a small R_S will also contribute to a higher gain, but for the source-follower, the gain is reduced from its maximum value of 1. In total, simply keep in mind that network parameters can affect the dc and ac levels in different ways. Often a balance must be made between a particular operating point and its impact on the ac response.

In most situations, the available dc supply voltage is known, the FET to be employed has been determined, and the capacitors to be employed at the chosen frequency are defined. It is then necessary to determine the resistive elements necessary to establish the desired gain or impedance level. The next three examples will determine the required parameters for a specific gain.

EXAMPLE 9.13 Design the fixed-bias network of Fig. 9.43 to have an ac gain of 10. That is, determine the value of R_D.

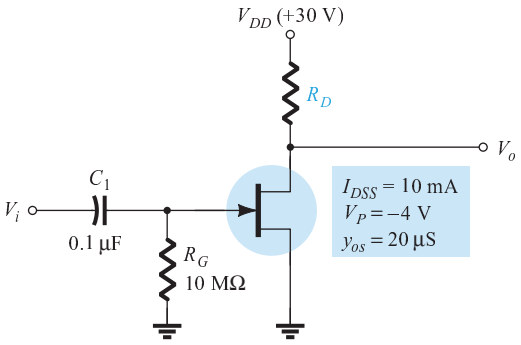


Figure 9.43 Circuit for desired voltage gain in Example 9.13.

Solution

Since $V_{GS_Q} = 0$ V, the level of g_m is g_{m0}. The gain is therefore determined by

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

with

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{4 \text{ V}} = 5 \text{ mS}$$

The result is

$$-10 = -5 \text{ mS}(R_D \| r_d)$$

and

$$R_D \| r_d = \frac{10}{5 \text{ mS}} = 2 \text{ k}\Omega$$

From the device specifications,

$$r_d = \frac{1}{y_{os}} = \frac{1}{20 \times 10^{-6} \text{ S}} = 50 \text{ k}\Omega$$

Substituting, we find

$$R_D \| r_d = R_D \| 50 \text{ k}\Omega = 2 \text{ k}\Omega$$

and

$$\frac{R_D(50 \text{ k}\Omega)}{R_D + 50 \text{ k}\Omega} = 2 \text{ k}\Omega$$

or

$$50R_D = 2(R_D + 50 \text{ k}\Omega) = 2R_D + 100 \text{ k}\Omega$$

with

$$48R_D = 100 \text{ k}\Omega$$

and

$$R_D = \frac{100 \text{ k}\Omega}{48} \cong 2.08 \text{ k}\Omega$$

The closest standard value is **2 kΩ** (Appendix C), which would be employed for this design.

The resulting level of V_{DS_Q} would then be determined as follows:

$$V_{DS_Q} = V_{DD} - I_{D_Q}R_D = 30 \text{ V} - (10 \text{ mA})(2 \text{ k}\Omega) = \mathbf{10 \text{ V}}$$

The levels of Z_i and Z_o are set by the levels of R_G and R_D, respectively. That is,

$$Z_i = R_G = \mathbf{10 \text{ M}\Omega}$$

$$Z_o = R_D \| r_d = 2 \text{ k}\Omega \| 50 \text{ k}\Omega = \mathbf{1.92 \text{ k}\Omega} \cong R_D = 2 \text{ k}\Omega.$$

EXAMPLE 9.14

Choose the values of R_D and R_S for the network of Fig. 9.44 that will result in a gain of 8 using a relatively high level of g_m for this device defined at $V_{GS_Q} = \frac{1}{4}V_P$.

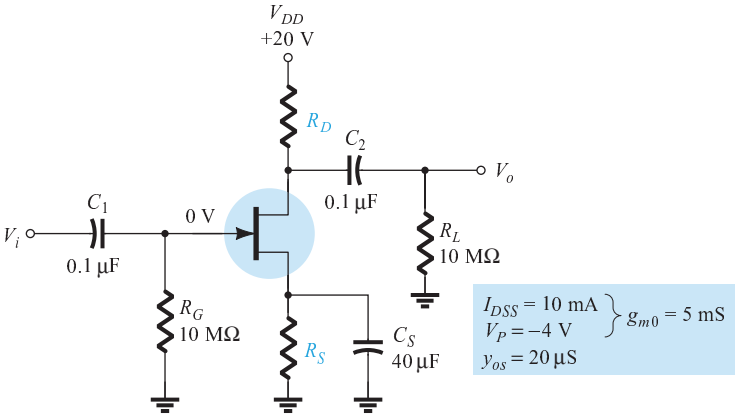


Figure 9.44 Network for desired voltage gain in Example 9.14.

Solution

The operating point is defined by

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\text{ V}) = -1\text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right)^2 = 5.625\text{ mA}$$

Determining g_m,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$= 5\text{ mS}\left(1 - \frac{(-1\text{ V})}{(-4\text{ V})}\right) = 3.75\text{ mS}$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_m(R_D \| r_d)$$

Substituting known values will result in

$$8 = (3.75\text{ mS})(R_D \| r_d)$$

so that

$$R_D \| r_d = \frac{8}{3.75\text{ mS}} = 2.13\text{ k}\Omega$$

The level of r_d is defined by

$$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

and

$$R_D \| 50\text{ k}\Omega = 2.13\text{ k}\Omega$$

with the result that

$$R_D = \mathbf{2.2\ k\Omega}$$

which is a standard value.

g_m

The level of R_S is determined by the dc operating conditions as follows:

$$V_{GS_Q} = -I_D R_S$$

$$-1\text{ V} = -(5.625\text{ mA})R_S$$

and

$$R_S = \frac{1\text{ V}}{5.625\text{ mA}} = 177.8\ \Omega$$

The closest standard value is 180 Ω. In this example, R_S does not appear in the ac design because of the shorting effect of C_S.

In the next example, R_S is unbypassed and the design becomes a bit more complicated.

EXAMPLE 9.15

Determine R_D and R_S for the network of Fig. 9.44 to establish a gain of 8 if the bypass capacitor C_S is removed.

Solution

V_{GS_Q} and I_{D_Q} are still −1 V and 5.625 mA, and since the equation $V_{GS} = -I_D R_S$ has not changed, R_S continues to equal the standard value of **180 Ω** obtained in Example 9.14.

The gain of an unbypassed self-bias configuration is

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

For the moment it is assumed that $r_d \geq 10(R_D + R_S)$. Using the full equation for A_v at this stage of the design would simply complicate the process unnecessarily.

Substituting (for the specified magnitude of 8 for the gain),

$$|8| = \left|\frac{-(3.75\text{ mS})R_D}{1 + (3.75\text{ mS})(180\ \Omega)}\right| = \frac{(3.75\text{ mS})R_D}{1 + 0.675}$$

and

$$8(1 + 0.675) = (3.75\text{ mS})R_D$$

so that

$$R_D = \frac{13.4}{3.75\text{ mS}} = 3.573\ \text{k}\Omega$$

with the closest standard value at **3.6 kΩ.**

We can now test the condition:

$$r_d \geq 10(R_D + R_S)$$

$$50\ \text{k}\Omega \geq 10(3.6\ \text{k}\Omega + 0.18\ \text{k}\Omega) = 10(3.78\ \text{k}\Omega)$$

and

$$50\ \text{k}\Omega \geq 37.8\ \text{k}\Omega$$

which is satisfied—the solution stands!

9.13 SUMMARY TABLE

In an effort to provide a quick comparison between configurations and offer a listing that can be helpful for a variety of reasons, Table 9.1 was developed. The exact and approximate equation for each important parameter are provided with a typical range of values for each. Although all the possible configurations are not present, the majority of the most frequently encountered are included. In fact, any configuration not

TABLE 9.1 Z_i, Z_o, and A_v for various FET configurations

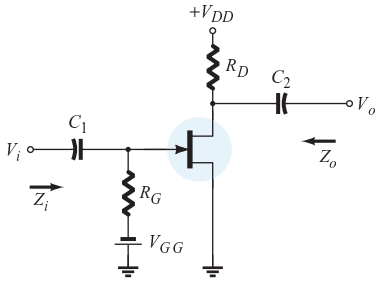
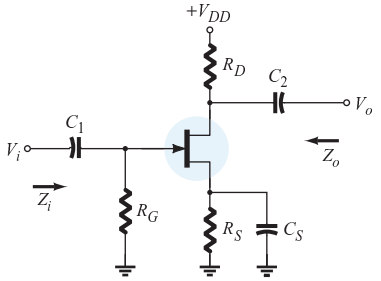
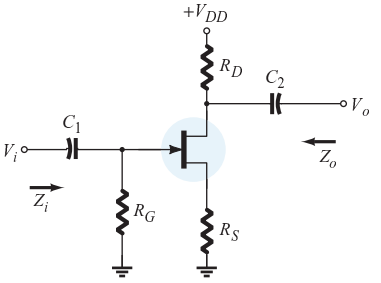
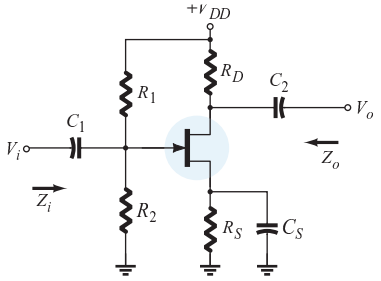
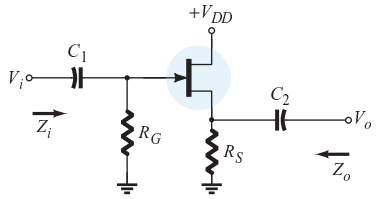
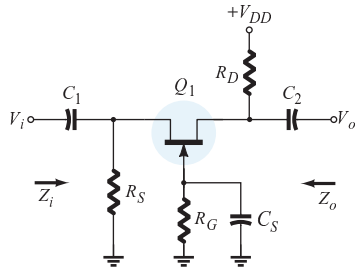
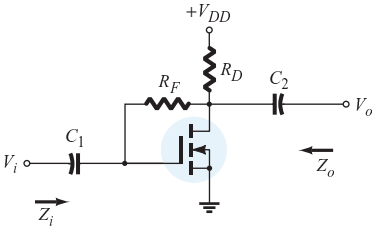
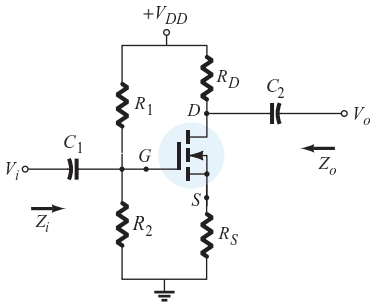
Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET]	 High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias bypassed R_s [JFET or D-MOSFET]	 High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET]	 High (10 MΩ) $= R_G$	$= \dfrac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}$ $= R_D$ $r_d \geq 10\,R_D$ or $r_d = \infty\Omega$	Low (−2) $= \dfrac{g_m R_D}{1 + g_m R_s + \frac{R_D + R_S}{r_d}}$ $\cong -\dfrac{g_m R_D}{1 + g_m R_S}$ $[r_d \geq 10(R_d + R_S)]$
Voltage-divider bias [JFET or D-MOSFET]	 High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$

TABLE 9.1 (Continued)

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \| R_S \| 1/g_m$ $\cong R_S \| 1/g_m \quad (r_d \geq 10\,R_S)$	Low (< 1) $= \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}$ $\cong \frac{g_m R_S}{1 + g_m R_S} \quad (r_d \geq 10\,R_S)$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= R_S \left\| \left[\frac{r_d + R_D}{1 + g_m r_d} \right] \right.$ $\cong R_S \| \frac{1}{g_m} \quad (r_d \geq 10\,R_D)$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D \quad (r_d \geq 10\,R_D)$	Medium (+10) $= \frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}$ $\cong g_m R_D \quad (r_d \geq 10\,R_S)$
Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}$ $\cong \frac{R_F}{1 + g_m R_D} \quad (r_d \geq 10\,R_D)$	Medium (2 kΩ) $= R_F \| r_d \| R_D$ $\cong R_D \quad (R_F, r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(R_F \| r_d \| R_D)$ $\cong -g_m R_D \quad (R_F, r_d \geq 10\,R_D)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D \quad (R_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D \quad (r_d \geq 10\,R_D)$

listed will probably be some variation of those appearing in the table, so at the very least, the listing will provide some insight as to what expected levels should be and which path will probably generate the desired equations. The format chosen was designed to permit a duplication of the entire table on the front and back of one $8\frac{1}{2}$ by 11 inch page.

9.14 TROUBLESHOOTING

As mentioned before, troubleshooting a circuit is a combination of knowing the theory and having experience using meters and an oscilloscope to check the operation of the circuit. A good troubleshooter has a "nose" for finding the trouble in a circuit—this ability to "see" what is happening being greatly developed through building, testing, and repairing many different circuits. For an FET small-signal amplifier, one could go about troubleshooting a circuit by performing a number of basic steps:

1. Look at the circuit board to see if any obvious problems can be seen: an area charred by excess heating of a component; a component that feels or seems too hot to touch; what appears to be a poor solder joint; any connection that appears to have come loose.
2. Use a dc meter: make some measurements as marked in a repair manual containing the circuit schematic diagram and a listing of test dc voltages.
3. Apply a test ac signal: measure the ac voltages starting at the input and working along toward the output.
4. If the problem is identified at a particular stage, the ac signal at various points should be checked using an oscilloscope to see the waveform, its polarity, amplitude, and frequency, as well as any unusual waveform "glitches" that may be present. In particular, observe that the signal is present for the full signal cycle.

Possible Symptoms and Actions

If there is no output ac voltage:

1. Check if the supply voltage is present.
2. Check if the output voltage at V_D is between 0 V and V_{DD}.
3. Check if there is any input ac signal at the gate terminal.
4. Check the ac voltage at each side of the coupling capacitor terminals.

When building and testing a FET amplifier circuit in the laboratory:

1. Check the color code of resistor values to be sure that they are correct. Even better, measure the resistor value as components used repeatedly may get overheated when used incorrectly, causing the nominal value to change.
2. Check that all dc voltages are present at the component terminals. Be sure that all ground connections are made common.
3. Measure the ac input signal to be sure the expected value is provided to the circuit.

9.15 PSPICE WINDOWS

JFET Fixed-Bias Configuration

The first JFET configuration to be analyzed using PSpice Windows is the fixed-bias configuration of Fig. 9.45, which has a JFET with $V_P = -4$ V and $I_{DSS} = 10$ mA. The 10-MΩ resistor was added to act as a path to ground for the capacitor

but is essentially an open-circuit as a load. The **J2N3819 *n*-channel JFET** from the **EVAL.slb** library will be used, and the ac voltage will be determined at four different points for comparison and review.

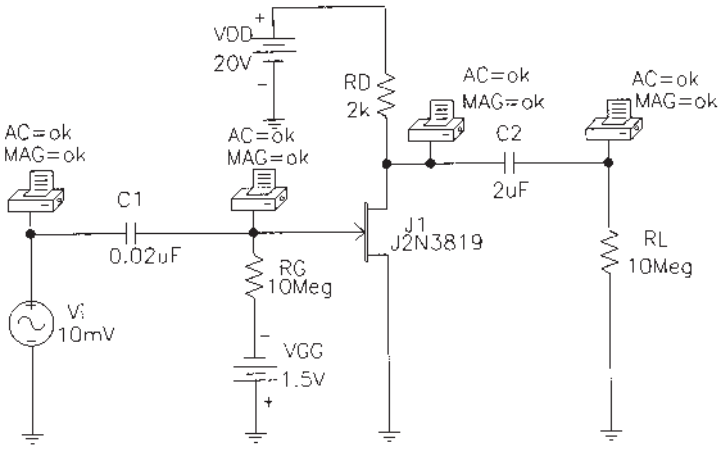


Figure 9.45 Fixed-bias JFET configuration with an ac source.

The constant **Beta** is determined by

$$\text{Beta} = \frac{I_{DSS}}{|V_p|^2} = \frac{10\text{ mA}}{4^2} = 0.625\text{ mA/V}^2$$

and inserted as a **Model Parameter** using the sequence **Edit-Model-Edit Instance Model (Text). Vto** must also be changed to -4 V. The remaining elements of the network are set as described for the transistor in Chapter 8.

An analysis of the network will result in the printout of Fig. 9.46. The **Schematics Netlist** reveals the nodes assigned to each parameter and defines the nodes for which the ac voltage is to be printed. In this case, note that **Vi** is set at 10 mV at a frequency of 10kHz from node 2 to 0. In the list of **Junction FET MODEL PARAMETERS, VTO** is -4 V and **BETA** is 625E-6 as entered. The **SMALL-SIGNAL BIAS SOLUTION** reveals that the voltage at both ends of R_G is -1.5 V, resulting in $V_{GS} = -1.5$ V. The voltage from drain to source (ground) is 12 V, leaving a drop of 8 V across R_D. The **AC ANALYSIS** at the end of the listing reveals that the voltage at the source (node 2) is 10 mV as set, but the voltage at the other end of the capacitor is 3 μV less due to the impedance of the capacitor at 10 kHz—certainly a drop to be ignored. The choice of 0.02 μ F for this frequency was obviously a good one. The voltages before and after the capacitor on the output side are exactly the same (to three places), revealing that the larger the capacitor, the closer the characteristics to a short circuit. The output of 6.275E-2 = 62.75 mV reflects a gain of 6.275. The **OPERATING POINT INFORMATION** reveals that I_D is 4 mA and g_m is 3.2 mS. Calculating the value of g_m from:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$= \frac{2\ (10\text{ mA})}{4\text{ V}}\left(1 - \frac{(-1.5\text{ V})}{(-4\text{ V})}\right)$$

$$= 3.125\text{ mS}$$

confirming our analysis.

```
 ****     CIRCUIT DESCRIPTION
******************************************************************************
* Schematics Netlist *

V_VDD          $N_0001 0 20V
C_C1           $N_0002 $N_0003  0.02uF
R_RG           $N_0004 $N_0003  10Meg
R_RD           $N_0005 $N_0001  2k
V_VGG          0 $N_0004 1.5V

.PRINT          AC
+ VM([$N_0003])

.PRINT          AC
+ VM([$N_0002])

.PRINT          AC
+ VM([$N_0005])

.PRINT          AC
+ VM([$N_0006])
C_C2           $N_0005 $N_0006  2uF
V_Vi           $N_0002 0  AC 10mV
+SIN 0 10mV 10kHz 0 0 0
R_RL           0 $N_0006  10Meg
J_J1           $N_0005 $N_0003 0 J2N3819-X

 ****     Junction FET MODEL PARAMETERS
******************************************************************************
               J2N3819-X
               NJF
         VTO   -4
        BETA  625.000000E-06
      LAMBDA    2.250000E-03
          IS   33.570000E-15
         ISR  322.400000E-15
       ALPHA  311.700000E-06
          VK  243.6
          RD    1
          RS    1
         CGD    1.600000E-12
         CGS    2.414000E-12
           M     .3622
       VTOTC   -2.500000E-03
     BETATCE    -.5
          KF    9.882000E-18

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
******************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

($N_0001)   20.0000                  ($N_0002)    0.0000

($N_0003)   -1.5000                  ($N_0004)   -1.5000

($N_0005)   12.0020                  ($N_0006)    0.0000

    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_VDD       -3.999E-03
    V_VGG       -1.366E-12

 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
******************************************************************************
**** JFETS

NAME         J_J1
MODEL        J2N3819-X
ID           4.00E-03
VGS         -1.50E+00
VDS          1.20E+01
GM           3.20E-03
GDS          8.76E-06
CGS          1.73E-12
CGD          6.07E-13 .
**** 10/08/97 11:23:59 ******** NT Evaluation PSpice (October 1996) **********

 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C
******************************************************************************
  FREQ        VM($N_0003)

   1.000E+04   9.997E-03


  FREQ        VM($N_0002)

   1.000E+04   1.000E-02


  FREQ        VM($N_0005)

   1.000E+04   6.275E-02


  FREQ        VM($N_0006)

   1.000E+04   6.275E-02
```

Figure 9.46 Output file for the network of Figure 9.45.

JFET Self-Bias Configuration

The self-bias configuration of Fig. 9.47 will be analyzed using the **J2N3819 JFET** from the library and then using an approximate equivalent circuit. It will be interesting to see if there are any major differences in solution.

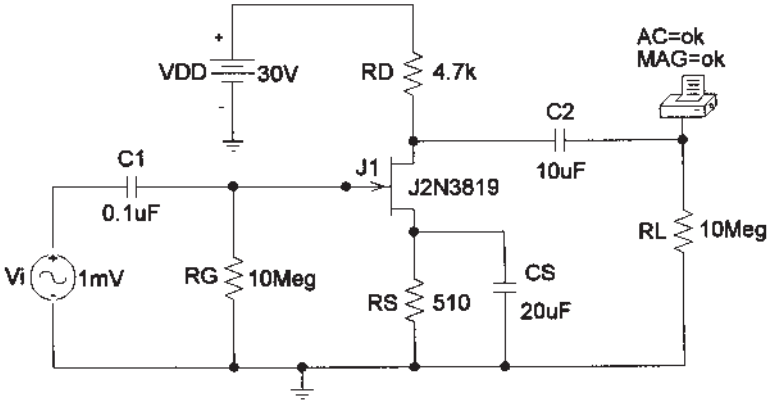


Figure 9.47 Self-bias configuration with an ac source.

Again, $V_P = -4$ V and $I_{DSS} = 10$ mA, resulting in a **Vto** of -4 and a **Beta** of 6.25E-4. The **Analysis** is run and the results of Fig. 9.48 obtained. The nodes are identified in the **Schematics Netlist** and the parameters in the **Junction FET MODEL PARAMETERS.** The **SMALL-SIGNAL BIAS SOLUTION** reveals that $V_{GS} = -1.7114$ V and $V_D = 14.228$ V—results that are very close to a hand-written solution of -1.68 V and 14.49 V. The **OPERATING POINT INFORMATION** reveals that I_D is 3.36 mA compared to a hand-calculated level of 3.3 mA and that g_m is 2.94 mS compared to a hand-calculated level of 2.90 mS. The **AC ANALYSIS** provides an output level of 13.3 mV at an angle of $-179.9°$, which compares well with a hand-calculated level of 13.63 mV at an angle of $-180°$. The results for JFETs are a lot closer than those obtained for transistors when we used the provided elements because of the special feature of having essentially infinite input impedance so that the gate current is zero ampere. Recall that for the transistor, V_{BE} is a function of the operating conditions.

We will now investigate the self-bias configuration using the approximate model as done for the transistor and see if there is an improvement in the results (compared to the hand-calculated levels). In this case, we need the voltage controlled current source **(VCCS)** found in the **ANALOG.slb** library as **G.** When selected, the **Description** reads **Voltage-controlled current source.** When placed on the schematic, it will appear as shown in Fig. 9.49. The sensing voltage is between the plus and minus sign, while the controlled current is between the other two external terminals.

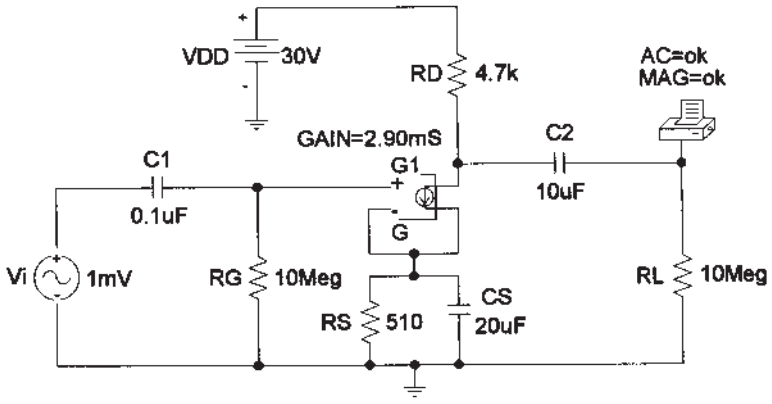


Figure 9.49 Network in Figure 9.47 following substitution of a **VCCS** for the JFET in the ac domain.

```
 ****     CIRCUIT DESCRIPTION
*******************************************************************************
* Schematics Netlist *


V_Vi          $N_0001 0  AC 1mV
+SIN 0V 1mV 10kHz 0 0 0
C_C1          $N_0001 $N_0002  0.1uF
R_RG          $N_0002 0  10Meg
V_VDD          $N_0003 0 30V
R_RD          $N_0003 $N_0004  4.7k
R_RS          $N_0005 0  510
C_CS          $N_0005 0  20uF
C_C2          $N_0004 $N_0006  10uF
R_RL          $N_0006 0  10Meg
J_J1          $N_0004 $N_0002 $N_0005 J2N3819-X
.
.PRINT          AC
+ VM([$N_0006])
+ VP([$N_0006])

 ****     Junction FET MODEL PARAMETERS

*******************************************************************************

               J2N3819-X
               NJF
        VTO    -4
       BETA   625.000000E-06
     LAMBDA     2.250000E-03
         IS    33.570000E-15
        ISR   322.400000E-15
      ALPHA   311.700000E-06
         VK   243.6
         RD     1
         RS     1
        CGD     1.600000E-12
        CGS     2.414000E-12
          M      .3622
      VTOTC    -2.500000E-03
    BETATCE     -.5
         KF     9.882000E-18

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

*******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

($N_0001)    0.0000                   ($N_0002) 13.95E-06

($N_0003)   30.0000                   ($N_0004)   14.2280

($N_0005)    1.7114                   ($N_0006)    0.0000


    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_Vi          0.000E+00
    V_VDD        -3.356E-03

    TOTAL POWER DISSIPATION   1.01E-01  WATTS

 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

*******************************************************************************

**** JFETS


NAME          J_J1
MODEL         J2N3819-X
ID            3.36E-03
VGS          -1.71E+00
VDS           1.25E+01
GM            2.94E-03
GDS           7.34E-06
CGS           1.68E-12
CGD           5.97E-13 .

 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C

*******************************************************************************

  FREQ        VM($N_0006) VP($N_0006)

   1.000E+04   1.330E-02  -1.799E+02
```

Figure 9.48 Output file for the network of Figure 9.47.

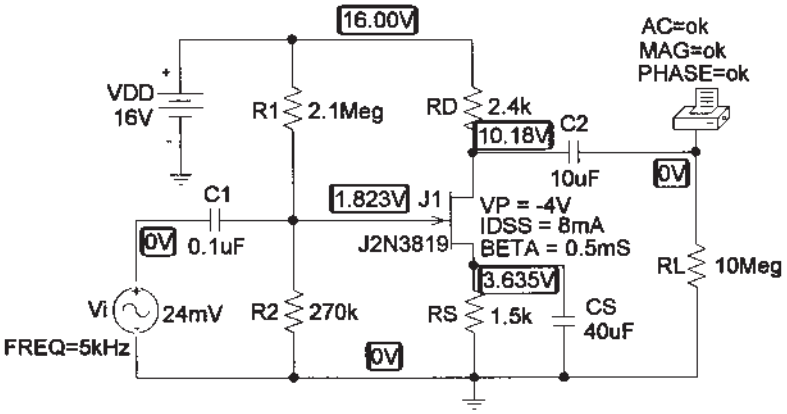


Figure 9.50 JFET voltage-divider configuration with an ac source.

Double-clicking on the schematic symbol will result in a **PartName: G** dialog box, in which the **GAIN(g_m)** can be set to the hand-calculated level of 2.90 mS.

The result of an analysis is a gain of 13.62—almost an exact match with the hand-written gain. This approach is certainly valid for an ac analysis, but if we examine the **SMALL-SIGNAL BIAS SOLUTION,** we find that the results are meaningless. Therefore, the equivalent appearing in Fig. 9.49 is only valid for the ac gain since the only parameter defined is the ac transconductance factor.

JFET Voltage-Divider Configuration

The last network to be analyzed in this PSpice Windows presentation is the voltage-divider configuration of Fig. 9.50. Note that the parameters chosen are different from those employed in earlier examples, with V_i at 24 mV and a frequency of 5 kHz. In addition, the dc levels are displayed and a plot of the output and input voltages will be obtained on the same screen.

After setting up the network, the source V_i must be set to the indicated parameters by double-clicking on the source and then sequentially double-clicking on each parameter and typing in the correct values. Each must be saved and then the display changed to print the magnitude of the ac voltage and the applied frequency. In this example, the JFET parameters were printed on the screen using the **ABC** icon. **BETA** is of course calculated from $I_{DSS}/|V_P|^2$. Under **Analysis-Probe Setup,** the option **Do not auto-run Probe** was chosen, and under **Setup, AC Sweep** was chosen and the frequency of 5 kHz entered. Finally, since we want the dc levels to be displayed, the **Display Results on Schematic** option is chosen under **Analysis,** and **Enable Voltage Display** is enabled. The resulting dc levels of Fig. 9.50 reveal that V_{GS} is 1.823 V − 3.635 V = −1.812 V, comparing very well with the −1.8 V calculated in Example 6.5. V_D is 10.18 V compared to the calculated level of 10.24 V, and V_{DS} is 10.18 V − 3.635 V = 6.545 V compared to 6.64 V.

For the ac solution, we can choose **Examine Output** under **Analysis** and find under **OPERATING POINT INFORMATION** that g_m is 2.22 mS, comparing very well with the hand-calculated value of 2.2 mS, and under **AC ANALYSIS** that the output ac voltage is 125.8 mV, resulting in a gain of 125.8 mV/24 mV = 5.24. The hand-calculated level is $g_m R_D$ = (2.2 mS)(2.4 kΩ) = 5.28. The ac waveform for the output can be obtained by first applying the sequence **Analysis-Probe Setup-Automatically run Probe after simulation.** Then, return to **Setup** under **Analysis,** and enable **Transient,** disable **AC Sweep,** and double-click **Transient** to obtain the **Transient** dialog box. For the frequency of 5 kHz, the period is 200 μs. A **Print Step** to 2 μs would then give us 100 plot points for each cycle. The **Final Time** will be 5 × 200 μs = 1 ms to show five cycles. The **No-Print Delay** will be 0s and the **Step Ceiling** 2μs. Then, click the **Trace** icon, choose **V(J1:d),** and the output waveform of Fig. 9.51 will appear. Choose **Plot-Add Plot-Trace-Add-V(Vi:+),** and both wave-

forms will appear as shown. Shift **SEL≫** to the bottom waveform by simply bringing the pointer to the left of the lower waveform and left-clicking the mouse once. Click the **Toggle cursor** icon, and a horizontal line will appear at the dc level of the output voltage at 10.184 V. A left click of the mouse and an intersecting set of lines will appear. Choose the **Cursor Peak** icon, and the intersection will automatically go to the peak value of the waveform (**A1** in the dialog box). The difference appearing in the dialog box is 125.496 mV, comparing well with the printed value in the output file. The difference is simply due to the number of points chosen for the plot; an increased number of plot points would have brought the two levels closer together.

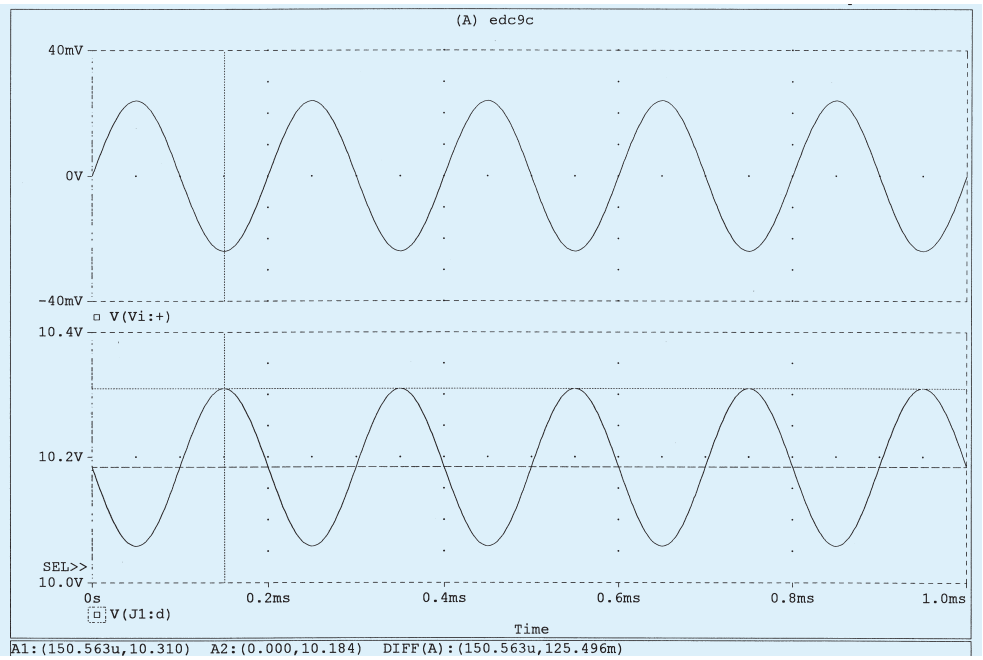


Figure 9.51 The ac drain and gate voltage for the voltage-divider JFET configuration of Figure 9.50.

§ 9.2 FET Small-Signal Model

PROBLEMS

1. Calculate g_{m0} for a JFET having device parameters $I_{DSS} = 15$ mA and $V_P = -5$ V.
2. Determine the pinch-off voltage of a JFET with $g_{m0} = 10$ mS and $I_{DSS} = 12$ mA.
3. For a JFET having device parameters $g_{m0} = 5$ mS and $V_P = -3.5$ V, what is the device current at $V_{GS} = 0$ V?
4. Calculate the value of g_m for a JFET ($I_{DSS} = 12$ mA, $V_P = -3$ V) at a bias point of $V_{GS} = -1$ V.
5. For a JFET having $g_m = 6$ mS at $V_{GS_Q} = -1$ V, what is the value of I_{DSS} if $V_P = -2.5$ V?
6. A JFET ($I_{DSS} = 10$ mA, $V_P = -5$ V) is biased at $I_D = I_{DSS}/4$. What is the value of g_m at that bias point?
7. Determine the value of g_m for a JFET ($I_{DSS} = 8$ mA, $V_P = -5$ V) when biased at $V_{GS_Q} = V_P/4$.
8. A specification sheet provides the following data (at a listed drain–source current)

$$y_{fs} = 4.5 \text{ mS}, \qquad y_{os} = 25\ \mu\text{S}$$

   At the listed drain–source current, determine:
   (a) g_m.
   (b) r_d.
9. For a JFET having specified values of $y_{fs} = 4.5$ mS and $y_{os} = 25\ \mu$S, determine the device output impedance, Z_o(FET), and device ideal voltage gain, A_v(FET).

10. If a JFET having a specified value of $r_d = 100\ \text{k}\Omega$ has an ideal voltage gain of $A_v(\text{FET}) = -200$, what is the value of g_m?

11. Using the transfer characteristic of Fig. 9.52:
(a) What is the value of g_{m0}?
(b) Determine g_m at $V_{GS} = -1.5$ V graphically.
(c) What is the value of g_m at $V_{GS_Q} = -1.5$ V using Eq. (9.6)? Compare with the solution to part (b).
(d) Graphically determine g_m at $V_{GS} = -2.5$ V.
(e) What is the value of g_m at $V_{GS_Q} = -2.5$ V using Eq. (9.6)? Compare with the solution to part (d).

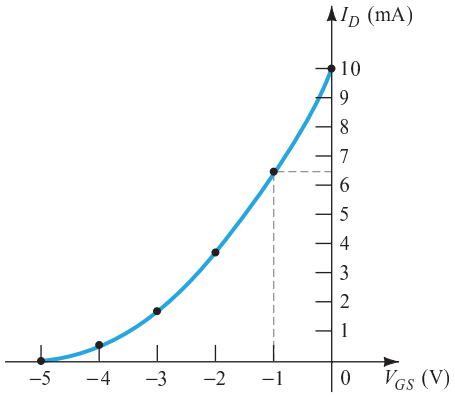


Figure 9.52 JFET transfer characteristic for Problem 11

12. Using the drain characteristic of Fig. 9.53:
(a) What is the value of r_d for $V_{GS} = 0$ V?
(b) What is the value of g_{m0} at $V_{DS} = 10$ V?

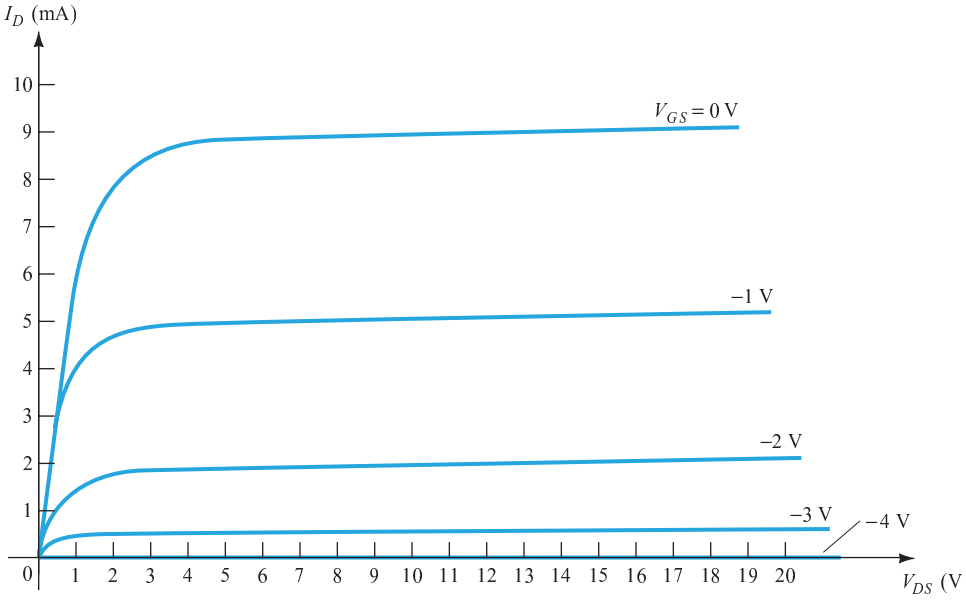


Figure 9.53 JFET drain characteristic for Problem 12

13. For a 2N4220 n-channel JFET (y_{fs}(minimum) = 750 μS, y_{os}(maximum) = 10 μS):
(a) What is the value of g_m?
(b) What is the value of r_d?

14. (a) Plot g_m vs. V_{GS} for an n-channel JFET with $I_{DSS} = 8$ mA and $V_P = -6$ V.
(b) Plot g_m vs. I_D for the same n-channel JFET as part (a).

15. Sketch the ac equivalent model for a JFET if $y_{fs} = 5.6$ mS and $y_{os} = 15\ \mu$S.

16. Sketch the ac equivalent model for a JFET if $I_{DSS} = 10$ mA, $V_P = -4$ V, $V_{GS_Q} = -2$ V, and $y_{os} = 25\ \mu$S.

§ 9.3 JFET Fixed-Bias Configuration

17. Determine Z_i, Z_o and A_v for the network of Fig. 9.54 if $I_{DSS} = 10$ mA, $V_P = -4$ V, and $r_d = 40$ kΩ.

18. Determine Z_i, Z_o, and A_v for the network of Fig. 9.54 if $I_{DSS} = 12$ mA, $V_P = -6$ V, and $y_{os} = 40\ \mu$S.

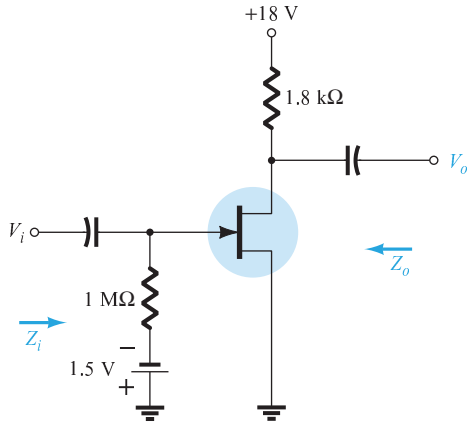


Figure 9.54 Fixed-bias amplifier for Problems 17 and 18

§ 9.4 JFET Self-Bias Configuration

19. Determine Z_i, Z_o, and A_v for the network of Fig. 9.55 if $y_{fs} = 3000\ \mu$S and $y_{os} = 50\ \mu$s.

20. Determine Z_i, Z_o, and A_v for the network of Fig. 9.56 if $I_{DSS} = 6$ mA, $V_P = -6$ V, and $y_{os} = 40\ \mu$S.

21. Determine Z_i, Z_o, and A_v for the network of Fig. 9.55 if the 20-μF capacitor is removed and the parameters of the network are the same as in Problem 19. Compare results with those of Problem 19.

22. Repeat Problem 19 if y_{os} is 10 μS. Compare the results to those of Problem 19.

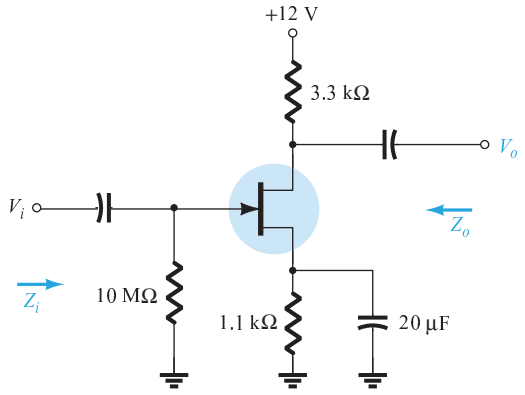


Figure 9.55 Problems 19, 21, and 46

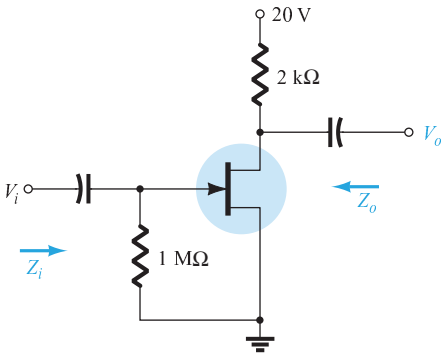


Figure 9.56 Self-bias configuration for Problems 20 and 47

§ 9.5 JFET Voltage-Divider Configuration

23. Determine Z_i, Z_o, and V_o for the network of Fig. 9.57 if $V_i = 20$ mV.

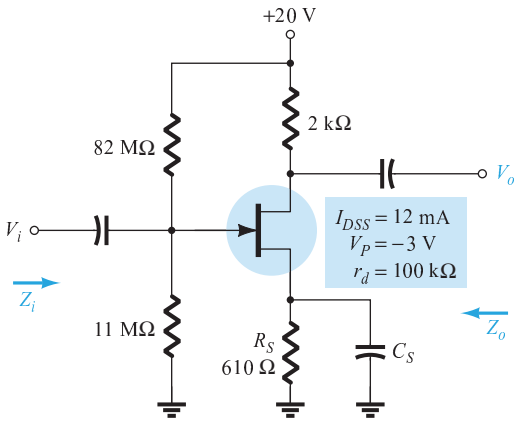


Figure 9.57 Problems 23–26 and 48

24. Determine Z_i, Z_o, and V_o for the network of Fig. 9.57 if $V_i = 20$ mV and the capacitor C_S is removed.

25. Repeat Problem 23 if $r_d = 20$ kΩ and compare results.

26. Repeat Problem 24 if $r_d = 20$ kΩ and compare results.

§ 9.6 JFET Source-Follower Configuration

27. Determine Z_i, Z_o, and A_v for the network of Fig. 9.58.

28. Repeat Problem 27 if $r_d = 20$ kΩ.

29. Determine Z_i, Z_o, and A_v for the network of Fig. 9.59.

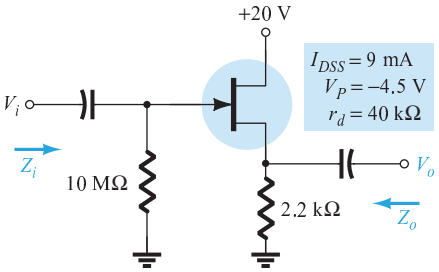


Figure 9.58 Problems 27 and 28

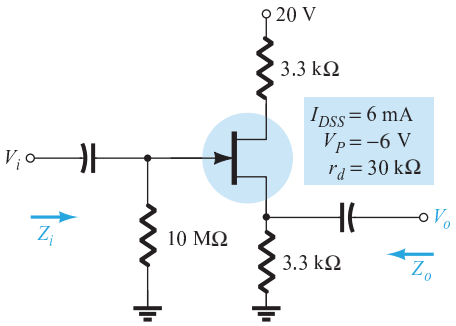


Figure 9.59 Problem 29

§ 9.7 JFET Common-Gate Configuration

30. Determine Z_i, Z_o, and V_o for the network of Fig. 9.60 if $V_i = 0.1$ mV.

31. Repeat Problem 30 if $r_d = 25$ kΩ.

32. Determine Z_i, Z_o, and A_v for the network of Fig. 9.61 if $r_d = 33$ kΩ.

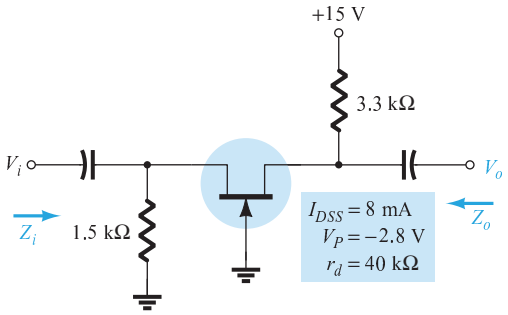


Figure 9.60 Problems 30, 31, and 49

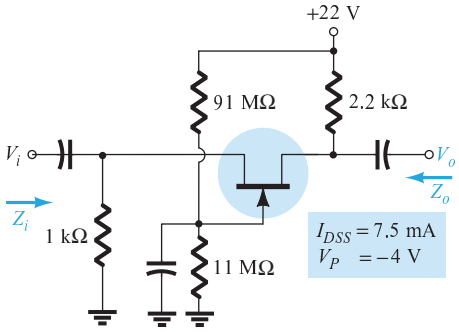


Figure 9.61 Problem 32

§ 9.8 Depletion-Type MOSFETs

33. Determine V_o for the network of Fig. 9.62 if $y_{os} = 20\ \mu$S.

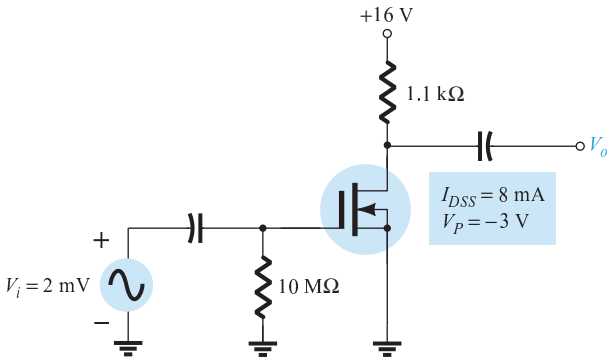


Figure 9.62 Problem 33

34. Determine Z_i, Z_o, and A_v for the network of Fig. 9.63 if $r_d = 60$ kΩ.

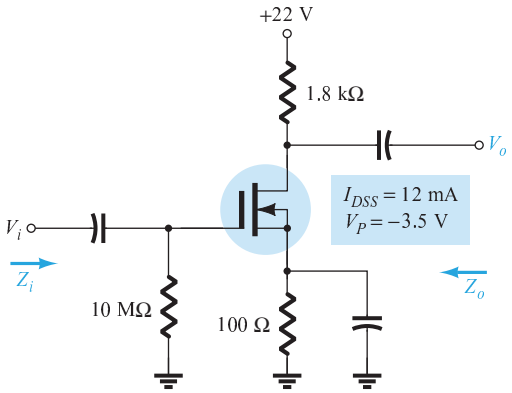


Figure 9.63 Problems 34, 35, and 50

35. Repeat Problem 34 if $r_d = 25\ \text{k}\Omega$.

36. Determine V_o for the network of Fig. 9.64 if $V_i = 4$ mV.

37. Determine Z_i, Z_o, and A_v for the network of Fig. 9.65.

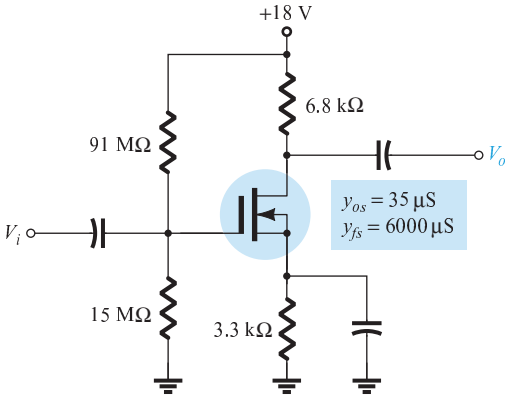


Figure 9.64 Problem 36

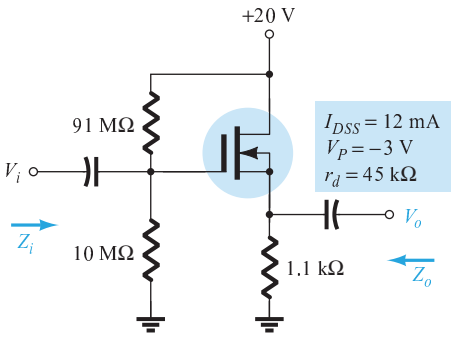


Figure 9.65 Problem 37

§ 9.10 E-MOSFET Drain-Feedback Configuration

38. Determine g_m for a MOSFET if $V_{GS(\text{Th})} = 3$ V and it is biased at $V_{GS_Q} = 8$ V. Assume $k = 0.3 \times 10^{-3}$.

39. Determine Z_i, Z_o, and A_v for the amplifier of Fig. 9.66 if $k = 0.3 \times 10^{-3}$.

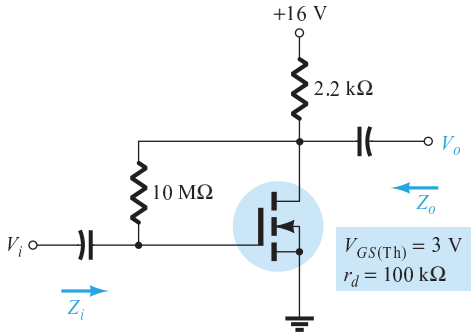


Figure 9.66 Problems 39, 40, and 51

40. Repeat Problem 39 if k drops to 0.2×10^{-3}. Compare results.

41. Determine V_o for the network of Fig. 9.67 if $V_i = 20$ mV.

42. Determine V_o for the network of Fig. 9.67 if $V_i = 4$ mV, $V_{GS(\text{Th})} = 4$ V, and $I_{D(\text{on})} = 4$ mA, with $V_{GS(\text{on})} = 7$ V and $y_{os} = 20\ \mu\text{S}$.

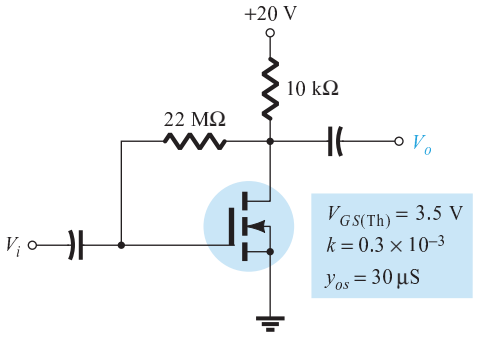


Figure 9.67 Problems 41 and 42

§ 9.11 E-MOSFET Voltage-Divider Configuration

43. Determine the output voltage for the network of Fig. 9.68 if $V_i = 0.8$ mV and $r_d = 40$ kΩ.

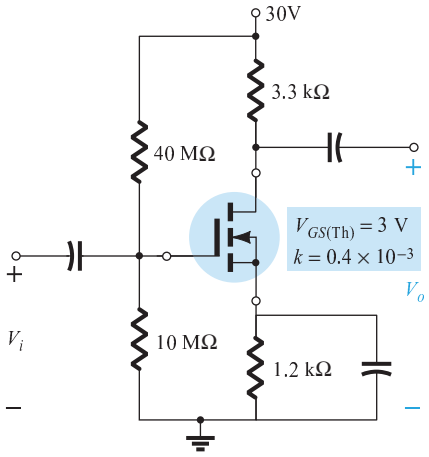


Figure 9.68 Problem 43

§ 9.12 Designing FET Amplifier Networks

44. Design the fixed-bias network of Fig. 9.69 to have a gain of 8.

45. Design the self-bias network of Fig. 9.70 to have a gain of 10. The device should be biased at $V_{GS_Q} = \frac{1}{3}V_P$.

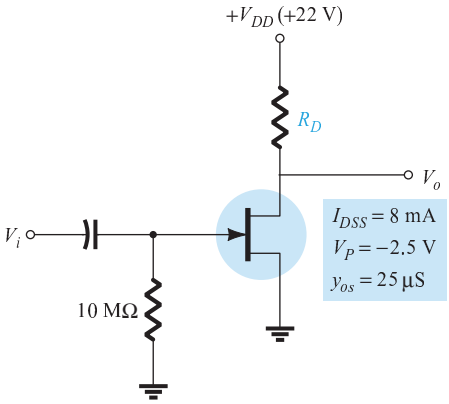


Figure 9.69 Problem 44

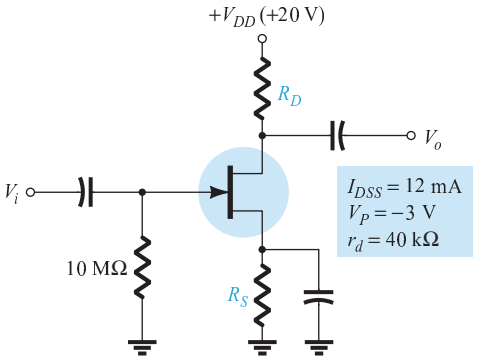


Figure 9.70 Problem 45

§ 9.13 PSpice Windows

46. Using PSpice Windows, determine the voltage gain for the network of Fig. 9.55.

47. Using PSpice Windows, determine the voltage gain for the network of Fig. 9.56.

48. Using PSpice Windows, determine the voltage gain for the network of Fig. 9.57.

49. Using PSpice Windows, determine the voltage gain for the network of Fig. 9.60.

50. Using PSpice Windows, determine the voltage gain for the network of Fig. 9.63.

51. Using PSpice Windows, determine the voltage gain for the network of Fig. 9.66.

R_s/R_L

CHAPTER

10 Systems Approach—Effects of R_s and R_L

10.1 INTRODUCTION

In recent years, the introduction of a wide variety of packaged networks and systems has generated an increasing interest in the systems approach to design and analysis. Fundamentally, this approach concentrates on the terminal characteristics of a package and treats each as a building block in the formation of the total package. The content of this chapter is a first step in developing some familiarity with this approach. The techniques introduced will be used in the remaining chapters and broadened as the need arises. The trend to packaged systems is quite understandable when you consider the enormous advances in the design and manufacturing of integrated circuits (ICs). The small IC packages contain stable, reliable, self-testing, sophisticated designs that would be quite bulky if built with discrete (individual) components. The systems approach is not a difficult one to apply once the basic definitions of the various parameters are correctly understood and the manner in which they are utilized is clearly demonstrated. In the next few sections, we develop the systems approach in a slow deliberate manner that will include numerous examples to make each salient point. If the content of this chapter is clearly and correctly understood, a first plateau in the understanding of system analysis will be accomplished.

10.2 TWO-PORT SYSTEMS

The description to follow can be applied to any two-port system—not only those containing BJTs and FETs—although the emphasis in this chapter is on these active devices. The emphasis in previous chapters on determining the two-port parameters for various configurations will be quite helpful in the analysis to follow. In fact, many of the results obtained in the last two chapters are utilized in the analysis to follow.

In Fig. 10.1, the important parameters of a two-port system have been identified. Note in particular the absence of a load and a source resistance. The impact of these important elements is considered in detail in a later section. For the moment recognize that the impedance levels and the gains of Fig. 10.1 are determined for no-load (absence of R_L) and no-source resistance (R_s) conditions.

If we take a "Thévenin look" at the output terminals we find with V_i set to zero that

$$Z_{\text{Th}} = Z_o = R_o \tag{10.1}$$

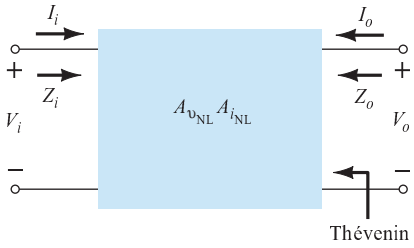


Figure 10.1 Two-port system.

E_{Th} is the open-circuit voltage between the output terminals identified as V_o. However,

$$A_{v_{\text{NL}}} = \frac{V_o}{V_i}$$

and

$$V_o = A_{v_{\text{NL}}} V_i$$

so that

$$\boxed{E_{\text{Th}} = A_{v_{\text{NL}}} V_i} \tag{10.2}$$

Note the use of the additional subscript notation "NL" to identify a no-load voltage gain.

Substituting the Thévenin equivalent circuit between the output terminals will result in the output configuration of Fig. 10.2. For the input circuit the parameters V_i and I_i are related by $Z_i = R_i$, permitting the use of R_i to represent the input circuit. Since our present interest is in BJT and FET amplifiers, both Z_o and Z_i can be represented by resistive elements.

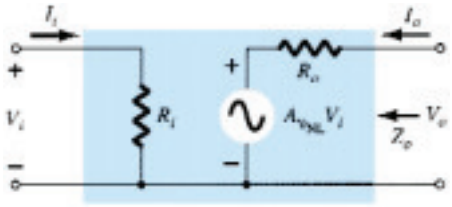


Figure 10.2 Substituting the internal elements for the two-port system of Fig. 10.1.

Before continuing let us check the results of Fig. 10.2 by finding Z_o and $A_{v_{\text{NL}}}$ in the usual manner. To find Z_o, V_i is set to zero, resulting in $A_{v_{\text{NL}}} V_i = 0$, permitting a short-circuit equivalent for the source. The result is an output impedance equal to R_o as originally defined. The absence of a load will result in $I_o = 0$, and the voltage drop across the impedance R_o will be 0 V. The open-circuit output voltage is therefore $A_{v_{\text{NL}}} V_i$, as it should be. Before looking at an example, take note of the fact that A_i does not appear in the two-port model of Fig. 10.2 and in fact is seldom part of the two-port system analysis of active devices. This is not to say that the quantity is seldom calculated, but it is most frequently calculated from the expression $A_i = -A_v(Z_i/R_L)$, where R_L is the defined load for the analysis of interest.

EXAMPLE 10.1

For the fixed-bias transistor network of Fig. 10.3 (Example 8.1), sketch the two-port equivalent of Fig. 10.2.

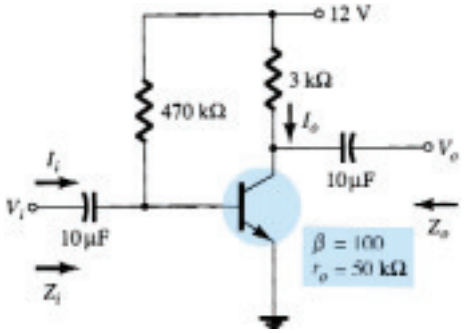


Figure 10.3 Example 10.1.

Solution

From Example 8.1,

$$Z_i = 1.069\ \text{k}\Omega$$
$$Z_o = 3\ \text{k}\Omega$$
$$A_{v_{\text{NL}}} = -280.11$$

Using the information above, the two-port equivalent of Fig. 10.4 can be drawn. Note in particular the negative sign associated with the controlled voltage source, revealing an opposite polarity for the controlled source than that indicated in the figure. It also reveals a 180° phase-shift between the input and output voltages.

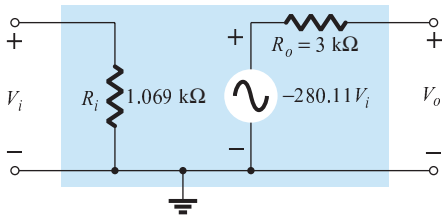


Figure 10.4 Two-port equivalent for the parameters specified in Example 10.1.

In Example 10.1, $R_C = 3\ \text{k}\Omega$ was included in defining the no-load voltage gain. Although this need not be the case (R_C could be defined as the load resistor in Chapter 8), the analysis of this chapter will assume that all biasing resistors are part of the no-load gain and that a loaded system requires an additional load R_L connected to the output terminals.

A second format for Fig. 10.2, particularly popular with op-amps (operational amplifiers), appears in Fig. 10.5. The only change is the general appearance of the model.

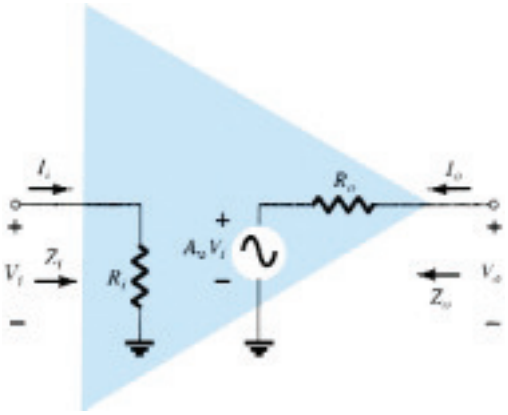


Figure 10.5 Operational amplifier (op-amp) notation.

10.3 EFFECT OF A LOAD IMPEDANCE (R_L)

In this section, the effect of an applied load is investigated using the two-port model of Fig. 10.2. The model can be applied to any current- or voltage-controlled amplifier. $A_{v_{\text{NL}}}$ is, as defined earlier, the gain of the system without an applied load. R_i and R_o are the input and output impedances of the amplifier as defined by the configuration. Ideally, all the parameters of the model are unaffected by changing loads or

source resistances (as normally encountered for op-amps to be described in Chapter 14). However, for some transistor amplifier configurations, R_i can be quite sensitive to the applied load, while for others R_o can be sensitive to the source resistance. In any case, once $A_{v_{NL}}$, R_i, and R_o are defined for a particular configuration, the equations about to be derived can be employed.

Applying a load to the two-port system of Fig. 10.2 will result in the configuration of Fig. 10.6. Applying the voltage-divider rule to the output circuit will result in

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}} \tag{10.3}$$

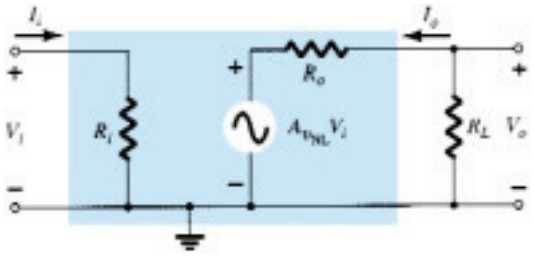


Figure 10.6 Applying a load to the two-port system of Fig. 10.2.

Since the ratio $R_L/(R_L + R_o)$ will always be less than 1:

The loaded voltage gain of an amplifier is always less than the no-load level.

Note also that the formula for the voltage gain does not include the input impedance or current gain.

Although the level of R_i may change with the configuration, the applied voltage and input current will always be related by

$$\boxed{I_i = \frac{V_i}{Z_i} = \frac{V_i}{R_i}} \tag{10.4}$$

Defining the output current as the current through the load will result in

$$\boxed{I_o = -\frac{V_o}{R_L}} \tag{10.5}$$

with the minus sign occurring due to the defined direction for I_o in Fig. 10.6.

The current gain is then determined by

$$A_i = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i} = -\frac{V_o}{V_i}\frac{Z_i}{R_L}$$

and

$$\boxed{A_i = -A_v\frac{Z_i}{R_L}} \tag{10.6}$$

for the unloaded situation. In general, therefore, the current gain can be obtained from the voltage gain and impedance parameters Z_i and R_L. The next example will demonstrate the usefulness and validity of Eqs. (10.3) through (10.6).

EXAMPLE 10.2

In Fig. 10.7, a load has been applied to the fixed-bias transistor amplifier of Example 10.1 (Fig. 10.3).

(a) Determine the voltage and current gain using the two-port systems approach defined by the model of Fig. 10.4.

(b) Determine the voltage and current gain using the r_e model and compare results.

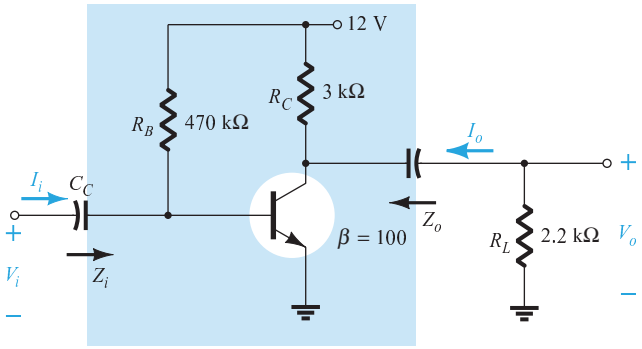


Figure 10.7 Example 10.2.

Solution

(a) Recall from Example 10.1 that

$$Z_i = 1.071\ \text{k}\Omega \qquad (\text{with } r_e = 10.71\ \Omega \text{ and } \beta = 100)$$

$$Z_o = 3\ \text{k}\Omega$$

$$A_{v_{\text{NL}}} = -280.11$$

Applying Eq. (10.3) yields

$$A_v = \frac{R_L}{R_L + R_o} A_{v_{\text{NL}}}$$

$$= \frac{2.2\ \text{k}\Omega}{2.2\ \text{k}\Omega + 3\ \text{k}\Omega}(-280.11)$$

$$= (0.423)(-280.11)$$

$$= \mathbf{-118.5}$$

For the current gain,

$$A_i = -A_v \frac{Z_i}{R_L}$$

In this case, Z_i is unaffected by the applied load and

$$A_i = -(-118.5)\frac{1.071\ \text{k}\Omega}{2.2\ \text{k}\Omega} = \mathbf{57.69}$$

(b) Substituting the r_e model will result in the network of Fig. 10.8. Note in particular that the applied load is in parallel with the collector resistor R_C defining a net parallel resistance

$$R'_L = R_C \| R_L = 3\ \text{k}\Omega \| 2.2\ \text{k}\Omega = 1.269\ \text{k}\Omega$$

The output voltage

$$V_o = -\beta I_B R'_L$$

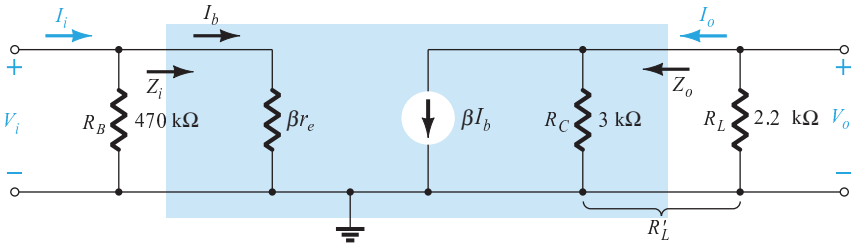


Figure 10.8 Substituting the r_e model in the ac equivalent network of Fig. 10.7.

with
$$I_b = \frac{V_i}{\beta r_e}$$

and
$$V_o = -\beta \frac{V_i}{\beta r_e} R'_L$$

so that
$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{R'_L}{r_e} = -\frac{R_C \| R_L}{r_e}} \qquad (10.7)$$

Substituting values gives

$$A_v = -\frac{1.269\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-118.5}$$

as obtained above. For the current gain, by the current-divider rule,

$$I_b = \frac{(470\ \text{k}\Omega) I_i}{470\ \text{k}\Omega + 1.071\ \text{k}\Omega} = 0.9977 I_i \cong I_i$$

and
$$I_o = \frac{3\ \text{k}\Omega(\beta I_b)}{3\ \text{k}\Omega + 2.2\ \text{k}\Omega}$$
$$= 0.5769 \beta I_b$$

so that
$$A_i = \frac{I_o}{I_i} = \frac{0.5769 \beta I_b}{I_i} = \frac{0.5769 \beta I_i}{I_i}$$
$$= 0.5769(100) = \mathbf{57.69}$$

as obtained using Eq. (10.6).

Example 10.2 demonstrated two techniques to solve the same problem. Although any network can be solved using the r_e model approach, the advantage of the systems approach is that once the two-port parameters of a system are known, the effect of changing the load can be determined directly from Eq. (10.3). No need to go back to the ac equivalent model and analyze the entire network. The advantages of the systems approach are similar to those associated with applying Thévenin's theorem. They permit concentrating on the effects of the load without having to re-examine the entire network. Of course, if the network of Fig. 10.7 were presented for analysis without the unloaded parameters, it would be a toss-up as to which approach would yield the desired results in the most direct, efficient manner. However, keep in mind that the "package" approach is the developing trend. When you purchase a "system" the two-port parameters are provided, and as with any trend, the user must be aware of how to utilize the given data.

The AC Load Line

For a system such as appearing in Fig. 10.9a, the dc load line was drawn on the output characteristics as shown in Fig. 10.9b. The load resistance did not contribute to the dc load line since it was isolated from the biasing network by the coupling capacitor (C_C). For the ac analysis, the coupling capacitors are replaced by a short-circuit equivalence that will place the load and collector resistors in a parallel arrangement defined by

$$R'_L = R_C \| R_L$$

The effect on the load line is shown in Fig. 10.9b with the levels to determine the new axes intersections. Note of particular importance that the ac and dc load lines pass through the same Q-point—a condition that must be satisfied to ensure a common solution for the network under dc and/or ac conditions.

For the unloaded situation, the application of a relatively small sinusoidal signal to the base of the transistor could cause the base current to swing from a level of I_{B_2} to I_{B_4} as shown in Fig. 10.9b. The resulting output voltage v_{ce} would then have the swing appearing in the same figure. The application of the same signal for a loaded situation would result in the same swing in the I_B level, as shown in Fig. 10.9b. The result, however, of the steeper slope of the ac load line is a smaller output voltage

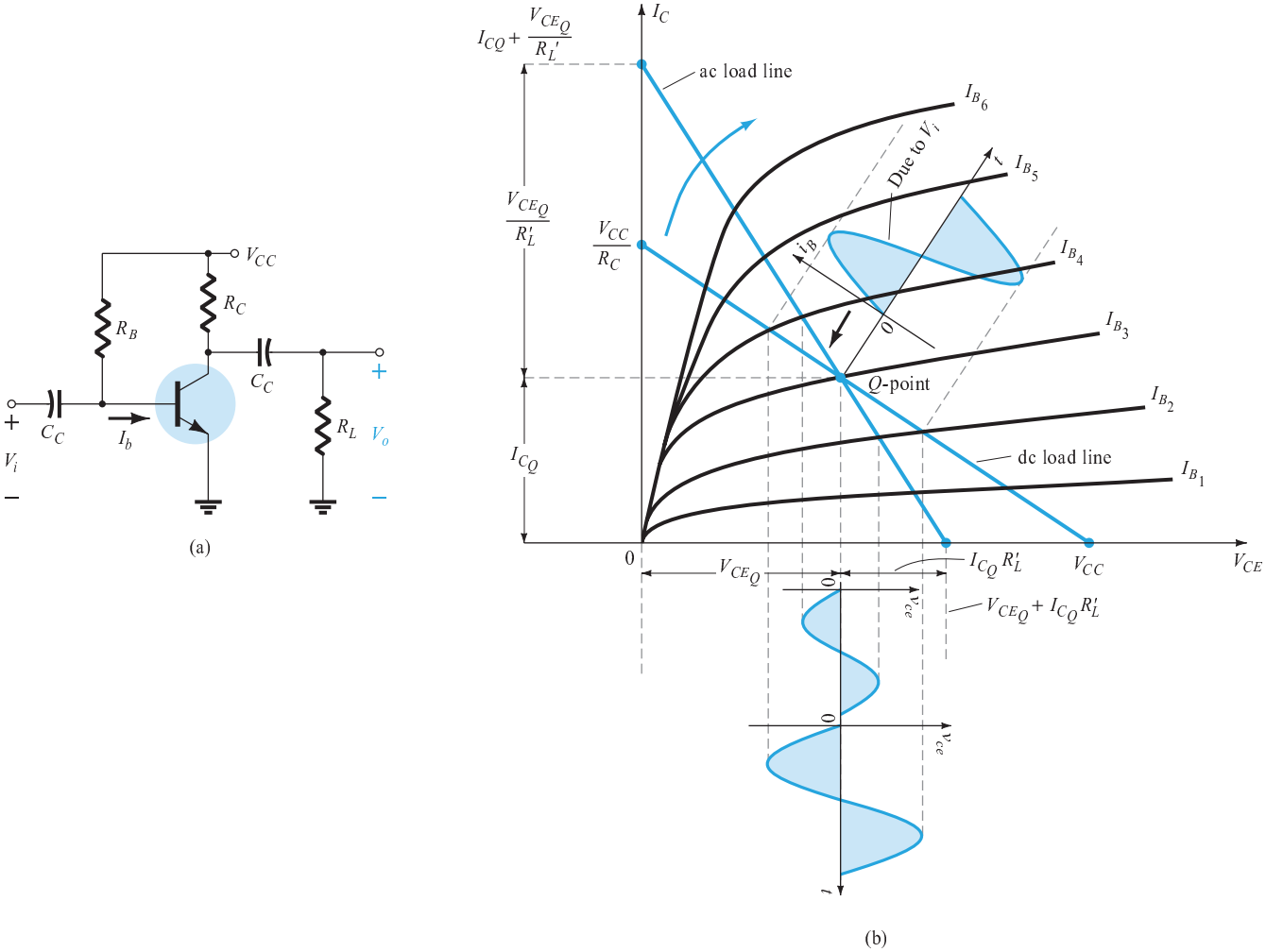


Figure 10.9 Demonstrating the differences between the dc and ac load lines.

swing (v_{ce}) and a drop in the gain of the system as demonstrated in the numerical analysis above. It should be obvious from the intersection of the ac load line on the vertical axis that the smaller the level of R'_L, the steeper the slope and the smaller the ac voltage gain. Since R'_L is smaller for reduced levels of R_L, it should be fairly clear that:

For a particular design, the smaller the level of R_L, the lower the level of ac voltage gain.

10.4 EFFECT OF THE SOURCE IMPEDANCE (R_S)

Our attention will now turn to the input side of the two-port system and the effect of an internal source resistance on the gain of an amplifier. In Fig. 10.10, a source with an internal resistance has been applied to the basic two-port system. The definitions of Z_i and $A_{v_{NL}}$ are such that:

The parameters Z_i and $A_{v_{NL}}$ of a two-port system are unaffected by the internal resistance of the applied source.

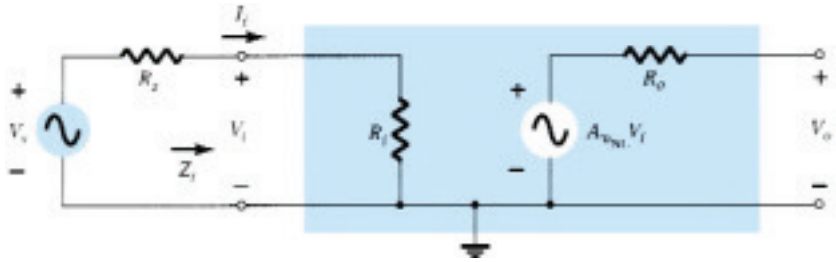


Figure 10.10 Including the effects of the source resistance R_s.

However:

The output impedance may be affected by the magnitude of R_s.

Recall Eq. (8.110) for the complete hybrid equivalent model. The fraction of the applied signal reaching the input terminals of the amplifier of Fig. 10.10 is determined by the voltage-divider rule. That is,

$$V_i = \frac{R_i V_s}{R_i + R_s} \tag{10.8}$$

Equation (10.8) clearly shows that the larger the magnitude of R_s, the less the voltage at the input terminals of the amplifier. In general, therefore:

For a particular amplifier, the larger the internal resistance of a signal source the less the overall gain of the system.

For the two-port system of Fig. 10.10,

$$V_o = A_{v_{NL}} V_i$$

and

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

so that

$$V_o = A_{v_{NL}} \frac{R_i}{R_i + R_s} V_s$$

and

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}} \tag{10.9}$$

The result clearly supports the statement above regarding the reduction in gain with increase in R_s. Using Eq. (10.9), if $R_s = 0\ \Omega$ (ideal voltage source), $A_{v_s} = A_{v_{NL}}$, which is the maximum possible value.

The input current is also altered by the presence of a source resistance as follows:

$$I_i = \frac{V_s}{R_s + R_i} \tag{10.10}$$

EXAMPLE 10.3

In Fig. 10.11, a source with an internal resistance has been applied to the fixed-bias transistor amplifier of Example 10.1 (Fig. 10.3).

(a) Determine the voltage gain $A_{v_s} = V_o/V_s$. What percent of the applied signal appears at the input terminals of the amplifier?

(b) Determine the voltage gain $A_{v_s} = V_o/V_s$ using the r_e model.

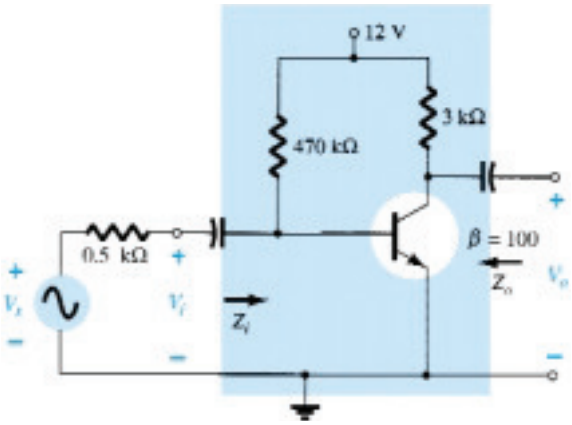


Figure 10.11 Example 10.3.

Solution

(a) The two-port equivalent for the network appears in Fig. 10.12.

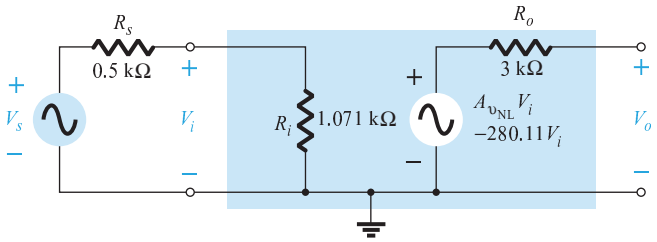


Figure 10.12 Substituting the two-port equivalent network for the fixed-bias transistor amplifier of Fig. 10.11.

$$\text{Eq. (10.9):}\quad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}} = \frac{1.071\ \text{k}\Omega}{1.071\ \text{k}\Omega + 0.5\ \text{k}\Omega}(-280.11)$$

$$= (0.6817)(-280.11)$$

$$= \mathbf{-190.96}$$

$$\text{Eq. (10.8):}\quad V_i = \frac{R_i V_s}{R_i + R_s} = \frac{(1.071\ \text{k}\Omega)V_s}{1.071\ \text{k}\Omega + 0.5\ \text{k}\Omega} = 0.6817 V_s$$

or **68.2%** of the available signal reached the amplifier and 31.8% was lost across the internal resistance of the source.

(b) Substituting the r_e model will result in the equivalent circuit of Fig. 10.13. Solving for V_o gives

$$V_o = -(100I_b)3\ \text{k}\Omega$$

with
$$Z_i \cong \beta r_e \text{ and } I_b \cong I_i = \frac{V_s}{R_s + \beta r_e} = \frac{V_s}{1.571\ \text{k}\Omega}$$

and
$$V_o = -100\left(\frac{V_s}{1.571\ \text{k}\Omega}\right)3\ \text{k}\Omega$$

so that
$$A_{v_s} = \frac{V_o}{V_s} = -\frac{(100)(3\ \text{k}\Omega)}{1.57\ \text{k}\Omega}$$
$$= \mathbf{-190.96}$$

as above.

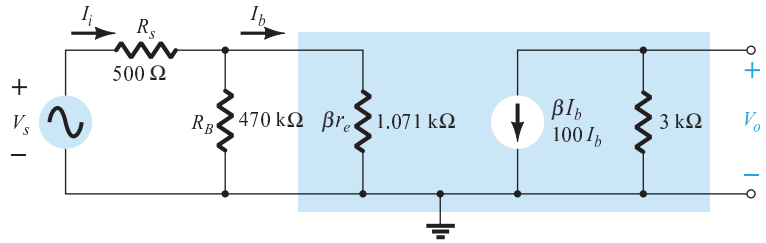


Figure 10.13 Substituting the r_e equivalent circuit for the fixed-bias transistor amplifier of Fig. 10.11.

Throughout the analysis above, note that R_s was not included in the definition of Z_i for the two-port system. Of course, the resistance "seen" by the source is now $R_s + Z_i$, but R_s remains a quantity associated only with the applied source.

Note again in Example 10.3 that the same results were obtained with the systems approach and using the r_e model. Certainly, if the two-port parameters are available, they should be applied. If not, the approach to the solution is simply a matter of preference.

10.5 COMBINED EFFECT OF R_s AND R_L

The effects of R_s and R_L have now been demonstrated on an individual basis. The next natural question is how the presence of both factors in the same network will affect the total gain. In Fig. 10.14, a source with an internal resistance R_s and a load R_L have been applied to a two-port system for which the parameters Z_i, $A_{v_{NL}}$, and Z_o have been specified. For the moment, let us assume that Z_i and Z_o are unaffected by R_L and R_s, respectively.

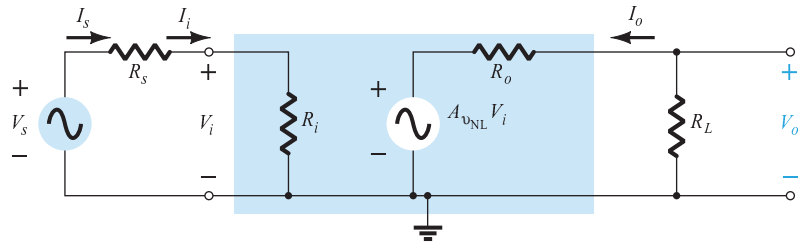


Figure 10.14 Considering the effects of R_s and R_L on the gain of an amplifier.

At the input side we find

$$\text{Eq. (10.8): } V_i = \frac{R_i V_s}{R_i + R_s}$$

or

$$\boxed{\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}} \tag{10.11}$$

and at the output side,

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o}$$

or

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_L A_{V_{NL}}}{R_L + R_o}} \tag{10.12}$$

For the total gain $A_{v_s} = V_o/V_s$, the following mathematical steps can be performed:

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i}\frac{V_i}{V_s} \tag{10.13}$$

and substituting Eqs. (10.11) and (10.12) will result in

$$A_{v_s} = \frac{R_L A_{v_{NL}}}{R_L + R_o}\frac{R_i}{R_i + R_s}$$

and

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s}\frac{R_L}{R_L + R_o}A_{v_{NL}}} \tag{10.14}$$

Since $I_i = V_i/R_i$, as before,

$$\boxed{A_i = -A_v\frac{R_i}{R_L}} \tag{10.15}$$

or using $I_s = V_s/(R_s + R_i)$,

$$\boxed{A_{i_s} = -A_{v_s}\frac{R_s + R_i}{R_L}} \tag{10.16}$$

However, $I_i = I_s$, so Eqs. (10.15) and (10.16) will generate the same result. Equation (10.14) clearly reveals that both the source and the load resistance will reduce the overall gain of the system. In fact:

The larger the source resistance and/or smaller the load resistance, the less the overall gain of an amplifier.

The two reduction factors of Eq. (10.14) form a product that has to be carefully considered in any design procedure. It is not sufficient to ensure that R_s is relatively small if the impact of the magnitude of R_L is ignored. For instance, in Eq. (10.14), if the first factor is 0.9 and the second factor is 0.2, the product of the two results in an overall reduction factor equal to (0.9)(0.2) = 0.18, which is close to the lower factor. The effect of the excellent 0.9 level was completely wiped out by the significantly lower second multiplier. If both were 0.9-level factors, the net result would be (0.9)(0.9) = 0.81, which is still quite high. Even if the first were 0.9 and the second 0.7, the net result of 0.63 would still be respectable. In general, therefore, for good overall gain the effect of both R_s and R_L must be evaluated individually and as a product.

EXAMPLE 10.4

For the single-stage amplifier of Fig. 10.15, with $R_L = 4.7\ \text{k}\Omega$ and $R_s = 0.3\ \text{k}\Omega$, determine:

(a) A_{v_s}.

(b) $A_v = V_o/V_i$.

(c) A_i.

The two-port parameters for the fixed-bias configuration are $Z_i = 1.071\ \text{k}\Omega$, $Z_o = 3\ \text{k}\Omega$, and $A_{v_{\text{NL}}} = -280.11$.

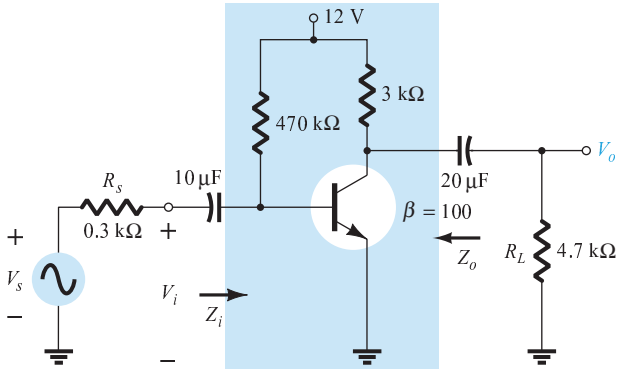


Figure 10.15 Example 10.4

Solution

(a) Eq. (10.14): $A_{v_s} = \dfrac{V_o}{V_s} = \dfrac{R_i}{R_i + R_s}\dfrac{R_L}{R_L + R_o}A_{v_{\text{NL}}}$

$$= \left(\frac{1.071\ \text{k}\Omega}{1.071\ \text{k}\Omega + 0.3\ \text{k}\Omega}\right)\left(\frac{4.7\ \text{k}\Omega}{4.7\ \text{k}\Omega + 3\ \text{k}\Omega}\right)(-280.11)$$

$$= (0.7812)(0.6104)(-280.11)$$

$$= (0.4768)(-280.11)$$

$$= \mathbf{-133.57}$$

(b) $A_v = \dfrac{V_o}{V_i} = \dfrac{R_L A_{v_{\text{NL}}}}{R_L + R_o} = \dfrac{(4.7\ \text{k}\Omega)(-280.11)}{4.7\ \text{k}\Omega + 3\ \text{k}\Omega}$

$$= (0.6104)(-280.11) = \mathbf{-170.98}$$

(c) $A_i = -A_v\dfrac{R_i}{R_L} = -(-170.98)\left(\dfrac{1.071\ \text{k}\Omega}{4.7\ \text{k}\Omega}\right)$

$$= \mathbf{38.96}$$

or $A_{i_s} = -A_{v_s}\dfrac{R_s + R_i}{R_L} = -(-133.57)\left(\dfrac{1.071\ \text{k}\Omega + 0.3\ \text{k}\Omega}{4.7\ \text{k}\Omega}\right)$

$$= \mathbf{38.96}$$

as above.

10.6 BJT CE NETWORKS

The fixed-bias configuration has been employed throughout the analysis of the early sections of this chapter to clearly show the effects of R_s and R_L. In this section, various CE configurations are examined with a load and a source resistance. A detailed analysis will not be performed for each configuration since they follow a very similar path to that demonstrated in the last few sections.

Fixed Bias

For the fixed-bias configuration examined in detail in recent sections, the system model with a load and source resistance will appear as shown in Fig. 10.16. In general,

$$V_o = \frac{R_L}{R_L + R_o} A_{v_{NL}} V_i$$

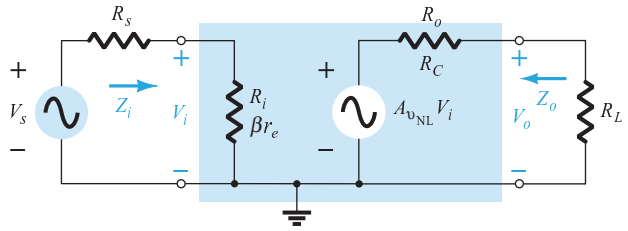


Figure 10.16 Fixed-bias configuration with R_s and R_L

Substituting Eq. (8.6), $A_{v_{NL}} = -R_C/r_e$ and $R_o = R_C$,

$$V_o = -\frac{R_L(-R_C/r_e)V_i}{R_L + R_C}$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{R_L R_C}{R_L + R_C}\frac{1}{r_e}$$

but

$$R_L \| R_C = \frac{R_L R_C}{R_L + R_C}$$

and

$$\boxed{A_v = -\frac{R_L \| R_C}{r_e}} \tag{10.17}$$

If the r_e model were substituted for the transistor in the fixed-bias configuration, the network of Fig. 10.17 would result, clearly revealing that R_C and R_L are in parallel.

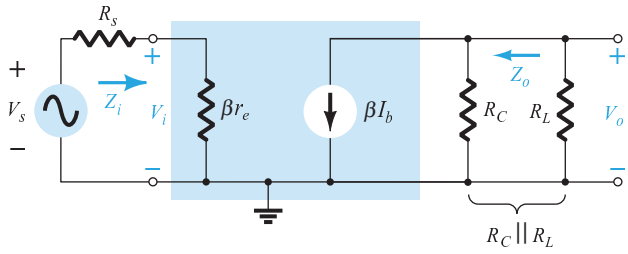


Figure 10.17 Fixed-bias configuration with the substitution of the r_e model.

For the voltage gain A_{v_s} of Fig. 10.16,

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

and

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

with

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\frac{V_o}{V_i}$$

so that
$$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_v \tag{10.18}$$

Since the load is connected to the collector terminal of the common-emitter configuration,
$$Z_i = \beta r_e \tag{10.19}$$

and
$$Z_o = R_C \tag{10.20}$$

as obtained earlier.

Voltage-Divider Bias

For the loaded voltage-divider bias configuration of Fig. 10.18, the load is again connected to the collector terminal and Z_i remains
$$Z_i \cong R' \| \beta r_e \qquad (R' = R_1 \| R_2) \tag{10.21}$$

and for the system's output impedance
$$Z_o = R_C \tag{10.22}$$

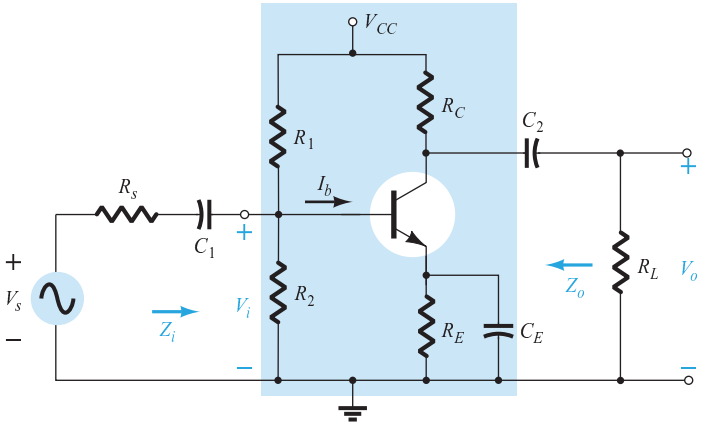


Figure 10.18 Voltage-divider bias configuration with R_s and R_L.

In the small-signal ac model, R_C and R_L will again be in parallel and
$$A_v = -\frac{R_C \| R_L}{r_e} \tag{10.23}$$

with
$$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_v \tag{10.24}$$

CE Unbypassed Emitter Bias

For the common-emitter unbypassed emitter-bias configuration of Fig. 10.19, Z_i remains independent of the applied load and
$$Z_i \cong R_B \| \beta R_E \tag{10.25}$$

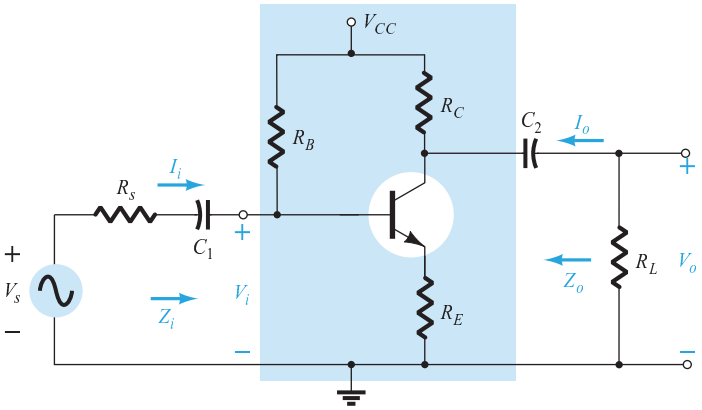


Figure 10.19 CE unbypassed emitter-bias configuration with R_s and R_L.

For the output impedance,

$$Z_o = R_C \tag{10.26}$$

For the voltage gain, the resistance R_C will again drop down in parallel with R_L and

$$A_v = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{R_E} \tag{10.27}$$

with

$$A_{v_s} = \frac{V_o}{V_s} = \frac{Z_i}{Z_i + R_s} A_v \tag{10.28}$$

and

$$A_i = \frac{I_o}{I_i} = -A_v \frac{Z_i}{R_L} \tag{10.29}$$

but keep in mind that $I_i = I_s = V_s/(R_s + Z_i) = V_i/Z_i$.

Collector Feedback

To keep with our connection of the load to the collector terminal the next configuration to be examined is the collector feedback configuration of Fig. 10.20. In the small-signal ac model of the system, R_C and R_L will again drop down in parallel and

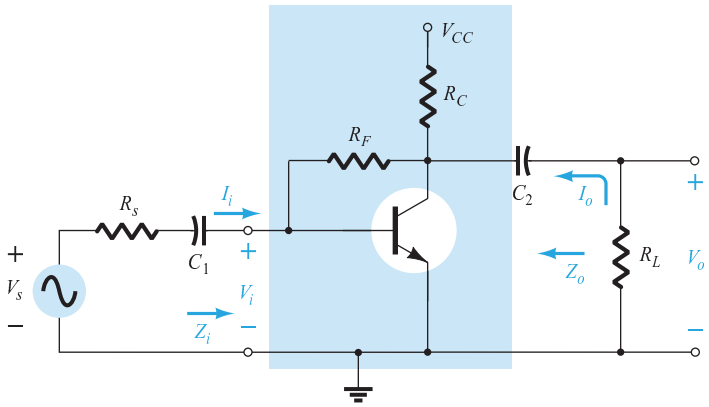


Figure 10.20 Collector feedback configuration with R_s and R_L.

$$A_v = -\frac{R_C \| R_L}{r_e} \tag{10.30}$$

with

$$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_v \tag{10.31}$$

The output impedance

$$Z_o \cong R_C \| R_F \tag{10.32}$$

and

$$Z_i = \beta r_e \| \frac{R_F}{|A_v|} \tag{10.33}$$

The fact that A_v [Eq. (10.30)] is a function of R_L will alter the level of Z_i from the no-load value. Therefore, if the no-load model is available, the level of Z_i must be modified as demonstrated in the next example.

EXAMPLE 10.5

The collector feedback amplifier of Fig. 10.21 has the following no-load system parameters: $A_{v_{NL}} = -238.94$, $Z_o = R_C \| R_F = 2.66\ \text{k}\Omega$, and $Z_i = 0.553\ \text{k}\Omega$, with $r_e = 11.3\ \Omega$, and $\beta = 200$. Using the systems approach, determine:

(a) A_v.

(b) A_{v_s}.

(c) A_i.

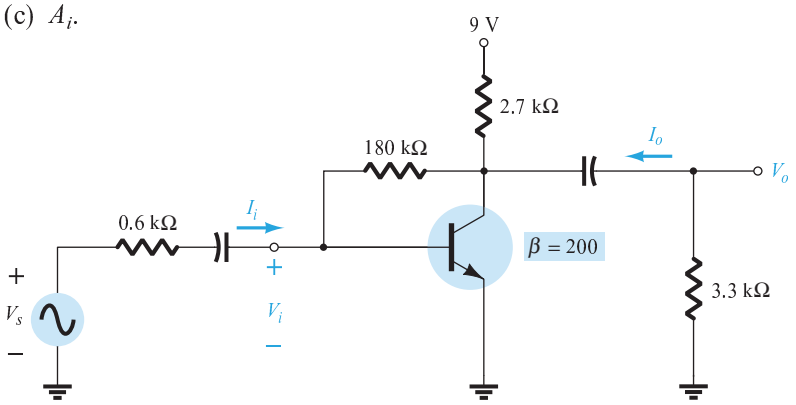


Figure 10.21 Example 10.5.

Solution

(a) For the two-port system:

$$A_v = -\frac{R_C \| R_L}{r_e} = -\frac{2.7\ \text{k}\Omega \| 3.3\ \text{k}\Omega}{11.3\ \Omega}$$

$$= -\frac{1.485\ \text{k}\Omega}{11.3\ \Omega} = \mathbf{-131.42}$$

with

$$Z_i = \beta r_e \| \frac{R_F}{|A_v|} = (200)(11.3\ \Omega) \| \frac{180\ \text{k}\Omega}{131.42}$$

$$= 2.26\ \text{k}\Omega \| 1.37\ \text{k}\Omega$$

$$= 0.853\ \text{k}\Omega$$

The system approach will result in the configuration of Fig. 10.22 with the value of Z_i as controlled by R_L and the voltage gain. Now the two-port gain equation can be applied (slight difference in A_v due to approximation $\beta I_b \gg I_{R_F}$ in Section 8.7):

$$A_v = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{(3.3\ \text{k}\Omega)(-238.94)}{3.3\ \text{k}\Omega + 2.66\ \text{k}\Omega} = \mathbf{-132.3}$$

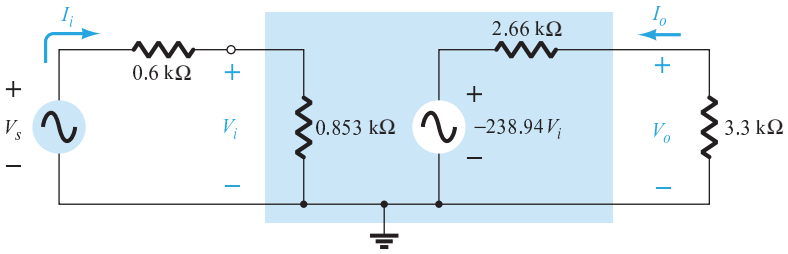


Figure 10.22 The ac equivalent circuit for the network of Fig. 10.21.

$$\text{(b)}\quad A_{v_s} = \frac{Z_i}{Z_i + R_s} A_v = \frac{0.853\ \text{k}\Omega}{0.853\ \text{k}\Omega + 0.6\ \text{k}\Omega}(-132.3)$$
$$= \mathbf{-77.67}$$

$$\text{(c)}\quad A_i = -A_v \frac{Z_i}{R_L} = -(-132.3)\left(\frac{0.853\ \text{k}\Omega}{3.3\ \text{k}\Omega}\right) = \frac{(132.3)(0.853\ \text{k}\Omega)}{3.3\ \text{k}\Omega}$$
$$= \mathbf{34.2}$$

$$\text{or}\quad A_i = -A_{v_s} \frac{Z_i + R_s}{R_L} = -(-77.67)\left(\frac{0.853\ \text{k}\Omega + 0.6\ \text{k}\Omega}{3.3\ \text{k}\Omega}\right)$$
$$= \mathbf{34.2}$$

10.7 BJT EMITTER-FOLLOWER NETWORKS

The input and output impedance parameters of the two-port model for the emitter-follower network are sensitive to the applied load and source resistance. For the emitter-follower configuration of Fig. 10.23, the small-signal ac model would appear as shown in Fig. 10.24. For the input section of Fig. 10.24, the resistance R_B is neglected because it is usually so much larger than the source resistance that a Thévenin equiv-

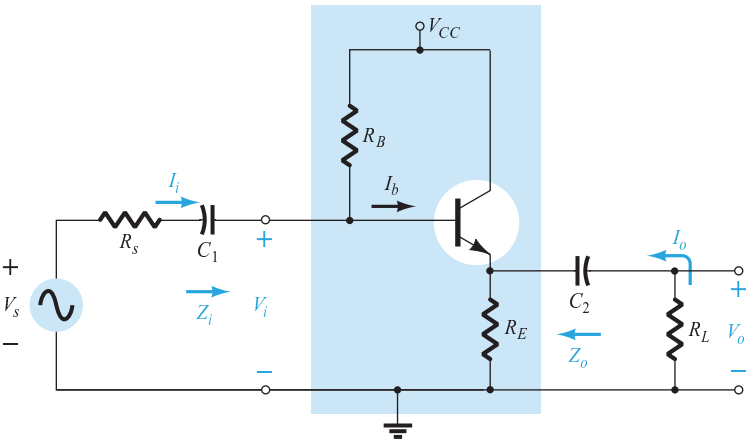


Figure 10.23 Emitter-follower configuraton with R_s and R_L.

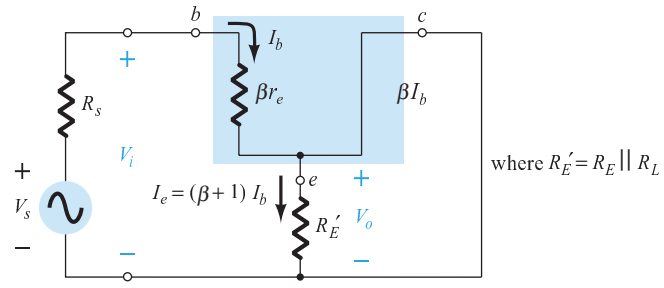


Figure 10.24 Emitter-follower configuration of Fig. 10.23 following the substitution of the r_e equivalent circuit.

alent circuit for the configuration of Fig. 10.25 would result in simply R_s and V_s as shown in Fig. 10.24. Of course, if current levels are to be determined such as I_i in the original diagram, the effect of R_B must be included.

Applying Kirchhoff's voltage law to the input circuit of Fig. 10.24 will result in

$$V_s - I_b R_s - I_b \beta r_e - (\beta + 1) I_b R_E' = 0$$

and

$$V_s - I_b(R_s + \beta r_e + (\beta + 1) R_E') = 0$$

so that

$$I_b = \frac{V_s}{R_s + \beta r_e + (\beta + 1) R_E'}$$

Establishing I_e, we have

$$I_e = (\beta + 1) I_b = \frac{(\beta + 1) V_s}{R_s + \beta r_e + (\beta + 1) R_E'}$$

and

$$I_e = \frac{V_s}{[(R_s + \beta r_e)/(\beta + 1)] + R_E'}$$

Using $\beta + 1 \cong \beta$ yields

$$\boxed{I_e = \frac{V_s}{(R_s/\beta + r_e) + R_E'}} \tag{10.34}$$

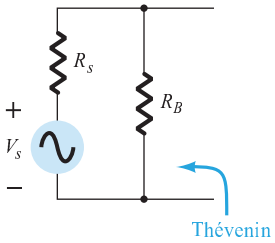


Figure 10.25 Determining the Thévenin equivalent circuit for the input circuit of Fig. 10.23.

Drawing the network to "fit" Eq. (10.34) will result in the configuration of Fig. 10.26a. In Fig. 10.26b, R_E and the load resistance R_L have been separated to permit a definition of Z_o and I_o.

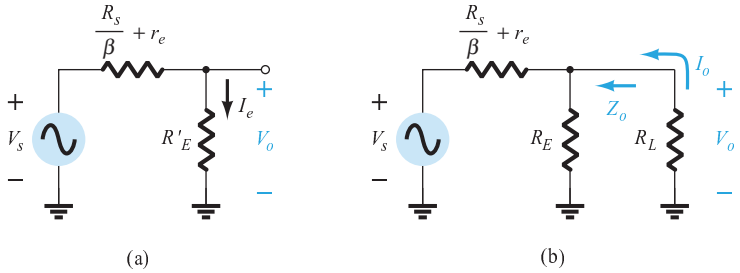


Figure 10.26 Networks resulting from the application of Kirchhoff's voltage law to the input circuit of Fig. 10.24.

The voltage gain can then be obtained directly from Fig. 10.26a using the voltage divider rule:

$$V_o = \frac{R_E' V_s}{R_E' + (R_s/\beta + r_e)}$$

or

$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_E'}{R_E' + (R_s/\beta + r_e)}$$

and
$$A_{v_s} = \frac{V_o}{V_s} = \frac{R_E \| R_L}{R_E \| R_L + R_s/\beta + r_e} \tag{10.35}$$

Setting $V_s = 0$ and solving for Z_o will result in

$$Z_o = R_E \| \left(\frac{R_s}{\beta} + r_e \right) \tag{10.36}$$

For the input impedance,

$$Z_b = \beta(r_e + R'_E)$$

and
$$Z_i = R_B \| Z_b$$

or
$$Z_i = R_B \| \beta(r_e + R_E \| R_L) \tag{10.37}$$

For no-load conditions, the gain equation is

$$A_{v_{NL}} \cong \frac{R_E}{R_E + r_e}$$

while for loaded conditions,

$$A_v \cong \frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e} \tag{10.38}$$

EXAMPLE 10.6

For the loaded emitter-follower configuration of Fig. 10.27 with a source resistance and the no-load two-port parameters of $Z_i = 157.54\ \text{k}\Omega$, $Z_o = 21.6\ \Omega$, and $A_{v_{NL}} = 0.993$ with $r_e = 21.74\ \Omega$ and $\beta = 65$, determine:

(a) The new values of Z_i and Z_o as determined by the load and R_s, respectively.
(b) A_v using the systems approach.
(c) A_{v_s} using the systems approach.
(d) $A_i = I_o/I_i$.

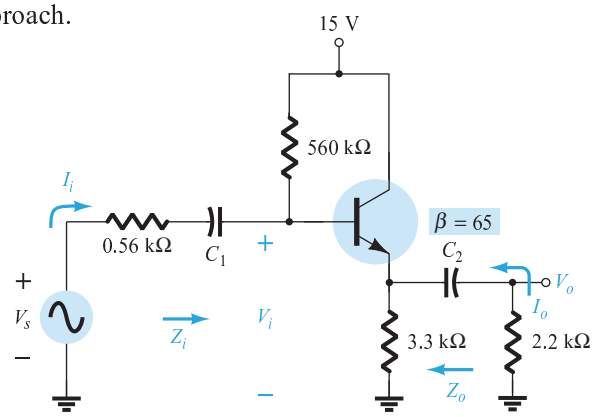


Figure 10.27 Example 10.6.

Solution

$$\text{Eq. (10.37):} \quad Z_i = R_B \| \beta(r_e + R_E \| R_L)$$
$$= 560\ \text{k}\Omega \| 65(21.74\ \Omega + \underbrace{3.3\ \text{k}\Omega \| 2.2\ \text{k}\Omega}_{1.32\ \text{k}\Omega})$$
$$= 560\ \text{k}\Omega \| 87.21\ \text{k}\Omega$$
$$= \mathbf{75.46\ k\Omega}$$

versus 157.54 kΩ (no-load).

$$Z_o = R_E \| \left(\frac{R_s}{\beta} + r_e \right)$$

$$= 3.3\ \text{k}\Omega \| \left(\frac{0.56\ \text{k}\Omega}{65} + 21.74\ \Omega \right)$$

$$= 3.3\ \text{k}\Omega \| 30.36\ \Omega$$

$$= \mathbf{30.08\ \Omega}$$

versus 21.6 Ω (no R_s).

(b) Substituting the two-port equivalent network will result in the small-signal ac equivalent network of Fig. 10.28.

$$V_o = \frac{R_L A_{v_{\text{NL}}} V_i}{R_L + R_o} = \frac{(2.2\ \text{k}\Omega)(0.993)V_i}{2.2\ \text{k}\Omega + 30.08\ \Omega}$$

$$\cong 0.98 V_i$$

$$\text{with } A_v = \frac{V_o}{V_i} \cong \mathbf{0.98}$$

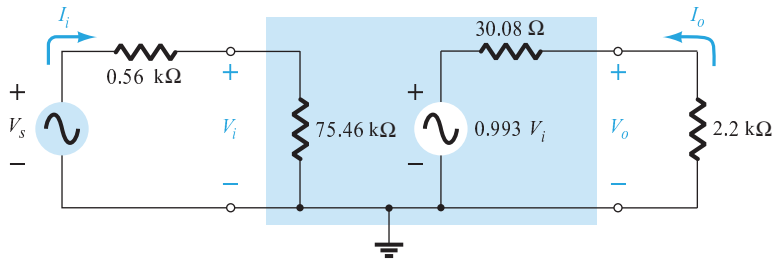


Figure 10.28 Small-signal ac equivalent circuit for the network of Fig. 10.27.

(c) $$V_i = \frac{Z_i V_s}{Z_i + R_s} = \frac{(75.46\ \text{k}\Omega)V_s}{75.46\ \text{k}\Omega + 0.56\ \text{k}\Omega} = 0.993 V_s$$

so that $$A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i}\frac{V_i}{V_s} = (0.98)(0.993) = \mathbf{0.973}$$

(d) $$A_i = \frac{I_o}{I_i} = -A_v \frac{Z_i}{R_L}$$

$$= -(0.98)\left(\frac{75.46\ \text{k}\Omega}{2.2\ \text{k}\Omega} \right)$$

$$= \mathbf{-33.61}$$

10.8 BJT CB NETWORKS

A common-base amplifier with an applied load and source resistance appear in Fig. 10.29. The fact that the load is connected between the collector and base terminals isolates it from the input circuit, and Z_i remains essentially the same for no-load or loaded conditions. The isolation that exists between input and output circuits also maintains Z_o at a fixed level even though the level of R_s may change. The voltage gain is now determined by

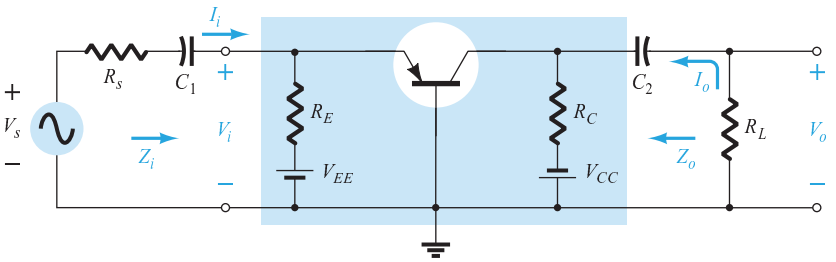


Figure 10.29 Common-base configuration with R_s and R_L.

$$A_v \cong \frac{R_C \| R_L}{r_e} \tag{10.39}$$

and the current gain:

$$A_i \cong -1 \tag{10.40}$$

EXAMPLE 10.7

For the common-base amplifier of Fig. 10.30, the no-load two-port parameters are (using $\alpha \cong 1$) $Z_i \cong r_e = 20\ \Omega$, $A_{v_{NL}} = 250$, and $Z_o = 5\ \text{k}\Omega$. Using the two-port equivalent model, determine:

(a) A_v.
(b) A_{v_s}.
(c) A_i.

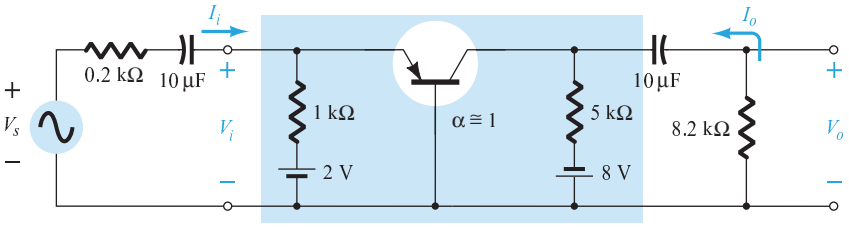


Figure 10.30 Example 10.7.

Solution

(a) The small-signal ac equivalent network appears in Fig. 10.31.

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o} = \frac{(8.2\ \text{k}\Omega)(250)V_i}{8.2\ \text{k}\Omega + 5\ \text{k}\Omega} = 155.3V_i$$

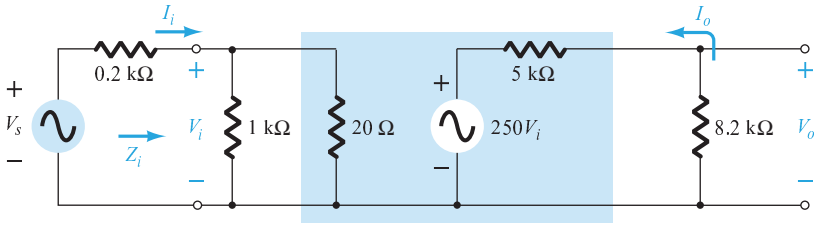


Figure 10.31 Small-signal ac equivalent circuit for the network of Fig. 10.30.

and $$A_v = \frac{V_o}{V_i} = \mathbf{155.3}$$

or $$A_v \cong \frac{R_C \| R_L}{r_e} = \frac{5\ \text{k}\Omega \| 8.2\ \text{k}\Omega}{20\ \Omega} = \frac{3.106\ \text{k}\Omega}{20\ \Omega}$$
$$= \mathbf{155.3}$$

(b) $$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\frac{V_o}{V_i}$$
$$= \frac{R_i}{R_i + R_s} A_v = \left(\frac{20\ \Omega}{20\ \Omega + 200\ \Omega}\right)(155.3)$$
$$= \mathbf{14.12}$$

Note the relatively low gain due to a source impedance much larger than the input impedance of the amplifier.

(c) $$A_i = -A_v \frac{Z_i}{R_L} = -(155.3)\left(\frac{20\ \Omega}{8.2\ \text{k}\Omega}\right)$$
$$= \mathbf{-0.379}$$

which is significantly less than 1 due to the division of output current between R_C and R_L.

10.9 FET NETWORKS

As noted in Chapter 9, the isolation that exists between gate and drain or source of an FET amplifier ensures that changes in R_L do not affect the level of Z_i and changes in R_{sig} do not affect R_o. In essence, therefore:

The no-load two-port model of Fig. 10.2 for an FET amplifier is unaffected by an applied load or source resistance.

Bypassed Source Resistance

For the FET amplifier of Fig. 10.32, the applied load will appear in parallel with R_D in the small-signal model, resulting in the following equation for the loaded gain:

$$A_v = -g_m(R_D \| R_L) \tag{10.41}$$

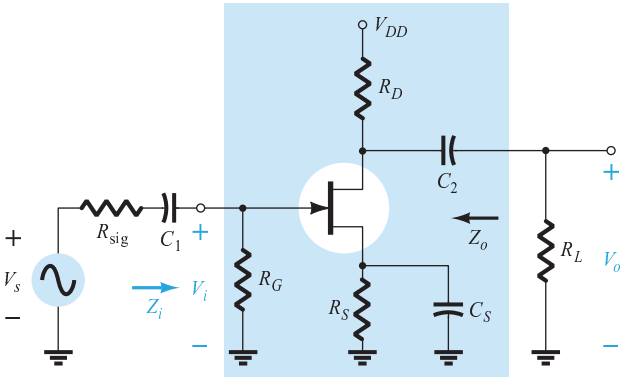


Figure 10.32 JFET amplifier with R_{sig} and R_L.

The impedance levels remain at

$$Z_i = R_G \tag{10.42}$$

$$Z_o = R_D \tag{10.43}$$

Unbypassed Source Resistance

For the FET amplifier of Fig. 10.33, the load will again appear in parallel with R_D and the loaded gain becomes

$$A_v = \frac{V_o}{V_i} = -\frac{g_m(R_D \| R_L)}{1 + g_m R_S} \tag{10.44}$$

with

$$Z_i = R_G \tag{10.45}$$

and

$$Z_o = R_D \tag{10.46}$$

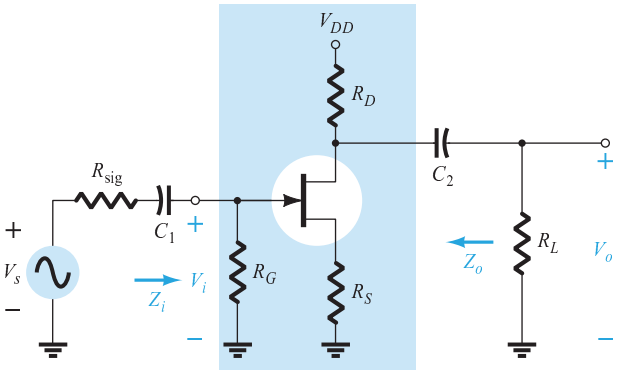


Figure 10.33 JFET amplifier with unbypassed R_S.

EXAMPLE 10.8

For the FET amplifier of Fig. 10.34, the no-load two-port parameters are $A_{v_{NL}} = -3.18$, $Z_i = R_1 \| R_2 = 239\ \text{k}\Omega$, and $Z_o = 2.4\ \text{k}\Omega$, with $g_m = 2.2$ mS.

(a) Using the two-port parameters above, determine A_v and A_{v_s}.

(b) Using Eq. (10.44), calculate the loaded gain and compare to the result of part (a).

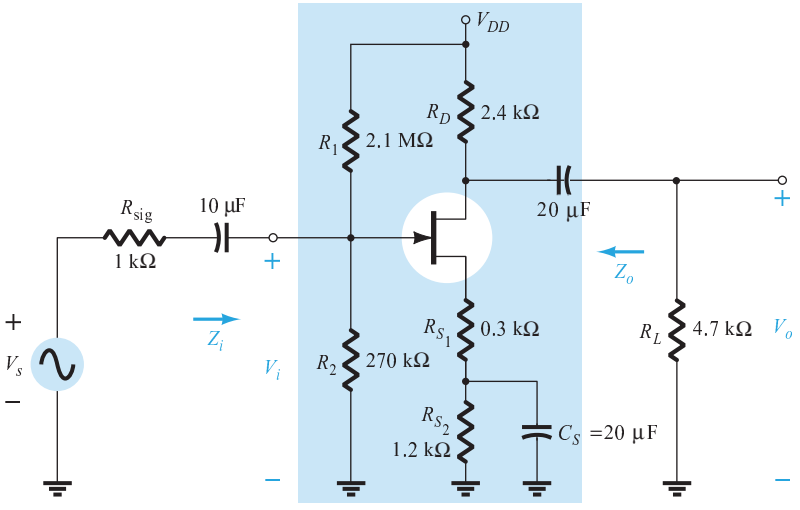


Figure 10.34 Example 10.8.

Solution

(a) The small-signal ac equivalent network appears in Fig. 10.35, and

$$A_v = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{(4.7\ \text{k}\Omega)(-3.18)}{4.7\ \text{k}\Omega + 2.4\ \text{k}\Omega}$$

$$= \mathbf{-2.105}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\frac{V_o}{V_i} = \frac{R_i}{R_i + R_{\text{sig}}} A_v$$

$$= \frac{(239\ \text{k}\Omega)(-2.105)}{239\ \text{k}\Omega + 1\ \text{k}\Omega}$$

$$= \mathbf{-2.096} \cong A_v$$

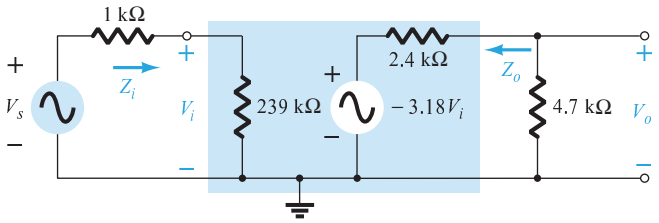


Figure 10.35 Small-signal ac equivalent circuit for the network of Fig. 10.34.

(b) Eq. (10.44): $A_v = \dfrac{-g_m(R_D \| R_L)}{1 + g_m R_{S_1}}$

$$= \frac{-(2.2\ \text{mS})(2.4\ \text{k}\Omega \| 4.7\ \text{k}\Omega)}{1 + (2.2\ \text{mS})(0.3\ \text{k}\Omega)} = \frac{-3.498}{1.66}$$

$$= \mathbf{-2.105}\ \text{as above}$$

Source Follower

For the source-follower configuration of Fig. 10.36, the level of Z_i is independent of the magnitude of R_L and determined by

$$\boxed{Z_i = R_G} \tag{10.47}$$

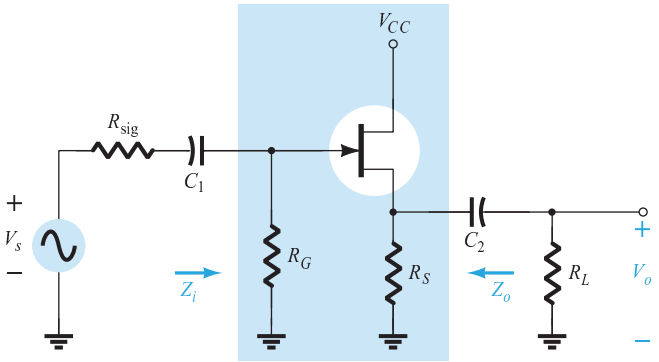


Figure 10.36 Source-follower configuration with R_{sig} and R_L.

The loaded voltage gain has the same format as the unloaded gain with R_S replaced by the parallel combination of R_S and R_L.

$$A_v = \frac{V_o}{V_i} = \frac{g_m(R_S \| R_L)}{1 + g_m(R_S \| R_L)} \tag{10.48}$$

The level of output impedance is as determined in Chapter 9:

$$Z_o = R_S \| \frac{1}{g_m} \tag{10.49}$$

revealing an insensitivity to the magnitude of the source resistance R_{sig}.

Common Gate

Even though the common-gate configuration of Fig. 10.37 is somewhat different from those described above with regard to the placement of R_L and R_{sig}, the input and output circuits remain isolated and

$$Z_i = \frac{R_S}{1 + g_m R_S} \tag{10.50}$$

$$Z_o = R_D \tag{10.51}$$

The loaded voltage gain is given by

$$A_v = g_m(R_D \| R_L) \tag{10.52}$$

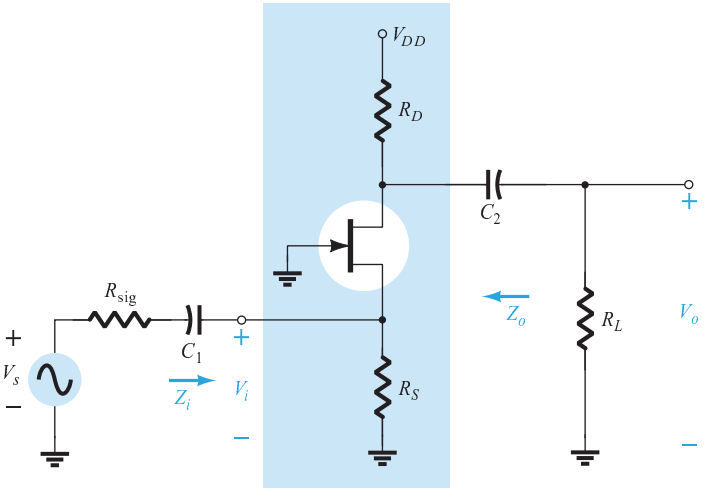


Figure 10.37 Common-gate configuration with R_{sig} and R_L.

10.10 SUMMARY TABLE

Now that the loaded and unloaded (Chapters 8 and 9) BJT and JFET amplifiers have been examined in some detail, a review of the equations developed is provided by Table 10.1. Although all the equations are for the loaded situation, the removal of R_L will result in the equations for the unloaded amplifier. The same is true for the effect of R_s (for BJTs) and R_{sig} (for JFETs) on Z_o. In each case, the phase relationship between the input and output voltages is also provided for quick reference. A review of

the equations will reveal that the isolation provided by the JFET between the gate and channel by the SiO_2 layer results in a series of less complex equations than those encountered for the BJT configurations. The linkage provided by I_b between input and output circuits of the BJT transistor amplifier adds a touch of complexity to some of the equations.

TABLE 10.1 Summary of Transistor Configurations (A_v, Z_i, Z_o)

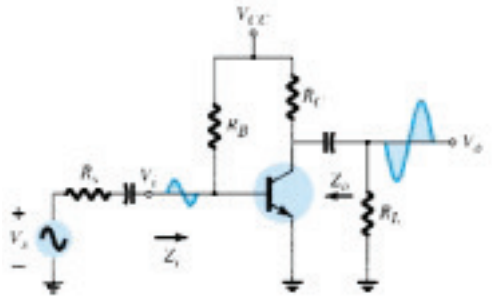
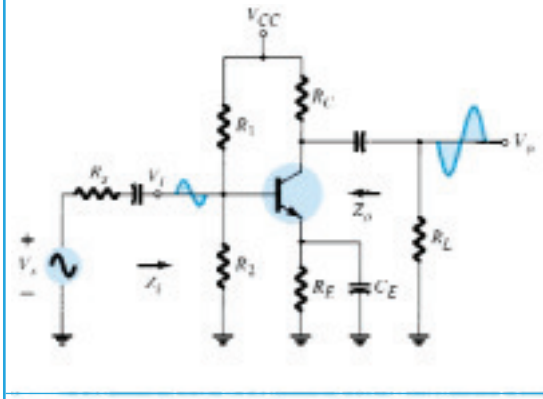
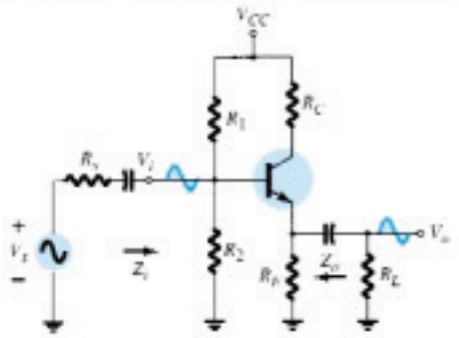
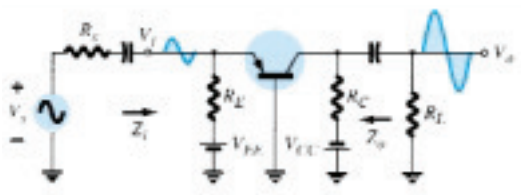
Configuration	$A_v = V_o/V_i$	Z_i	Z_o
	$\dfrac{-R_L\|R_C)}{r_e}$ $\dfrac{-h_{fe}}{h_{ie}}(R_L\|R_C)$ Including r_o: $-\dfrac{(R_L\|R_C\|r_o)}{r_e}$	$R_B\|\beta r_e$ $R_B\|h_{ie}$ $R_B\|\beta r_e$	R_C R_C $R_C\|r_o$
	$\dfrac{-(R_L\|R_C)}{r_e}$ $\dfrac{-h_{fe}}{h_{ie}}(R_L\|R_C)$ Including r_o: $\dfrac{-(R_L\|R_C\|r_o)}{r_e}$	$R_1\|R_2\|\beta r_e$ $R_1\|R_2\|h_{ie}$ $R_1\|R_2\|\beta r_e$	R_C R_C $R_C\|r_o$
	$\cong 1$ $\cong 1$ Including r_o: $\cong 1$	$R'_E = R_L\|R_E$ $R_1\|R_2\|\beta(r_e + R'_E)$ $R_1\|R_2\|(h_{ie} + h_{fe}R'_E)$ $R_1\|R_2\|\beta(r_e + R'_E)$	$R'_s = R_s\|R_1\|R_2$ $R_E\|\left(\dfrac{R'_s}{\beta} + r_e\right)$ $R_E\|\left(\dfrac{R'_s + h_{ie}}{h_{fe}}\right)$ $R_E\|\left(\dfrac{R'_s}{\beta} + r_e\right)$
	$\cong \dfrac{-(R_L\|R_C)}{r_e}$ $\cong \dfrac{-h_{fb}}{h_{ib}}(R_L\|R_C)$ Including r_o: $\cong \dfrac{-(R_L\|R_C\|r_o)}{r_e}$	$R_E\|r_e$ $R_E\|h_{ib}$ $R_E\|r_e$	R_C R_C $R_C\|r_o$

TABLE 10.1 Summary of Transistor Configurations (A_v, Z_i, Z_o) (Continued)

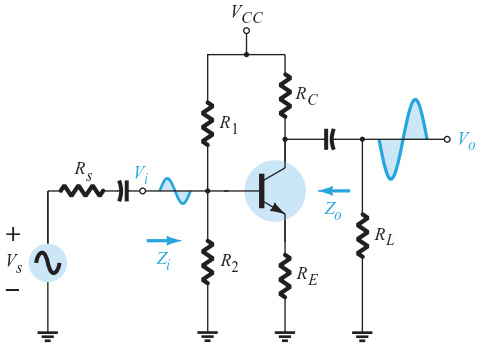
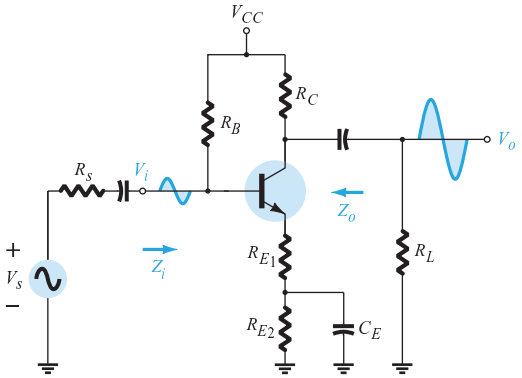
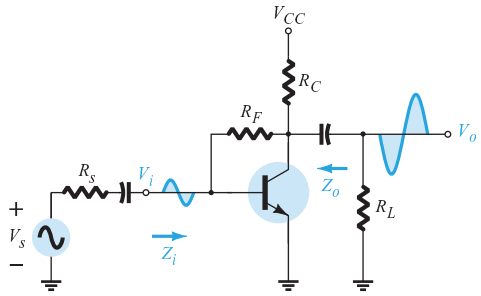
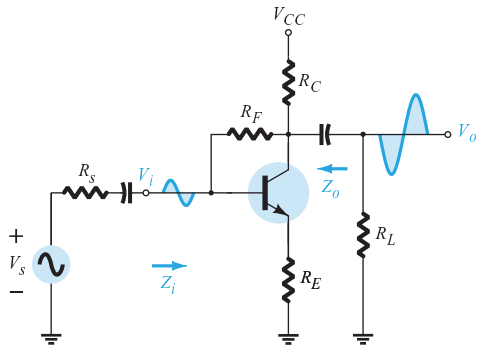
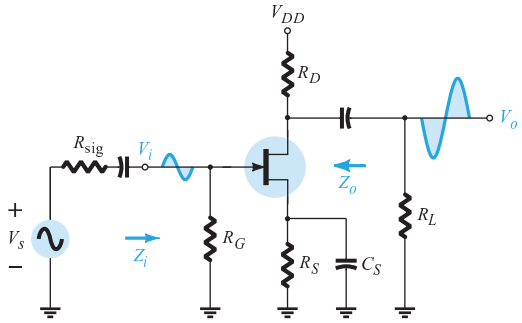
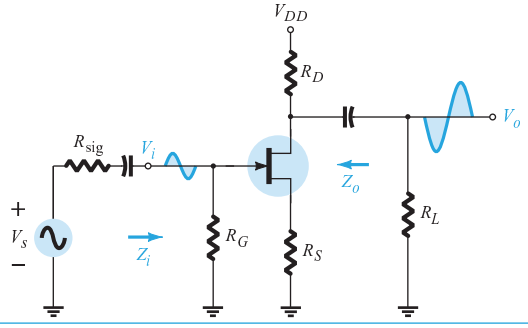
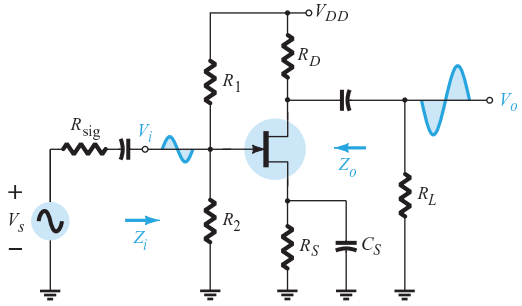
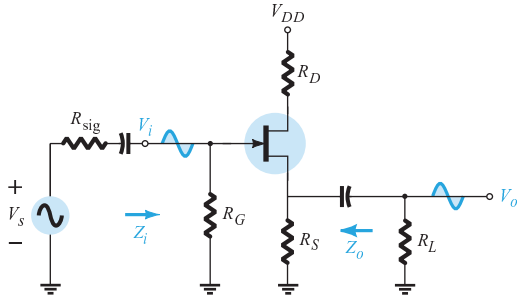
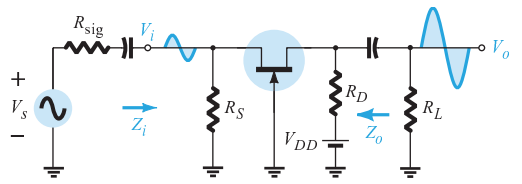
Configuration	$A_v = V_o/V_i$	Z_i	Z_o
	$\dfrac{-R_L \| R_C)}{R_E}$ $\dfrac{-(R_L \| R_C)}{R_E}$ Including r_o: $\dfrac{-(R_L \| R_C)}{R_E}$	$R_1 \| R_2 \| \beta(r_e + R_E)$ $R_1 \| R_2 \| (h_{ie} + h_{fe}R_E)$ $R_1 \| R_2 \| \beta(r_e + R_E)$	R_C R_C $\cong R_C$
	$\dfrac{-R_L \| R_C}{R_{E_1}}$ $\dfrac{-(R_L \| R_C)}{R_{E_1}}$ Including r_o: $\dfrac{-R_L \| R_C}{R_{E_1}}$	$R_B \| \beta(r_e + R_{E_1})$ $R_B \| (h_{ie} + h_{fe}R_{E_1})$ $R_B \| \beta(r_e + R_{E_1})$	R_C R_C $\cong R_C$
	$\dfrac{-(R_L \| R_C)}{r_e}$ $\dfrac{-h_{fe}}{h_{ie}}(R_L \| R_C)$ Including r_o: $\dfrac{-(R_L \| R_C \| r_o)}{r_e}$	$\beta r_e \| \dfrac{R_F}{\|A_v\|}$ $h_{ie} \| \dfrac{R_F}{\|A_v\|}$ $\beta r_e \| \dfrac{R_F}{\|A_v\|}$	R_C R_C $R_C \| R_F \| r_o$
	$\dfrac{-(R_L \| R_C)}{R_E}$ $\dfrac{-(R_L \| R_C)}{R_E}$ Including r_o: $\cong \dfrac{-(R_L \| R_C)}{R_E}$	$\beta R_E \| \dfrac{R_F}{\|A_v\|}$ $h_{fe}R_E \| \dfrac{R_F}{\|A_v\|}$ $\cong \beta R_E \| \dfrac{R_F}{\|A_v\|}$	$\cong R_C \| R_F$ $\cong R_C \| R_F$ $\cong R_C \| R_F$

TABLE 10.1 (Continued)

Configuration	$A_v = V_o/V_i$	Z_i	Z_o
	$-g_m(R_D\|\|R_L)$ Including r_d: $-g_m(R_D\|\|R_L\|\|r_d)$	R_G R_G	R_D $R_D\|\|r_d$
	$\dfrac{-g_m(R_D\|\|R_L)}{1+g_mR_S}$ Including r_d: $\dfrac{-g_m(R_D\|\|R_L)}{1+g_mR_S+\dfrac{R_D+R_S}{r_d}}$	R_G R_G	$\dfrac{R_D}{1+g_mR_S}$ $\cong \dfrac{R_D}{1+g_mR_S}$
	$-g_m(R_D\|\|R_L)$ Including r_d: $-g_m(R_D\|\|R_L\|\|r_d)$	$R_1\|\|R_2$ $R_1\|\|R_2$	R_D $R_D\|\|r_d$
	$\dfrac{g_m(R_S\|\|R_L)}{1+g_m(R_S\|\|R_L)}$ Including r_d: $= \dfrac{g_mr_d(R_S\|\|R_L)}{r_d+R_D+g_mr_d(R_S\|\|R_L)}$	R_G R_G	$R_S\|\|1/g_m$ $\dfrac{R_S}{1+\dfrac{g_mr_dR_S}{r_d+R_D}}$
	$g_m(R_D\|\|R_L)$ Including r_d: $\cong g_m(R_D\|\|R_L)$	$\dfrac{R_S}{1+g_mR_S}$ $Z_i = \dfrac{R_S}{1+\dfrac{g_mr_dR_S}{r_d+R_D\|\|R_L}}$	R_D $R_D\|\|r_d$

10.11 CASCADED SYSTEMS

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 10.38, where A_{v_1}, A_{v_2}, A_{v_3}, and so on, are the voltage gains of each stage *under loaded conditions*. That is, A_{v1} is determined with the input impedance to A_{v_2} acting as the load on A_{v_1}. For A_{v_2}, A_{v_1} will determine the signal strength and source impedance at the input to A_{v_2}. The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots \tag{10.53}$$

and the total current gain by

$$A_{i_T} = -A_{v_T} \frac{Z_{i_1}}{R_L} \tag{10.54}$$

No matter how perfect the system design, the application of a load to a two-port system will affect the voltage gain. Therefore, there is no possibility of a situation where A_{v_1}, A_{v_2}, and so on, of Fig. 10.38 are simply the no-load values. The loading of each succeeding stage must be considered. The no-load parameters can be used to determine the loaded gains of Fig. 10.38, but Eq. (10.53) requires the loaded values.

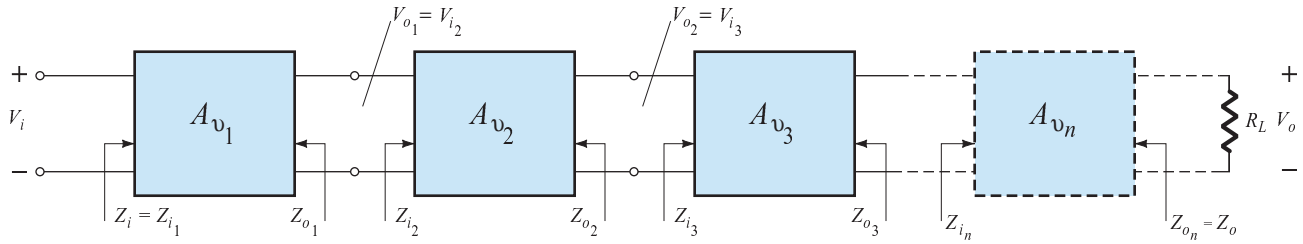


Figure 10.38 Cascaded system.

EXAMPLE 10.9

The two-stage system of Fig. 10.39 employed a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percent of the applied signal appears at the input terminals of the common-base amplifier. In Fig. 10.39, the no-load values are provided for each system, with the exception of Z_i and Z_o for the emitter-follower, which are the loaded values. For the configuration of Fig. 10.39, determine:

(a) The loaded gain for each stage.
(b) The total gain for the system, A_v and A_{v_s}.
(c) The total current gain for the system.
(d) The total gain for the system if the emitter-follower configuration were removed.

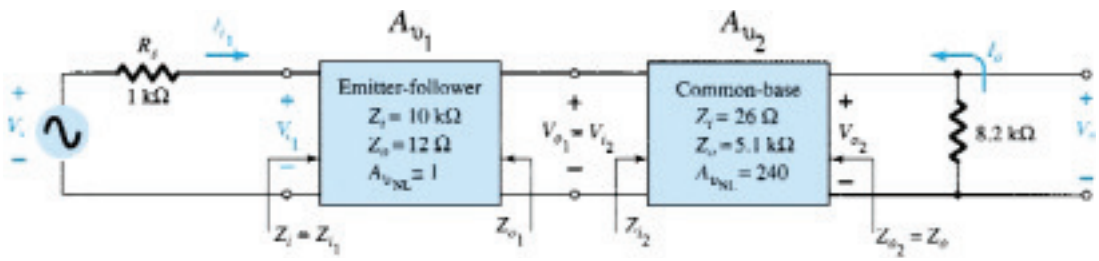


Figure 10.39 Example 10.9.

Solution

(a) For the emitter-follower configuration, the loaded gain is

$$V_{o_1} = \frac{Z_{i_2} A_{v_{NL}} V_{i_1}}{Z_{i_2} + Z_{o_1}} = \frac{(26\ \Omega)(1)V_{i_1}}{26\ \Omega + 12\ \Omega} = 0.684V_{i_1}$$

and $$A_{v_1} = \frac{V_{o_1}}{V_{i_1}} = \mathbf{0.684}$$

For the common-base configuration,

$$V_{o_2} = \frac{R_L A_{v_{NL}} V_{i_2}}{R_L + R_{o_2}} = \frac{(8.2\ \text{k}\Omega)(240)V_{i_2}}{8.2\ \text{k}\Omega + 5.1\ \text{k}\Omega} = 147.97V_{i_2}$$

and $$A_{v_L} = \frac{V_{o_2}}{V_{i_2}} = \mathbf{147.97}$$

(b) $$A_{v_T} = A_{v_1}A_{v_2}$$
$$= (0.684)(147.97)$$
$$= \mathbf{101.20}$$
$$A_{v_s} = \frac{Z_{i_1}}{Z_{i_1} + R_s} A_{v_T} = \frac{(10\ \text{k}\Omega)(101.20)}{10\ \text{k}\Omega + 1\ \text{k}\Omega}$$
$$= \mathbf{92}$$

(c) $$A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} = -(101.20)\left(\frac{10\ \text{k}\Omega}{8.2\ \text{k}\Omega}\right)$$
$$= \mathbf{-123.41}$$

(d) $$V_{i_{CB}} = \frac{Z_{i_{CB}} V_s}{Z_{i_{CB}} + R_s} = \frac{(26\ \Omega)V_s}{26\ \Omega + 1\ \text{k}\Omega} = 0.025V_s$$

and $$\frac{V_i}{V_s} = 0.025 \quad \text{with} \quad \frac{V_o}{V_i} = 147.97 \quad \text{from above}$$

and $$A_{v_s} = \frac{V_i}{V_s}\frac{V_o}{V_i} = (0.025)(147.97) = \mathbf{3.7}$$

In total, therefore, the gain is about 25 times greater with the emitter-follower configuration to draw the signal to the amplifier stages. Take note, however, that it was also important that the output impedance of the first stage was relatively close to the input impedance of the second stage or the signal would have been "lost" again by the voltage-divider action.

10.12 PSPICE WINDOWS

Loaded Voltage-Divider BJT Transistor Configuration

The computer analysis of this section includes a PSpice Windows evaluation of the response of a loaded BJT and FET amplifier with a source resistance. The BJT network of Fig. 10.40 employs the same unloaded configuration examined in the PSpice analysis of Chapter 8, where the unloaded gain was 369 (Example 8.2, $r_e = 18.44\ \Omega$). For the transistor, all the parameters listed under **Model Editor** were removed except I_s and beta, which were set to 2E-15A and 90, respectively. In this way, the results

will be as close to the hand-written solutions as possible without going to the controlled source equivalents. Note the placement of the **VPRINT1** option to pick up the voltage lost across the source resistance and to note if there is any drop in gain across the capacitor. The option **Do not auto-run Probe** was chosen, and under **Analysis Setup,** the **AC Sweep** was set at a fixed frequency of 10 kHz. In addition, **Display Results on Schematic** under **Analysis** was chosen and the **Voltage Display** enabled.

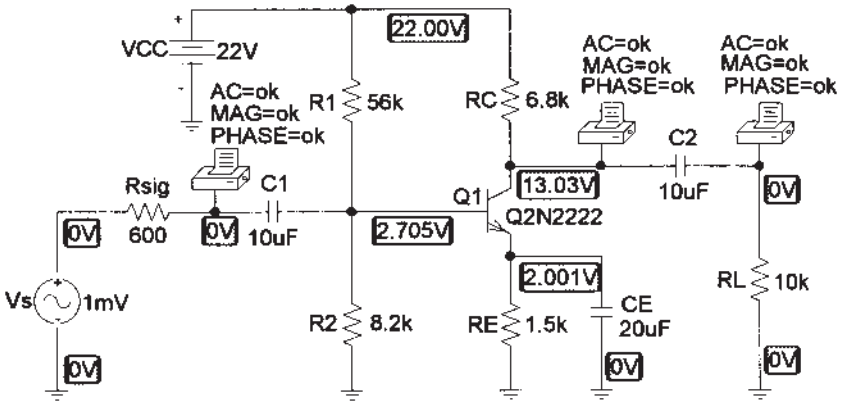


Figure 10.40 Loaded voltage-divider BJT transistor configuration.

An **Analysis** resulted in the dc levels appearing in Fig. 10.40. In particular, note the zero volt levels at the left side of C_1 and the right side of C_2. In addition, note that V_{BE} is essentially 0.7 V and the dc levels of each terminal of the transistor are very close to those calculated in Example 8.2 (using the approximate approach). Reviewing the output file following **Analysis-Examine Output** will result in the data listings of Fig. 10.41. The nodes are defined in the **Schematics Netlist,** and the **BJT MODEL PARAMETERS** reveal our choices for this run—although the last three are default values. The **SMALL-SIGNAL BIAS SOLUTION** simply confirms the levels printed on the schematic, and the **Operating Point Information** reveals that beta (dc and ac) is 90, that V_{BE} is 0.7 V, that I_C is 1.32 mA, and that I_B is 14.7 μA (in addition to a host of other levels). The **AC ANALYSIS** reveals that the voltage on the other side of R_{sig} is about 0.7 mV, resulting in a drop of about 0.3 mV (30% loss in signal voltage) of the applied signal across R_{sig}. The remaining two ac levels are the same, revealing that the capacitor is an effective short circuit for ac. The loaded gain from source to output is 144.9. The gain from the base of the transistor to the output is 144.9 mV/0.7 mV = 207. Both levels are certainly significantly less than the no-load level of 369. If we return to the network and change R_L to 10 MΩ, the output voltage will rise to 243.3 mV, resulting in a gain of 243.3 mV/0.7 mV = 347.57, which is quite close to the hand-calculated, approximate level of 369.

For interest's sake, let us now calculate the loaded voltage gain and compare to the PSpice solution of 144.9.

$$r_e = 18.44\ \Omega$$

and

$$Z_i \cong R_1 \| R_2 \| \beta r_e$$
$$= 56\ \text{k}\Omega \| 8.2\ \text{k}\Omega \| (90)(18.44\ \Omega)$$
$$\cong 1.35\ \text{k}\Omega$$

$$V_i = \frac{Z_i V_s}{Z_i + R_s} = \frac{(1.35\ \text{k}\Omega)V_s}{1.35\ \text{k}\Omega + 0.6\ \text{k}\Omega} = 0.69V_s$$

and

$$\frac{V_i}{V_s} = 0.69$$

```
 ****     CIRCUIT DESCRIPTION
******************************************************************************
* Schematics Netlist *

V_Vs          $N_0001 0  AC 1mV
+SIN 0V 1mV 10kHz 0 0 0
R_Rsig          $N_0001 $N_0002  600

.PRINT          AC
+ VM([$N_0002])
+ VP([$N_0002])
C_C1          $N_0002 $N_0003  10uF
V_VCC          $N_0004 0 22V
R_R1          $N_0004 $N_0003  56k
R_R2          $N_0003 0  8.2k
R_RC          $N_0004 $N_0005  6.8k
R_RE          $N_0006 0  1.5k
C_CE          $N_0006 0  20uF
R_RL          $N_0007 0  10k
C_C2          $N_0005 $N_0007  10uF

.PRINT          AC
+ VM([$N_0005])
+ VP([$N_0005])

.PRINT          AC
+ VM([$N_0007])
+ VP([$N_0007])
Q_Q1          $N_0005 $N_0003 $N_0006 Q2N2222-X

 ****     BJT MODEL PARAMETERS
******************************************************************************

               Q2N2222-X
               NPN
          IS    2.000000E-15
          BF    90
          NF     1
          BR     1
          NR     1

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

($N_0001)     0.0000                   ($N_0002)     0.0000

($N_0003)     2.7051                   ($N_0004)    22.0000

($N_0005)    13.0280                   ($N_0006)     2.0012

($N_0007)     0.0000

    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_Vs          0.000E+00
    V_VCC        -1.664E-03

    TOTAL POWER DISSIPATION   3.66E-02  WATTS

 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

******************************************************************************

**** BIPOLAR JUNCTION TRANSISTORS

NAME          Q_Q1
MODEL         Q2N2222-X
IB            1.47E-05
IC            1.32E-03
VBE           7.04E-01
VBC          -1.03E+01
VCE           1.10E+01
BETADC        9.00E+01
GM            5.10E-02
RPI           1.76E+03
RX            0.00E+00
RO            1.00E+12
CBE           0.00E+00
CBC           0.00E+00
CJS           0.00E+00
BETAAC        9.00E+01
CBX           0.00E+00
FT            8.12E+17

 ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C

******************************************************************************

   FREQ        VM($N_0002) VP($N_0002)

    1.000E+04   7.025E-04  -5.801E-01

  FREQ        VM($N_0005) VP($N_0005)

   1.000E+04   1.449E-01  -1.782E+02

  FREQ        VM($N_0007) VP($N_0007)

   1.000E+04   1.449E-01  -1.782E+02
```

Figure 10.41 Output file for the network of Fig. 10.40.

$$A_v = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{(10\ \text{k}\Omega)(-350.4)}{10\ \text{k}\Omega + 6.8\ \text{k}\Omega}$$
$$= -208.57$$

with
$$A_{v_s} = \frac{V_i}{V_s}\frac{V_o}{V_i} = (0.69)(-208.57)$$
$$\cong \mathbf{-144}$$

which is an excellent comparison with the computer solution.

Loaded JFET Self-Bias Transistor Configuration

The network of Fig. 10.42 is a loaded version of the network examined in Chapter 9, which resulted in a no-load gain of 13.3. In the **Model Editor** dialog box, **Beta** was set to 0.625mA/V^2 and **Vto** = −4V. The remaining parameters were left alone to permit a close comparison with the Chapter 9 solution and because they have less effect on the response than for a BJT transistor.

Again, note the effectiveness of the capacitors to block the dc voltages. In addition, note the small voltage at the gate, indicating that the input impedance to the device is in reality not infinite (although for all practical purposes it is an excellent assumption.) Again, the frequency was set to 10 kHz and an Analysis called for without the **Probe** option. The sequence **Analysis-Examine Output** will result in the listing of Fig. 10.43. The **Schematics Netlist** provides a listing of assigned nodes, and the **OPERATING POINT INFORMATION** reveals that the drain current is 3.36 mA, that V_{GS} is −1.71 V, and that g_m is 2.94 mS. The **AC ANALYSIS** reveals that there is negligible drop across either capacitor at this frequency, and the short-circuit equivalency can be assumed. The output voltage is 5.597mV resulting in a loaded gain of 5.597 compared to the unloaded gain of 13.3. Note also that the drop across R_{sig} is negligible due to the high input impedance of the device.

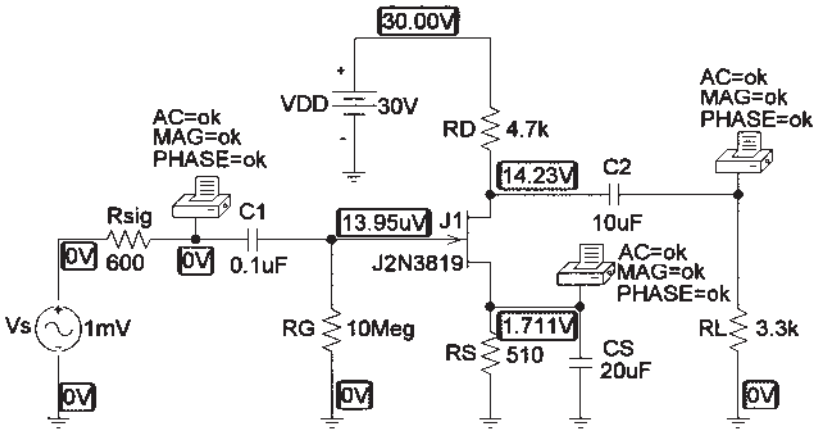


Figure 10.42 Loaded self-bias JFET transistor configuration.

Using the value of g_m hand-calculated earlier, the equation for the loaded gain will result in a gain of 5.62 as shown below—an excellent comparison with the computer solution.

$$A_v = -g_m(R_D \| R_L)$$
$$= -(2.90\ \text{mS})(4.7\ \text{k}\Omega \| 3.3\ \text{k}\Omega)$$
$$= -5.62$$

The results obtained above have clearly substantiated the analysis and equations presented in this chapter for a loaded amplifier.

```
 ****     CIRCUIT DESCRIPTION
******************************************************************************

* Schematics Netlist *

V_Vs          $N_0001 0  AC 1mV
+SIN 0V 1mV 10kHz 0 0 0
R_Rsig          $N_0001 $N_0002  600

.PRINT          AC
+ VM([$N_0002])
+ VP([$N_0002])
C_C1          $N_0002 $N_0003  0.1uF
R_RG          $N_0003 0  10Meg
C_C2          $N_0004 $N_0005  10uF

.PRINT          AC
+ VM([$N_0006])
+ VP([$N_0006])

.PRINT          AC
+ VM([$N_0005])
+ VP([$N_0005])
V_VDD          $N_0007 0 30V
R_RD          $N_0007 $N_0004  4.7k
R_RS          $N_0006 0  510
C_CS          $N_0006 0  20uF
J_J1          $N_0004 $N_0003 $N_0006 J2N3819-X1
R_RL          $N_0005 0  3.3k

 ****     Junction FET MODEL PARAMETERS
******************************************************************************
               J2N3819-X1
               NJF
         VTO   -4
        BETA  625.000000E-06
      LAMBDA    2.250000E-03
          IS   33.570000E-15
         ISR  322.400000E-15
       ALPHA  311.700000E-06
          VK  243.6
          RD    1
          RS    1
         CGD    1.600000E-12
         CGS    2.414000E-12
           M     .3622
       VTOTC   -2.500000E-03
     BETATCE    -.5
          KF    9.882000E-18

 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
******************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

($N_0001)    0.0000                   ($N_0002)    0.0000

($N_0003) 13.95E-06                   ($N_0004)   14.2280

($N_0005)    0.0000                   ($N_0006)    1.7114

($N_0007)   30.0000

     VOLTAGE SOURCE CURRENTS
     NAME         CURRENT

     V_Vs          0.000E+00
     V_VDD        -3.356E-03

     TOTAL POWER DISSIPATION   1.01E-01  WATTS
  ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C
******************************************************************************
**** JFETS


NAME          J_J1
MODEL         J2N3819-X1
ID            3.36E-03
VGS          -1.71E+00
VDS           1.25E+01
GM            2.94E-03
GDS           7.34E-06
CGS           1.68E-12
CGD           5.97E-13 *
  ****     AC ANALYSIS                      TEMPERATURE =   27.000 DEG C
******************************************************************************
   FREQ        VM($N_0002) VP($N_0002)

    1.000E+04   9.999E-04  -1.213E-02

   FREQ        VM($N_0006) VP($N_0006)

    1.000E+04   2.297E-06  -8.979E+01

   FREQ        VM($N_0005) VP($N_0005)

    1.000E+04   5.597E-03  -1.799E+02
```

Figure 10.43 Output file for the network of Fig. 10.42.

PROBLEMS

§ 10.3 Effect of a Load Impedance (R_L)

1. For the fixed-bias configuration of Fig. 10.44:
(a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
(b) Sketch the two-port model of Fig. 10.2 with the parameters determined in part (a) in place.
(c) Calculate the gain A_v using the model of part (b) and Eq. (10.3).
(d) Determine the current gain using Eq. (10.6).
(e) Determine A_v, Z_i, and Z_o using the r_e model and compare with the solutions above.

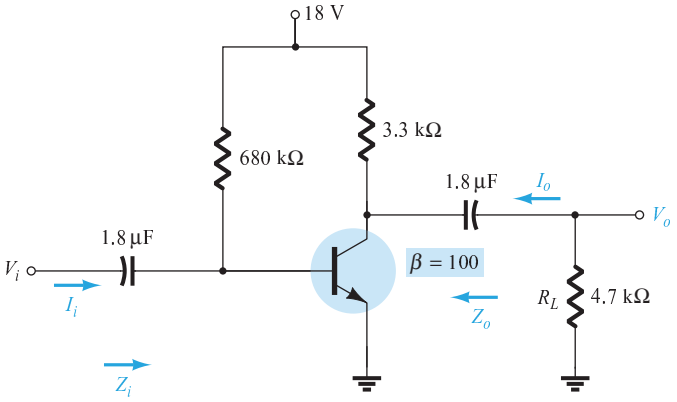


Figure 10.44 Problems 1, 2, and 3

*** 2.** (a) Draw the dc and ac load lines for the network of Fig. 10.44 on the characteristics of Fig. 10.45.
(b) Determine the peak-to-peak value of I_c and V_{ce} from the graph if V_i has a peak value of 10 mV. Determine the voltage gain $A_v = V_o/V_i$ and compare with the solution obtained in Problem 1.

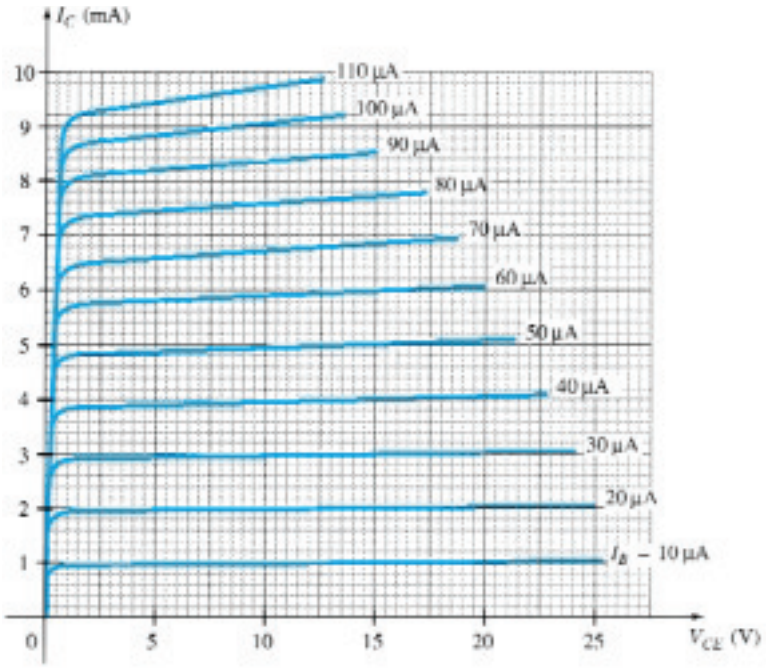


Figure 10.45 Problems 2 and 7

3. (a) Determine the voltage gain A_v for the network of Fig. 10.44 for $R_L = 4.7$, 2.2, and 0.5 kΩ. What is the effect of decreasing levels of R_L on the voltage gain?
(b) How will Z_i, Z_o, and $A_{v_{NL}}$ change with decreasing values of R_L?

§ 10.4 Effect of a Source Impedance (R_s)

* **4.** For the network of Fig. 10.46:
(a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
(b) Sketch the two-port model of Fig. 10.2 with the parameters determined in part (a) in place.
(c) Determine A_v using the results of part (b).
(d) Determine A_{v_s}.
(e) Determine A_{v_s} using the r_e model and compare the results to that obtained in part (d).
(f) Change R_s to 1 kΩ and determine A_v. How does A_v change with the level of R_s?
(g) Change R_s to 1 kΩ and determine A_{v_s}. How does A_{v_s} change with the level of R_s?
(h) Change R_s to 1 kΩ and determine $A_{v_{NL}}$, Z_i, and Z_o. How do they change with change in R_s?

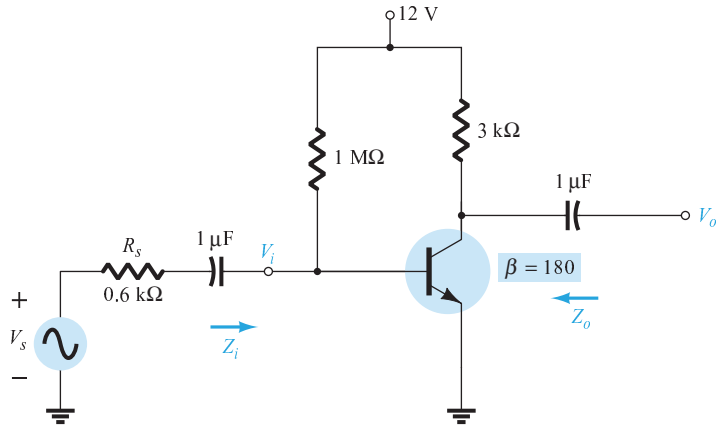


Figure 10.46 Problem 4

§ 10.5 Combined Effect of R_s and R_L

* **5.** For the network of Fig. 10.47:
(a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
(b) Sketch the two-port model of Fig. 10.2 with the parameters determined in part (a) in place.
(c) Determine A_v and A_{v_s}.
(d) Calculate A_i.
(e) Change R_L to 5.6 kΩ and calculate A_{v_s}. What is the effect of increasing levels of R_L on the gain?
(f) Change R_s to 0.5 kΩ (with R_L at 2.7 kΩ) and comment on the effect of reducing R_s on A_{v_s}.
(g) Change R_L to 5.6 kΩ and R_s to 0.5 kΩ and determine the new levels of Z_i and Z_o. How are the impedance parameters affected by changing levels of R_L and R_s?

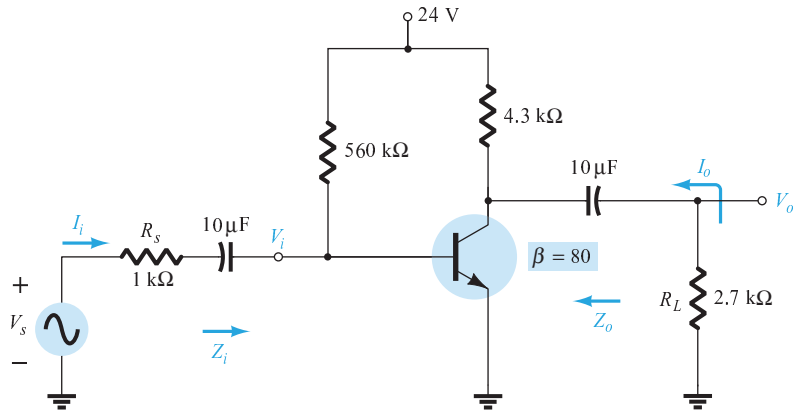


Figure 10.47 Problems 5 and 17

§ 10.6 BJT CE Networks

6. For the voltage-divider configuration of Fig. 10.48:
(a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
(b) Sketch the two-port model of Fig. 10.2 with the parameters determined in part (a) in place.
(c) Calculate the gain A_v using the model of part (b).
(d) Determine the current gain A_i.
(e) Determine A_v, Z_i, and Z_o using the r_e model and compare solutions.

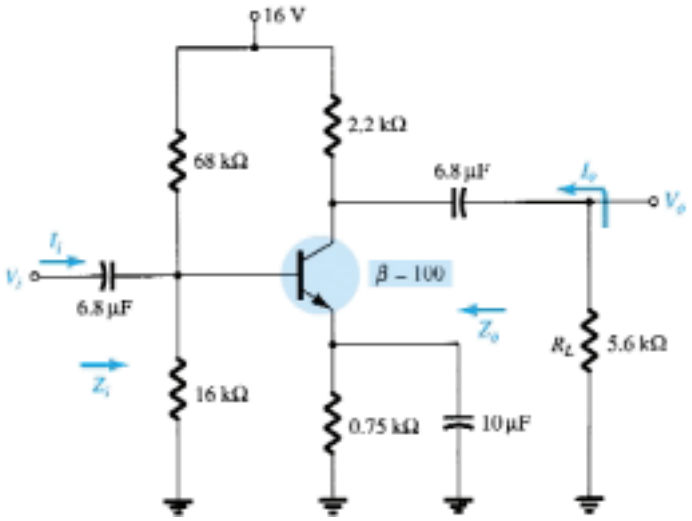


Figure 10.48 Problems 6, 7, and 8

* **7.** (a) Draw the dc and ac load lines for the network of Fig. 10.48 on the characteristics of Fig. 10.45.
(b) Determine the peak-to-peak value of I_c and V_{ce} from the graph if V_i has a peak value of 10 mV. Determine the voltage gain $A_v = V_o/V_i$ and compare the solution with that obtained in Problem 6.

8. (a) Determine the voltage gain A_v for the network of Fig. 10.48 with $R_L = 4.7$, 2.2, and 0.5 kΩ. What is the effect of decreasing levels of R_L on the voltage gain?
(b) How will Z_i, Z_o, and $A_{v_{NL}}$ change with decreasing levels of R_L?

9. For the emitter-stabilized network of Fig. 10.49:
(a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
(b) Sketch the two-port model of Fig. 10.2 with the values determined in part (a).
(c) Determine A_v and A_{v_s}.
(d) Change R_s to 1 kΩ. What is the effect on $A_{v_{NL}}$, Z_i, and Z_o?
(e) Change R_s to 1 kΩ and determine A_v and A_{v_s}. What is the effect of increasing levels of R_s on A_v and A_{v_s}?

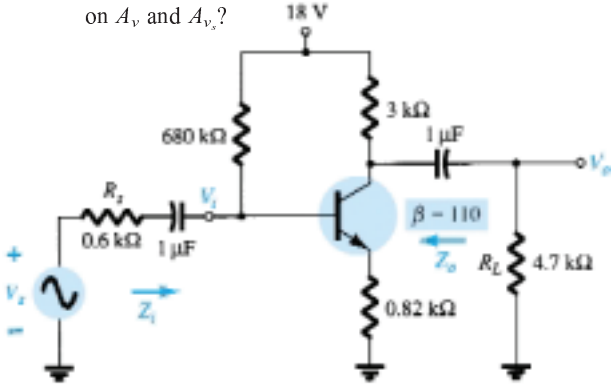


Figure 10.49 Problem 9

§ 10.7 BJT Emitter-Follower Networks

* **10.** For the network of Fig. 10.50:
  (a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
  (b) Sketch the two-port model of Fig. 10.2 with the values determined in part (a).
  (c) Determine A_v and A_{v_s}.
  (d) Change R_s to 1 kΩ and determine A_v and A_{v_s}. What is the effect of increasing levels of R_s on the voltage gains?
  (e) Change R_s to 1 kΩ and determine $A_{v_{NL}}$, Z_i, and Z_o. What is the effect of increasing levels of R_s on the parameters?
  (f) Change R_L to 5.6 kΩ and determine A_v and A_{v_s}. What is the effect of increasing levels of R_L on the voltage gains? Maintain R_s at its original level of 0.6 kΩ.

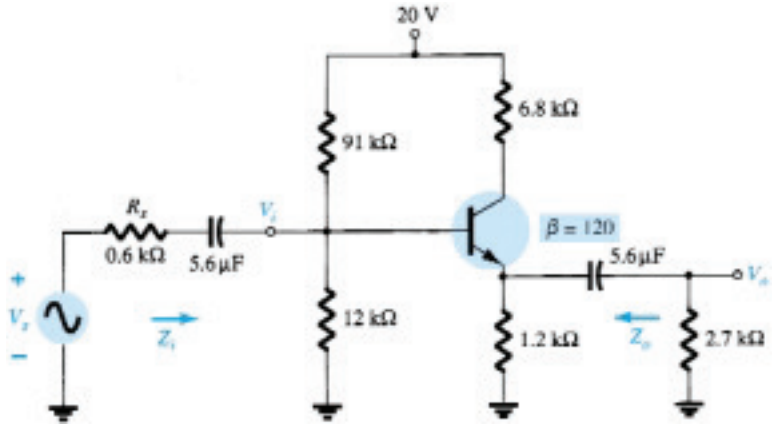


Figure 10.50 Problems 10 and 18

§ 10.8 BJT CB Networks

* **11.** For the common-base network of Fig. 10.51:
  (a) Determine Z_i, Z_o, and $A_{v_{NL}}$.
  (b) Sketch the two-port model of Fig. 10.2 with the parameters of part (a) in place.
  (c) Determine A_v and A_{v_s}.
  (d) Determine A_v and A_{v_s} using the r_e model and compare with the results of part (c).
  (e) Change R_s to 0.5 kΩ and R_L to 2.2 kΩ and calculate A_v and A_{v_s}. What is the effect of changing levels of R_s and R_L on the voltage gains?
  (f) Determine Z_o if R_s changed to 0.5 kΩ with all other parameters as appearing in Fig. 10.51. How is Z_o affected by changing levels of R_s?
  (g) Determine Z_i if R_L is reduced to 2.2 kΩ. What is the effect of changing levels of R_L on the input impedance?

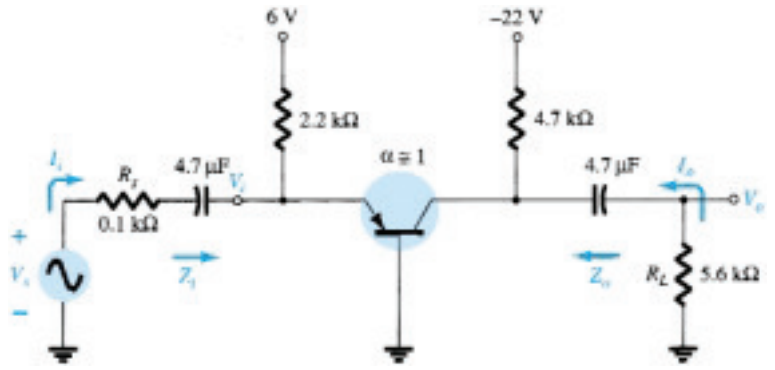


Figure 10.51 Problems 11 and 19

§ 10.9 FET Networks

12. For the self-bias JFET network of Fig. 10.52:
(a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
(b) Sketch the two-port model of Fig. 10.2 with the parameters determined in part (a) in place.
(c) Determine A_v and A_{v_s}.
(d) Change R_L to 6.8 kΩ and R_{sig} to 1 kΩ and calculate the new levels of A_v and A_{v_s}. How are the voltage gains affected by changes in R_{sig} and R_L?
(e) For the same changes as part (d), determine Z_i and Z_o. What was the impact on both impedances?

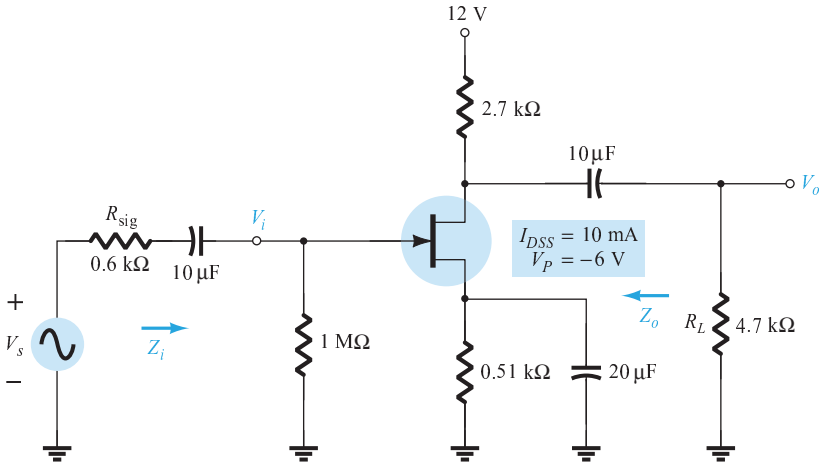


Figure 10.52 Problems 12 and 20

13. For the source-follower network of Fig. 10.53:
(a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
(b) Sketch the two-port model of Fig. 10.2 with the parameters determined in part (a) in place.
(c) Determine A_v and A_{v_s}.
(d) Change R_L to 4.7 kΩ and calculate A_v and A_{v_s}. What was the effect of increasing levels of R_L on both voltage gains?
(e) Change R_{sig} to 1 kΩ (with R_L at 2.2 kΩ) and calculate A_v and A_{v_s}. What was the effect of increasing levels of R_{sig} on both voltage gains?
(f) Change R_L to 4.7 kΩ and R_{sig} to 1 kΩ and calculate Z_i and Z_o. What was the effect on both parameters?

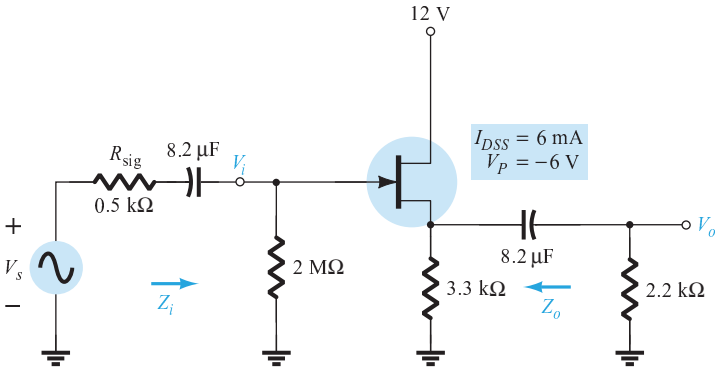


Figure 10.53 Problem 13

* **14.** For the common-gate configuration of Fig. 10.54:
  (a) Determine $A_{v_{NL}}$, Z_i, and Z_o.
  (b) Sketch the two-port model of Fig. 10.2 with the parameters determined in part (a) in place.
  (c) Determine A_v and A_{v_s}.
  (d) Change R_L to 2.2 kΩ and calculate A_v and A_{v_s}. What was the effect of changing R_L on the voltage gains?
  (e) Change R_{sig} to 0.5 kΩ (with R_L at 4.7 kΩ) and calculate A_v and A_{v_s}. What was the effect of changing R_{sig} on the voltage gains?
  (f) Change R_L to 2.2 kΩ and R_{sig} to 0.5 kΩ and calculate Z_i and Z_o. What was the effect on both parameters?

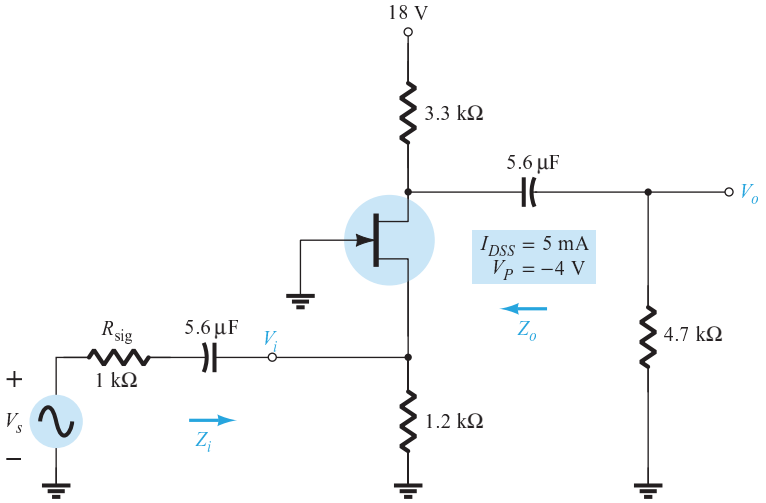


Figure 10.54 Problem 14

§ 10.11 Cascaded Systems

* **15.** For the cascaded system of Fig. 10.55 with two identical stages, determine:
  (a) The loaded voltage gain of each stage.
  (b) The total gain of the system, A_v and A_{v_s}.
  (c) The loaded current gain of each stage.
  (d) The total current gain of the system.
  (e) How Z_i is affected by the second stage and R_L.
  (f) How Z_o is affected by the first stage and R_s.
  (g) The phase relationship between V_o and V_i.

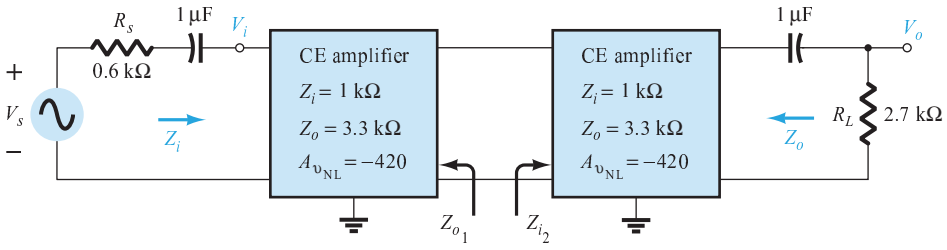


Figure 10.55 Problem 15

* **16.** For the cascaded system of Fig. 10.56, determine:
(a) The loaded voltage gain of each stage.
(b) The total gain of the system, A_v and A_{v_s}.
(c) The loaded current gain of each stage.
(d) The total current gain of the system.
(e) How Z_i is affected by the second stage and R_L.
(f) How Z_o is affected by the first stage and R_s.
(g) The phase relationship between V_o and V_i.

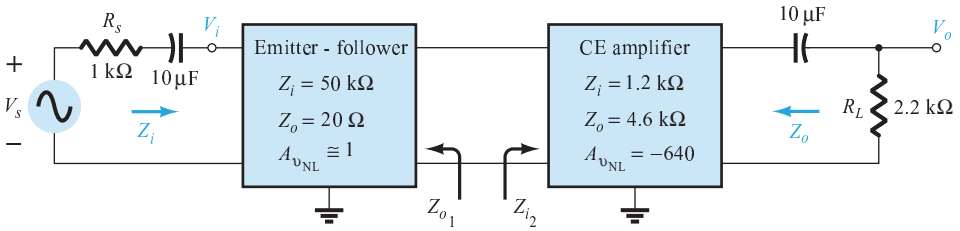


Figure 10.56 Problem 16

§ 10.12 PSpice Windows

17. Using PSpice Windows, determine the level of V_o for V_s = 1 mV for the network of Fig. 10.47. For the capacitive elements assume a frequency of 1 kHz.

18. Repeat Problem 17 for the network of Fig. 10.50 and compare the results with those of Problem 10.

19. Repeat Problem 17 for the network of Fig. 10.51 and compare with the results of Problem 11.

20. Repeat Problem 17 for the network of Fig. 10.52 and compare with the results of Problem 12.

*Please Note: Asterisks indicate more difficult problems.

CHAPTER 11

BJT and JFET Frequency Response

11.1 INTRODUCTION

The analysis thus far has been limited to a particular frequency. For the amplifier, it was a frequency that normally permitted ignoring the effects of the capacitive elements, reducing the analysis to one that included only resistive elements and sources of the independent and controlled variety. We will now investigate the frequency effects introduced by the larger capacitive elements of the network at low frequencies and the smaller capacitive elements of the active device at the high frequencies. Since the analysis will extend through a wide frequency range, the logarithmic scale will be defined and used throughout the analysis. In addition, since industry typically uses a decibel scale on its frequency plots, the concept of the decibel is introduced in some detail. The similarities between the frequency response analyses of both BJTs and FETs permit a coverage of each in the same chapter.

11.2 LOGARITHMS

There is no escaping the need to become comfortable with the logarithmic function. The plotting of a variable between wide limits, comparing levels without unwieldy numbers, and identifying levels of particular importance in the design, review, and analysis procedures are all positive features of using the logarithmic function.

As a first step in clarifying the relationship between the variables of a logarithmic function, consider the following mathematical equations:

$$a = b^x, \qquad x = \log_b a \tag{11.1}$$

The variables a, b, and x are the same in each equation. If a is determined by taking the base b to the x power, the same x will result if the log of a is taken to the base b. For instance, if $b = 10$ and $x = 2$,

$$a = b^x = (10)^2 = 100$$

but

$$x = \log_b a = \log_{10} 100 = 2$$

In other words, if you were asked to find the power of a number that would result in a particular level such as shown below:

$$10{,}000 = 10^x$$

f

the level of x could be determined using logarithms. That is,

$$x = \log_{10} 10{,}000 = 4$$

For the electrical/electronics industry and in fact for the vast majority of scientific research, the base in the logarithmic equation is limited to 10 and the number $e = 2.71828\ldots$.

Logarithms taken to the base 10 are referred to as *common logarithms,* while logarithms taken to the base e are referred to as *natural logarithms.* In summary:

$$\text{Common logarithm:} \quad x = \log_{10} a \tag{11.2}$$

$$\text{Natural logarithm:} \quad y = \log_e a \tag{11.3}$$

The two are related by

$$\log_e a = 2.3 \log_{10} a \tag{11.4}$$

On today's scientific calculators, the common logarithm is typically denoted by the log key and the natural logarithm by the ln key.

EXAMPLE 11.1

Using the calculator, determine the logarithm of the following numbers to the base indicated.

(a) $\log_{10} 10^6$.
(b) $\log_e e^3$.
(c) $\log_{10} 10^{-2}$.
(d) $\log_e e^{-1}$.

Solution

(a) **6** (b) **3** (c) **−2** (d) **−1**

The results in Example 11.1 clearly reveal that the logarithm of a number taken to a power is simply the power of the number if the number matches the base of the logarithm. In the next example, the base and the variable x are not related by an integer power of the base.

EXAMPLE 11.2

Using the calculator, determine the logarithm of the following numbers.

(a) $\log_{10} 64$.
(b) $\log_e 64$.
(c) $\log_{10} 1600$.
(d) $\log_{10} 8000$.

Solution

(a) **1.806** (b) **4.159** (c) **3.204** (d) **3.903**

Note in parts (a) and (b) of Example 11.2 that the logarithms $\log_{10} a$ and $\log_e a$ are indeed related as defined by Eq. (11.4). In addition, note that the logarithm of a number does not increase in the same linear fashion as the number. That is, 8000 is 125 times larger than 64, but the logarithm of 8000 is only about 2.16 times larger

than the magnitude of the logarithm of 64, revealing a very nonlinear relationship. In fact, Table 11.1 clearly shows how the logarithm of a number increases only as the exponent of the number. If the antilogarithm of a number is desired, the 10^x or e^x calculator functions are employed.

TABLE 11.1

$\log_{10} 10^0$	$= 0$
$\log_{10} 10$	$= 1$
$\log_{10} 100$	$= 2$
$\log_{10} 1{,}000$	$= 3$
$\log_{10} 10{,}000$	$= 4$
$\log_{10} 100{,}000$	$= 5$
$\log_{10} 1{,}000{,}000$	$= 6$
$\log_{10} 10{,}000{,}000$	$= 7$
$\log_{10} 100{,}000{,}000$	$= 8$
and so on	

EXAMPLE 11.3

Using a calculator, determine the antilogarithm of the following expressions:
(a) $1.6 = \log_{10} a$.
(b) $0.04 = \log_e a$.

Solution

(a) $a = 10^{1.6}$
Calculator keys: 1 . 6 2nd F 10^x
and $a =$ **39.81**

(b) $a = e^{0.04}$
Calculator keys: 0 . 0 4 2nd F e^x
and $a =$ **1.0408**

Since the remaining analysis of this chapter employs the common logarithm, let us now review a few properties of logarithms using solely the common logarithm. In general, however, the same relationships hold true for logarithms to any base.

$$\log_{10} 1 = 0 \tag{11.5}$$

As clearly revealed by Table 11.1, since $10^0 = 1$,

$$\log_{10} \frac{a}{b} = \log_{10} a - \log_{10} b \tag{11.6}$$

which for the special case of $a = 1$ becomes

$$\log_{10} \frac{1}{b} = -\log_{10} b \tag{11.7}$$

revealing that for any b greater than 1 the logarithm of a number less than 1 is always negative.

$$\log_{10} ab = \log_{10} a + \log_{10} b \tag{11.8}$$

In each case, the equations employing natural logarithms will have the same format.

EXAMPLE 11.4

Using a calculator, determine the logarithm of the following numbers:

(a) $\log_{10} 0.5$.

(b) $\log_{10} \dfrac{4000}{250}$.

(c) $\log_{10} (0.6 \times 30)$.

Solution

(a) $\mathbf{-0.3}$

(b) $\log_{10} 4000 - \log_{10} 250 = 3.602 - 2.398 = \mathbf{1.204}$

Check: $\log_{10} \dfrac{4000}{250} = \log_{10} 16 = \mathbf{1.204}$

(c) $\log_{10} 0.6 + \log_{10} 30 = -0.2218 + 1.477 = \mathbf{1.255}$

Check: $\log_{10} (0.6 \times 30) = \log_{10} 18 = \mathbf{1.255}$

The use of log scales can significantly expand the range of variation of a particular variable on a graph. Most graph paper available is of the semilog or double-log (log-log) variety. The term *semi* (meaning one-half) indicates that only one of the two scales is a log scale, whereas double-log indicates that both scales are log scales. A semilog scale appears in Fig. 11.1. Note that the vertical scale is a linear scale with equal divisions. The spacing between the lines of the log plot is shown on the graph.

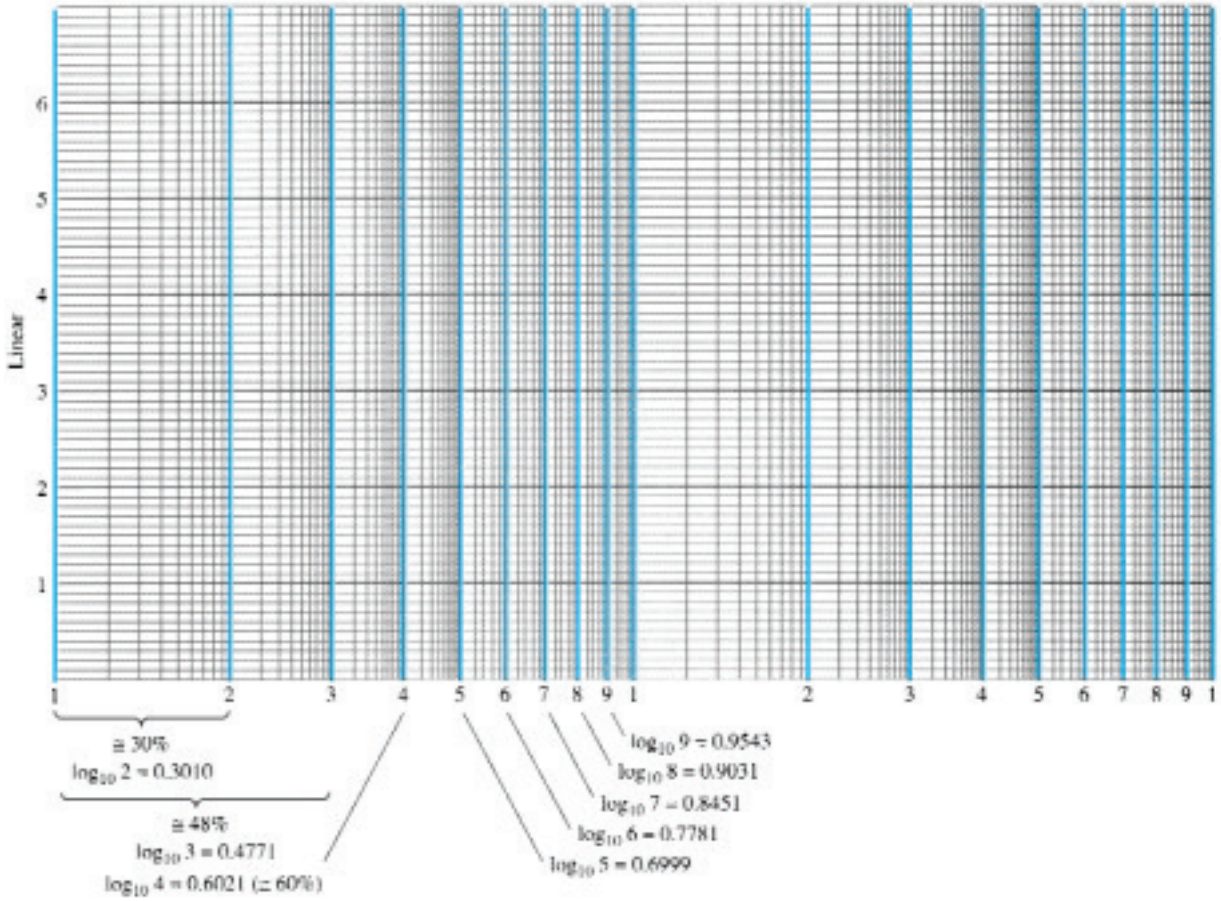


Figure 11.1 Semilog graph paper.

The log of 2 to the base 10 is approximately 0.3. The distance from 1 ($\log_{10} 1 = 0$) to 2 is therefore 30% of the span. The log of 3 to the base 10 is 0.4771 or almost 48% of the span (very close to one-half the distance between power of 10 increments on the log scale). Since $\log_{10} 5 \cong 0.7$, it is marked off at a point 70% of the distance. Note that between any two digits the same compression of the lines appears as you progress from the left to the right. It is important to note the resulting numerical value and the spacing, since plots will typically only have the tic marks indicated in Fig. 11.2 due to a lack of space. You must realize that the longer bars for this figure have the numerical values of 0.3, 3, and 30 associated with them, whereas the next shorter bars have values of 0.5, 5, and 50 and the shortest bars 0.7, 7, and 70.

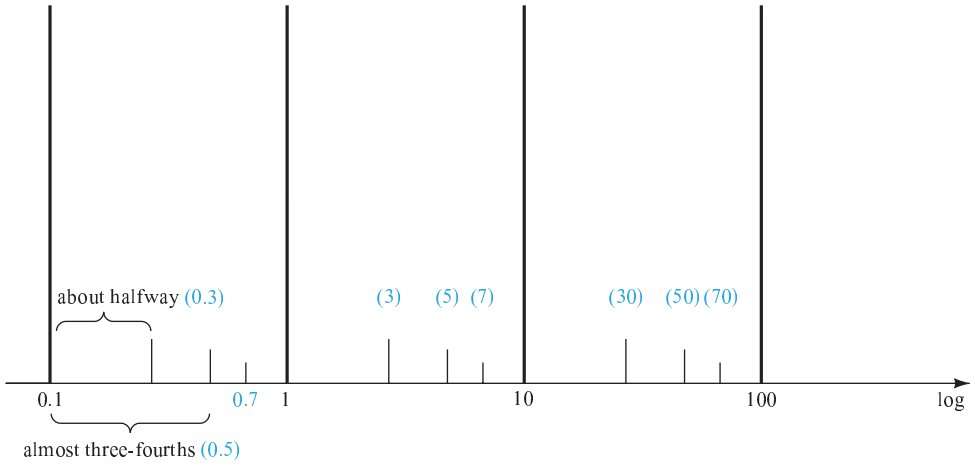


Figure 11.2 Identifying the numerical values of the tic marks on a log scale.

Be aware that plotting a function on a log scale can change the general appearance of the waveform as compared to a plot on a linear scale. A straight-line plot on a linear scale can develop a curve on a log scale, and a nonlinear plot on a linear scale can take on the appearance of a straight line on a log plot. The important point is that the results extracted at each level be correctly labeled by developing a familiarity with the spacing of Figs. 11.1 and 11.2. This is particularly true for some of the log-log plots that appear later in the book.

11.3 DECIBELS

The concept of the decibel (dB) and the associated calculations will become increasingly important in the remaining sections of this chapter. The background surrounding the term *decibel* has its origin in the established fact that power and audio levels are related on a logarithmic basis. That is, an increase in power level, say 4 to 16 W, does not result in an audio level increase by a factor of 16/4 = 4. It will increase by a factor of 2 as derived from the power of 4 in the following manner: $(4)^2 = 16$. For a change of 4 to 64 W, the audio level will increase by a factor of 3 since $(4)^3 = 64$. In logarithmic form, the relationship can be written as $\log_4 64 = 3$.

The term *bel* was derived from the surname of Alexander Graham Bell. For standardization, the bel (B) was defined by the following equation to relate power levels P_1 and P_2:

$$G = \log_{10} \frac{P_2}{P_1} \quad \text{bel} \tag{11.9}$$

f

It was found, however, that the bel was too large a unit of measurement for practical purposes, so the decibel (dB) was defined such that 10 decibels = 1 bel. Therefore,

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} \quad \text{dB} \tag{11.10}$$

The terminal rating of electronic communication equipment (amplifiers, microphones, etc.) is commonly rated in decibels. Equation (11.10) indicates clearly, however, that the decibel rating is a measure of the difference in magnitude between *two* power levels. For a specified terminal (output) power (P_2) there must be a reference power level (P_1). The reference level is generally accepted to be 1 mW, although on occasion, the 6-mW standard of earlier years is applied. The resistance to be associated with the 1-mW power level is 600 Ω, chosen because it is the characteristic impedance of audio transmission lines. When the 1-mW level is employed as the reference level, the decibel symbol frequently appears as dBm. In equation form,

$$G_{\text{dBm}} = 10 \log_{10} \frac{P_2}{1 \text{ mW}}\bigg|_{600\ \Omega} \quad \text{dBm} \tag{11.11}$$

There exists a second equation for decibels that is applied frequently. It can be best described through the system of Fig. 11.3. For V_i equal to some value V_1, $P_1 = V_1^2/R_i$, where R_i, is the input resistance of the system of Fig. 11.3. If V_i should be increased (or decreased) to some other level, V_2, then $P_2 = V_2^2/R_i$. If we substitute into Eq. (11.10) to determine the resulting difference in decibels between the power levels,

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} = 10 \log_{10} \frac{V_2^2/R_i}{V_1^2/R_i} = 10 \log_{10} \left(\frac{V_2}{V_1}\right)^2$$

and

$$G_{\text{dB}} = 20 \log_{10} \frac{V_2}{V_1} \quad \text{dB} \tag{11.12}$$

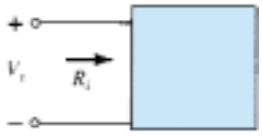


Figure 11.3 Configuration employed in the discussion of Eq. (11.12).

Frequently, the effect of different impedances ($R_1 \neq R_2$) is ignored and Eq. (11.12) applied simply to establish a basis of comparison between levels—voltage or current. For situations of this type, the decibel gain should more correctly be referred to as the voltage or current gain in decibels to differentiate it from the common usage of decibel as applied to power levels.

One of the advantages of the logarithmic relationship is the manner in which it can be applied to cascaded stages. For example, the magnitude of the overall voltage gain of a cascaded system is given by

$$|A_{v_T}| = |A_{v_1}||A_{v_2}||A_{v_3}|\cdots|A_{v_n}| \tag{11.13}$$

Applying the proper logarithmic relationship results in

$$G_v = 20 \log_{10} |A_{v_T}| = 20 \log_{10} |A_{v_1}| + 20 \log_{10} |A_{v_2}| + 20 \log_{10} |A_{v_3}| + \cdots + 20 \log_{10} |A_{v_n}| \quad \text{(dB)} \tag{11.14}$$

In words, the equation states that the decibel gain of a cascaded system is simply the sum of the decibel gains of each stage, that is,

$$\boxed{G_v = G_{v_1} + G_{v_2} + G_{v_3} + \cdots + G_{v_n}} \quad \text{dB} \tag{11.15}$$

In an effort to develop some association between dB levels and voltage gains, Table 11.2 was developed. First note that a gain of 2 results in a dB level of +6 dB while a drop to $\frac{1}{2}$ results in a −6-dB level. A change in V_o/V_i from 1 to 10, 10 to 100, or 100 to 1000 results in the same 20-dB change in level. When $V_o = V_i$, $V_o/V_i = 1$ and the dB level is 0. At a very high gain of 1000, the dB level is 60, while at the much higher gain of 10,000, the dB level is 80 dB, an increase of only 20 dB—a result of the logarithmic relationship. Table 11.2 clearly reveals that voltage gains of 50 dB or higher should immediately be recognized as being quite high.

TABLE 11.2

Voltage Gain, V_o/V_i	*dB Level*
0.5	−6
0.707	−3
1	0
2	6
10	20
40	32
100	40
1000	60
10,000	80
etc.	

EXAMPLE 11.5

Find the magnitude gain corresponding to a decibel gain of 100.

Solution

By Eq. (11.10),

$$G_{\text{dB}} = 10 \log_{10} \frac{P_2}{P_1} = 100 \text{ dB} \rightarrow \log_{10} \frac{P_2}{P_1} = 10$$

so that

$$\frac{P_2}{P_1} = \mathbf{10^{10} = 10{,}000{,}000{,}000}$$

This example clearly demonstrates the range of decibel values to be expected from practical devices. Certainly, a future calculation giving a decibel result in the neighborhood of 100 should be questioned immediately.

EXAMPLE 11.6

The input power to a device is 10,000 W at a voltage of 1000 V. The output power is 500 W, while the output impedance is 20 Ω.

(a) Find the power gain in decibels.

(b) Find the voltage gain in decibels.

(c) Explain why parts (a) and (b) agree or disagree.

Solution

(a) $$G_{\text{dB}} = 10 \log_{10} \frac{P_o}{P_i} = 10 \log_{10} \frac{500 \text{ W}}{10 \text{ kW}} = 10 \log_{10} \frac{1}{20} = -10 \log_{10} 20$$

$$= -10(1.301) = \mathbf{-13.01 \text{ dB}}$$

(b) $$G_v = 20 \log_{10} \frac{V_o}{V_i} = 20 \log_{10} \frac{\sqrt{PR}}{1000} = 20 \log_{10} \frac{\sqrt{(500 \text{ W})(20 \ \Omega)}}{1000 \text{ V}}$$

$$= 20 \log_{10} \frac{100}{1000} = 20 \log_{10} \frac{1}{10} = -20 \log_{10} 10 = \mathbf{-20 \text{ dB}}$$

(c) $$R_i = \frac{V_i^2}{P_i} = \frac{(1 \text{ kV})^2}{10 \text{ kW}} = \frac{10^6}{10^4} = \mathbf{100 \ \Omega} \neq R_o = \mathbf{20 \ \Omega}$$

EXAMPLE 11.7

An amplifier rated at 40-W output is connected to a 10-Ω speaker.

(a) Calculate the input power required for full power output if the power gain is 25 dB.

(b) Calculate the input voltage for rated output if the amplifier voltage gain is 40 dB.

Solution

(a) Eq. (11.10): $25 = 10 \log_{10} \frac{40\text{ W}}{P_i} \Rightarrow P_i = \frac{40\text{ W}}{\text{antilog } (2.5)} = \frac{40\text{ W}}{3.16 \times 10^2}$

$$= \frac{40\text{ W}}{316} \cong \mathbf{126.5\ mW}$$

(b) $G_v = 20 \log_{10} \frac{V_o}{V_i} \Rightarrow 40 = 20 \log_{10} \frac{V_o}{V_i}$

$$\frac{V_o}{V_i} = \text{antilog } 2 = 100$$

$$V_o = \sqrt{PR} = \sqrt{(40\text{ W})(10\text{ V})} = 20\text{ V}$$

$$V_i = \frac{V_o}{100} = \frac{20\text{ V}}{100} = 0.2\text{ V} = \mathbf{200\ mV}$$

11.4 GENERAL FREQUENCY CONSIDERATIONS

The frequency of the applied signal can have a pronounced effect on the response of a single-stage or multistage network. The analysis thus far has been for the midfrequency spectrum. At low frequencies, we shall find that the coupling and bypass capacitors can no longer be replaced by the short-circuit approximation because of the increase in reactance of these elements. The frequency-dependent parameters of the small-signal equivalent circuits and the stray capacitive elements associated with the active device and the network will limit the high-frequency response of the system. An increase in the number of stages of a cascaded system will also limit both the high- and low-frequency responses.

The magnitudes of the gain response curves of an *RC*-coupled, direct-coupled, and transformer-coupled amplifier system are provided in Fig. 11.4. Note that the horizontal scale is a logarithmic scale to permit a plot extending from the low- to the high-frequency regions. For each plot, a low-, high-, and mid-frequency region has been defined. In addition, the primary reasons for the drop in gain at low and high frequencies have also been indicated within the parentheses. For the *RC*-coupled amplifier, the drop at low frequencies is due to the increasing reactance of C_C, C_s, or C_E, while its upper frequency limit is determined by either the parasitic capacitive elements of the network and frequency dependence of the gain of the active device. An explanation of the drop in gain for the transformer-coupled system requires a basic understanding of "transformer action" and the transformer equivalent circuit. For the moment, let us say that it is simply due to the "shorting effect" (across the input terminals of the transformer) of the magnetizing inductive reactance at low frequencies ($X_L = 2\pi fL$). The gain must obviously be zero at $f = 0$ since at this point there is no longer a changing flux established through the core to induce a secondary or output voltage. As indicated in Fig. 11.4, the high-frequency response is controlled primarily by the stray capacitance between the turns of the primary and secondary wind-

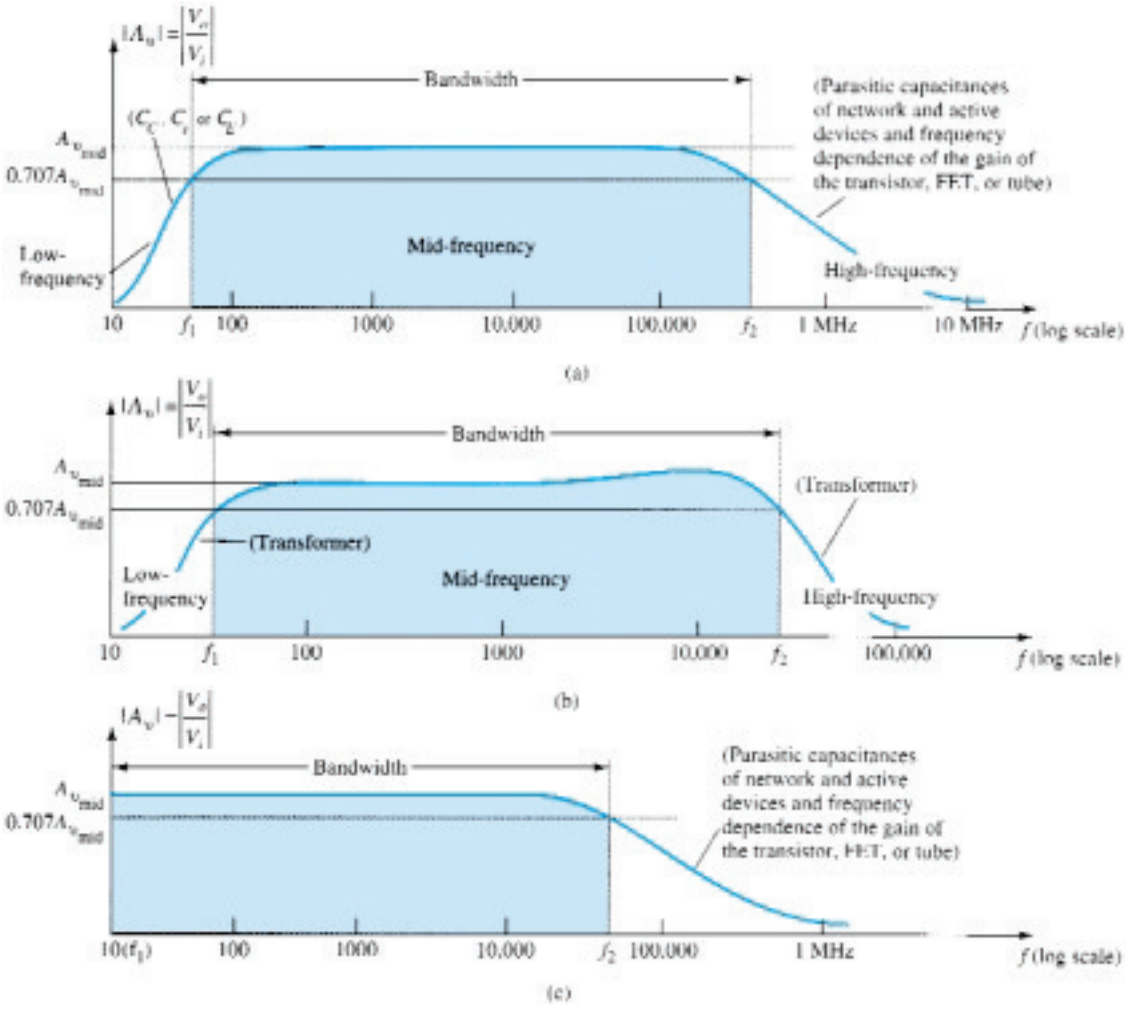


Figure 11.4 Gain versus frequency: (a) *RC*-coupled amplifiers; (b) transformer-coupled amplifiers; (c) direct-coupled amplifiers.

ings. For the direct-coupled amplifier, there are no coupling or bypass capacitors to cause a drop in gain at low frequencies. As the figure indicates, it is a flat response to the upper cutoff frequency, which is determined by either the parasitic capacitances of the circuit or the frequency dependence of the gain of the active device.

For each system of Fig. 11.4, there is a band of frequencies in which the magnitude of the gain is either equal or relatively close to the midband value. To fix the frequency boundaries of relatively high gain, $0.707A_{v_{\text{mid}}}$ was chosen to be the gain at the cutoff levels. The corresponding frequencies f_1 and f_2 are generally called the *corner, cutoff, band, break,* or *half-power frequencies.* The multiplier 0.707 was chosen because at this level the output power is half the midband power output, that is, at midfrequencies,

$$P_{o_{\text{mid}}} = \frac{|V^2{}_o|}{R_o} = \frac{|A_{v_{\text{mid}}} V_i|^2}{R_o}$$

and at the half-power frequencies,

$$P_{o_{HPF}} = \frac{|0.707A_{v_{\text{mid}}} V_i|^2}{R_o} = 0.5\,\frac{|A_{v_{\text{mid}}} V_i|^2}{R_o}$$

and $$P_{o_{HPF}} = 0.5P_{o_{mid}} \tag{11.16}$$

The bandwidth (or passband) of each system is determined by f_1 and f_2, that is,

$$\text{bandwidth (BW)} = f_2 - f_1 \tag{11.17}$$

For applications of a communications nature (audio, video), a decibel plot of the voltage gain versus frequency is more useful than that appearing in Fig. 11.4. Before obtaining the logarithmic plot, however, the curve is generally normalized as shown in Fig. 11.5. In this figure, the gain at each frequency is divided by the midband value. Obviously, the midband value is then 1 as indicated. At the half-power frequencies, the resulting level is $0.707 = 1/\sqrt{2}$. A decibel plot can now be obtained by applying Eq. (11.12) in the following manner:

$$\frac{A_v}{A_{v_{mid}}}\Big|_{dB} = 20 \log_{10} \frac{A_v}{A_{v_{mid}}} \tag{11.18}$$

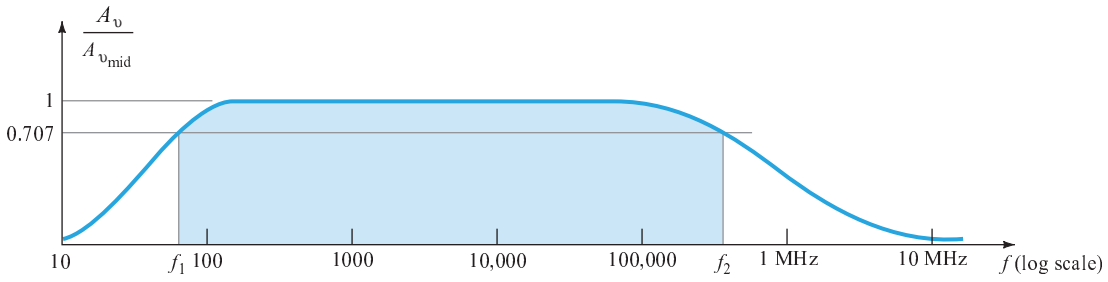


Figure 11.5 Normalized gain versus frequency plot.

At midband frequencies, $20 \log_{10} 1 = 0$, and at the cutoff frequencies, $20 \log_{10} 1/\sqrt{2} = -3$ dB. Both values are clearly indicated in the resulting decibel plot of Fig. 11.6. The smaller the fraction ratio, the more negative the decibel level.

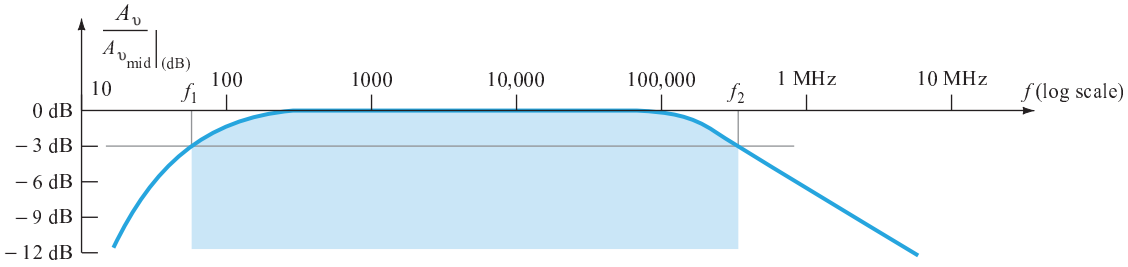


Figure 11.6 Decibel plot of the normalized gain versus frequency plot of Fig. 11.5.

For the greater part of the discussion to follow, a decibel plot will be made only for the low- and high-frequency regions. Keep Fig. 11.6 in mind, therefore, to permit a visualization of the broad system response.

It should be understood that most amplifiers introduce a 180° phase shift between input and output signals. This fact must now be expanded to indicate that this is the case only in the midband region. At low frequencies, there is a phase shift such that V_o lags V_i by an increased angle. At high frequencies, the phase shift will drop below 180°. Figure 11.7 is a standard phase plot for an *RC*-coupled amplifier.

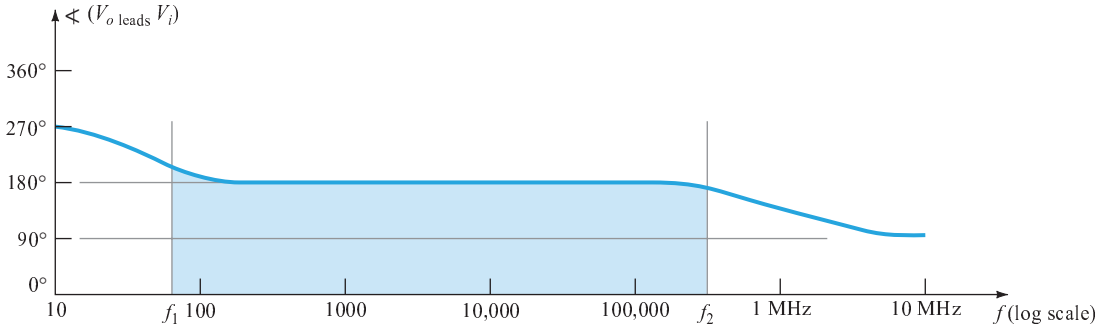


Figure 11.7 Phase plot for an *RC*-coupled amplifier system.

11.5 LOW-FREQUENCY ANALYSIS—BODE PLOT

In the low-frequency region of the single-stage BJT or FET amplifier, it is the *R-C* combinations formed by the network capacitors C_C, C_E, and C_s and the network resistive parameters that determine the cutoff frequencies. In fact, an *R-C* network similar to Fig. 11.8 can be established for each capacitive element and the frequency at which the output voltage drops to 0.707 of its maximum value determined. Once the cutoff frequencies due to each capacitor are determined, they can be compared to establish which will determine the low-cutoff frequency for the system.

Our analysis, therefore, will begin with the series *R-C* combination of Fig. 11.8 and the development of a procedure that will result in a plot of the frequency response with a minimum of time and effort. At very high frequencies,

$$X_C = \frac{1}{2\pi fC} \cong 0\ \Omega$$

and the short-circuit equivalent can be substituted for the capacitor as shown in Fig. 11.9. The result is that $V_o \cong V_i$ at high frequencies. At $f = 0$ Hz,

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(0)C} = \infty\ \Omega$$

and the open-circuit approximation can be applied as shown in Fig. 11.10, with the result that $V_o = 0$ V.

Between the two extremes, the ratio $A_v = V_o/V_i$ will vary as shown in Fig. 11.11. As the frequency increases, the capacitive reactance decreases and more of the input voltage appears across the output terminals.

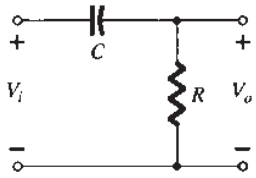


Figure 11.8 *R-C* combination that will define a low cutoff frequency.

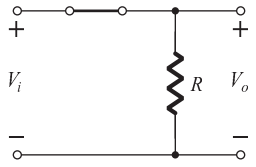


Figure 11.9 *R-C* circuit of Figure 11.8 at very high frequencies.

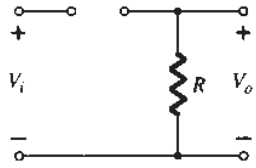


Figure 11.10 *R-C* circuit of Figure 11.8 at $f = 0$ Hz.

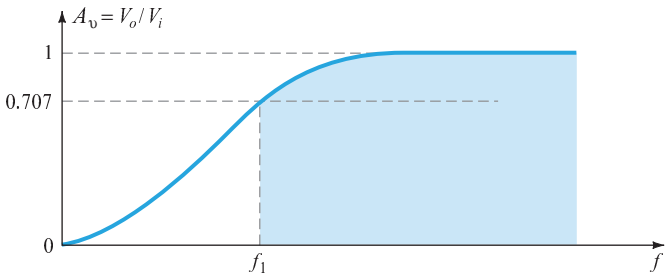


Figure 11.11 Low frequency response for the *R-C* circuit of Figure 11.8.

f

The output and input voltages are related by the voltage-divider rule in the following manner:

$$\mathbf{V}_o = \frac{\mathbf{R}\mathbf{V}_i}{\mathbf{R} + \mathbf{X}_C}$$

with the magnitude of V_o determined by

$$V_o = \frac{RV_i}{\sqrt{R^2 + X_C^2}}$$

For the special case where $X_C = R$,

$$V_o = \frac{RV_i}{\sqrt{R^2X_C^2}} = \frac{RV_i}{} = \frac{RV_i}{\sqrt{2R^2}} = \frac{RV_i}{\sqrt{2R}} = \frac{1}{\sqrt{2}}\,V_i$$

and

$$\boxed{|A_v| = \frac{V_o}{V_i} = \frac{1}{\sqrt{2}} = 0.707|_{X_C=R}} \tag{11.19}$$

the level of which is indicated on Fig. 11.11. In other words, at the frequency of which $X_C = R$, the output will be 70.7% of the input for the network of Fig. 11.8.

The frequency at which this occurs is determined from

$$X_C = \frac{1}{2\pi f_1 C} = R$$

and

$$\boxed{f_1 = \frac{1}{2\pi RC}} \tag{11.20}$$

In terms of logs,

$$G_v = 20\log_{10} A_v = 20\log_{10}\frac{1}{\sqrt{2}} = -3 \text{ dB}$$

while at $A_v = V_o/V_i = 1$ or $V_o = V_i$ (the maximum value),

$$G_v = 20\log_{10} 1 = 20(0) = 0 \text{ dB}$$

In Fig. 11.6, we recognize that there is a 3-dB drop in gain from the midband level when $f = f_1$. In a moment, we will find that an *RC* network will determine the low-frequency cutoff frequency for a BJT transistor and f_1 will be determined by Eq. (11.20).

If the gain equation is written as

$$A_v = \frac{V_o}{V_i} = \frac{R}{R - jX_C} = \frac{1}{1 - j(X_C/R)} = \frac{1}{1 - j(1/\omega CR)} = \frac{1}{1 - j(1/2\pi fCR)}$$

and using the frequency defined above,

$$\boxed{A_v = \frac{1}{1 - j(f_1/f)}} \tag{11.21}$$

In the magnitude and phase form,

$$A_v = \frac{V_o}{V_i} = \underbrace{\frac{1}{\sqrt{1 + (f_1/f)^2}}}_{\text{magnitude of } A_v}\ \underbrace{\angle \tan^{-1}(f_1/f)}_{\substack{\text{phase } \sphericalangle \text{ by which} \\ V_o \text{ leads } V_i}} \tag{11.22}$$

For the magnitude when $f = f_1$,

$$|A_v| = \frac{1}{\sqrt{1 + (1)^2}} = \frac{1}{\sqrt{2}} = 0.707 \rightarrow -3 \text{ dB}$$

In the logarithmic form, the gain in dB is

$$A_{v(\text{dB})} = 20 \log_{10} \frac{1}{\sqrt{1 + (f_1/f)^2}} = -20 \log_{10} \left[1 + \left(\frac{f_1}{f}\right)^2\right]^{1/2}$$

$$= -(\tfrac{1}{2})(20) \log_{10} \left[1 + \left(\frac{f_1}{f}\right)^2\right]$$

$$= -10 \log_{10} \left[1 + \left(\frac{f_1}{f}\right)^2\right]$$

For frequencies where $f \ll f_1$ or $(f_1/f)^2 \gg 1$, the equation above can be approximated by

$$A_{v(\text{dB})} = -10 \log_{10} \left(\frac{f_1}{f}\right)^2$$

and finally,

$$\boxed{A_{v(\text{dB})} = -20 \log_{10} \frac{f_1}{f}}_{f \ll f_1} \qquad (11.23)$$

Ignoring the condition $f \ll f_1$ for a moment, a plot of Eq. (11.23) on a frequency log scale will yield a result of a very useful nature for future decibel plots.

$$\text{At } f = f_1\text{: } \frac{f_1}{f} = 1 \text{ and } -20 \log_{10} 1 = 0 \text{ dB}$$

$$\text{At } f = \tfrac{1}{2} f_1\text{: } \frac{f_1}{f} = 2 \text{ and } -20 \log_{10} 2 \cong -6 \text{ dB}$$

$$\text{At } f = \tfrac{1}{4} f_1\text{: } \frac{f_1}{f} = 4 \text{ and } -20 \log_{10} 4 \cong -12 \text{ dB}$$

$$\text{At } f = \tfrac{1}{10} f_1\text{: } \frac{f_1}{f} = 10 \text{ and } -20 \log_{10} 10 = -20 \text{ dB}$$

A plot of these points is indicated in Fig. 11.12 from $0.1f_1$ to f_1. Note that this results in a straight line when plotted against a log scale. In the same figure, a straight

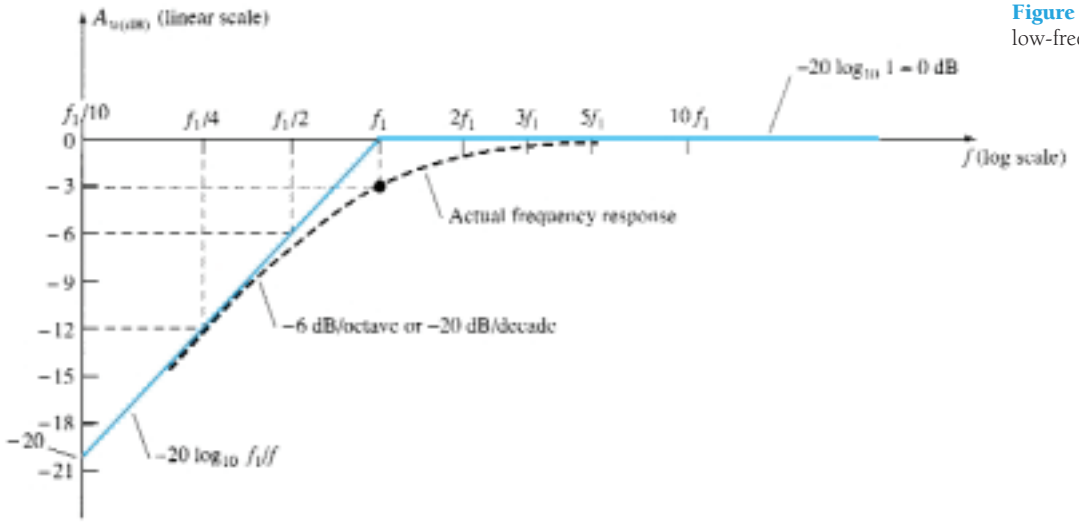


Figure 11.12 Bode plot for the low-frequency region.

line is also drawn for the condition of 0 dB for $f \gg f_1$. As stated earlier, the straight-line segments (asymptotes) are only accurate for 0 dB when $f \gg f_1$ and the sloped line when $f_1 \gg f$. We know, however, that when $f = f_1$, there is a 3-dB drop from the mid-band level. Employing this information in association with the straight-line segments permits a fairly accurate plot of the frequency response as indicated in the same figure. The piecewise linear plot of the asymptotes and associated breakpoints is called a *Bode plot* of the magnitude versus frequency.

The calculations above and the curve itself demonstrate clearly that:

A change in frequency by a factor of 2, equivalent to 1 octave, results in a 6-dB change in the ratio as noted by the change in gain from $f_1/2$ to f_1.

As noted by the change in gain from $f_1/2$ to f_1:

For a 10:1 change in frequency, equivalent to 1 decade, there is a 20-dB change in the ratio as demonstrated between the frequencies of $f_1/10$ and f_1.

In the future, therefore, a decibel plot can easily be obtained for a function having the format of Eq. (11.23). First, simply find f_1 from the circuit parameters and then sketch two asymptotes—one along the 0-dB line and the other drawn through f_1 sloped at 6 dB/octave or 20 dB/decade. Then, find the 3-dB point corresponding to f_1 and sketch the curve.

EXAMPLE 11.8

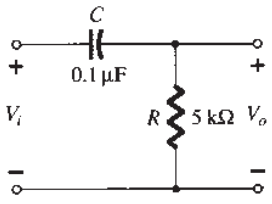


Figure 11.13 Example 11.8

For the network of Fig. 11.13:

(a) Determine the break frequency.

(b) Sketch the asymptotes and locate the −3-dB point.

(c) Sketch the frequency response curve.

Solution

(a) $$f_1 = \frac{1}{2\pi RC} = \frac{1}{(6.28)(5 \times 10^3\ \Omega)(0.1 \times 10^{-6}\ \text{F})}$$

$$\cong \mathbf{318.5\ Hz}$$

(b) and (c). See Fig. 11.14.

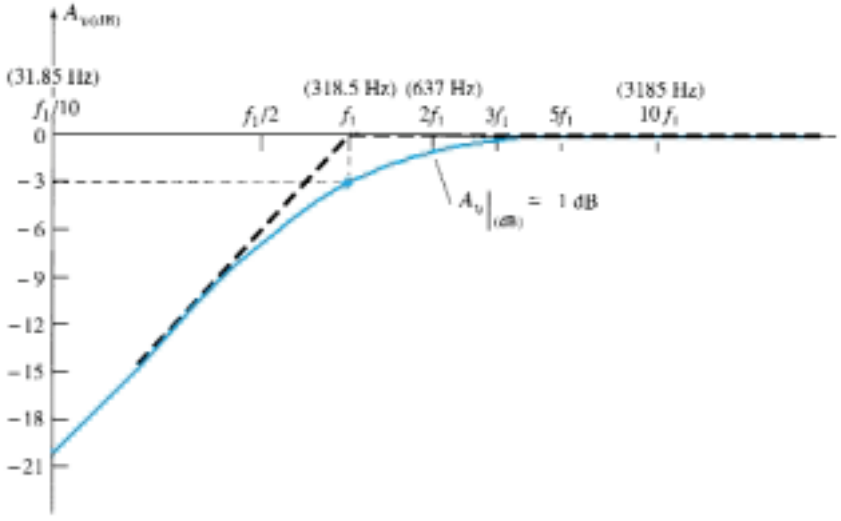


Figure 11.14 Frequency response for the *R-C* circuit of Figure 11.13.

The gain at any frequency can then be determined from the frequency plot in the following manner:

$$A_{v(\text{dB})} = 20 \log_{10} \frac{V_o}{V_i}$$

but

$$\frac{A_{v(\text{dB})}}{20} = \log_{10} \frac{V_o}{V_i}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = 10^{\left(\frac{A_{v(\text{dB})}}{20}\right)}} \tag{11.24}$$

For example, if $A_{v(\text{dB})} = -3$ dB,

$$A_v = \frac{V_o}{V_i} = 10^{(-3/20)} = 10^{(-0.15)} \cong 0.707 \qquad \text{as expected}$$

The quantity $10^{-0.15}$ is determined using the 10^x function found on most scientific calculators.

From Fig. 11.14, $A_{v(\text{dB})} \cong -1$ dB at $f = 2f_1 = 637$ Hz. The gain at this point is

$$A_v = \frac{V_o}{V_i} = 10^{\left(\frac{A_{v(\text{dB})}}{20}\right)} = 10^{(-1/20)} = 10^{(-0.05)} = 0.891$$

and

$$V_o = 0.891 V_i$$

or V_o is 89.1% of V_i at $f = 637$ Hz.

The phase angle of θ is determined from

$$\boxed{\theta = \tan^{-1} \frac{f_1}{f}} \tag{11.25}$$

from Eq. (11.22).

For frequencies $f \ll f_1$,

$$\theta = \tan^{-1} \frac{f_1}{f} \rightarrow 90°$$

For instance, if $f_1 = 100f$,

$$\theta = \tan^{-1} \frac{f_1}{f} = \tan^{-1}(100) = 89.4°$$

For $f = f_1$,

$$\theta = \tan^{-1} \frac{f_1}{f} = \tan^{-1} 1 = 45°$$

For $f \gg f_1$,

$$\theta = \tan^{-1} \frac{f_1}{f} \rightarrow 0°$$

For instance, if $f = 100f_1$,

$$\theta = \tan^{-1} \frac{f_1}{f} = \tan^{-1} 0.01 = 0.573°$$

A plot of $\theta = \tan^{-1}(f_1/f)$ is provided in Fig. 11.15. If we add the additional 180° phase shift introduced by an amplifier, the phase plot of Fig. 11.7 will be obtained. The magnitude and phase response for an *R-C* combination have now been established. In Section 11.6, each capacitor of importance in the low-frequency region will be redrawn in an *R-C* format and the cutoff frequency for each determined to establish the low-frequency response for the BJT amplifier.

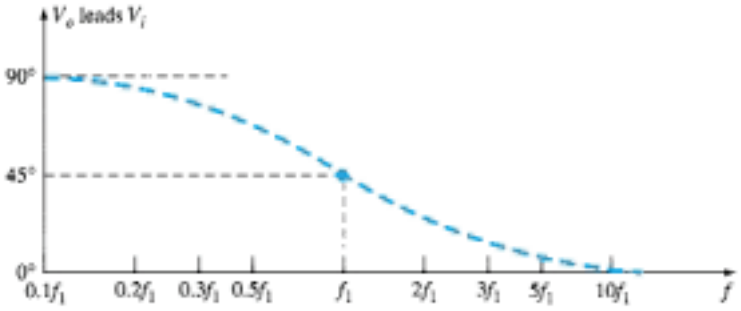


Figure 11.15 Phase response for the *R-C* circuit of Figure 11.8.

11.6 LOW-FREQUENCY RESPONSE — BJT AMPLIFIER

The analysis of this section will employ the loaded voltage-divider BJT bias configuration, but the results can be applied to any BJT configuration. It will simply be necessary to find the appropriate equivalent resistance for the *R-C* combination. For the network of Fig. 11.16, the capacitors C_s, C_C, and C_E will determine the low-frequency response. We will now examine the impact of each independently in the order listed.

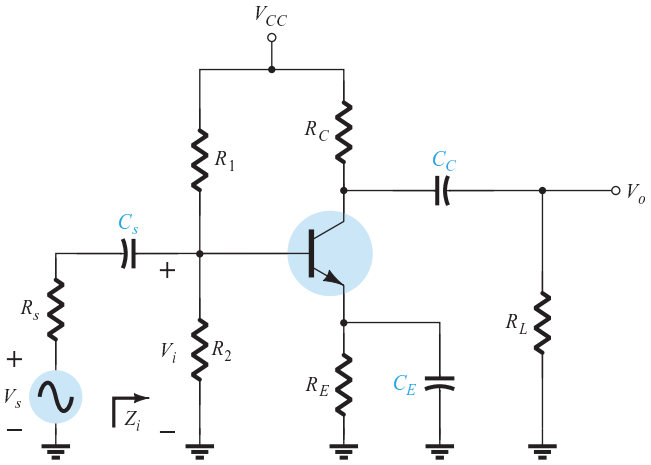


Figure 11.16 Loaded BJT amplifier with capacitors that affect the low-frequency response.

C_s

Since C_s is normally connected between the applied source and the active device, the general form of the *R-C* configuration is established by the network of Fig. 11.17. The total resistance is now $R_s + R_i$, and the cutoff frequency as established in Section 11.5 is

$$f_{L_s} = \frac{1}{2\pi\,(R_s + R_i)C_s} \tag{11.26}$$

At mid or high frequencies, the reactance of the capacitor will be sufficiently small to permit a short-circuit approximation for the element. The voltage V_i will then be related to V_s by

$$V_i\big|_{\text{mid}} = \frac{R_i V_s}{R_i + R_s} \tag{11.27}$$

At f_{L_s}, the voltage V_i will be 70.7% of the value determined by Eq. (11.27), assuming that C_s is the only capacitive element controlling the low-frequency response.

For the network of Fig. 11.16, when we analyze the effects of C_s we must make the assumption that C_E and C_C are performing their designed function or the analysis becomes too unwieldy, that is, that the magnitude of the reactances of C_E and C_C permits employing a short-circuit equivalent in comparison to the magnitude of the other series impedances. Using this hypothesis, the ac equivalent network for the input section of Fig. 11.16 will appear as shown in Fig. 11.18.

The value of R_i for Eq. (11.26) is determined by

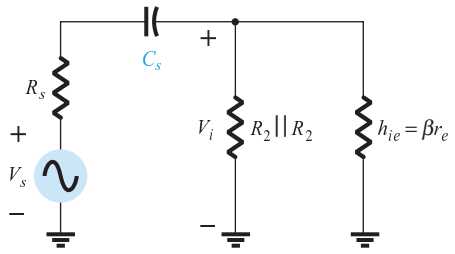


Figure 11.18 Localized ac equivalent for C_s.

$$R_i = R_1 \| R_2 \| \beta r_e \tag{11.28}$$

The voltage $\mathbf{V}_i$ applied to the input of the active device can be calculated using the voltage-divider rule:

$$\mathbf{V}_i = \frac{R_i \mathbf{V}_s}{R_s + R_i - jX_{C_s}} \tag{11.29}$$

C_C

Since the coupling capacitor is normally connected between the output of the active device and the applied load, the R-C configuration that determines the low cutoff frequency due to C_C appears in Fig. 11.19. From Fig. 11.19, the total series resistance is now $R_o + R_L$ and the cutoff frequency due to C_C is determined by

$$f_{L_C} = \frac{1}{2\pi\,(R_o + R_L)C_C} \tag{11.30}$$

Ignoring the effects of C_s and C_E, the output voltage V_o will be 70.7% of its midband value at f_{L_C}. For the network of Fig. 11.16, the ac equivalent network for the output section with $V_i = 0$ V appears in Fig. 11.20. The resulting value for R_o in Eq. (11.30) is then simply

$$R_o = R_C \| r_o \tag{11.31}$$

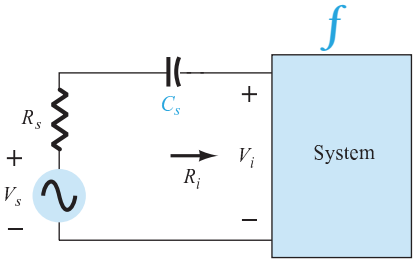


Figure 11.17 Determining the effect of C_s on the low frequency response.

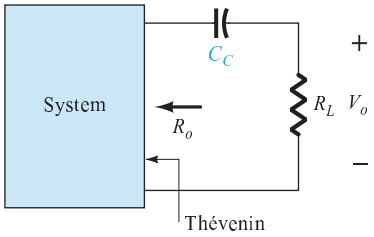


Figure 11.19 Determining the effect of C_C on the low-frequency response.

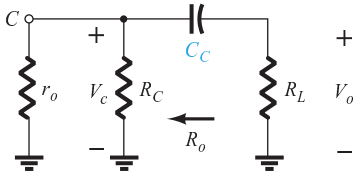


Figure 11.20 Localized ac equivalent for C_C with $V_i = 0$ V.

f

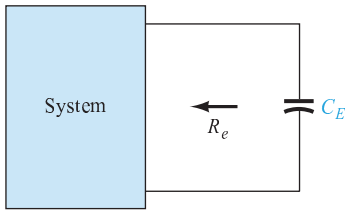


Figure 11.21 Determining the effect of C_E on the low-frequency response.

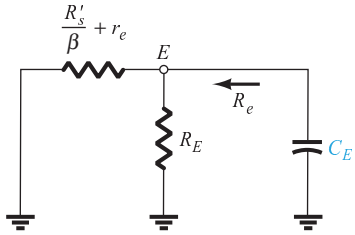


Figure 11.22 Localized ac equivalent of C_E.

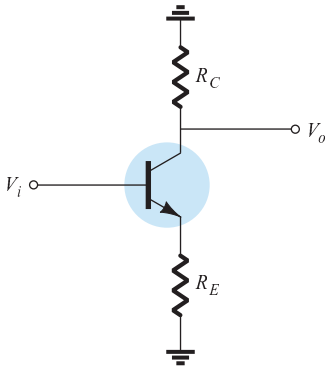


Figure 11.23 Network employed to describe the effect of C_E on the amplifier gain.

C_E

To determine f_{L_E}, the network "seen" by C_E must be determined as shown in Fig. 11.21. Once the level of R_e is established, the cutoff frequency due to C_E can be determined using the following equation:

$$f_{L_E} = \frac{1}{2\pi R_e C_E} \tag{11.32}$$

For the network of Fig. 11.16, the ac equivalent as "seen" by C_E appears in Fig. 11.22. The value of R_e is therefore determined by

$$R_e = R_E \| \left(\frac{R'_s}{\beta} + r_e \right) \tag{11.33}$$

where $R'_s = R_s \| R_1 \| R_2$.

The effect of C_E on the gain is best described in a quantitative manner by recalling that the gain for the configuration of Fig. 11.23 is given by

$$A_v = \frac{-R_C}{r_e + R_E}$$

The maximum gain is obviously available where R_E is zero ohms. At low frequencies, with the bypass capacitor C_E in its "open-circuit" equivalent state, all of R_E appears in the gain equation above, resulting in the minimum gain. As the frequency increases, the reactance of the capacitor C_E will decrease, reducing the parallel impedance of R_E and C_E until the resistor R_E is effectively "shorted out" by C_E. The result is a maximum or midband gain determined by $A_v = -R_C/r_e$. At f_{L_E} the gain will be 3 dB below the midband value determined with R_E "shorted out."

Before continuing, keep in mind that C_s, C_C, and C_E will affect only the low-frequency response. At the midband frequency level, the short-circuit equivalents for the capacitors can be inserted. Although each will affect the gain $A_v = V_o/V_i$ in a similar frequency range, the highest low-frequency cutoff determined by C_s, C_C, or C_E will have the greatest impact since it will be the last encountered before the midband level. If the frequencies are relatively far apart, the highest cutoff frequency will essentially determine the lower cutoff frequency for the entire system. If there are two or more "high" cutoff frequencies, the effect will be to raise the lower cutoff frequency and reduce the resulting bandwidth of the system. In other words, there is an interaction between capacitive elements that can affect the resulting low cutoff frequency. However, if the cutoff frequencies established by each capacitor are sufficiently separated, the effect of one on the other can be ignored with a high degree of accuracy—a fact that will be demonstrated by the printouts to appear in the following example.

EXAMPLE 11.9

(a) Determine the lower cutoff frequency for the network of Fig. 11.16 using the following parameters:

$C_s = 10\ \mu\text{F}$, $C_E = 20\ \mu\text{F}$, $C_C = 1\ \mu\text{F}$

$R_s = 1\ \text{k}\Omega$, $R_1 = 40\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_E = 2\ \text{k}\Omega$, $R_C = 4\ \text{k}\Omega$, $R_L = 2.2\ \text{k}\Omega$

$\beta = 100$, $r_o = \infty\ \Omega$, $V_{CC} = 20\ \text{V}$

(b) Sketch the frequency response using a Bode plot.

Solution

(a) Determining r_e for dc conditions:

$$\beta R_E = (100)(2\ \text{k}\Omega) = 200\ \text{k}\Omega \gg 10R_2 = 100\ \text{k}\Omega$$

The result is:

$$V_B \cong \frac{R_2 V_{CC}}{R_2 + R_1} = \frac{10\ \text{k}\Omega(20\ \text{V})}{10\ \text{k}\Omega + 40\ \text{k}\Omega} = \frac{200\ \text{V}}{50} = 4\ \text{V}$$

with

$$I_E = \frac{V_E}{R_E} = \frac{4\ \text{V} - 0.7\ \text{V}}{2\ \text{k}\Omega} = \frac{3.3\ \text{V}}{2\ \text{k}\Omega} = 1.65\ \text{mA}$$

so that

$$r_e = \frac{26\ \text{mV}}{1.65\ \text{mA}} \cong \mathbf{15.76\ \Omega}$$

and

$$\beta r_e = 100(15.76\ \Omega) = 1576\ \Omega = \mathbf{1.576\ k\Omega}$$

Midband Gain

$$A_v = \frac{V_o}{V_i} = \frac{-R_C \| R_L}{r_e} = -\frac{(4\ \text{k}\Omega)\|(2.2\ \text{k}\Omega)}{15.76\ \Omega} \cong -90$$

The input impedance

$$\begin{aligned} Z_i = R_i &= R_1 \| R_2 \| \beta r_e \\ &= 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \\ &\cong 1.32\ \text{k}\Omega \end{aligned}$$

and from Fig. 11.24,

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

or

$$\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s} = \frac{1.32\ \text{k}\Omega}{1.32\ \text{k}\Omega + 1\ \text{k}\Omega} = 0.569$$

so that

$$\begin{aligned} A_{v_s} = \frac{V_o}{V_s} &= \frac{V_o}{V_i}\frac{V_i}{V_s} = (-90)(0.569) \\ &= \mathbf{-51.21} \end{aligned}$$

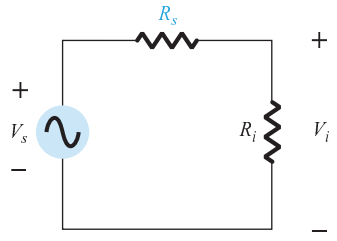


Figure 11.24 Determining the effect of R_s on the gain A_{v_s}.

C_s

$$R_i = R_1 \| R_2 \| \beta r_e = 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.576\ \text{k}\Omega \cong 1.32\ \text{k}\Omega$$

$$f_{L_S} = \frac{1}{2\pi(R_s + R_i)C_s} = \frac{1}{(6.28)(1\ \text{k}\Omega + 1.32\ \text{k}\Omega)(10\ \mu\text{F})}$$

$$f_{L_S} \cong \mathbf{6.86\ Hz}$$

f

The results just obtained will now be verified using PSpice Windows. The network with its various capacitors appears in Fig. 11.25. The **Model Editor** was used to set I_s to 2E-15A and beta to 100. The remaining parameters were removed from the listing to idealize the response to the degree possible. Under **Analysis Setup-AC Sweep,** the frequency was set to 10 kHz to establish a frequency in the midband region. A simulation of the network resulted in the dc levels of Fig. 11.25. Note that V_B is 3.9 V versus the calculated level of 4 V and that V_E is 3.2 V versus the calculated level of 3.3 V. Very close when you consider that the approximate model was used. V_{BE} is very close to the 0.7 V at 0.71 V. The output file reveals that the ac voltage across the load at a frequency of 10 kHz is 49.67 mV, resulting in a gain of 49.67, which is very close to the calculated level of 51.21.

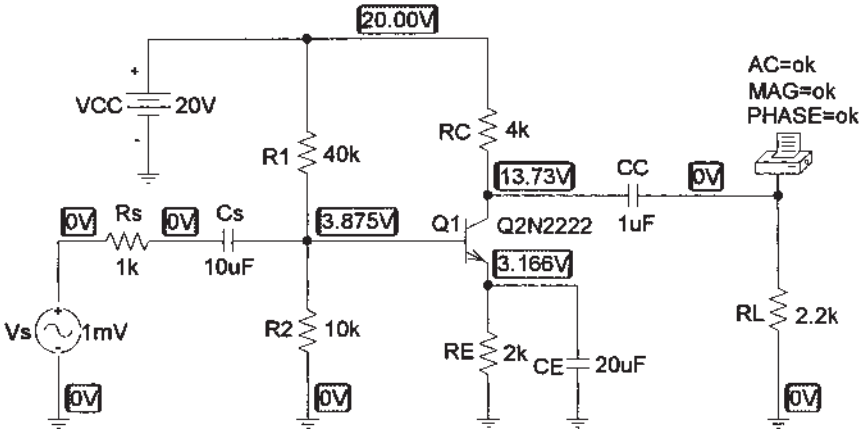


Figure 11.25 Network of Figure 11.16 with assigned values.

A plot of the gain versus frequency will now be obtained with only C_S as a determining factor. The other capacitors, C_C and C_E, will be set to very high values so they are essentially short circuits at any of the frequencies of interest. Setting C_C and C_E to 1 F will remove any affect they will have on the response on the low-frequency region. Here, one must be careful as the program does not recognize 1F as one Farad. It must be entered as 1E6uF. Since the pattern desired is gain versus frequency, we must use the sequence **Analysis-Setup-Analysis Setup-Enable AC Sweep-AC Sweep** to obtain the **AC Sweep and Noise Analysis** dialog box. Since our interest will be in the low-frequency range, we will choose a range of 1 Hz (0 Hz is an invalid entry) to 100 Hz. If you want a frequency range starting close to 0 Hz, you would have to choose a frequency such as 0.001 Hz or something small enough not to be noticeable on the plot. The **Total Pts.:** will be set at 1000 for a good continuous plot, the **Start Freq.:** at 1 Hz, and the **End Freq.:** at 100 Hz. The **AC Sweep Type** will be left on **Linear.** A simulation followed by **Trace-Add-V(RL:1)** will result in the desired plot. However, the computer has selected a log scale for the horizontal axis that extends from 1 Hz to 1 kHz even though we requested a linear scale. If we choose **Plot-X-Axis Settings-Linear-OK,** we will get a linear plot to 120 Hz, but the curve of interest is all in the low end—the log axis obviously provided a better plot for our region of interest. Returning to **Plot-X-Axis Settings** and choosing **Log,** we return to the original plot. Our interest only lies in the region of 1 to 100 Hz, so the remaining frequencies to 1 kHz should be removed with **Plot-X-Axis Settings-User Defined-1Hz to 100Hz-OK.** The vertical axis also goes to 60 mV, and we want to limit to 50 mV for this frequency range. This is accomplished with **Plot-Y-Axis Settings-User Defined-0V to 50mV-OK,** after which the pattern of Fig. 11.26 will be obtained.

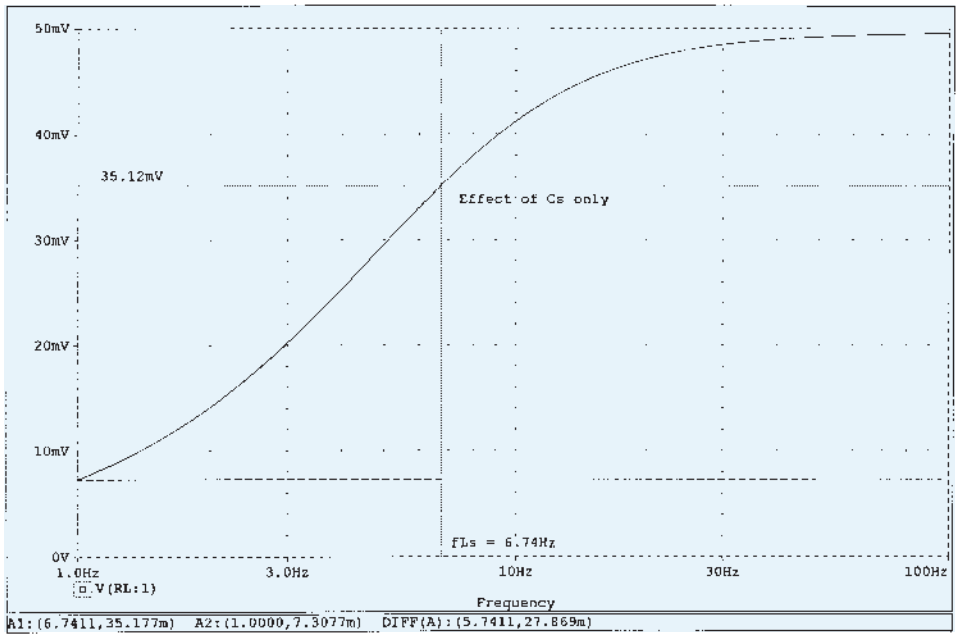


Figure 11.26 Low-frequency response due to C_S.

Note how closely the curve approaches 50 mV in this range. The cutoff level is determined by 0.707(49.67 mV) = 35.12 mV, which can be found by clicking the **Toggle cursor** icon and moving the intersection up the graph until the 35.177-mV level is reached for **A1.** At this point, the frequency of the horizontal axis can be read as 6.74 Hz, comparing very well to the predicted value of 6.86 Hz. Note that **A2** remains at the lowest level of the plot, at 1 Hz.

C_C

$$f_{L_C} = \frac{1}{2\pi(R_C + R_L)C_C}$$

$$= \frac{1}{(6.28)(4\ \text{k}\Omega + 2.2\ \text{k}\Omega)(1\ \mu\text{F})}$$

$$\cong \mathbf{25.68\ Hz}$$

To investigate the effects of C_C on the lower cutoff frequency, both C_S and C_E must be set to 1 Farad as described above. Following the procedure outlined above will result in the plot of Fig. 11.27, with a cutoff frequency of 25.58 Hz, providing a close match with the calculated level of 25.68 Hz.

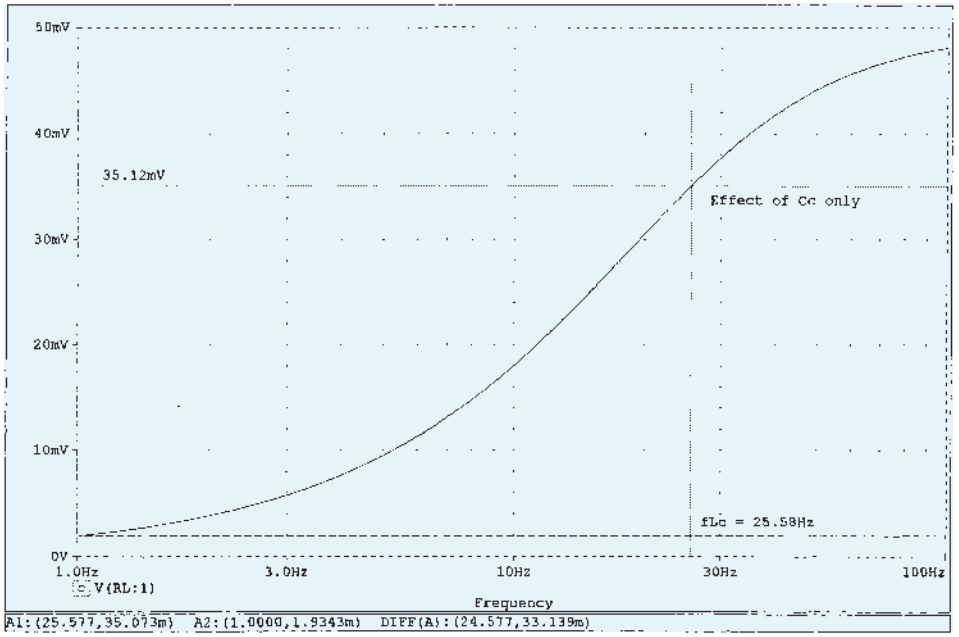


Figure 11.27 Low-frequency response due to C_C.

C_E

$$R_s' = R_s \| R_1 \| R_2 = 1\ \text{k}\Omega \| 40\ \text{k}\Omega \| 10\ \text{k}\Omega \cong 0.889\ \text{k}\Omega$$

$$R_e = R_E \left\| \left(\frac{R'_s}{\beta} + r_e \right) = 2\ \text{k}\Omega \right\| \left(\frac{0.889\ \text{k}\Omega}{100} + 15.76\ \Omega \right)$$

$$= 2\ \text{k}\Omega \| (8.89\ \Omega + 15.76\ \Omega) = 2\ \text{k}\Omega \| 24.65\ \Omega \cong 24.35\ \Omega$$

$$f_{L_E} = \frac{1}{2\pi R_e C_E} = \frac{1}{(6.28)(24.35\ \Omega)(20\ \mu\text{F})} = \frac{10^6}{3058.36} \cong \mathbf{327\ Hz}$$

The effect of C_E can be examined using PSpice Windows by setting both C_S and C_C to 1 Farad. In addition, since the frequency range is greater, the start frequency has to be changed to 10 Hz and the final frequency to 1 kHz. The result is the plot of Fig. 11.28, with a cutoff frequency of 321.17 Hz, providing a close match with the calculated value of 327 Hz.

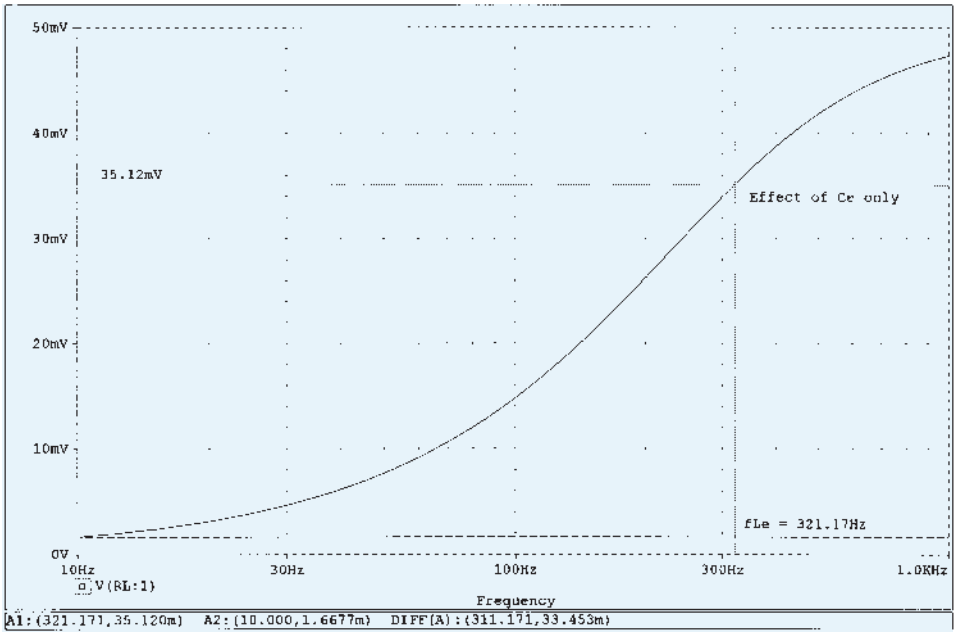


Figure 11.28 Low-frequency response due to C_E.

The fact that f_{L_E} is significantly higher than f_{L_S} or f_{L_C} suggests that it will be the predominant factor in determining the low-frequency response for the complete system. To test the accuracy of our hypothesis, the network is simulated with all the initial values of capacitance level to obtain the results of Fig. 11.29. Note the strong similarity with the waveform of Fig. 11.28, with the only visible difference being the higher gain at lower frequencies on Fig. 11.28. Without question, the plot supports the fact that the highest of the low cutoff frequencies will have the most impact on the low cutoff frequency for the system.

(b) It was mentioned earlier that dB plots are usually normalized by dividing the voltage gain A_v by the magnitude of the midband gain. For Fig. 11.16, the magnitude of the midband gain is 51.21, and naturally the ratio $|A_v/A_{v_{\text{mid}}}|$ will be 1 in the midband region. The result is a 0-dB asymptote in the midband region as shown in Fig. 11.30. Defining f_{L_E} as our lower cutoff frequency f_1, an asymptote at -6 dB/octave can be drawn as shown in Fig. 11.30 to form the Bode plot and our

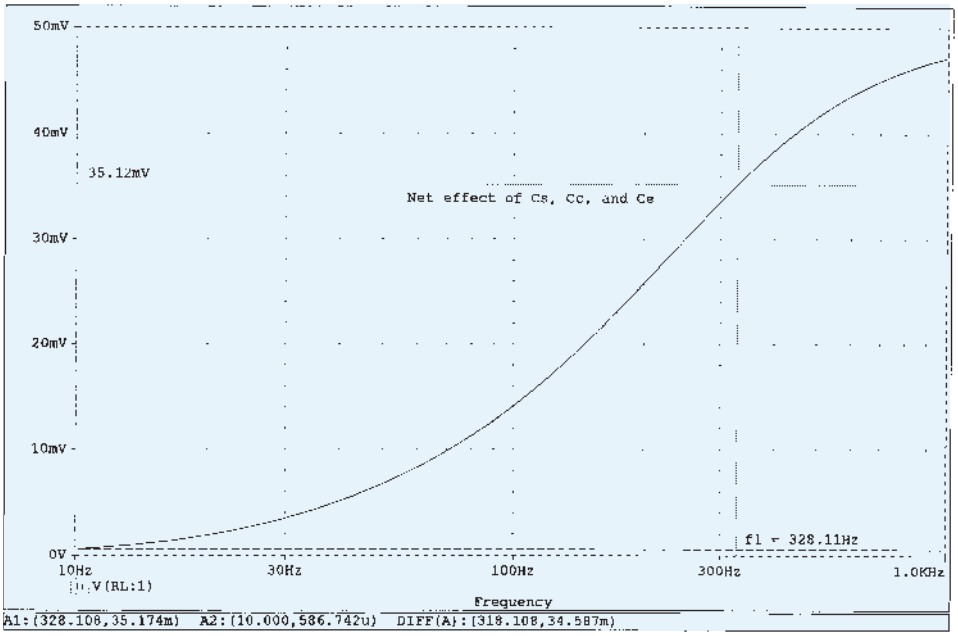


Figure 11.29 Low-frequency response due to C_S, C_E, and C_C.

envelope for the actual response. At f_1, the actual curve is -3 dB down from the midband level as defined by the $0.707A_{V_{\text{mid}}}$ level, permitting a sketch of the actual frequency response curve as shown in Fig. 11.30. A -6-dB/octave asymptote was drawn at each frequency defined in the analysis above to demonstrate clearly that it is f_{L_E} for this network that will determine the -3-dB point. It is not until about -24 dB that f_{L_C} begins to affect the shape of the envelope. The magnitude plot shows that the slope of the resultant asymptote is the sum of the asymptotes having the same sloping direction in the same frequency interval. Note in Fig. 11.30 that the slope has dropped to -12 dB/octave for frequencies less

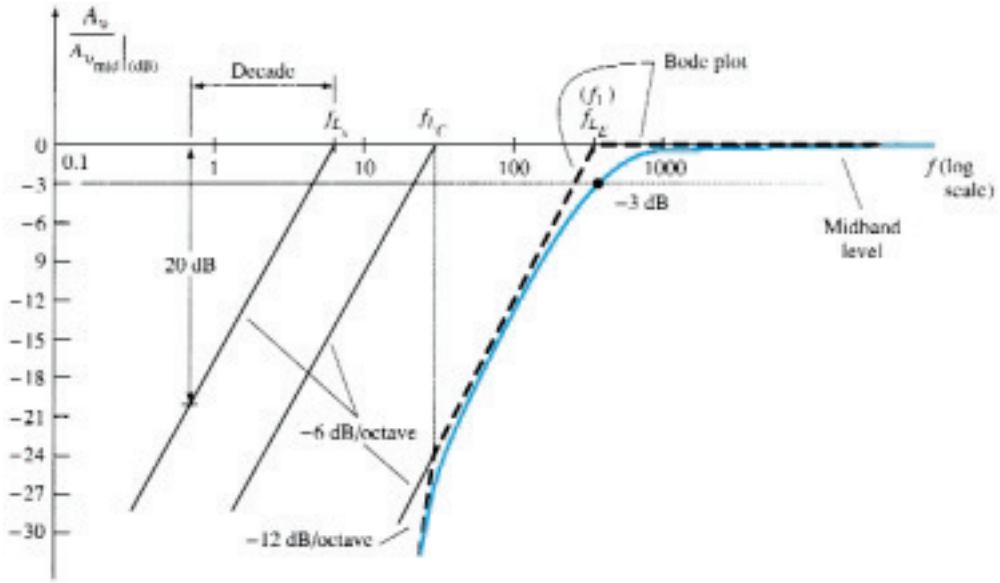


Figure 11.30 Low-frequency plot for the network of Example 11.9.

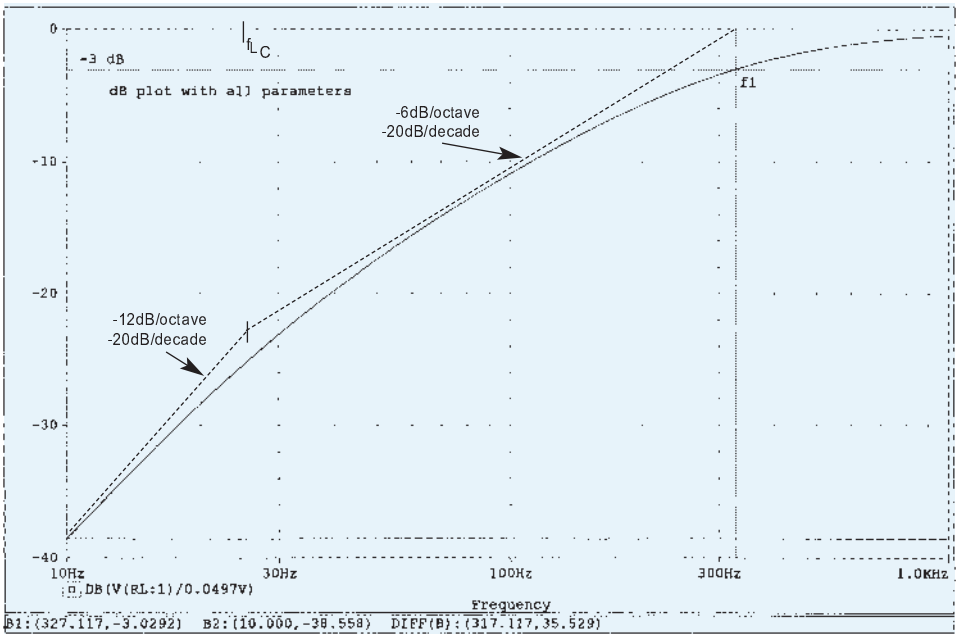


Figure 11.31 dB plot of the low-frequency response of the BJT amplifier of Fig. 11.25.

than f_{L_C} and could drop to -18 dB/octave if the three defined cutoff frequencies of Fig. 11.30 were closer together.

Using **PROBE,** a plot of $20 \log_{10}|A_v/A_{v_{mid}}| = A_v/A_{v_{mid}}|_{dB}$ can be obtained by recalling that if $V_s = 1$ mV, the magnitude of $|A_v/A_{v_{mid}}|$ is the same as $|V_o/A_{v_{mid}}|$ since V_o will have the same numerical value as A_v. The required **Trace Expression,** which is entered on the bottom of the **Add Traces** dialog box, appears on the horizontal axis of Fig. 11.31. The plot clearly reveals the change in slope of the asymptote at f_{L_C} and how the actual curve follows the envelope created by the Bode plot. In addition, note the 3-dB drop at f_1.

Keep in mind as we proceed to the next section that the analysis of this section is not limited to the network of Fig. 11.16. For any transistor configuration it is simply necessary to isolate each *R-C* combination formed by a capacitive element and determine the break frequencies. The resulting frequencies will then determine whether there is a strong interaction between capacitive elements in determining the overall response and which element will have the greatest impact on establishing the lower cutoff frequency. In fact, the analysis of the next section will parallel this section as we determine the low cutoff frequencies for the FET amplifier.

11.7 LOW-FREQUENCY RESPONSE — FET AMPLIFIER

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier of Section 11.6. There are again three capacitors of primary concern as appearing in the network of Fig. 11.32: C_G, C_C, and C_S. Although Fig. 11.32 will be used to establish the fundamental equations, the procedure and conclusions can be applied to most FET configurations.

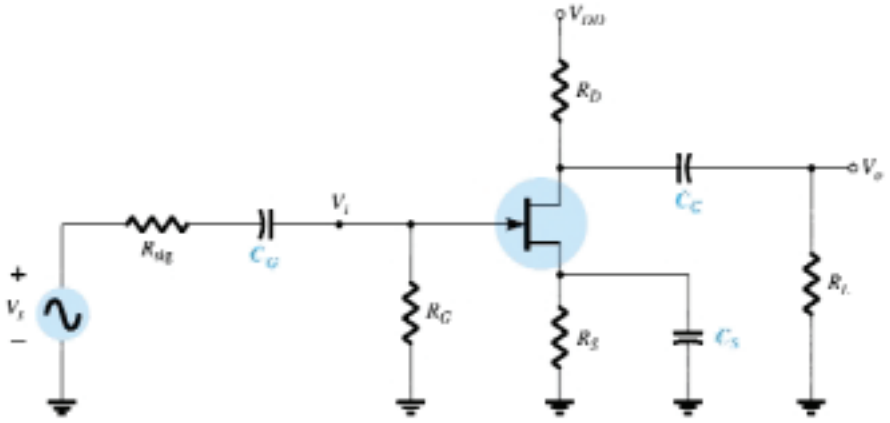


Figure 11.32 Capacitive elements that affect the low-frequency response of a JFET amplifier.

C_G

For the coupling capacitor between the source and the active device, the ac equivalent network will appear as shown in Fig. 11.33. The cutoff frequency determined by C_G will then be

$$f_{L_G} = \frac{1}{2\pi(R_{\text{sig}} + R_i)C_G} \tag{11.34}$$

which is an exact match of Eq. (11.26). For the network of Fig. 11.32,

$$R_i = R_G \tag{11.35}$$

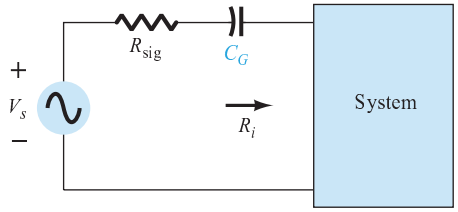


Figure 11.33 Determining the effect of C_G on the low-frequency response.

Typically, $R_G \gg R_{\text{sig}}$, and the lower cutoff frequency will be determined primarily by R_G and C_G. The fact that R_G is so large permits a relatively low level of C_G while maintaining a low cutoff frequency level for f_{L_G}.

C_C

For the coupling capacitor between the active device and the load the network of Fig. 11.34 will result, which is also an exact match of Fig. 11.19. The resulting cutoff frequency is

$$f_{L_C} = \frac{1}{2\pi(R_o + R_L)C_C} \tag{11.36}$$

For the network of Fig. 11.32,

$$R_o = R_D \| r_d \tag{11.37}$$

f

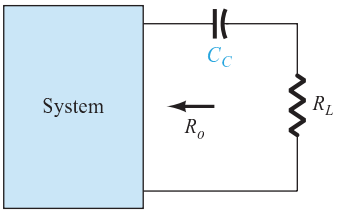


Figure 11.34 Determining the effect of C_C on the low-frequency response.

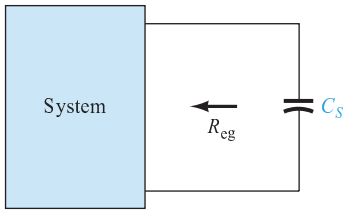


Figure 11.35 Determining the effect of C_S on the low-frequency response.

C_S

For the source capacitor C_S, the resistance level of importance is defined by Fig. 11.35. The cutoff frequency will be defined by

$$f_{L_S} = \frac{1}{2\pi R_{\text{eq}} C_S} \tag{11.38}$$

For Fig. 11.32, the resulting value of R_{eq}:

$$R_{\text{eq}} = \frac{R_S}{1 + R_S(1 + g_m r_d)/(r_d + R_D \| R_L)} \tag{11.39}$$

which for $r_d \cong \infty\ \Omega$ becomes

$$R_{\text{eq}} = R_S \| \frac{1}{g_m} \tag{11.40}$$

EXAMPLE 11.10

(a) Determine the lower cutoff frequency for the network of Fig. 11.32 using the following parameters:

$C_G = 0.01\ \mu\text{F}$, $C_C = 0.5\ \mu\text{F}$, $C_S = 2\ \mu\text{F}$

$R_{\text{sig}} = 10\ \text{k}\Omega$, $R_G = 1\ \text{M}\Omega$, $R_D = 4.7\ \text{k}\Omega$, $R_S = 1\ \text{k}\Omega$, $R_L = 2.2\ \text{k}\Omega$

$I_{DSS} = 8\text{mA}$, $V_P = -4\ \text{V}$ $r_d = \infty\ \Omega$, $\text{V}_{\text{DD}} = 20\ \text{V}$

(b) Sketch the frequency response using a Bode plot.

Solution

(a) DC Analysis: Plotting the transfer curve of $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$ and superimposing the curve defined by $V_{GS} = -I_D R_S$ will result in an intersection at $V_{GS_Q} = -2$ V and $I_{D_Q} = 2$ mA. In addition,

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\ \text{mA})}{4\ \text{V}} = 4\ \text{mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\ \text{mS}\left(1 - \frac{-2\ \text{V}}{-4\ \text{V}}\right) = 2\ \text{mS}$$

C_G

$$\text{Eq. (11.34)}: \quad f_{L_G} = \frac{1}{2\pi\,(10\ \text{k}\Omega + 1\ \text{M}\Omega)(0.01\ \mu\text{F})} \cong \mathbf{15.8\ Hz}$$

C_C

$$\text{Eq. (11.36):} \quad f_{L_C} = \frac{1}{2\pi\,(4.7\ \text{k}\Omega + 2.2\ \text{k}\Omega)(0.5\ \mu\text{F})} \cong \mathbf{46.13\ Hz}$$

C_S

$$R_{\text{eq}} = R_S \| \frac{1}{g_m} = 1\ \text{k}\Omega \| \frac{1}{2\ \text{mS}} = 1\ \text{k}\Omega \| 0.5\ \text{k}\Omega = 333.33\ \Omega$$

$$\text{Eq. (11.38):} \quad f_{L_S} = \frac{1}{2\pi\,(333.33\ \Omega)(2\ \mu\text{F})} = \mathbf{238.73\ Hz}$$

Since f_{L_S} is the largest of the three cutoff frequencies, it defines the low cutoff frequency for the network of Fig. 11.32.

(b) The midband gain of the system is determined by

$$A_{v_{\text{mid}}} = \frac{V_o}{V_i} = -g_m(R_D \| R_L) = -(2\ \text{mS})(4.7\ \text{k}\Omega \| 2.2\ \text{k}\Omega)$$
$$= -(2\ \text{mS})(1.499\ \text{k}\Omega)$$
$$\cong \mathbf{-3}$$

Using the midband gain to normalize the response for the network of Fig. 11.32 will result in the frequency plot of Fig. 11.36.

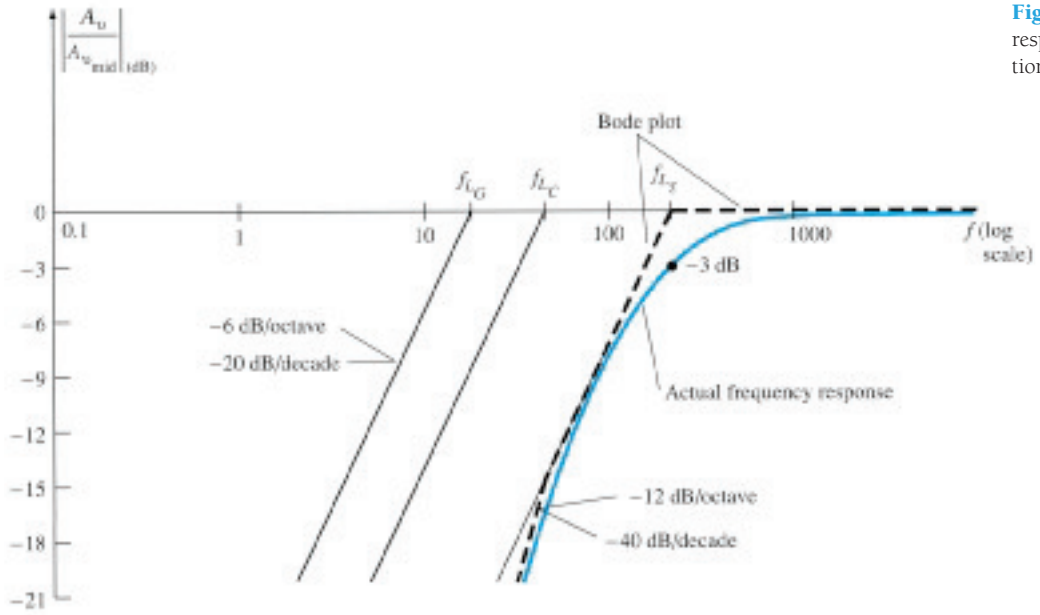


Figure 11.36 Low-frequency response for the JFET configuration of Example 11.10.

Using PSpice Windows, the network will appear as shown in Fig. 11.37, with the JFET parameters **Beta** set at 0.5mA/V^2 and **Vto** at −4 V (all others set to zero) and the frequency of interest at a midband value of 10 kHz. The resulting dc levels confirm that V_{GS} is −2 V and place V_D at 10.60 V, which should be right in the middle of the linear active region since $V_{GS} = 1/2(V_D = -4\ \text{V})$ and $V_{DS} = 1/2(V_{DD} = 20\ \text{V})$. The 0-V levels clearly reveal that the capacitors have isolated the transistor for the dc biasing. The ac response results in an ac level of 2.993 mV across the load for a gain of 2.993, which is essentially equal to the calculated gain of 3.

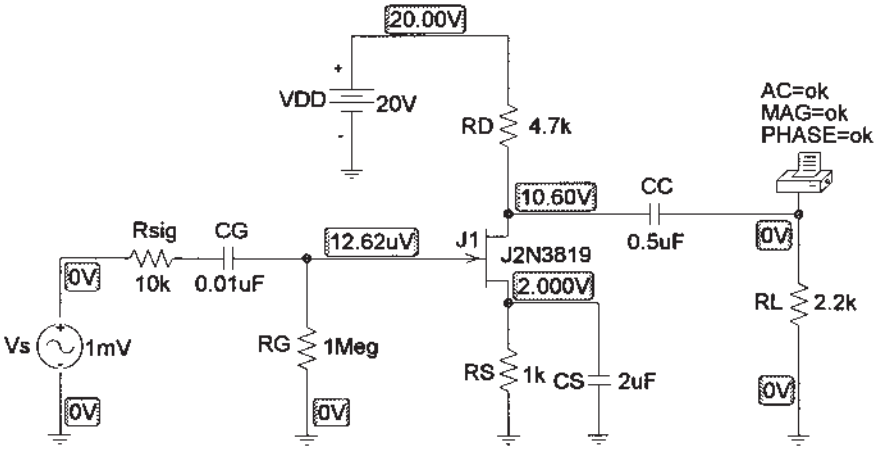


Figure 11.37 Schematic network for Example 11.10.

Returning to **Analysis** and choosing **Automatically run Probe after simulation** followed by **Setup-AC Sweep-Decade-Pts/Decade** = 1000, **Start Freq.:** 10Hz, and **End Freq.:** 10 kHz will setup **Simulation-Trace-Add-Trace Expression: DB (V(RL:1)/2.993mV)-OK,** which will result in the plot of Fig. 11.38, with a low cut-off frequency of 227.5 Hz primarily determined by the source capacitance.

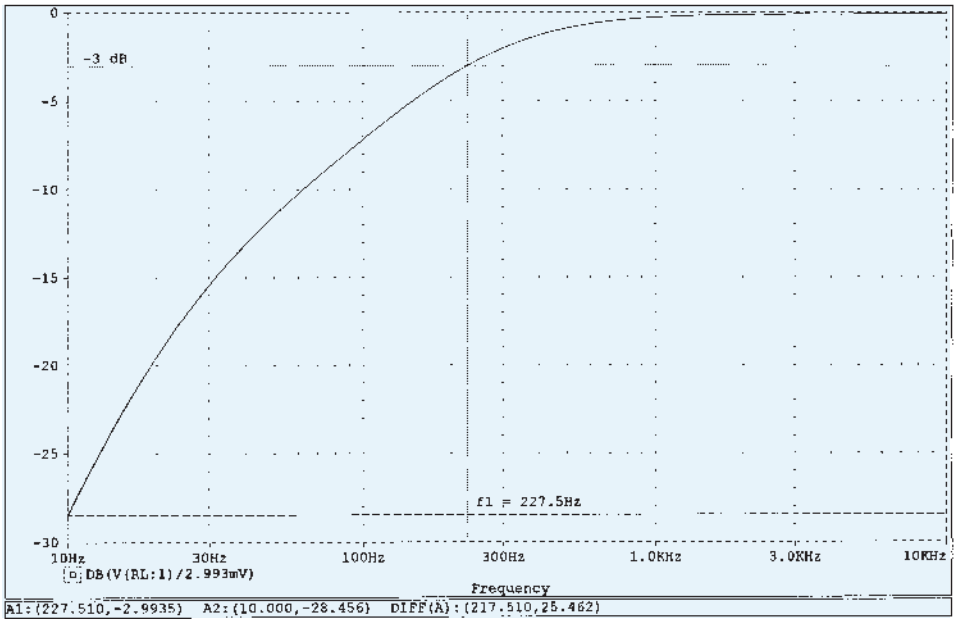


Figure 11.38 dB response for the low-frequency region in the network of Example 11.10.

11.8 MILLER EFFECT CAPACITANCE

In the high-frequency region, the capacitive elements of importance are the inter-electrode (between terminals) capacitances internal to the active device and the wiring capacitance between leads of the network. The large capacitors of the network that controlled the low-frequency response have all been replaced by their short-circuit equivalent due to their very low reactance levels.

For *inverting* amplifiers (phase shift of 180° between input and output resulting in a negative value for A_v), the input and output capacitance is increased by a capacitance level sensitive to the interelectrode capacitance between the input and output terminals of the device and the gain of the amplifier. In Fig. 11.39, this "feedback" capacitance is defined by C_f.

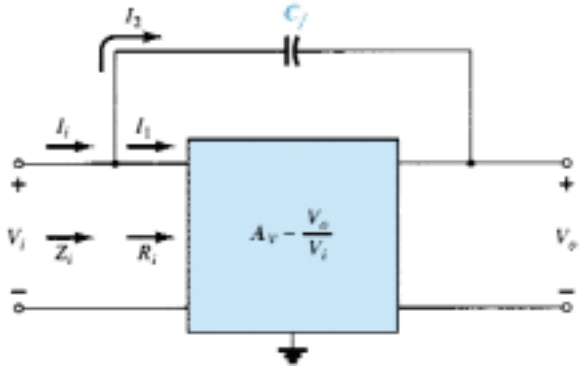


Figure 11.39 Network employed in the derivation of an equation for the Miller input capacitance.

Applying Kirchhoff's current law gives

$$I_i = I_1 + I_2$$

Using Ohm's law yields

$$I_i = \frac{V_i}{Z_i}, \qquad I_1 = \frac{V_i}{R_i}$$

and

$$I_2 = \frac{V_i - V_o}{X_{C_f}} = \frac{V_i - A_v V_i}{X_{C_f}} = \frac{(1 - A_v)V_i}{X_{C_f}}$$

Substituting, we obtain

$$\frac{V_i}{Z_i} = \frac{V_i}{R_i} + \frac{(1 - A_v)V_i}{X_{C_f}}$$

and

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_f}/(1 - A_v)}$$

but

$$\frac{X_{C_f}}{1 - A_v} = \underbrace{\frac{1}{\omega\,(1 - A_v)C_f}}_{C_M} = X_{CM}$$

and

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_M}}$$

establishing the equivalent network of Fig. 11.40. The result is an equivalent input impedance to the amplifier of Fig. 11.39 that includes the same R_i that we have dealt with in previous chapters, with the addition of a feedback capacitor magnified by the

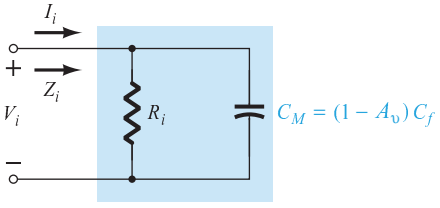


Figure 11.40 Demonstrating the impact of the Miller effect capacitance.

gain of the amplifier. Any interelectrode capacitance at the input terminals to the amplifier will simply be added in parallel with the elements of Fig. 11.40.

In general, therefore, the Miller effect input capacitance is defined by

$$C_{M_i} = (1 - A_v)C_f \tag{11.41}$$

This shows us that:

For any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode capacitance connected between the input and output terminals of the active device.

The dilemma of an equation such as Eq. (11.41) is that at high frequencies the gain A_v will be a function of the level of C_{M_i}. However, since the maximum gain is the midband value, using the midband value will result in the highest level of C_{M_i} and the worst-case scenario. In general, therefore, the midband value is typically employed for A_v in Eq. (11.41).

The reason for the constraint that the amplifier be of the inverting variety is now more apparent when one examines Eq. (11.41). A positive value for A_v would result in a negative capacitance (for $A_v > 1$).

The Miller effect will also increase the level of output capacitance, which must also be considered when the high-frequency cutoff is determined. In Fig. 11.41, the parameters of importance to determine the output Miller effect are in place. Applying Kirchhoff's current law will result in

$$I_o = I_1 + I_2$$

with $$I_1 = \frac{V_o}{R_o} \quad \text{and} \quad I_2 = \frac{V_o - V_i}{X_{C_f}}$$

The resistance R_o is usually sufficiently large to permit ignoring the first term of the equation compared to the second term and assuming that

$$I_o \cong \frac{V_o - V_i}{X_{C_f}}$$

Substituting $V_i = V_o/A_v$ from $A_v = V_o/V_i$ will result in

$$I_o = \frac{V_o - V_o/A_v}{X_{C_f}} = \frac{V_o(1 - 1/A_v)}{X_{C_f}}$$

and

$$\frac{I_o}{V_o} = \frac{1 - 1/A_v}{X_{C_f}}$$

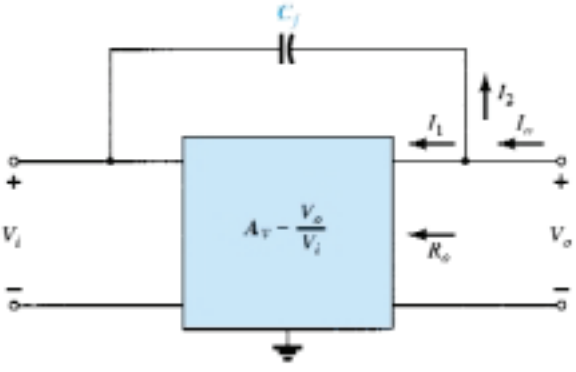


Figure 11.41 Network employed in the derivation of an equation for the Miller output capacitance.

or
$$\frac{V_o}{I_o} = \frac{X_{C_f}}{1 - 1/A_v} = \frac{1}{\omega C_f (1 - 1/A_v)} = \frac{1}{\omega C_{M_o}}$$

resulting in the following equation for the Miller output capacitance:

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right) C_f \tag{11.42a}$$

For the usual situation where $A_v \gg 1$, Eq. (11.42a) reduces to

$$C_{M_o} \cong C_f \quad |A_v| \gg 1 \tag{11.42b}$$

Examples in the use of Eq. (11.42) will appear in the next two sections as we investigate the high-frequency responses of BJT and FET amplifiers.

11.9 HIGH-FREQUENCY RESPONSE — BJT AMPLIFIER

At the high-frequency end, there are two factors that will define the −3-dB point: the network capacitance (parasitic and introduced) and the frequency dependence of $h_{fe}(\beta)$.

Network Parameters

In the high-frequency region, the *RC* network of concern has the configuration appearing in Fig. 11.42. At increasing frequencies, the reactance X_C will decrease in magnitude, resulting in a shorting effect across the output and a decrease in gain. The derivation leading to the corner frequency for this *RC* configuration follows along similar lines to that encountered for the low-frequency region. The most significant difference is in the general form of A_v appearing below:

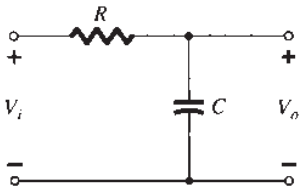


Figure 11.42 *R-C* combination that will define a high cutoff frequency.

$$A_v = \frac{1}{1 + j(f/f_2)} \tag{11.43}$$

which results in a magnitude plot such as shown in Fig. 11.43 that drops off at 6 dB/octave with increasing frequency. Note that f_2 is in the denominator of the frequency ratio rather than the numerator as occurred for f_1 in Eq. (11.21).

In Fig. 11.44, the various parasitic capacitances (C_{be}, C_{bc}, C_{ce}) of the transistor

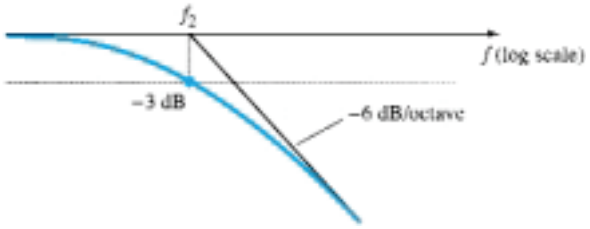


Figure 11.43 Asymptotic plot as defined by Eq. (11.43).

have been included with the wiring capacitances (C_{W_i}, C_{W_o}) introduced during construction. The high-frequency equivalent model for the network of Fig. 11.44 appears in Fig. 11.45. Note the absence of the capacitors C_s, C_C, and C_E, which are all assumed to be in the short-circuit state at these frequencies. The capacitance C_i includes

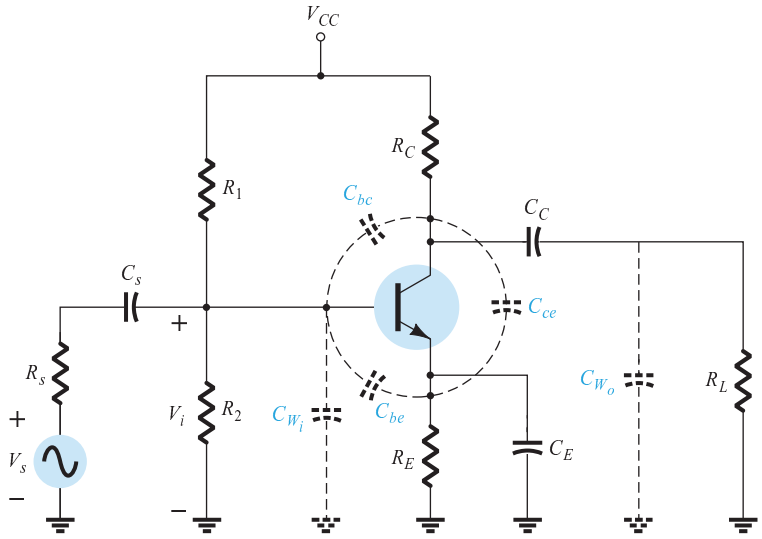


Figure 11.44 Network of Fig. 11.16 with the capacitors that affect the high-frequency response.

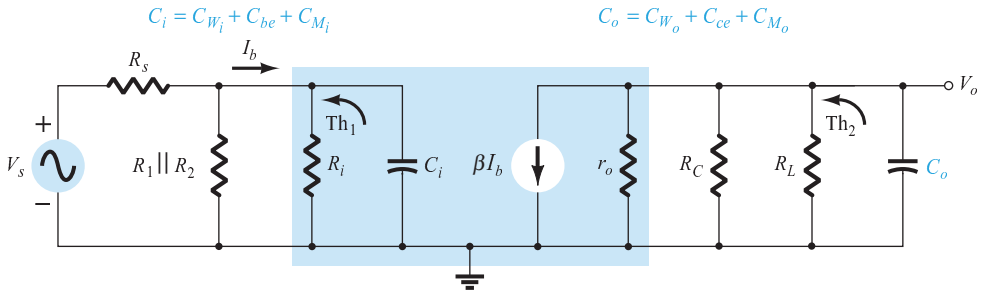


Figure 11.45 High-frequency ac equivalent model for the network of Fig. 11.44.

the input wiring capacitance C_{W_i}, the transition capacitance C_{be}, and the Miller capacitance C_{M_i}. The capacitance C_o includes the output wiring capacitance C_{W_o}, the parasitic capacitance C_{ce}, and the output Miller capacitance C_{M_o}. In general, the capacitance C_{be} is the largest of the parasitic capacitances, with C_{ce} the smallest. In fact, most specification sheets simply provide the levels of C_{be} and C_{bc} and do not include C_{ce} unless it will affect the response of a particular type of transistor in a specific area of application.

Determining the Thévenin equivalent circuit for the input and output networks of Fig. 11.45 will result in the configurations of Fig. 11.46. For the input network, the −3-dB frequency is defined by

$$f_{H_i} = \frac{1}{2\pi R_{\mathrm{Th}_1} C_i} \tag{11.44}$$

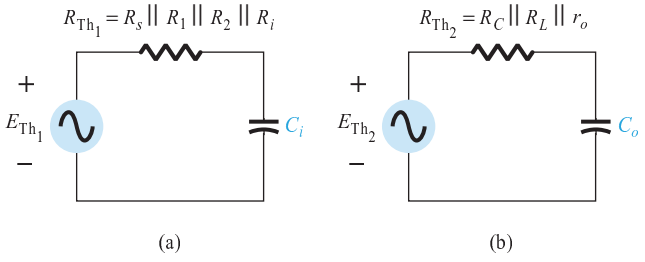


Figure 11.46 Thévenin circuits for the input and output networks of the network of Fig. 11.45.

with $$R_{\text{Th}_1} = R_s \| R_1 \| R_2 \| R_i \tag{11.45}$$

and $$C_i = C_{W_i} + C_{be} + C_{M_i} = C_{W_i} + C_{be} + (1 - A_v)C_{bc} \tag{11.46}$$

At very high frequencies, the effect of C_i is to reduce the total impedance of the parallel combination of R_1, R_2, R_i, and C_i in Fig. 11.45. The result is a reduced level of voltage across C_i, a reduction in I_b, and a gain for the system.

For the output network,

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_2} C_o} \tag{11.47}$$

with $$R_{\text{Th}_2} = R_C \| R_L \| r_o \tag{11.48}$$

and $$C_o = C_{W_o} + C_{ce} + C_{M_o} \tag{11.49}$$

At very high frequencies, the capacitive reactance of C_o will decrease and consequently reduce the total impedance of the output parallel branches of Fig. 11.45. The net result is that V_o will also decline toward zero as the reactance X_C becomes smaller. The frequencies f_{H_i} and f_{H_o} will each define a -6-dB/octave asymptote such as depicted in Fig. 11.43. If the parasitic capacitors were the only elements to determine the high cutoff frequency, the lowest frequency would be the determining factor. However, the decrease in h_{fe} (or β) with frequency must also be considered as to whether its break frequency is lower than f_{H_i} or f_{H_o}.

h_{fe} (or β) Variation

The variation of h_{fe} (or β) with frequency will approach, with some degree of accuracy, the following relationship:

$$h_{fe} = \frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)} \tag{11.50}$$

The use of h_{fe} rather than β in some of this descriptive material is due primarily to the fact that manufacturers typically use the hybrid parameters when covering this issue in their specification sheets, and so on.

The only undefined quantity, f_β, is determined by a set of parameters employed in the *hybrid* π or *Giacoletto* model frequently applied to best represent the transistor in the high-frequency region. It appears in Fig. 11.47. The various parameters warrant a moment of explanation. The resistance $r_{bb'}$ includes the base contact, base bulk, and base spreading resistance. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of

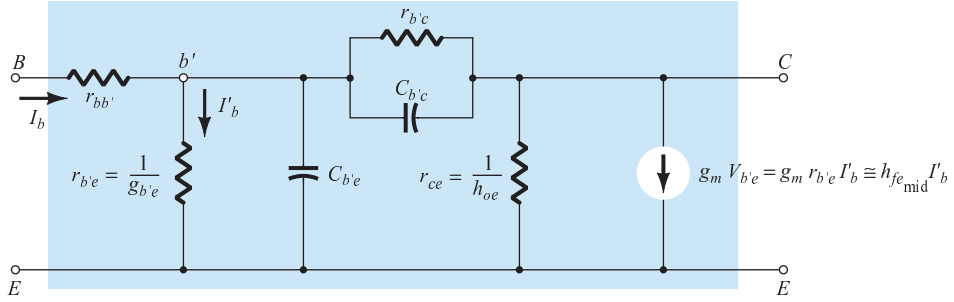


Figure 11.47 Giacoletto (or hybrid π) high-frequency transistor small-signal ac equivalent circuit.

the transistors, while the last is the actual resistance within the active base region. The resistances $r_{b'e}$, r_{ce}, and $r_{b'c}$ are the resistances between the indicated terminals when the device is in the active region. The same is true for the capacitances $C_{b'c}$ and $C_{b'e}$, although the former is a transition capacitance while the latter is a diffusion capacitance. A more detailed explanation of the frequency dependence of each can be found in a number of readily available texts.

In terms of these parameters,

$$f_\beta \text{ (sometimes appearing as } f_{h_{fe}}) = \frac{g_{b'e}}{2\pi(C_{b'e} + C_{b'c})} \tag{11.51}$$

or since the hybrid parameter h_{fe} is related to $g_{b'e}$ through $g_m = h_{fe_{\text{mid}}} g_{b'e}$,

$$f_\beta = \frac{1}{h_{fe_{\text{mid}}}} \frac{g_m}{2\pi(C_{b'e} + C_{b'c})} \tag{11.52}$$

Taking it a step further,

$$g_m = h_{fe_{\text{mid}}} g_{b'e} = h_{fe_{\text{mid}}} \frac{1}{r_{b'e}} \cong \frac{h_{fe_{\text{mid}}}}{h_{ie}} = \frac{\beta_{\text{mid}}}{\beta_{\text{mid}} r_e} = \frac{1}{r_e}$$

and using the approximations

$$C_{b'e} \cong C_{be} \qquad \text{and} \qquad C_{b'c} \cong C_{bc}$$

will result in the following form for Eq. (11.50):

$$f_\beta \cong \frac{1}{2\pi\beta_{\text{mid}} r_e (C_{be} + C_{bc})} \tag{11.53}$$

Equation (11.53) clearly reveals that since r_e is a function of the network design:

f_β is a function of the bias conditions.

The basic format of Eq. (11.50) is exactly the same as Eq. (11.43) if we extract the multiplying factor $h_{fe_{\text{mid}}}$, revealing that h_{fe} will drop off from its midband value with a 6-dB/octave slope as shown in Fig. 11.48. The same figure has a plot of h_{fb} (or α) versus frequency. Note the small change in h_{fb} for the chosen frequency range, revealing that the common-base configuration displays improved high-frequency characteristics over the common-emitter configuration. Recall also the absence of the Miller effect capacitance due to the noninverting characteristics of the common-base configuration. For this very reason, common-base high-frequency parameters rather than common-emitter parameters are often specified for a transistor—especially those designed specifically to operate in the high-frequency regions.

The following equation permits a direct conversion for determining f_β if f_α and α are specified.

$$f_\beta = f_\alpha(1 - \alpha) \tag{11.54}$$

A quantity called the *gain–bandwidth product* is defined for the transistor by the condition

$$\left| \frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)} \right| = 1$$

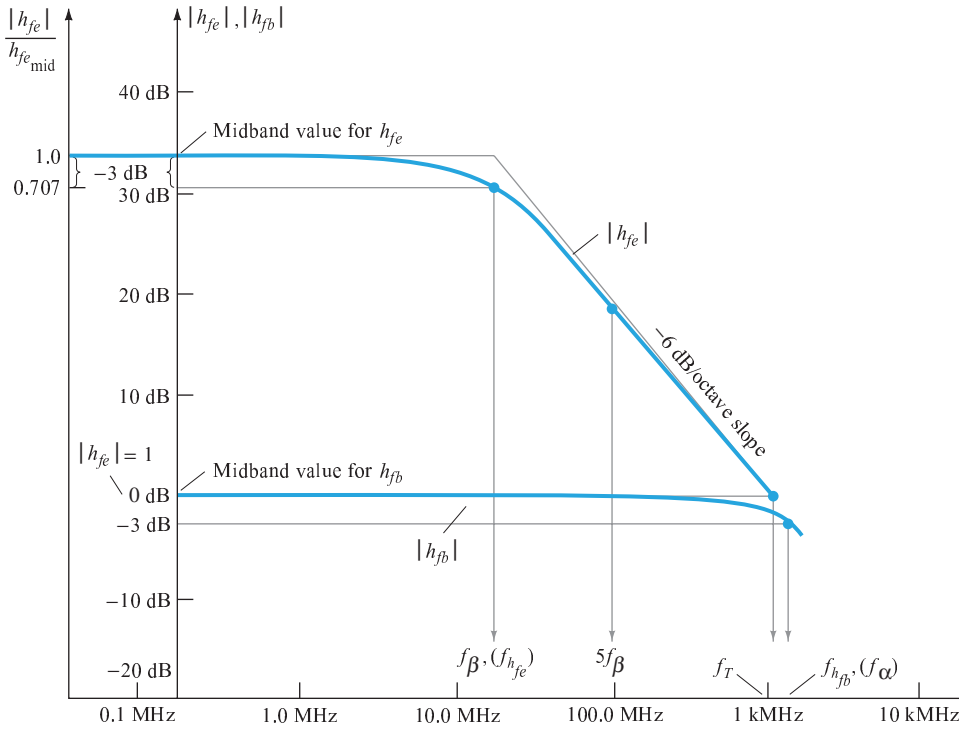


Figure 11.48 h_{fe} and h_{fb} versus frequency in the high-frequency region.

so that $$|h_{fe}|_{\text{dB}} = 20 \log_{10} \left| \frac{h_{fe_{\text{mid}}}}{1 + j(f/f_\beta)} \right| = 20 \log_{10} 1 = 0 \text{ dB}$$

The frequency at which $|h_{fe}|_{\text{dB}} = 0$ dB is clearly indicated by f_T in Fig. 11.48. The magnitude of h_{fe} at the defined condition point ($f_T \gg f_\beta$) is given by

$$\frac{h_{fe_{\text{mid}}}}{\sqrt{1 + (f_T/f_\beta)^2}} \cong \frac{h_{fe_{\text{mid}}}}{f_T/f_\beta} = 1$$

so that $$\boxed{f_T \cong h_{fe_{\text{mid}}} \cdot \overbrace{f_\beta}^{(\cong \text{BW})}} \quad \text{(gain–bandwidth product)} \tag{11.55}$$

or $$\boxed{f_T \cong \beta_{\text{mid}} f_\beta} \tag{11.56}$$

with $$\boxed{f_\beta = \frac{f_T}{\beta_{\text{mid}}}} \tag{11.57}$$

Substituting Eq. (11.53) for f_β in Eq. (11.55) gives

$$f_T \cong \beta_{\text{mid}} \frac{1}{2\pi\beta_{\text{mid}} r_e (C_{be} + C_{bc})}$$

and $$\boxed{f_T \cong \frac{1}{2\pi r_e (C_{be} + C_{bc})}} \tag{11.58}$$

EXAMPLE 11.11

For the network of Fig. 11.44 with the same parameters as in Example 11.9, that is,

$R_s = 1\ \text{k}\Omega$, $R_1 = 40\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_E = 2\ \text{k}\Omega$, $R_C = 4\ \text{k}\Omega$, $R_L = 2.2\ \text{k}\Omega$

$C_s = 10\ \mu\text{F}$, $C_C = 1\ \mu\text{F}$, $C_E = 20\ \mu\text{F}$

$\beta = 100$, $r_o = \infty\ \Omega$, $V_{CC} = 20\ \text{V}$

with the addition of

$$C_{be} = 36\ \text{pF},\ C_{bc} = 4\ \text{pF},\ C_{ce} = 1\ \text{pF},\ C_{W_i} = 6\ \text{pF},\ C_{W_o} = 8\ \text{pF}$$

(a) Determine f_{H_i} and f_{H_o}.
(b) Find f_β and f_T.
(c) Sketch the frequency response for the low- and high-frequency regions using the results of Example 11.9 and the results of parts (a) and (b).
(d) Obtain a **PROBE** response for the full frequency spectrum and compare with the results of part (c).

Solution

(a) From Example 11.9:

$$R_i = 1.32\ \text{k}\Omega, \qquad A_{v_{\text{mid}}}(\text{amplifier}) = -90$$

and

$$R_{\text{Th}_1} = R_s \| R_1 \| R_2 \| R_i = 1\ \text{k}\Omega \| 40\ \text{k}\Omega \| 10\ \text{k}\Omega \| 1.32\ \text{k}\Omega$$
$$\cong 0.531\ \text{k}\Omega$$

with

$$C_i = C_{W_i} + C_{be} + (1 - A_v)C_{be}$$
$$= 6\ \text{pF} + 36\ \text{pF} + [1 - (-90)]4\ \text{pF}$$
$$= 406\ \text{pF}$$

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_1} C_i} = \frac{1}{2\pi(0.531\ \text{k}\Omega)(406\ \text{pF})}$$
$$= \mathbf{738.24\ kHz}$$

$$R_{\text{Th}_2} = R_C \| R_L = 4\ \text{k}\Omega \| 2.2\ \text{k}\Omega = 1.419\ \text{k}\Omega$$

$$C_o = C_{W_o} + C_{ce} + C_{M_o} = 8\ \text{pF} + 1\ \text{pF} + \left(1 - \frac{1}{-90}\right) 4\ \text{pF}$$
$$= 13.04\ \text{pF}$$

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_2} C_o} = \frac{1}{2\pi(1.419\ \text{k}\Omega)(13.04\ \text{pF})}$$
$$= \mathbf{8.6\ MHz}$$

(b) Applying Eq. (11.53) gives

$$f_\beta = \frac{1}{2\pi\beta_{\text{mid}} r_e (C_{be} + C_{bc})}$$

$$= \frac{1}{2\pi(100)(15.76\ \Omega)(36\ \text{pF} + 4\ \text{pF})} = \frac{1}{2\pi(100)(15.76\ \Omega)(40\ \text{pF})}$$

$$= \mathbf{2.52\ MHz}$$

$$f_T = \beta_{\text{mid}} f_\beta = (100)(2.52\ \text{MHz})$$

$$= \mathbf{252\ MHz}$$

(c) See Fig. 11.49. Both f_β and f_{H_o} will lower the upper cutoff frequency below the level determined by f_{H_i}. f_β is closer to f_{H_i} and therefore will have a greater impact than f_{H_o}. In any event, the bandwidth will be less than that defined solely by f_{H_i}. In fact, for the parameters of this network the upper cutoff frequency will be relatively close to 600 kHz.

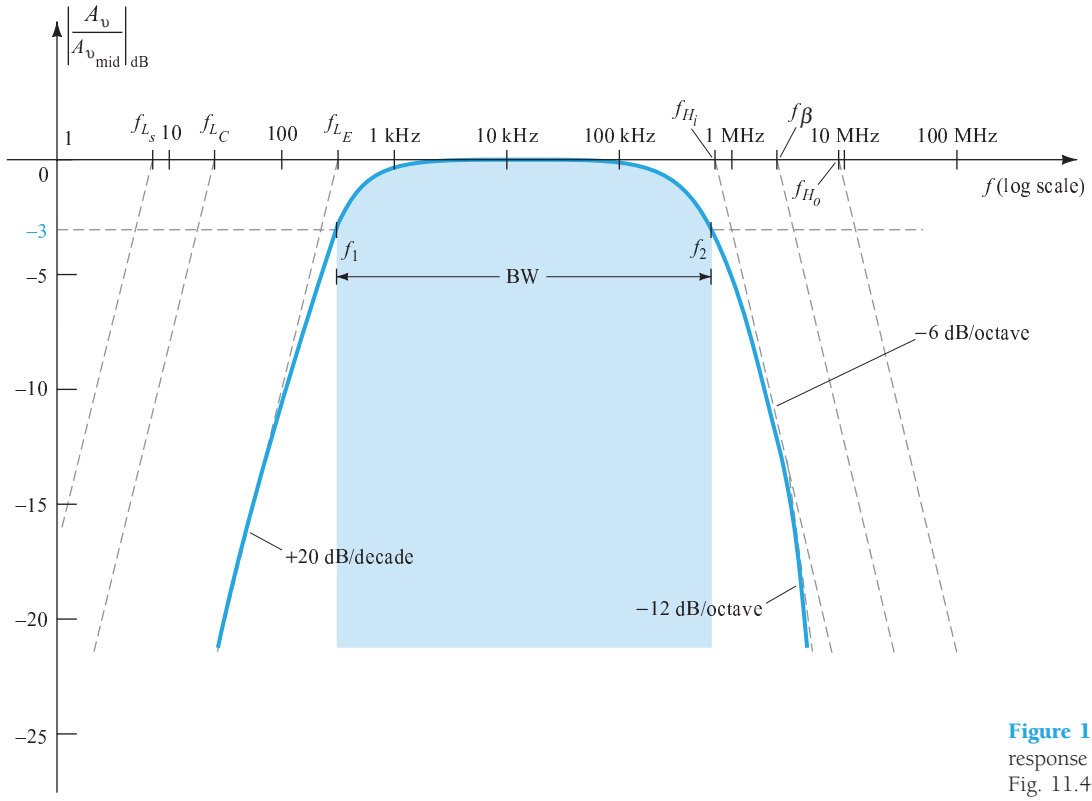


Figure 11.49 Full frequency response for the network of Fig. 11.44.

In general, therefore, the lowest of the upper-cutoff frequencies defines a maximum possible bandwidth for a system.

(d) In order to obtain a PSpice analysis for the full frequency range, the parasitic capacitances have to be added to the network as shown in Fig. 11.50.

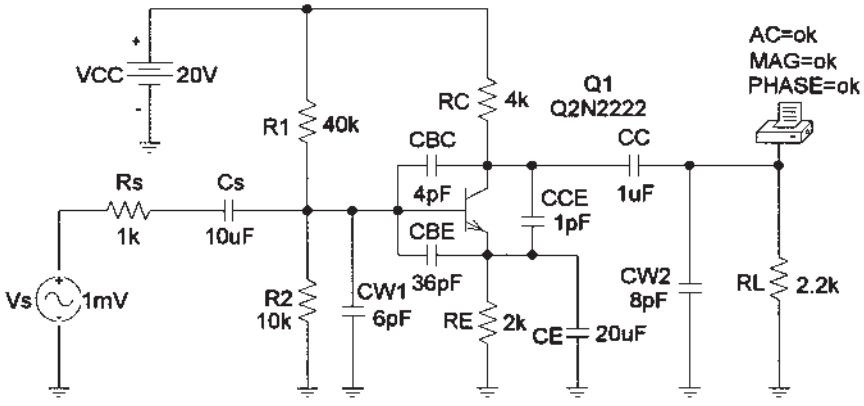


Figure 11.50 Network of Figure 11.25 with parasitic capacitances in place.

An **Analysis** will result in the plot of Fig. 11.51 using the **Trace Expression** appearing at the bottom of the plot. The vertical scale was changed from −60 to 0 dB to −30 to 0 dB to highlight the area of interest using the **Y-Axis Settings.** The low cutoff frequency of 324 Hz is as determined primarily by f_{L_E}, and the high cutoff frequency is near 667kHz. Even though f_{H_o} is more than a decade higher than f_{H_i}, it will have an impact on the high cutoff frequency. In total, however, the PSpice analysis has been a welcome verification of the hand-written approach.

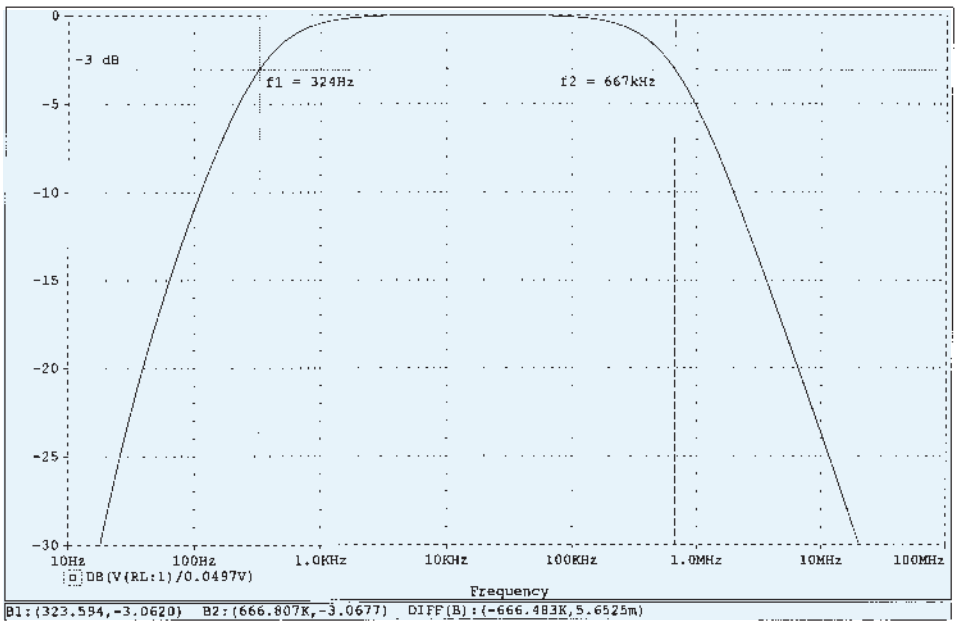


Figure 11.51 Full frequency response for the network of Fig. 11.50.

11.10 HIGH-FREQUENCY RESPONSE — FET AMPLIFIER

The analysis of the high-frequency response of the FET amplifier will proceed in a very similar manner to that encountered for the BJT amplifier. As shown in Fig. 11.52, there are interelectrode and wiring capacitances that will determine the high-frequency characteristics of the amplifier. The capacitors C_{gs} and C_{gd} typically vary from 1 to 10 pF, while the capacitance C_{ds} is usually quite a bit smaller, ranging from 0.1 to 1 pF.

Since the network of Fig. 11.52 is an inverting amplifier, a Miller effect capacitance will appear in the high-frequency ac equivalent network appearing in Fig. 11.53. At high frequencies, C_i will approach a short-circuit equivalent and V_{gs} will drop in value and reduce the overall gain. At frequencies where C_o approaches its short-circuit equivalent, the parallel output voltage V_o will drop in magnitude.

The cutoff frequencies defined by the input and output circuits can be obtained by first finding the Thévenin equivalent circuits for each section as shown in Fig. 11.54. For the input circuit,

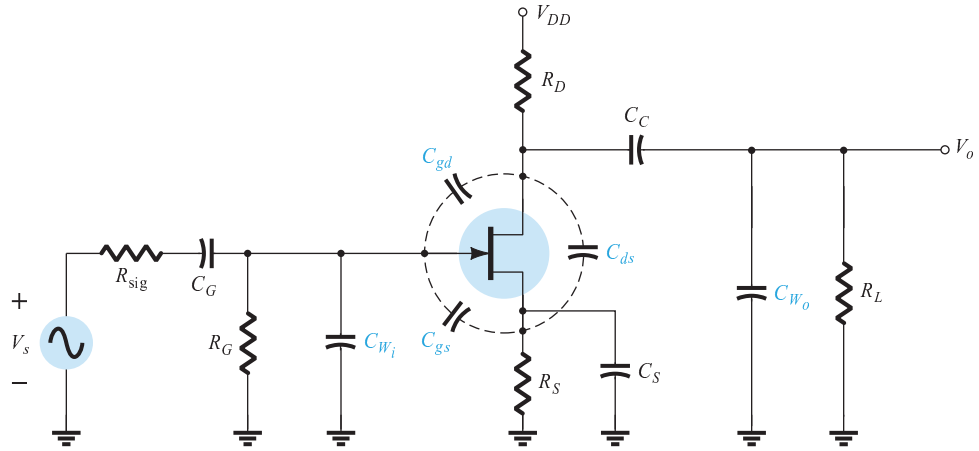


Figure 11.52 Capacitive elements that affect the high frequency response of a JFET amplifier.

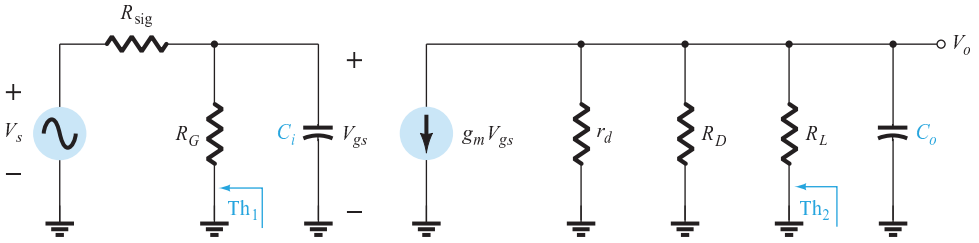


Figure 11.53 High-frequency ac equivalent circuit for Fig. 11.52.

$$f_{H_i} = \frac{1}{2\pi R_{\text{Th}_1} C_i} \tag{11.59}$$

and

$$R_{\text{Th}_1} = R_{\text{sig}} \| R_G \tag{11.60}$$

with

$$C_i = C_{W_i} + C_{gs} + C_{M_i} \tag{11.61}$$

and

$$C_{M_i} = (1 - A_v) C_{gd} \tag{11.62}$$

and for the output circuit,

$$f_{H_o} = \frac{1}{2\pi R_{\text{Th}_2} C_o} \tag{11.63}$$

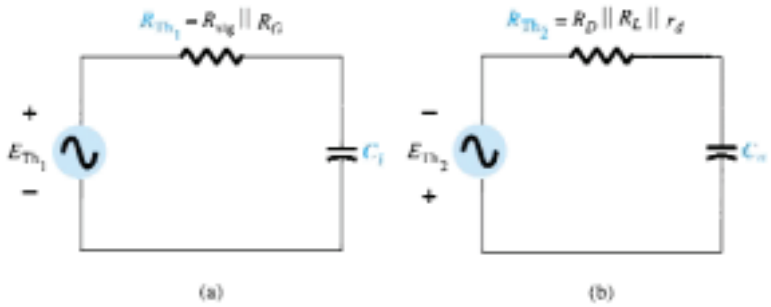


Figure 11.54 The Thévenin equivalent circuits for the (a) input circuit and (b) output circuit.

f

with $$R_{\text{Th}_2} = R_D \| R_L \| r_d \tag{11.64}$$

and $$C_o = C_{W_o} + C_{ds} + C_{M_o}$$

and $$C_{M_o} = \left(1 - \frac{1}{Av}\right) C_{gd} \tag{11.65}$$

EXAMPLE 11.12

(a) Determine the high cutoff frequencies for the network of Fig. 11.52 using the same parameters as Example 11.10:

$$C_G = 0.01\ \mu\text{F}, \quad C_C = 0.5\ \mu\text{F}, \quad C_S = 2\ \mu\text{F}$$

$$R_{\text{sig}} = 10\ \text{k}\Omega, \quad R_G = 1\ \text{M}\Omega, \quad R_D = 4.7\ \text{k}\Omega, \quad R_S = 1\ \text{k}\Omega, \quad R_L = 2.2\ \text{k}\Omega$$

$$I_{DSS} = 8\ \text{mA}, \quad V_P = -4\ \text{V}, \quad r_d = \infty\ \Omega, \quad V_{DD} = 20\ \text{V}$$

with the addition of

$$C_{gd} = 2\ \text{pF}, \quad C_{gs} = 4\ \text{pF}, \quad C_{ds} = 0.5\ \text{pF}, \quad C_{W_i} = 5\ \text{pF}, \quad C_{W_o} = 6\ \text{pF}$$

(b) Review a **PROBE** response for the full frequency range and note whether it supports the conclusions of Example 11.10 and the calculations above.

Solution

(a) $R_{\text{Th}_1} = R_{\text{sig}} \| R_G = 10\ \text{k}\Omega \| 1\ \text{M}\Omega = 9.9\ \text{k}\Omega$

From Example 11.10, $A_v = -3$.

$$\begin{aligned} C_i &= C_{W_i} + C_{gs} + (1 - A_v)C_{gd} \\ &= 5\ \text{pF} + 4\ \text{pF} + (1 + 3)2\ \text{pF} \\ &= 9\ \text{pF} + 8\ \text{pF} \\ &= 17\ \text{pF} \end{aligned}$$

$$f_{H_i} = \frac{1}{2\pi R_{Th_1} C_i}$$

$$= \frac{1}{2\pi(9.9\ \text{k}\Omega)(17\ \text{pF})} = \mathbf{945.67\ kHz}$$

$$\begin{aligned} R_{\text{Th}_2} &= R_D \| R_L \\ &= 4.7\ \text{k}\Omega \| 2.2\ \text{k}\Omega \\ &\cong 1.5\ \text{k}\Omega \end{aligned}$$

$$C_o = C_{W_o} + C_{ds} + C_{M_o} = 6\ \text{pF} + 0.5\ \text{pF} + \left(1 - \frac{1}{-3}\right)2\ \text{pF} = 9.17\ \text{pF}$$

$$f_{H_o} = \frac{1}{2\pi(1.5\ \text{k}\Omega)(9.17\ \text{pF})} = \mathbf{11.57\ MHz}$$

The results above clearly indicate that the input capacitance with its Miller effect capacitance will determine the upper cutoff frequency. This is typically the case due to the smaller value of C_{ds} and the resistance levels encountered in the output circuit.

(b) Using PSpice Windows, the schematic for the network will appear as shown in Fig. 11.55.

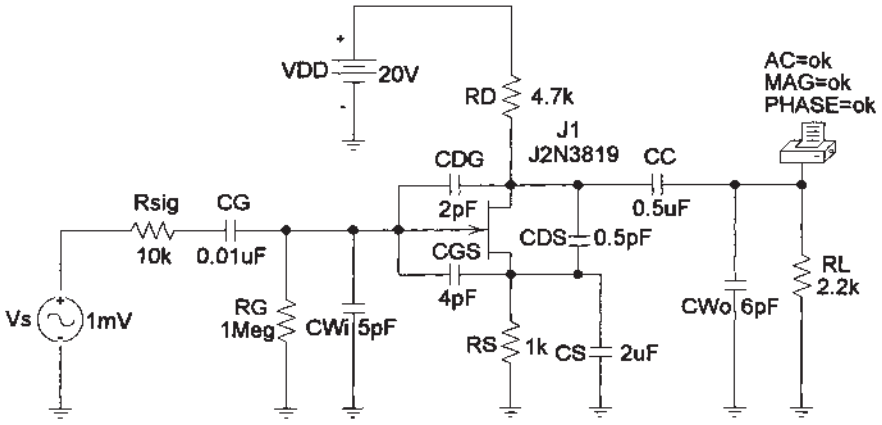


Figure 11.55 Network of Figure 11.52 with assigned values.

Under **Analysis,** the **AC Sweep** is set to **Decade** with **Pts/Decade** at 1000, **Start Freq.:** at 10 Hz, and **End Freq.:** at 10 MHz. Under the **Add Traces** dialog box, the **Trace Expression** is entered as **DB(V(RL:1)/2.993mV),** and the plot of Fig. 11.56 is obtained. Just for a moment, consider how much time it must have taken to obtain a plot such as in Fig. 11.56 without computer methods for a network as complicated as Fig. 11.55. Often, we forget how computer systems have helped us through some painstaking, lengthy, and boring series of calculations.

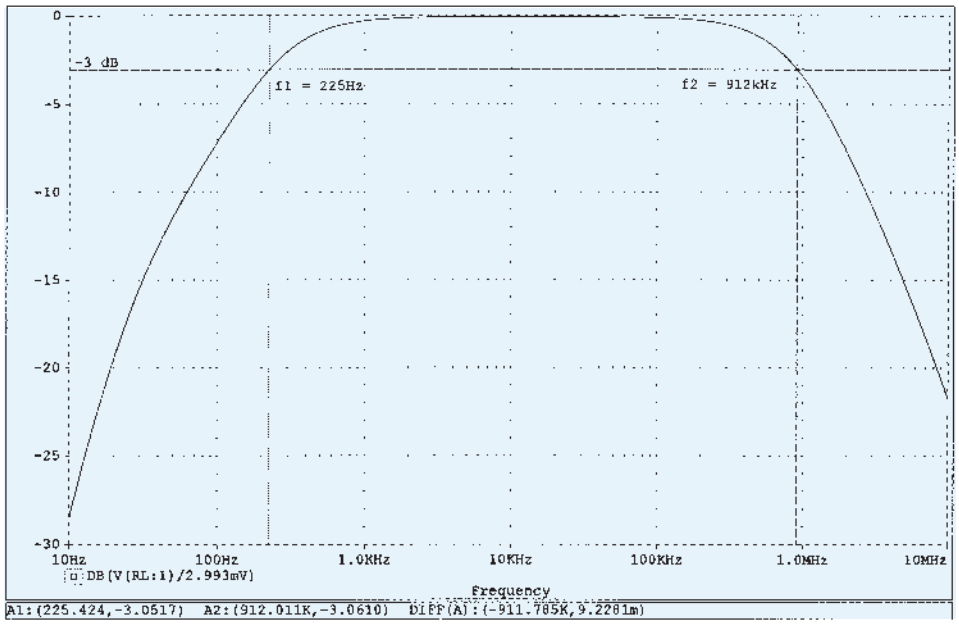


Figure 11.56 Frequency response for the network of Example 11.12.

Using the cursor, we find the lower and upper cutoff frequencies to be 225 Hz and 921 kHz, respectively, providing a nice match with the calculated values.

Even though the analysis of the past few sections has been limited to two configurations, the exposure to the general procedure for determining the cutoff frequencies should support the analysis of any other transistor configuration. Keep in mind that the Miller capacitance is limited to inverting amplifiers and that f_α is significantly greater than f_β if the common-base configuration is encountered. There is a great deal more literature on the analysis of single-stage amplifiers that goes beyond the coverage of this chapter. However, the content of this chapter should provide a firm foundation for any future analysis of frequency effects.

11.11 MULTISTAGE FREQUENCY EFFECTS

For a second transistor stage connected directly to the output of a first stage, there will be a significant change in the overall frequency response. In the high-frequency region, the output capacitance C_o must now include the wiring capacitance (C_{W_1}), parasitic capacitance (C_{be}), and Miller capacitance (C_{M_1}) of the following stage. Further, there will be additional low-frequency cutoff levels due to the second stage that will further reduce the overall gain of the system in this region. For each additional stage, the upper cutoff frequency will be determined primarily by that stage having the lowest cutoff frequency. The low-frequency cutoff is primarily determined by that stage having the highest low-frequency cutoff frequency. Obviously, therefore, one poorly designed stage can offset an otherwise well-designed cascaded system.

The effect of increasing the number of *identical* stages can be clearly demonstrated by considering the situations indicated in Fig. 11.57. In each case, the upper and lower cutoff frequencies of each of the cascaded stages are identical. For a single stage, the cutoff frequencies are f_1 and f_2 as indicated. For two identical stages in cascade, the drop-off rate in the high- and low-frequency regions has increased to -12 dB/octave or -40 dB/decade. At f_1 and f_2, therefore, the decibel drop is now -6 dB rather than the defined band frequency gain level of -3 dB. The -3-dB point has shifted to f_1' and f_2' as indicated, with a resulting drop in the bandwidth. A -18-dB/octave or -60-dB/decade slope will result for a three-stage system of identical stages with the indicated reduction in bandwidth (f_1'' and f_2'').

Assuming identical stages, an equation for each band frequency as a function of the number of stages (n) can be determined in the following manner: For the low-frequency region,

$$A_{v_{\text{low, (overall)}}} = A_{v_{1_{\text{low}}}} A_{v_{2_{\text{low}}}} A_{v_{3_{\text{low}}}} \cdots A_{v_{n_{\text{low}}}}$$

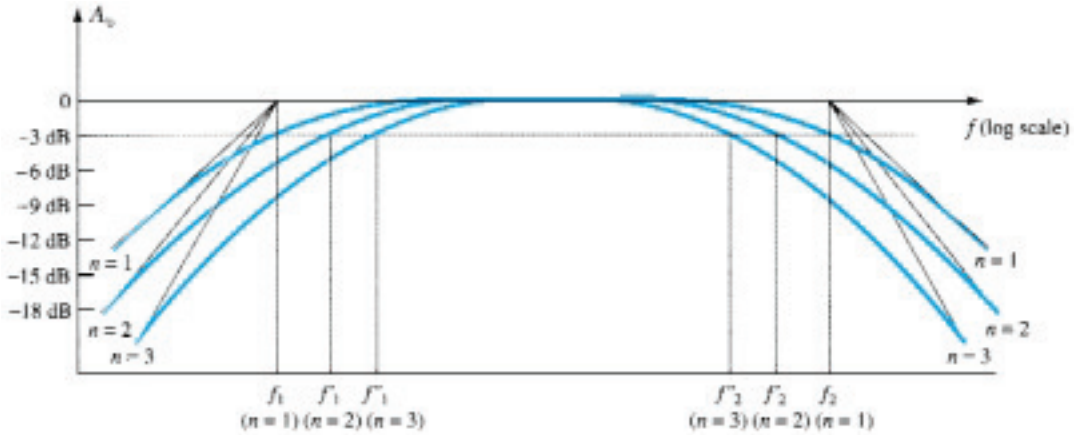


Figure 11.57 Effect of an increased number of stages on the cutoff frequencies and the bandwidth.

but since each stage is identical, $A_{v_{1_{low}}} = A_{v_{2_{low}}} = \text{etc.}$ and

$$A_{v_{low,\,(overall)}} = (A_{v_{1_{low}}})^n$$

or

$$\frac{A_{v_{low}}}{A_{v_{mid}}}\,(\text{overall}) = \left(\frac{A_{v_{1_{low}}}}{A_{v_{mid}}}\right)^n = \frac{1}{(1 - jf_1/f)^n}$$

Setting the magnitude of this result equal to $1/\sqrt{2}$(−3 dB level) results in

$$\frac{1}{\sqrt{1 + (f_1/f_1')^2]^n}} = \frac{1}{\sqrt{2}}$$

or

$$\left\{\left[1 + \left(\frac{f_1}{f_1'}\right)^{2-}\right]^{1/2}\right\}^n = \left\{\left[1 + \left(\frac{f_1}{f_1'}\right)^2\right]^n\right\}^{1/2} = (2)^{1/2}$$

so that

$$\left[1 + \left(\frac{f_1}{f_1'}\right)^2\right]^n = 2$$

and

$$1 + \left(\frac{f_1}{f_1'}\right)^2 = 2^{1/n}$$

with the result that

$$\boxed{f_1' = \frac{f_1}{\sqrt{2^{1/n} - 1}}} \tag{11.66}$$

In a similar manner, it can be shown that for the high-frequency region,

$$\boxed{f_2' = (\sqrt{2^{1/n} - 1})f_2} \tag{11.67}$$

Note the presence of the same factor $\sqrt{2^{1/n} - 1}$ in each equation. The magnitude of this factor for various values of n is listed below.

n	$\sqrt{2^{1/n} - 1}$
2	0.64
3	0.51
4	0.43
5	0.39

For $n = 2$, consider that the upper cutoff frequency $f_2'' = 0.64f_2$ or 64% of the value obtained for a single stage, while $f_1' = (1/0.64)f_1 = 1.56f_1$. For $n = 3$, $f_2' = 0.51f_2$ or approximately $\frac{1}{2}$ the value of a single stage with $f_1' = (1/0.51)f_1 = 1.96f_1$ or approximately *twice* the single-stage value.

For the *RC*-coupled transistor amplifier, if $f_2 = f_\beta$, or if they are close enough in magnitude for both to affect the upper 3-dB frequency, the number of stages must be increased by a factor of 2 when determining f_2' due to the increased number of factors $1/(1 + jf/f_x)$.

A decrease in bandwidth is not always associated with an increase in the number of stages if the midband gain can remain fixed and independent of the number of stages. For instance, if a single-stage amplifier produces a gain of 100 with a bandwidth of 10,000 Hz, the resulting gain–bandwidth product is $10^2 \times 10^4 = 10^6$. For a two-stage system the same gain can be obtained by having two stages with a gain of 10 since $(10 \times 10 = 100)$. The bandwidth of each stage would then increase by a factor of 10 to 100,000 due to the lower gain requirement and fixed gain–bandwidth product of 10^6. Of course, the design must be such as to permit the increased bandwidth and establish the lower gain level.

11.12 SQUARE-WAVE TESTING

A sense for the frequency response of an amplifier can be determined experimentally by applying a square-wave signal to the amplifier and noting the output response. The shape of the output waveform will reveal whether the high or low frequencies are being properly amplified. The use of *square-wave testing* is significantly less time-consuming than applying a series of sinusoidal signals at different frequencies and magnitudes to test the frequency response of the amplifier.

The reason for choosing a square-wave signal for the testing process is best described by examining the *Fourier series* expansion of a square wave composed of a series of sinusoidal components of different magnitudes and frequencies. The summation of the terms of the series will result in the original waveform. In other words, even though a waveform may not be sinusoidal, it can be reproduced by a series of sinusoidal terms of different frequencies and magnitudes.

The Fourier series expansion for the square wave of Fig. 11.58 is

$$v = \frac{4}{\pi} V_m \left(\sin 2\pi f_s t + \frac{1}{3} \sin 2\pi(3f_s)t + \frac{1}{5} \sin 2\pi(5f_s)t + \frac{1}{7} \sin 2\pi(7f_s)t + \frac{1}{9} \sin 2\pi(9f_s)t + \cdots + \frac{1}{n} \sin 2\pi(nf_s)t \right) \qquad (11.68)$$

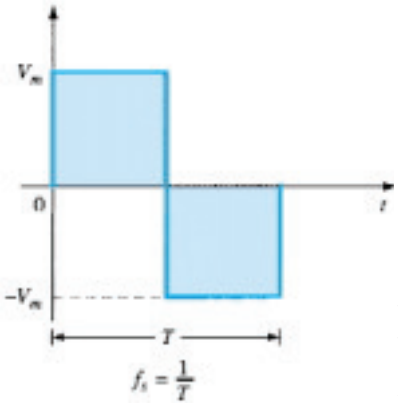


Figure 11.58 Square wave.

The first term of the series is called the *fundamental* term and in this case has the same frequency, f_s, as the square wave. The next term has a frequency equal to three times the fundamental and is referred to as the *third harmonic*. Its magnitude is one-third the magnitude of the fundamental term. The frequencies of the succeeding terms are odd multiples of the fundamental term, and the magnitude decreases with each higher harmonic. Figure 11.59 demonstrates how the summation of terms of a Fourier series can result in a nonsinusoidal waveform. The generation of the square wave of Fig. 11.58 would require an infinite number of terms. However, the summation of just the fundamental term and the third harmonic in Fig. 11.59a clearly results in a waveform that is beginning to take on the appearance of a square wave. Including the fifth and seventh harmonics as in Fig. 11.59b takes us a step closer to the waveform of Fig. 11.58.

Since the ninth harmonic has a magnitude greater than 10% of the fundamental term [$\frac{1}{9}(100\%) = 11.1\%$], the fundamental term through the ninth harmonic are the major contributors to the Fourier series expansion of the square-wave function. It is therefore reasonable to assume that if the application of a square wave of a particular frequency results in a nice clean square wave at the output, then the fundamental

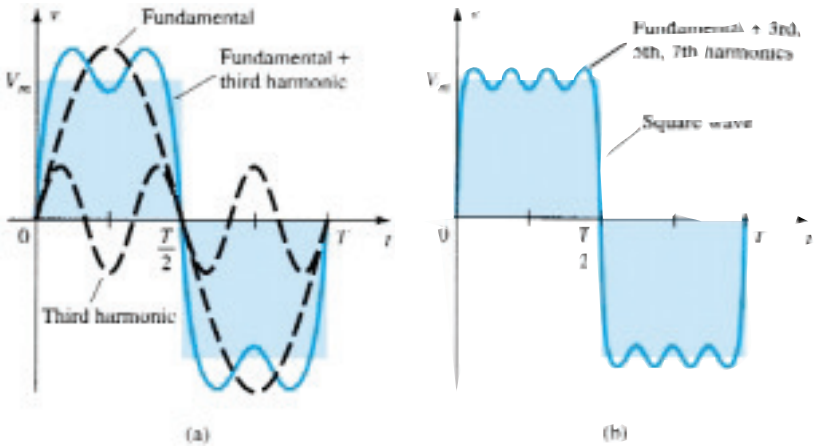


Figure 11.59 Harmonic content of a square wave.

through the ninth harmonic are being amplified without visual distortion by the amplifier. For instance, if an audio amplifier with a bandwidth of 20 kHz (audio range is from 20 Hz to 20 kHz) is to be tested, the frequency of the applied signal should be at least 20 kHz/9 = 2.22 kHz.

If the response of an amplifier to an applied square wave is an undistorted replica of the input, the frequency response (or BW) of the amplifier is obviously sufficient for the applied frequency. If the response is as shown in Fig. 11.60a and b, the low frequencies are not being amplified properly and the low cutoff frequency has to be investigated. If the waveform has the appearance of Fig. 11.60c, the high-frequency components are not receiving sufficient amplification and the high cutoff frequency (or BW) has to be reviewed.

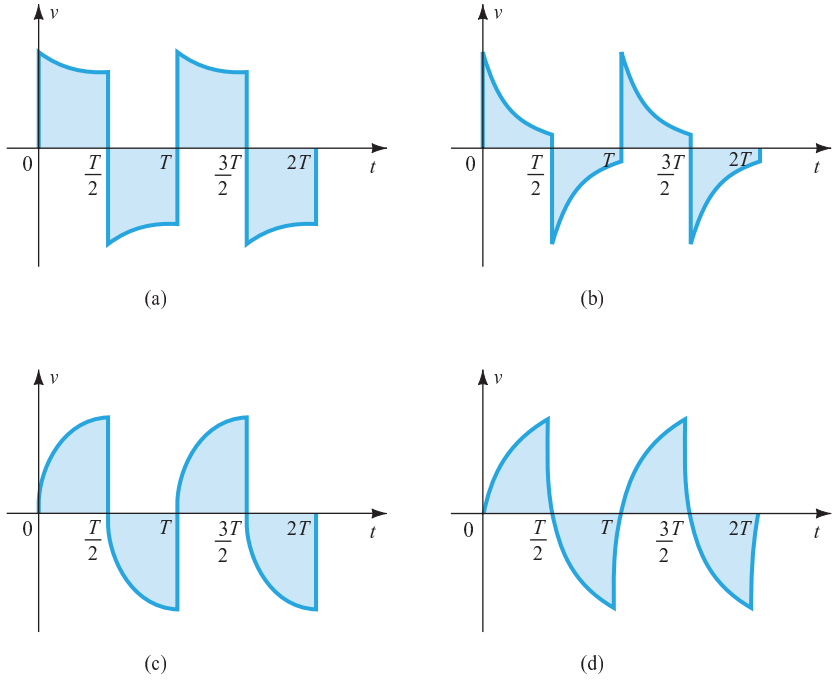


Figure 11.60 (a) Poor low frequency response; (b) very poor low-frequency response; (c) poor high-frequency response; (d) very poor high-frequency response.

The actual high cutoff frequency (or BW) can be determined from the output waveform by carefully measuring the rise time defined between 10% and 90% of the peak value, as shown in Fig. 11.61. Substituting into the following equation will provide the upper cutoff frequency, and since $BW = f_{H_i} - f_{L_o} \cong f_{H_i}$, the equation also provides an indication of the BW of the amplifier.

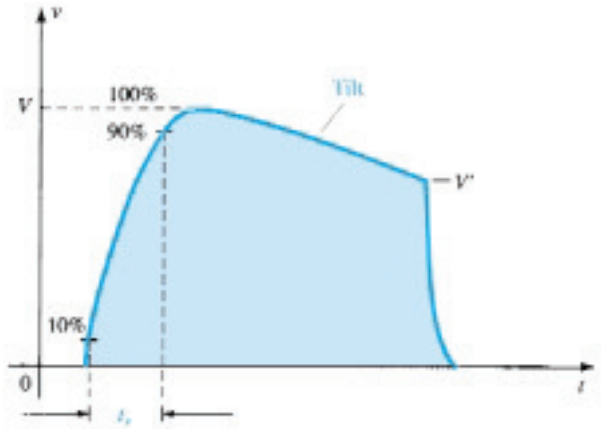


Figure 11.61 Defining the rise time and tilt of a square wave response.

$$\text{BW} \cong f_{H_i} = \frac{0.35}{t_r} \tag{11.69}$$

The low cutoff frequency can be determined from the output response by carefully measuring the tilt of Fig. 11.61 and substituting into one of the following equations:

$$\%\ \text{tilt} = P\% = \frac{V - V'}{V} \times 100\% \tag{11.70}$$

$$\text{tilt} = P = \frac{V - V'}{V} \quad \text{(decimal form)} \tag{11.71}$$

The low cutoff frequency is then determined from

$$f_{L_o} = \frac{P}{\pi} f_s \tag{11.72}$$

EXAMPLE 11.13

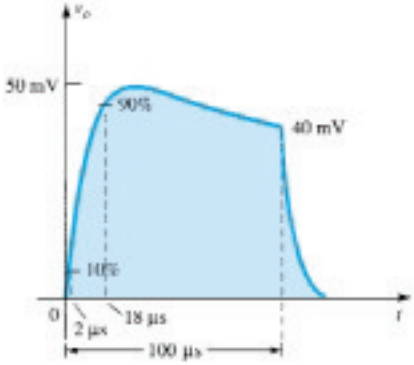


Figure 11.62 Example 11.13

The application of a 1-mV, 5-kHz square wave to an amplifier resulted in the output waveform of Fig. 11.62.

(a) Write the Fourier series expansion for the square wave through the ninth harmonic.

(b) Determine the bandwidth of the amplifier.

(c) Calculate the low cutoff frequency.

Solution

(a) $$v_i = \frac{4\ \text{mV}}{\pi}\left(\sin 2\pi\,(5 \times 10^3)t + \frac{1}{3}\sin 2\pi(15 \times 10^3)t + \frac{1}{5}\sin 2\pi(25 \times 10^3)t + \frac{1}{7}\sin 2\pi(35 \times 10^3)t + \frac{1}{9}\sin 2\pi(45 \times 10^3)t\right)$$

(b) $$t_r = 18\ \mu\text{s} - 2\ \mu\text{s} = 16\ \mu\text{s}$$

$$\text{BW} = \frac{0.35}{t_r} = \frac{0.35}{16\ \mu\text{s}} = \mathbf{21{,}875\ Hz} \cong 4.4 f_s$$

(c) $$P = \frac{V - V'}{V} = \frac{50\ \text{mV} - 40\ \text{mV}}{50\ \text{mV}} = 0.2$$

$$f_{L_o} = \frac{P}{\pi} f_s = \left(\frac{0.2}{\pi}\right)(5\ \text{kHz}) = \mathbf{318.31\ Hz}$$

11.13 PSPICE WINDOWS

The computer analysis of this chapter was integrated into the chapter for emphasis and a clear demonstration of the power of the PSpice software package. The complete frequency response of a single-stage or multistage system can be determined in a relatively short period of time to verify theoretical calculations or provide an immediate indication of the low and high cutoff frequencies of the system. The exercises in the chapter will provide an opportunity to apply the PSpice software package to a variety of networks.

§ 11.2 Logarithms

1. (a) Determine the common logarithm of the following numbers: 10^3, 50, and 0.707.
(b) Determine the natural logarithm of the same numbers appearing in part (a).
(c) Compare the solutions of parts (a) and (b).

2. (a) Determine the common logarithm of the number 2.2×10^3.
(b) Determine the natural logarithm of the number of part (a) using Eq. (11.4).
(c) Determine the natural logarithm of the number of part (a) using natural logarithms and compare with the solution of part (b).

3. Determine:
(a) $20 \log_{10} \frac{40}{8}$ using Eq. (11.6) and compare with $20 \log_{10} 5$.
(b) $10 \log_{10} \frac{1}{20}$ using Eq. (11.7) and compare with $10 \log_{10} 0.05$.
(c) $\log_{10}(40)(0.125)$ using Eq. (11.8) and compare with $\log_{10} 5$.

4. Calculate the power gain in decibels for each of the following cases.
(a) $P_o = 100$ W, $P_i = 5$ W.
(b) $P_o = 100$ mW, $P_i = 5$ mW.
(c) $P_o = 100\ \mu$W, $P_i = 20\ \mu$W.

5. Determine G_{dBm} for an output power level of 25 W.

6. Two voltage measurements made across the same resistance are $V_1 = 25$ V and $V_2 = 100$ V. Calculate the power gain in decibels of the second reading over the first reading.

7. Input and output voltage measurements of $V_i = 10$ mV and $V_o = 25$ V are made. What is the voltage gain in decibels?

* **8.** (a) The total decibel gain of a three-stage system is 120 dB. Determine the decibel gain of each stage if the second stage has twice the decibel gain of the first and the third has 2.7 times the decibel gain of the first.
(b) Determine the voltage gain of each stage.

* **9.** If the applied ac power to a system is 5 μW at 100 mV and the output power is 48 W, determine:
(a) The power gain in decibels.
(b) The voltage gain in decibels if the output impedance is 40 kΩ.
(c) The input impedance.
(d) The output voltage.

§ 11.4 General Frequency Considerations

10. Given the characteristics of Fig. 11.63, sketch:
(a) The normalized gain.
(b) The normalized dB gain (and determine the bandwidth and cutoff frequencies).

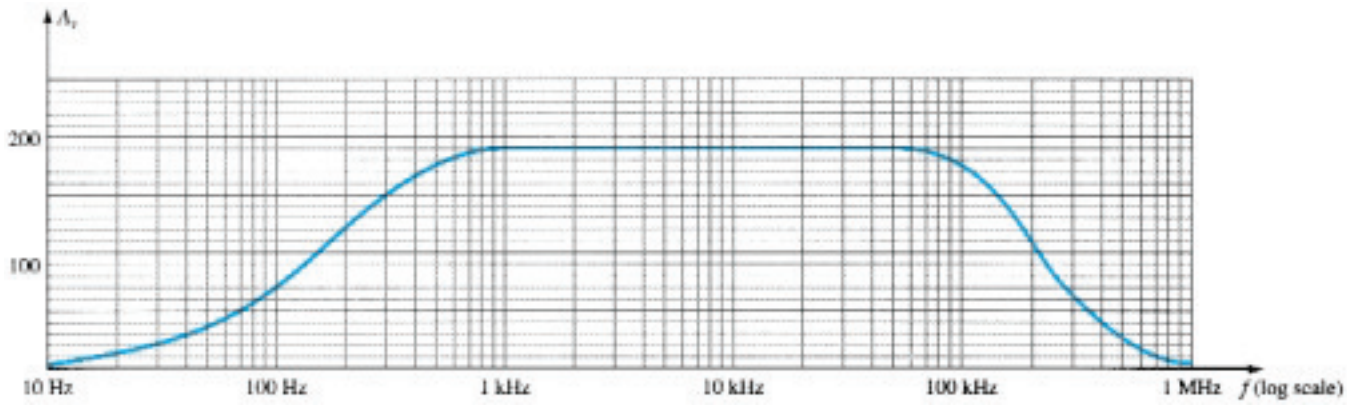


Figure 11.63 Problem 10

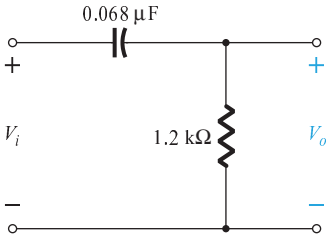


Figure 11.64 Problems 11, 12, and 32

§ 11.5 Low-Frequency Analysis—Bode Plot

11. For the network of Fig. 11.64:
(a) Determine the mathematical expression for the magnitude of the ratio V_o/V_i.
(b) Using the results of part (a), determine V_o/V_i at 100 Hz, 1 kHz, 2 kHz, 5 kHz, and 10 kHz, and plot the resulting curve for the frequency range of 100 Hz to 10 kHz. Use a log scale.
(c) Determine the break frequency.
(d) Sketch the asymptotes and locate the −3-dB point.
(e) Sketch the frequency response for V_o/V_i and compare to the results of part (b).

12. For the network of Fig. 11.64:
(a) Determine the mathematical expression for the angle by which V_o leads V_i.
(b) Determine the phase angle at f = 100 Hz, 1 kHz, 2 kHz, 5 kHz, and 10 kHz, and plot the resulting curve for the frequency range of 100 Hz to 10 kHz.
(c) Determine the break frequency.
(d) Sketch the frequency response of θ for the same frequency spectrum of part (b) and compare results.

13. (a) What frequency is 1 octave above 5 kHz?
(b) What frequency is 1 decade below 10 kHz?
(c) What frequency is 2 octaves below 20 kHz?
(d) What frequency is 2 decades above 1 kHz?

§ 11.6 Low-Frequency Response — BJT Amplifier

14. Repeat the analysis of Example 11.9 with $r_o = 40$ kΩ. What is the effect on $A_{v_{\text{mid}}}$, f_{L_S}, f_{L_C}, f_{L_E}, and the resulting cutoff frequency?

15. For the network of Fig. 11.65:
(a) Determine r_e.
(b) Find $A_{v_{mid}} = V_o/V_i$.
(c) Calculate Z_i.
(d) Find $A_{v_{Smid}} = V_o/V_s$.
(e) Determine f_{L_S}, f_{L_C}, and f_{L_E}.
(f) Determine the low cutoff frequency.
(g) Sketch the asymptotes of the Bode plot defined by the cutoff frequencies of part (e).
(h) Sketch the low-frequency response for the amplifier using the results of part (f).

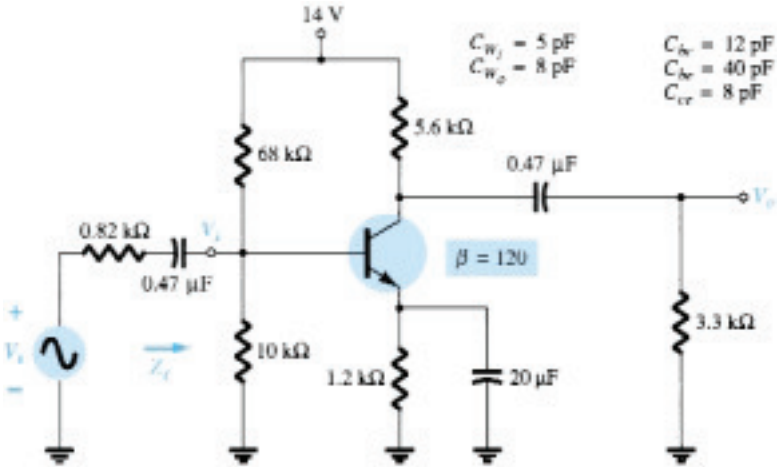


Figure 11.65 Problems 15, 22, and 33

* **16.** Repeat Problem 15 for the emitter-stabilized network of Fig. 11.66.

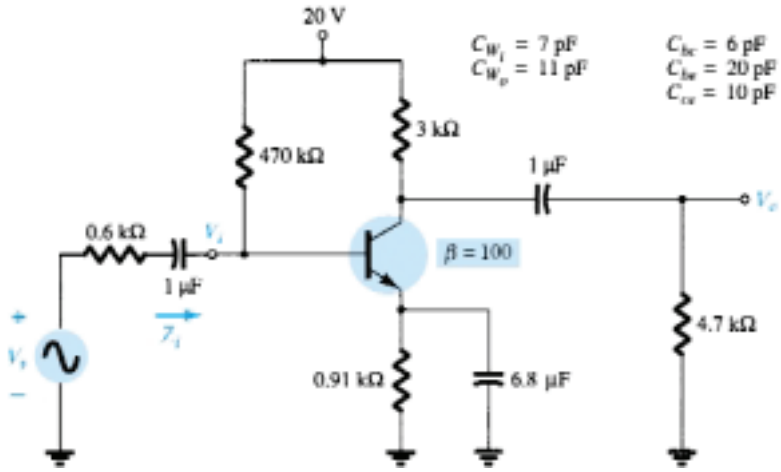


Figure 11.66 Problems 16 and 23

* **17.** Repeat Problem 15 for the emitter-follower network of Fig. 11.67.

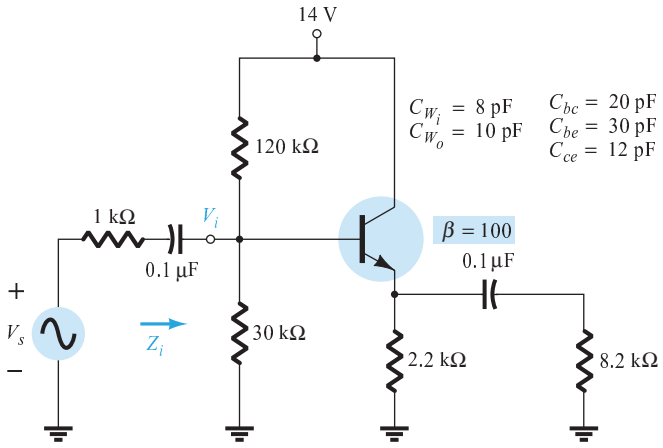


Figure 11.67 Problems 17 and 24

* **18.** Repeat Problem 15 for the common-base configuration of Fig. 11.68. Keep in mind that the common-base configuration is a noninverting network when you consider the Miller effect.

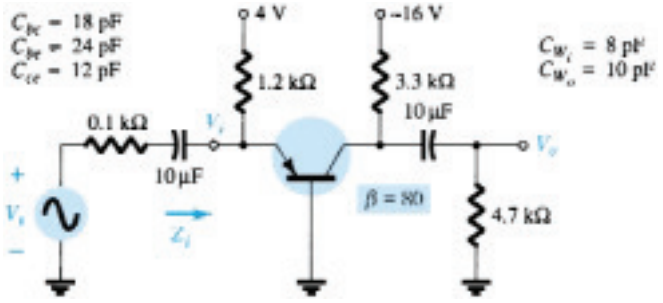


Figure 11.68 Problems 18, 25, and 34

§ 11.7 Low-Frequency Response — FET Amplifier

19. For the network of Fig. 11.69:
(a) Determine V_{GS_Q} and I_{D_Q}.
(b) Find g_{m0} and g_m.
(c) Calculate the midband gain of $A_v = V_o/V_i$.
(d) Determine Z_i.
(e) Calculate $A_{v_s} = V_o/V_s$.
(f) Determine f_{L_G}, f_{L_C}, and f_{L_S}.
(g) Determine the low cutoff frequency.
(h) Sketch the asymptotes of the Bode plot defined by part (f).
(i) Sketch the low-frequency response for the amplifier using the results of part (f).

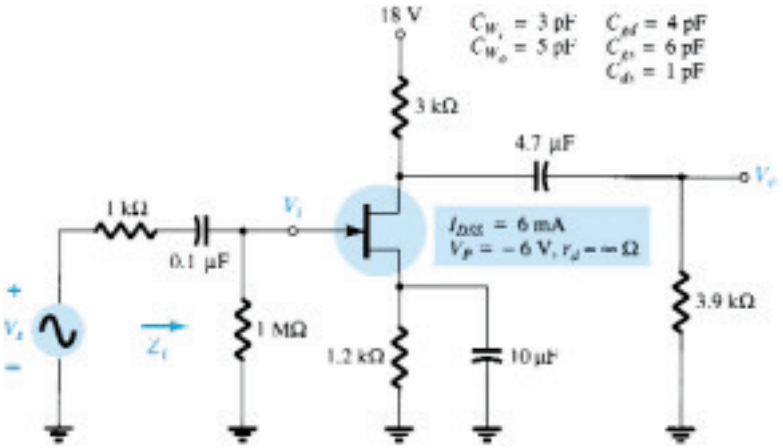


Figure 11.69 Problems 19, 20, 26, and 35

* **20.** Repeat the analysis of Problem 19 with $r_d = 100$ kΩ. Does it have an impact of any consequence on the results? If so, which elements?

* **21.** Repeat the analysis of Problem 19 for the network of Fig. 11.70. What effect did the voltage-divider configuration have on the input impedance and the gain A_{v_s} compared to the biasing arrangement of Fig. 11.69?

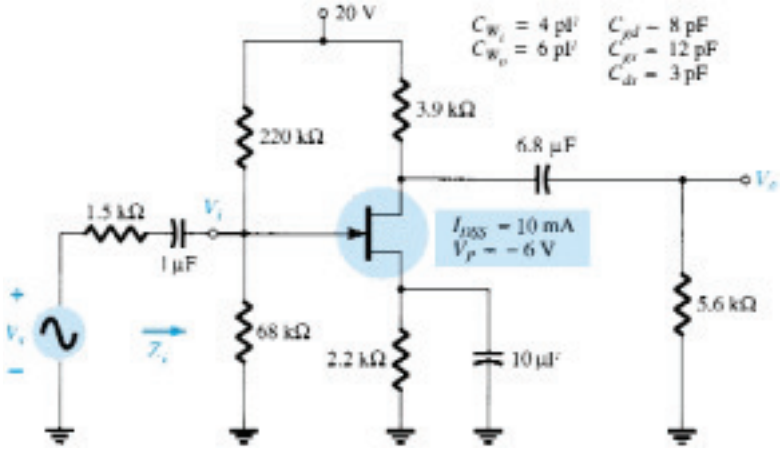


Figure 11.70 Problems 21 and 27

§ 11.9 High-Frequency Response — BJT Amplifier

22. For the network of Fig. 11.65:
(a) Determine f_{H_i} and f_{H_o}.
(b) Assuming that $C_{b'e} = C_{be}$ and $C_{b'c} = C_{bc}$, find f_β and f_T.
(c) Sketch the frequency response for the high-frequency region using a Bode plot and determine the cutoff frequency.

* **23.** Repeat the analysis of Problem 22 for the network of Fig. 11.66.

* **24.** Repeat the analysis of Problem 22 for the network of Fig. 11.67.

* **25.** Repeat the analysis of Problem 22 for the network of Fig. 11.68.

§ 11.10 High-Frequency Response — FET Amplifier

26. For the network of Fig. 11.69:
(a) Determine g_{m_0} and g_m.
(b) Find A_v and A_{v_s} in the mid-frequency range.
(c) Determine f_{H_i} and f_{H_o}.
(d) Sketch the frequency response for the high-frequency region using a Bode plot and determine the cutoff frequency.

* **27.** Repeat the analysis of Problem 26 for the network of Fig. 11.70.

§ 11.11 Multistage Frequency Effects

28. Calculate the overall voltage gain of four identical stages of an amplifier, each having a gain of 20.

29. Calculate the overall upper 3-dB frequency for a four-stage amplifier having an individual stage value of $f_2 = 2.5$ MHz.

30. A four-stage amplifier has a lower 3-dB frequency for an individual stage of $f_1 = 40$ Hz. What is the value of f_1 for this full amplifier?

§ 11.12 Square-Wave Testing

* **31.** The application of a 10-mV, 100-kHz square wave to an amplifier resulted in the output waveform of Fig. 11.71.
(a) Write the Fourier series expansion for the square wave through the ninth harmonic.
(b) Determine the bandwidth of the amplifier to the accuracy available by the waveform of Fig. 11.71.
(c) Calculate the low cutoff frequency.

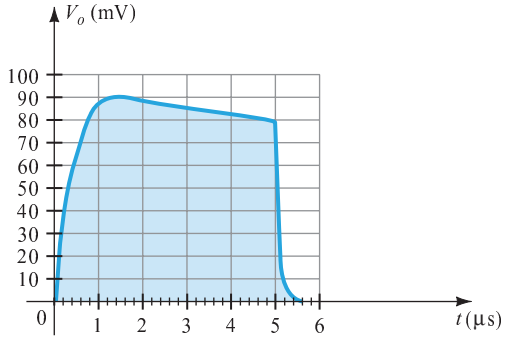


Figure 11.71 Problem 31

§ 11.13 PSpice Windows

32. Using PSpice Windows, determine the frequency response of V_o/V_i for the high-pass filter of Fig. 11.64.

33. Using PSpice Windows, determine the frequency response of V_o/V_s for the BJT amplifier of Fig. 11.65.

34. Repeat Problem 33 for the network of Fig. 11.68.

35. Repeat Problem 33 for the JFET configuration of Fig. 11.69.

*Please Note: Asterisks indicate more difficult problems.

CHAPTER

17 Linear-Digital ICs

17.1 INTRODUCTION

While there are many ICs containing only digital circuits and many that contain only linear circuits, there are a number of units that contain both linear and digital circuits. Among the linear/digital ICs are comparator circuits, digital/analog converters, interface circuits, timer circuits, voltage-controlled oscillator (VCO) circuits, and phase-locked loops (PLLs).

The comparator circuit is one to which a linear input voltage is compared to another reference voltage, the output being a digital condition representing whether the input voltage exceeded the reference voltage.

Circuits that convert digital signals into an analog or linear voltage, and those that convert a linear voltage into a digital value, are popular in aerospace equipment, automotive equipment, and compact disk (CD) players, among many others.

Interface circuits are used to enable connecting signals of different digital voltage levels, from different types of output devices, or from different impedances so that both the driver stage and the receiver stage operate properly.

Timer ICs provide linear and digital circuits to use in various timing operations, as in a car alarm, a home timer to turn lights on or off, and a circuit in electromechanical equipment to provide proper timing to match the intended unit operation. The 555 timer has long been a popular IC unit. A voltage-controlled oscillator provides an output clock signal whose frequency can be varied or adjusted by an input voltage. One popular application of a VCO is in a phase-locked loop unit, as used in various communication transmitters and receivers.

17.2 COMPARATOR UNIT OPERATION

A comparator circuit accepts input of linear voltages and provides a digital output that indicates when one input is less than or greater than the second. A basic comparator circuit can be represented as in Fig. 17.1a. The output is a digital signal that stays at a high voltage level when the noninverting (+) input is greater than the voltage at the inverting (−) input and switches to a lower voltage level when the noninverting input voltage goes below the inverting input voltage.

Figure 17.1b shows a typical connection with one input (the inverting input in this example) connected to a reference voltage, the other connected to the input signal voltage. As long as V_{in} is less than the reference voltage level of +2 V, the output remains at a low voltage level (near −10 V). When the input rises just above +2 V, the

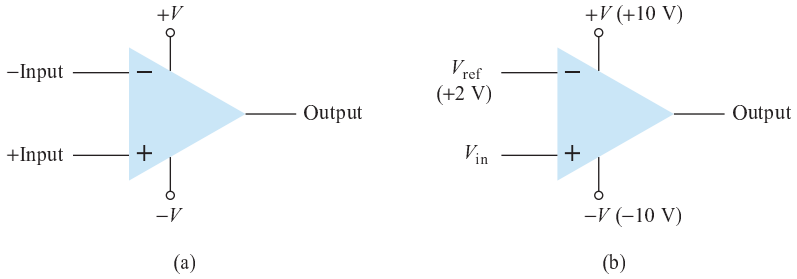


Figure 17.1 Comparator unit: (a) basic unit; (b) typical application.

output quickly switches to a high-voltage level (near +10 V). Thus the high output indicates that the input signal is greater than +2 V.

Since the internal circuit used to build a comparator contains essentially an op-amp circuit with very high voltage gain, we can examine the operation of a comparator using a 741 op-amp, as shown in Fig. 17.2. With reference input (at pin 2) set to 0 V, a sinusoidal signal applied to the noninverting input (pin 3) will cause the output to switch between its two output states, as shown in Fig. 17.2b. The input V_i going even a fraction of a millivolt above the 0-V reference level will be amplified by the very high voltage gain (typically over 100,000) so that the output rises to its positive output saturation level and remains there while the input stays above $V_{ref} = 0$ V. When the input drops just below the 0-V reference level, the output is driven to its lower saturation level and stays there while the input remains below $V_{ref} = 0$ V. Figure 17.2b clearly shows that the input signal is linear while the output is digital.

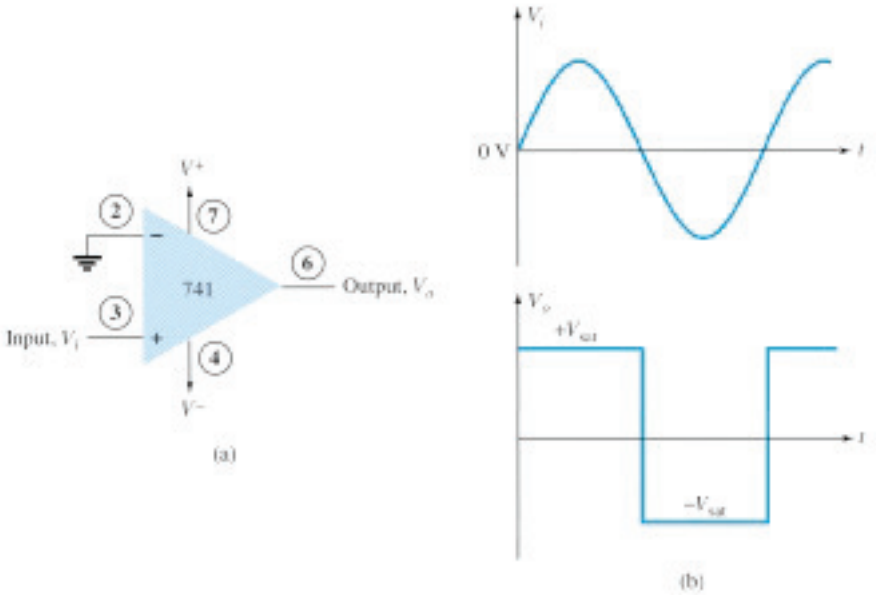


Figure 17.2 Operation of 741 op-amp as comparator.

In general use, the reference level need not be 0 V but can be any desired positive or negative voltage. Also, the reference voltage may be connected to either plus or minus input and the input signal then applied to the other input.

Use of Op-Amp as Comparator

Figure 17.3a shows a circuit operating with a positive reference voltage connected to the minus input and the output connected to an indicator LED. The reference voltage level is set at

$$V_{ref} = \frac{10\ \text{k}\Omega}{10\ \text{k}\Omega + 10\ \text{k}\Omega}(+12\ \text{V}) = +6\ \text{V}$$

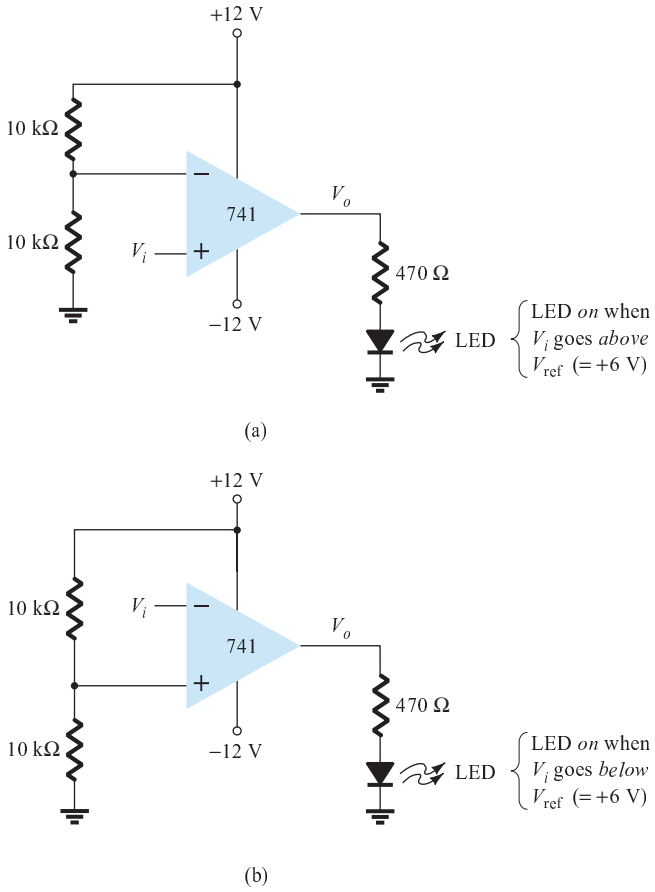


Figure 17.3 A 741 op-amp used as a comparator.

Since the reference voltage is connected to the inverting input, the output will switch to its positive saturation level when the input, V_i, goes more positive than the +6-V reference voltage level. The output, V_o, then drives the LED on as an indication that the input is more positive than the reference level.

As an alternative connection, the reference voltage could be connected to the noninverting input as shown in Fig. 17.3b. With this connection, the input signal going below the reference level would cause the output to drive the LED on. The LED can thus be made to go on when the input signal goes above or below the reference level, depending on which input is connected as signal input and which as reference input.

Using Comparator IC Units

While op-amps can be used as comparator circuits, separate IC comparator units are more suitable. Some of the improvements built into a comparator IC are faster switching between the two output levels, built-in noise immunity to prevent the output from oscillating when the input passes by the reference level, and outputs capable of directly driving a variety of loads. A few popular IC comparators are covered next, describing their pin connections and how they may be used.

311 COMPARATOR

The 311 voltage comparator shown in Fig. 17.4 contains a comparator circuit that can operate as well from dual power supplies of ±15 V as from a single +5-V supply (as used in digital logic circuits). The output can provide a voltage at one of two distinct levels or can be used to drive a lamp or a relay. Notice that the output is taken

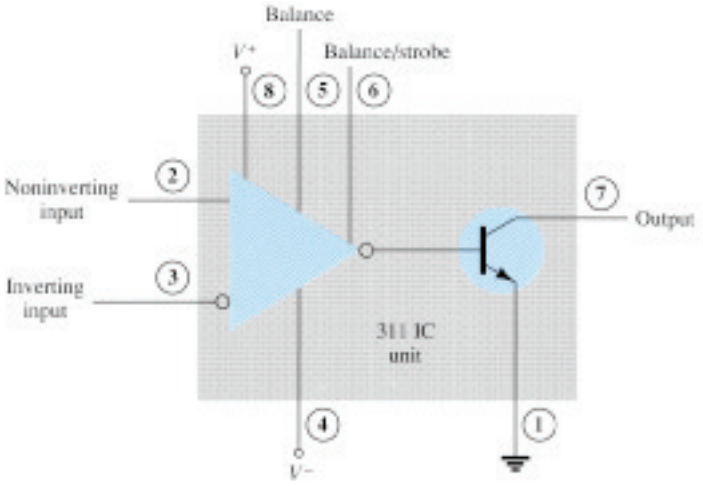


Figure 17.4 A 311 comparator (eight-pin DIP unit).

from a bipolar transistor to allow driving a variety of loads. The unit also has balance and strobe inputs, the strobe input allowing gating of the output. A few examples will show how this comparator unit can be used in some common applications.

A zero-crossing detector that senses (detects) the input voltage crossing through 0 V is shown using the 311 IC in Fig. 17.5. The inverting input is connected to ground (the reference voltage). The input signal going positive drives the output transistor on, with the output then going low (−10 V in this case). The input signal going negative (below 0 V) will drive the output transistor off, the output then going high (to +10 V). The output is thus an indication of whether the input is above or below 0 V. When the input is any positive voltage, the output is low, while any negative voltage will result in the output going to a high voltage level.

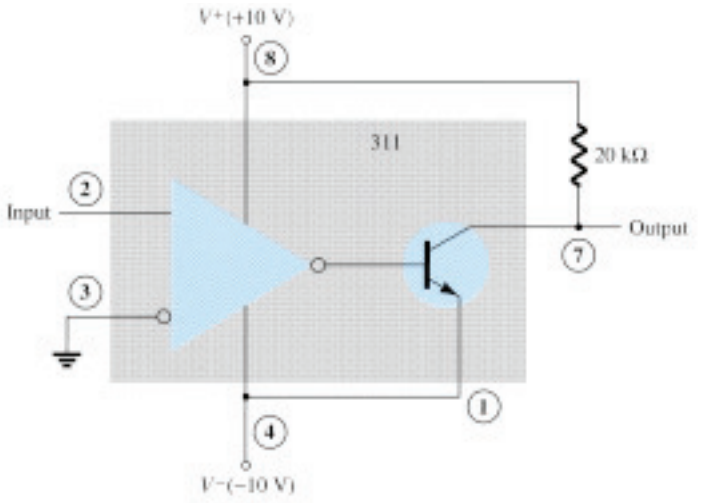


Figure 17.5 Zero-crossing detector using a 311 IC.

Figure 17.6 shows how a 311 comparator can be used with strobing. In this example, the output will go high when the input goes above the reference level—but only if the TTL strobe input is off (or 0 V). If the TTL strobe input goes high, it drives the 311 strobe input at pin 6 low, causing the output to remain in the off state (with output high) regardless of the input signal. In effect, the output remains high

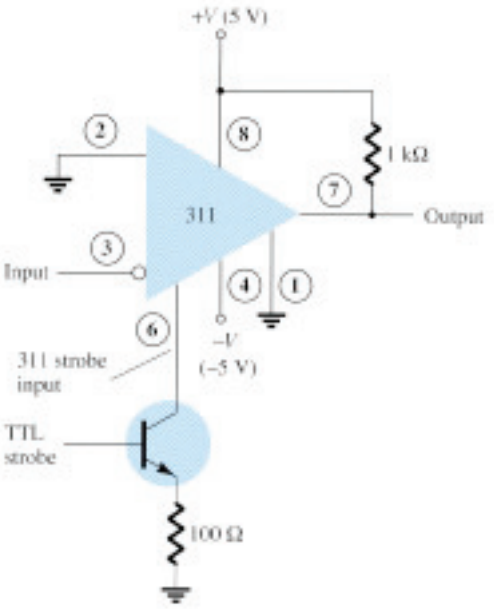


Figure 17.6 Operation of a 311 comparator with strobe input.

unless strobed. If strobed, the output then acts normally, switching from high to low depending on the input signal level. In operation, the comparator output will respond to the input signal only during the time the strobe signal allows such operation.

Figure 17.7 shows the comparator output driving a relay. When the input goes below 0 V, driving the output low, the relay is activated, closing the normally open (N.O.) contacts at that time. These contacts can then be connected to operate a large variety of devices. For example, a buzzer or bell wired to the contacts can be driven on whenever the input voltage drops below 0 V. As long as the voltage is present at the input terminal, the buzzer will remain off.

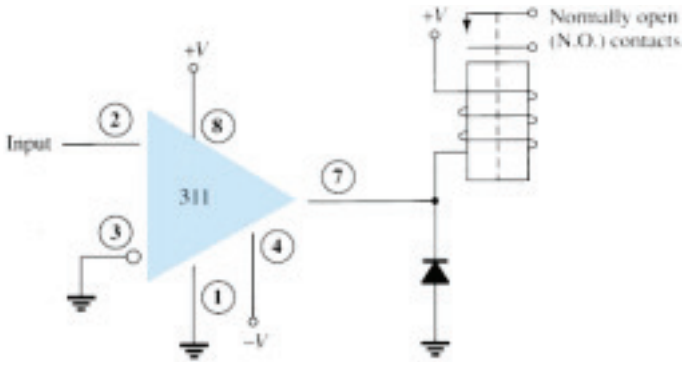


Figure 17.7 Operation of a 311 comparator with relay output.

339 COMPARATOR

The 339 IC is a quad comparator containing four independent voltage comparator circuits connected to external pins as shown in Fig. 17.8. Each comparator has inverting and noninverting inputs and a single output. The supply voltage applied to a pair of pins powers all four comparators. Even if one wishes to use one comparator, all four will be drawing power.

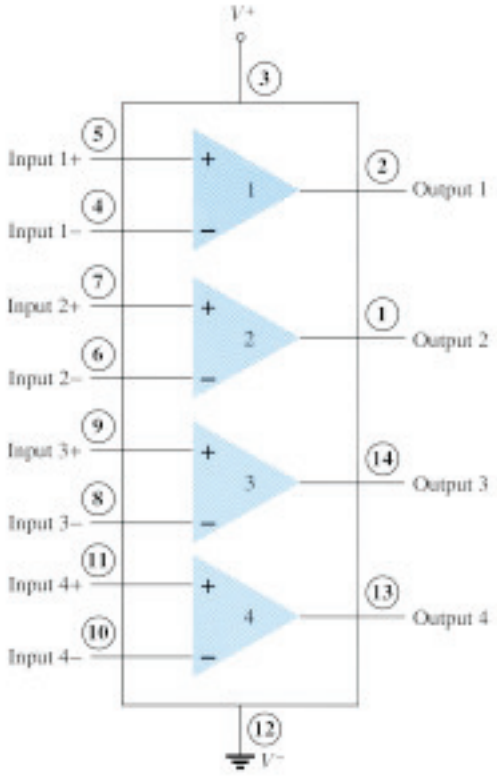


Figure 17.8 Quad comparator IC (339).

To see how these comparator circuits can be used, Fig. 17.9 shows one of the 339 comparator circuits connected as a zero-crossing detector. Whenever the input signal goes above 0 V, the output switches to V^+. The input switches to V^- only when the input goes below 0 V.

A reference level other than 0 V can also be used, and either input terminal could be used as the reference, the other terminal then being connected to the input signal. The operation of one of the comparator circuits is described next.

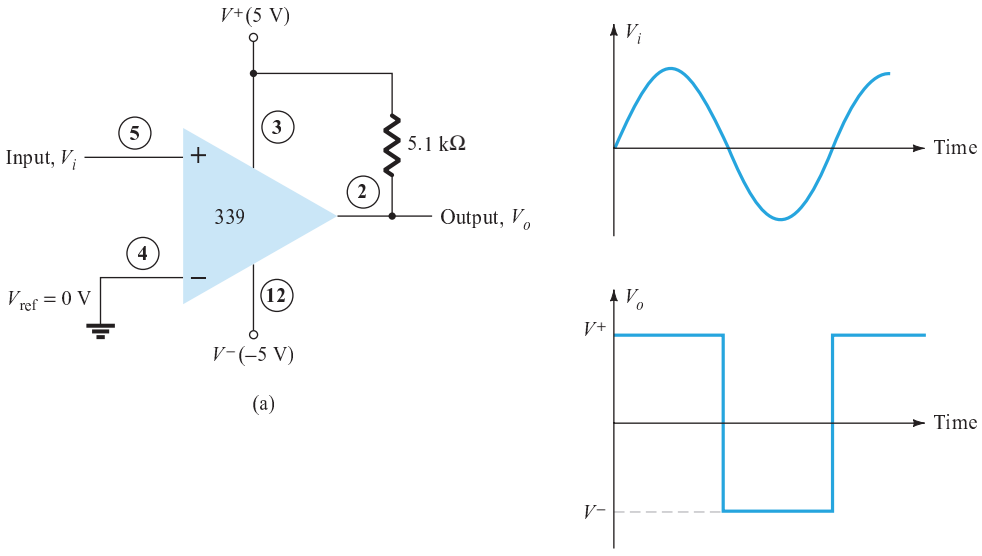


Figure 17.9 Operation of one 339 comparator circuit as a zero-crossing detector.

The differential input voltage (difference voltage across input terminals) going positive drives the output transistor off (open circuit), while a negative differential input voltage drives the output transistor on—the output then at the supply low level.

If the negative input is set at a reference level V_{ref}, the positive input goes above V_{ref} and results in a positive differential input with output driven to the open-circuit state. When the noninverting input goes below V_{ref}, resulting in a negative differential input, the output will be driven to V^-.

If the positive input is set at the reference level, the inverting input going below V_{ref} results in the output open circuit while the inverting input going above V_{ref} results in the output at V^-. This operation is summarized in Fig. 17.10.

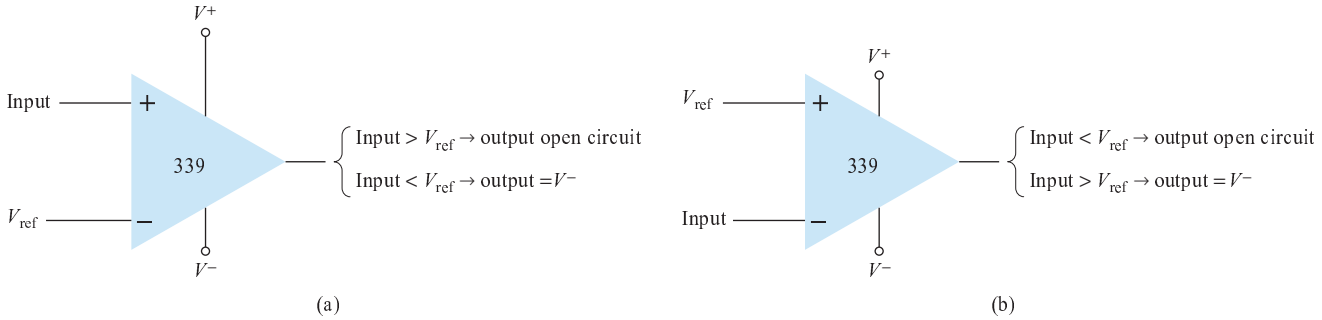


Figure 17.10 Operation of a 339 comparator circuit with reference input: (a) minus input; (b) plus input.

Since the output of one of these comparator circuits is from an open-circuit collector, applications in which the outputs from more than one circuit can be wire-ORed are possible. Figure 17.11 shows two comparator circuits connected with common output and also with common input. Comparator 1 has a +5-V reference voltage in-

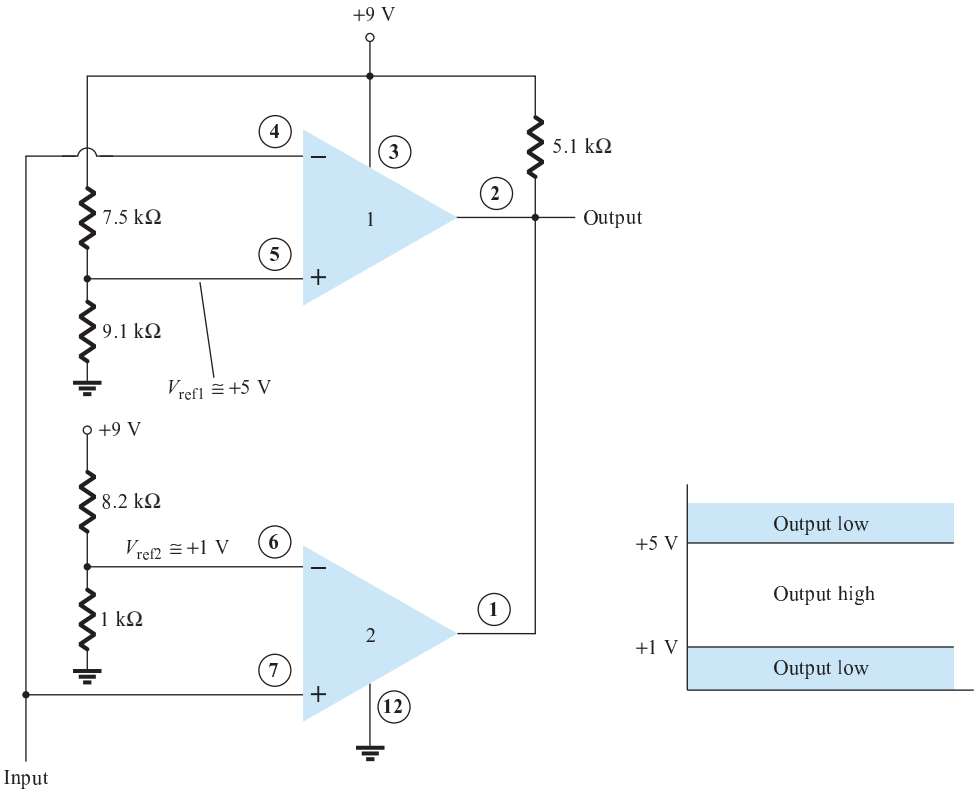


Figure 17.11 Operation of two 339 comparator circuits as a window detector.

put connected to the noninverting input. The output will be driven low by comparator 1 when the input signal goes above +5 V. Comparator 2 has a reference voltage of +1 V connected to the inverting input. The output of comparator 2 will be driven low when the input signal goes below +1 V. In total, the output will go low whenever the input is below +1 V or above +5 V, as shown in Fig. 17.11, the overall operation being that of a voltage window detector. The high output indicates that the input is within a voltage window of +1 to +5 V (these values being set by the reference voltage levels used).

17.3 DIGITAL–ANALOG CONVERTERS

Many voltages and currents in electronics vary continuously over some range of values. In digital circuitry the signals are at either one of two levels, representing the binary values of 1 or zero. An analog–digital converter (ADC) obtains a digital value representing an input analog voltage, while a digital–analog converter (DAC) changes a digital value back into an analog voltage.

Digital-to-Analog Conversion

LADDER NETWORK CONVERSION

Digital-to-analog conversion can be achieved using a number of different methods. One popular scheme uses a network of resistors, called a *ladder network*. A ladder network accepts inputs of binary values at, typically, 0 V or V_{ref} and provides an output voltage proportional to the binary input value. Figure 17.12a shows a ladder network with four input voltages, representing 4 bits of digital data and a dc voltage output. The output voltage is proportional to the digital input value as given by the relation

$$V_o = \frac{D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + D_3 \times 2^3}{2^4} V_{\text{ref}} \tag{17.1}$$

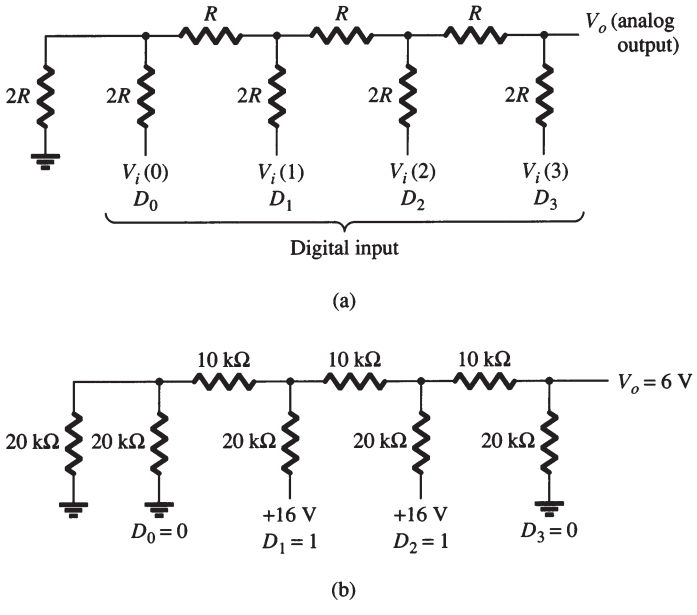


Figure 17.12 Four-stage ladder network used as a DAC: (a) basic circuit; (b) circuit example with 0110 input.

In the example shown in Fig. 17.12b, the output voltage resulting should be

$$V_o = \frac{0 \times 1 + 1 \times 2 + 1 \times 4 + 0 \times 8}{16} (16 \text{ V}) = 6 \text{ V}$$

Therefore, 0110_2, digital, converts to 6 V, analog.

The function of the ladder network is to convert the 16 possible binary values from 0000 to 1111 into one of 16 voltage levels in steps of $V_{\text{ref}}/16$. Using more sections of ladder allows having more binary inputs and greater quantization for each step. For example, a 10-stage ladder network could extend the number of voltage steps or the voltage resolution to $V_{\text{ref}}/2^{10}$ or $V_{\text{ref}}/1024$. A reference voltage of $V_{\text{ref}} = 10$ V would then provide output voltage steps of 10 V/1024 or approximately 10 mV. More ladder stages provide greater voltage resolution. In general, the voltage resolution for n ladder stages is

$$\boxed{\frac{V_{\text{ref}}}{2^n}} \tag{17.2}$$

Figure 17.13 shows a block diagram of a typical DAC using a ladder network. The ladder network, referred in the diagram as an *R-2R ladder,* is sandwiched between the reference current supply and current switches connected to each binary input, the resulting output current proportional to the input binary value. The binary input turns on selected legs of the ladder, the output current being a weighted summing of the reference current. Connecting the output current through a resistor will produce an analog voltage, if desired.

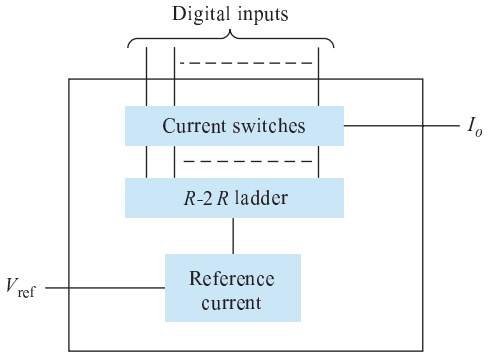


Figure 17.13 DAC IC using R-2R ladder network.

Analog-to-Digital Conversion

DUAL-SLOPE CONVERSION

A popular method for converting an analog voltage into a digital value is the dual-slope method. Figure 17.14a shows a block diagram of the basic dual-slope converter. The analog voltage to be converted is applied through an electronic switch to an integrator or ramp-generator circuit (essentially a constant current charging a capacitor to produce a linear ramp voltage). The digital output is obtained from a counter operated during both positive and negative slope intervals of the integrator.

The method of conversion proceeds as follows. For a fixed time interval (usually the full count range of the counter), the analog voltage connected to the integrator raises the voltage at the comparator input to some positive level. Figure 17.14b shows that at the end of the fixed time interval the voltage from the integrator is greater for the larger input voltage. At the end of the fixed count interval, the count is set to zero and the electronic switch connects the integrator to a reference or fixed input voltage.

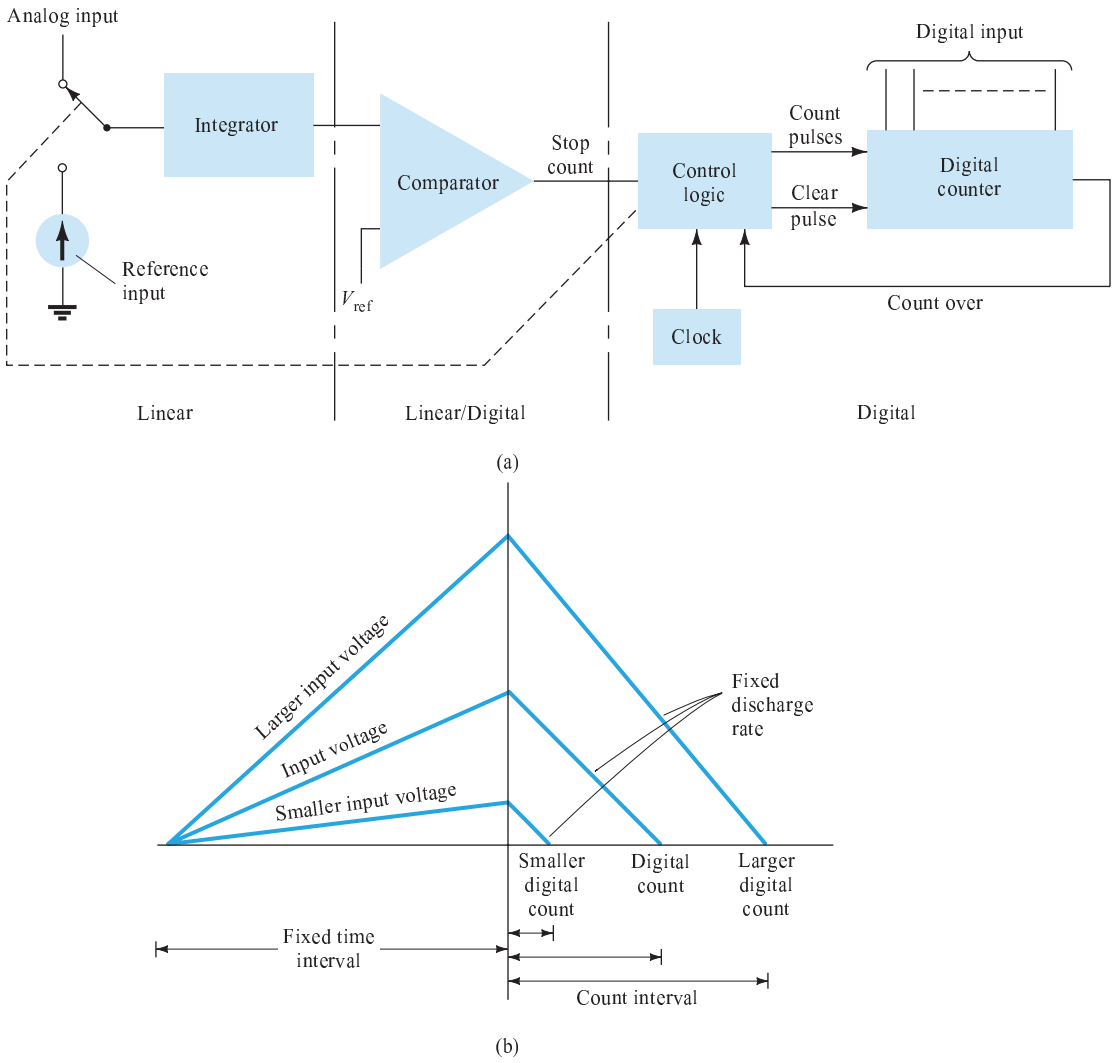


Figure 17.14 Analog-to-digital conversion using dual-slope method: (a) logic diagram; (b) waveform.

The integrator output (or capacitor input) then decreases at a fixed rate. The counter advances during this time, while the integrator's output decreases at a fixed rate until it drops below the comparator reference voltage, at which time the control logic receives a signal (the comparator output) to stop the count. The digital value stored in the counter is then the digital output of the converter.

Using the same clock and integrator to perform the conversion during positive and negative slope intervals tends to compensate for clock frequency drift and integrator accuracy limitations. Setting the reference input value and clock rate can scale the counter output as desired. The counter can be a binary, BCD, or other form of digital counter, if desired.

LADDER-NETWORK CONVERSION

Another popular method of analog-to-digital conversion uses a ladder network along with counter and comparator circuits (see Fig. 17.15). A digital counter advances from a zero count while a ladder network driven by the counter outputs a staircase voltage, as shown in Fig. 17.15b, which increases one voltage increment for each count step. A comparator circuit, receiving both staircase voltage and analog input

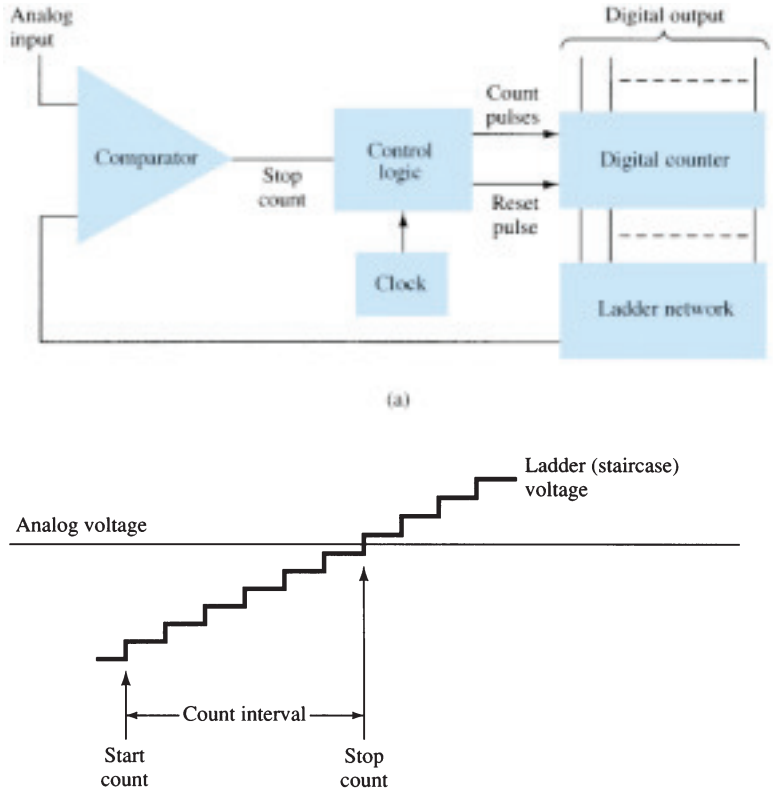


Figure 17.15 Analog-to-digital conversion using ladder network: (a) logic diagram; (b) waveform.

voltage, provides a signal to stop the count when the staircase voltage rises above the input voltage. The counter value at that time is the digital output.

The amount of voltage change stepped by the staircase signal depends on the number of count bits used. A 12-stage counter operating a 12-stage ladder network using a reference voltage of 10 V would step each count by a voltage of

$$\frac{V_{\text{ref}}}{2^{12}} = \frac{10\text{ V}}{4096} = 2.4\text{ mV}$$

This would result in a conversion resolution of 2.4 mV. The clock rate of the counter would affect the time required to carry out a conversion. A clock rate of 1 MHz operating a 12-stage counter would need a maximum conversion time of

$$4096 \times 1\ \mu\text{s} = 4096\ \mu\text{s} \approx 4.1\text{ ms}$$

The minimum number of conversions that could be carried out each second would then be

$$\text{number of conversions} = 1/4.1\text{ ms} \approx 244\text{ conversions/second}$$

Since on the average, with some conversions requiring little count time and others near maximum count time, a conversion time of 4.1 ms/2 = 2.05 ms would be needed, and the average number of conversions would be $2 \times 244 = 488$ conversions/second. A slower clock rate would result in fewer conversions per second. A converter using fewer count stages (and less conversion resolution) would carry out more conversions per second. The conversion accuracy depends on the accuracy of the comparator.

17.4 TIMER IC UNIT OPERATION

Another popular analog–digital integrated circuit is the versatile 555 timer. The IC is made of a combination of linear comparators and digital flip-flops as described in Fig. 17.16. The entire circuit is usually housed in an 8-pin package as specified in Fig. 17.16. A series connection of three resistors sets the reference voltage levels to the two comparators at $2V_{CC}/3$ and $V_{CC}/3$, the output of these comparators setting or resetting the flip-flop unit. The output of the flip-flop circuit is then brought out through an output amplifier stage. The flip-flop circuit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor.

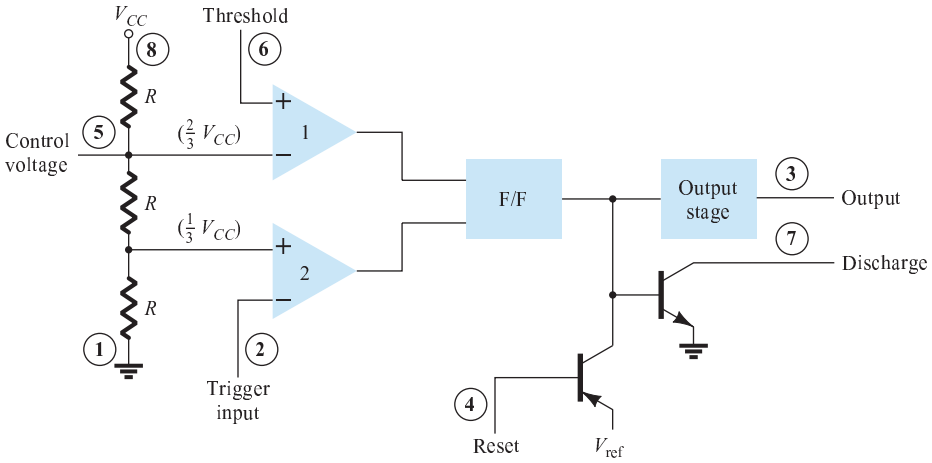


Figure 17.16 Details of 555 timer IC.

Astable Operation

One popular application of the 555 timer IC is as an astable multivibrator or clock circuit. The following analysis of the operation of the 555 as an astable circuit includes details of the different parts of the unit and how the various inputs and outputs are utilized. Figure 17.17 shows an astable circuit built using an external resistor and capacitor to set the timing interval of the output signal.

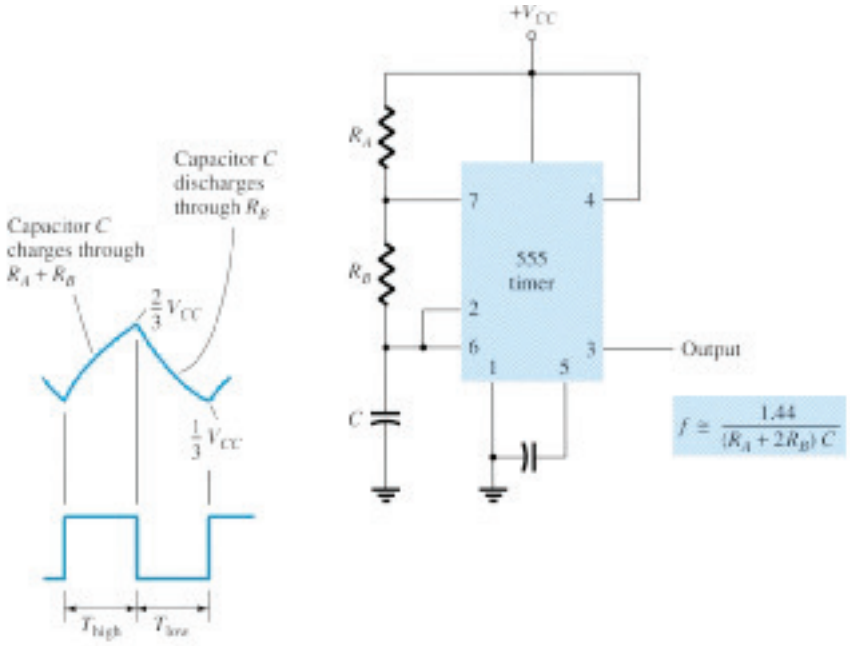


Figure 17.17 Astable multivibrator using 555 IC.

Capacitor C charges toward V_{CC} through external resistors R_A and R_B. Referring to Fig. 17.17, the capacitor voltage rises until it goes above $2V_{CC}/3$. This voltage is the threshold voltage at pin 6, which drives comparator 1 to trigger the flip-flop so that the output at pin 3 goes low. In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor R_B. The capacitor voltage then decreases until it drops below the trigger level ($V_{CC}/3$). The flip-flop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors R_A and R_B toward V_{CC}.

Figure 17.18a shows the capacitor and output waveforms resulting from the astable circuit. Calculation of the time intervals during which the output is high and low can be made using the relations

$$T_{\text{high}} \approx 0.7(R_A + R_B)C \tag{17.3}$$

$$T_{\text{low}} \approx 0.7R_BC \tag{17.4}$$

The total period is

$$T = \text{period} = T_{\text{high}} + T_{\text{low}} \tag{17.5}$$

The frequency of the astable circuit is then calculated using*

$$f = \frac{1}{T} \approx \frac{1.44}{(R_A + 2R_B)C} \tag{17.6}$$

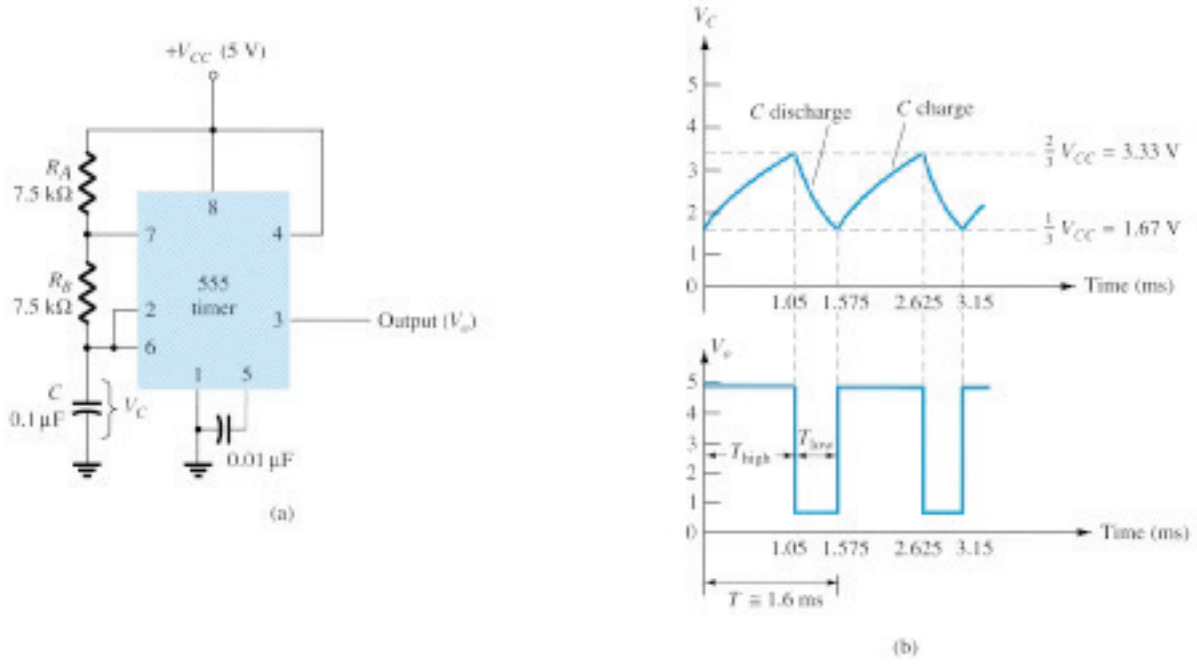


Figure 17.18 Astable multivibrator for Example 17.1: (a) circuit; (b) waveforms.

*The period can be directly calculated from

$$T = 0.693(R_A + 2R_B)C \approx 0.7(R_A + 2R_B)C$$

and the frequency from

$$f \approx \frac{1.44}{(R_A + 2R_B)C}$$

EXAMPLE 17.1

Determine the frequency and draw the output waveform for the circuit of Fig. 17.18a.

Solution

Using Eqs. (17.3) through (17.6) yields

$$T_{\text{high}} = 0.7(R_A + R_B)C = 0.7(7.5 \times 10^3 + 7.5 \times 10^3)(0.1 \times 10^{-6})$$

$$= 1.05 \text{ ms}$$

$$T_{\text{low}} = 0.7R_BC = 0.7(7.5 \times 10^3)(0.1 \times 10^{-6}) = 0.525 \text{ ms}$$

$$T = T_{\text{high}} + T_{\text{low}} = 1.05 \text{ ms} + 0.525 \text{ ms} = 1.575 \text{ ms}$$

$$f = \frac{1}{T} = \frac{1}{1.575 \times 10^{-3}} \approx \mathbf{635 \text{ Hz}}$$

The waveforms are drawn in Fig. 17.18b.

Monostable Operation

The 555 timer can also be used as a one-shot or monostable multivibrator circuit, as shown in Fig. 17.19. When the trigger input signal goes negative, it triggers the one-shot, with output at pin 3 then going high for a time period

$$T_{\text{high}} = 1.1R_AC \tag{17.7}$$

Referring back to Fig. 17.16, the negative edge of the trigger input causes comparator 2 to trigger the flip-flop, with the output at pin 3 going high. Capacitor C charges toward V_{CC} through resistor R_A. During the charge interval, the output remains high. When the voltage across the capacitor reaches the threshold level of $2V_{CC}/3$, comparator 1 triggers the flip-flop, with output going low. The discharge transistor also goes low, causing the capacitor to remain at near 0 V until triggered again.

Figure 17.19b shows the input trigger signal and the resulting output waveform for the 555 timer operated as a one-shot. Time periods for this circuit can range from microseconds to many seconds, making this IC useful for a range of applications.

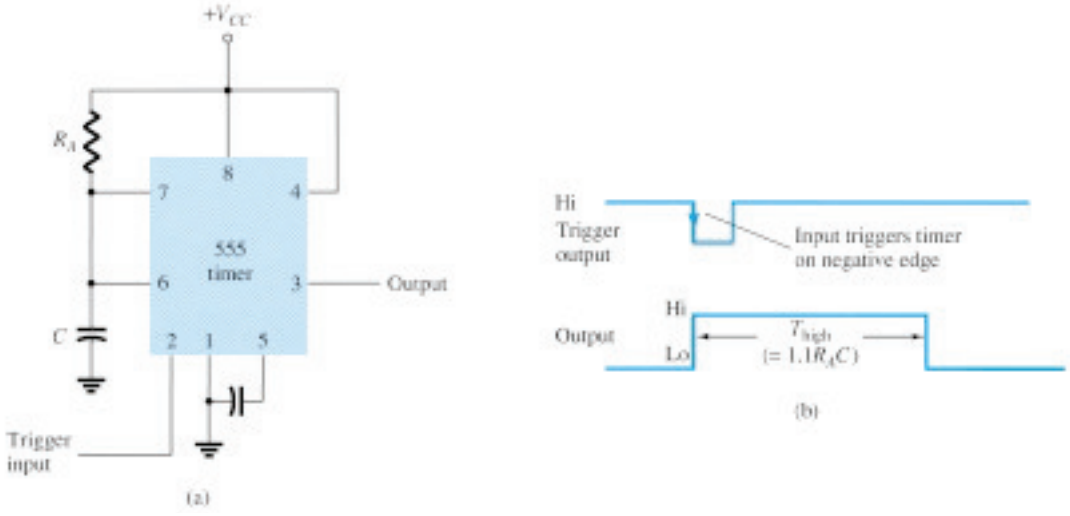


Figure 17.19 Operation of 555 timer as one-shot: (a) circuit; (b) waveforms.

Determine the period of the output waveform for the circuit of Fig. 17.20 when triggered by a negative pulse.

EXAMPLE 17.2

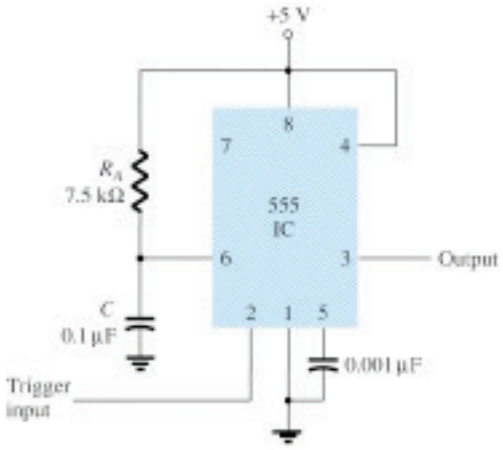


Figure 17.20 Monostable circuit for Example 17.2.

Solution

Using Eq. (17.7), we obtain

$$T_{\text{high}} = 1.1R_AC = 1.1(7.5 \times 10^3)(0.1 \times 10^{-6}) = \mathbf{0.825\ ms}$$

17.5 VOLTAGE-CONTROLLED OSCILLATOR

A voltage-controlled oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by a dc voltage. An example of a VCO is the 566 IC unit, which contains circuitry to generate both square-wave and triangular-wave signals whose frequency is set by an external resistor and capacitor and then varied by an applied dc voltage. Figure 17.21a shows that the 566 contains current sources to charge and discharge an external capacitor C_1 at a rate set by external resistor R_1 and the modulating dc input voltage. A Schmitt trigger circuit is used to switch the current sources between charging and discharging the capacitor, and the triangular voltage developed across the capacitor and square wave from the Schmitt trigger are provided as outputs through buffer amplifiers.

Figure 17.21b shows the pin connection of the 566 unit and a summary of formula and value limitations. The oscillator can be programmed over a 10-to-1 frequency range by proper selection of an external resistor and capacitor, and then modulated over a 10-to-1 frequency range by a control voltage, V_C.

A free-running or center-operating frequency, f_o, can be calculated from

$$f_o = \frac{2}{R_1C_1}\left(\frac{V^+ - V_C}{V^+}\right) \tag{17.8}$$

with the following practical circuit value restrictions:

1. R_1 should be within the range $2\ \text{k}\Omega \le R_1 \le 20\ \text{k}\Omega$.
2. V_C should be within range $\frac{3}{4}V^+ \le V_C \le V^+$.

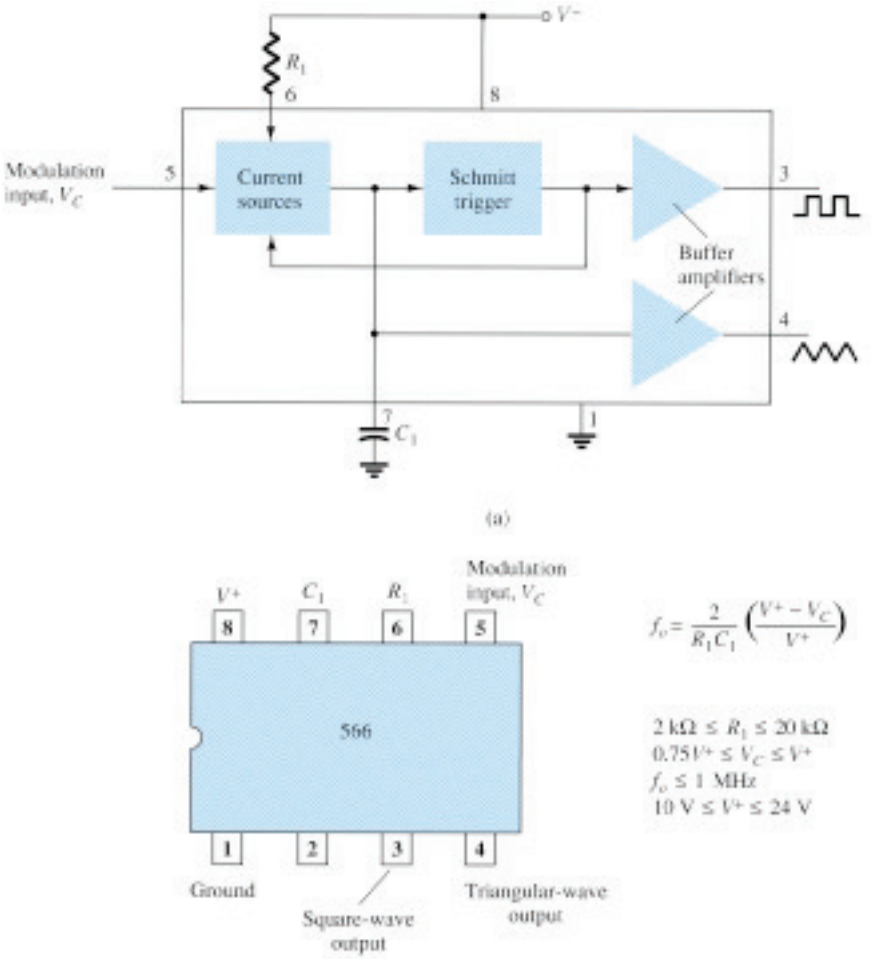


Figure 17.21 A 566 function generator: (a) block diagram; (b) pin configuration and summary of operating data.

3. f_o should be below 1 MHz.
4. V^+ should range between 10 V and 24 V.

Figure 17.22 shows an example in which the 566 function generator is used to provide both square-wave and triangular-wave signals at a fixed frequency set by R_1, C_1, and V_C. A resistor divider R_2 and R_3 sets the dc modulating voltage at a fixed value

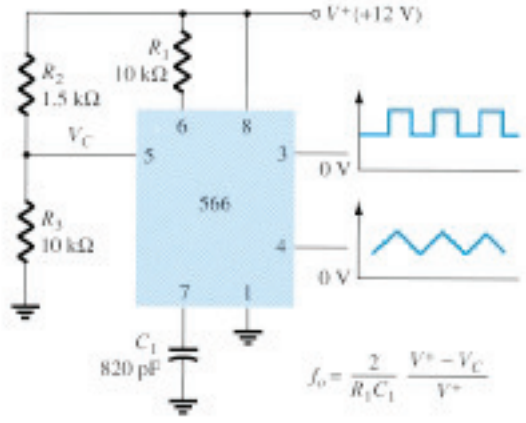


Figure 17.22 Connection of 566 VCO unit.

$$V_C = \frac{R_3}{R_2 + R_3} V^+ = \frac{10\ \text{k}\Omega}{1.5\ \text{k}\Omega + 10\ \text{k}\Omega}(12\ \text{V}) = 10.4\ \text{V}$$

(which falls properly in the voltage range $0.75V^+ = 9$ V and $V^+ = 12$ V). Using Eq. (17.8) yields

$$f_o = \frac{2}{(10 \times 10^3)(820 \times 10^{-12})}\left(\frac{12 - 10.4}{12}\right) \approx 32.5\ \text{kHz}$$

The circuit of Fig. 17.23 shows how the output square-wave frequency can be adjusted using the input voltage, V_C, to vary the signal frequency. Potentiometer R_3 allows varying V_C from about 9 V to near 12 V, over the full 10-to-1 frequency range. With the potentiometer wiper set at the top, the control voltage is

$$V_C = \frac{R_3 + R_4}{R_2 + R_3 + R_4}(V^+) = \frac{5\ \text{k}\Omega + 18\ \text{k}\Omega}{510\ \Omega + 5\ \text{k}\Omega + 18\ \text{k}\Omega}(+12\ \text{V}) = 11.74\ \text{V}$$

resulting in a lower output frequency of

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 11.74}{12}\right) \approx 19.7\ \text{kHz}$$

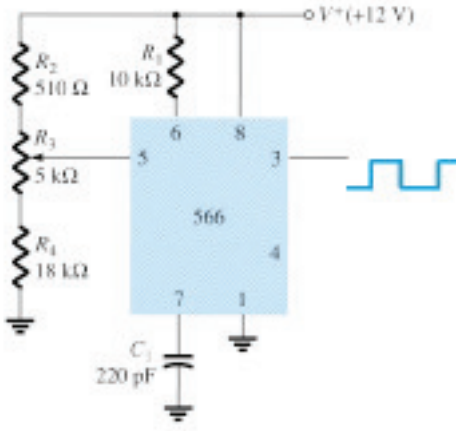


Figure 17.23 Connection of 566 as a VCO unit.

With the wiper arm of R_3 set at the bottom, the control voltage is

$$V_C = \frac{R_4}{R_2 + R_3 + R_4}(V^+) = \frac{18\ \text{k}\Omega}{510\ \Omega + 5\ \text{k}\Omega + 18\ \text{k}\Omega}(+12\ \text{V}) = 9.19\ \text{V}$$

resulting in an upper frequency of

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 9.19}{12}\right) \approx 212.9\ \text{kHz}$$

The frequency of the output square wave can then be varied using potentiometer R_3 over a frequency range of at least 10 to 1.

Rather than varying a potentiometer setting to change the value of V_C, an input modulating voltage, V_{in}, can be applied as shown in Fig. 17.24. The voltage divider sets V_C at about 10.4 V. An input ac voltage of about 1.4 V peak can drive V_C around the bias point between voltages of 9 and 11.8 V, causing the output frequency to vary over about a 10-to-1 range. The input signal V_{in} thus frequency-modulates the output voltage around the center frequency set by the bias value of $V_C = 10.4$ V ($f_o = 121.2$ kHz).

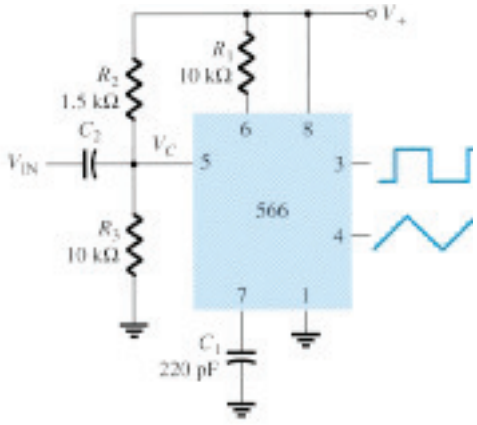


Figure 17.24 Operation of VCO with frequency-modulating input.

17.6 PHASE-LOCKED LOOP

A phase-locked loop (PLL) is an electronic circuit that consists of a phase detector, a low-pass filter, and a voltage-controlled oscillator connected as shown in Fig. 17.25. Common applications of a PLL include: (1) frequency synthesizers that provide multiples of a reference signal frequency [e.g., the carrier frequency for the multiple channels of a citizens' band (CB) unit or marine-radio-band unit can be generated using a single-crystal-controlled frequency and its multiples generated using a PLL]; (2) FM demodulation networks for FM operation with excellent linearity between the input signal frequency and the PLL output voltage; (3) demodulation of the two data transmission or carrier frequencies in digital-data transmission used in frequency-shift keying (FSK) operation; and (4) a wide variety of areas including modems, telemetry receivers and transmitters, tone decoders, AM detectors, and tracking filters.

An input signal, V_i, and that from a VCO, V_o, are compared by a phase comparator (refer to Fig. 17.25) providing an output voltage, V_e, that represents the phase difference between the two signals. This voltage is then fed to a low-pass filter that pro-

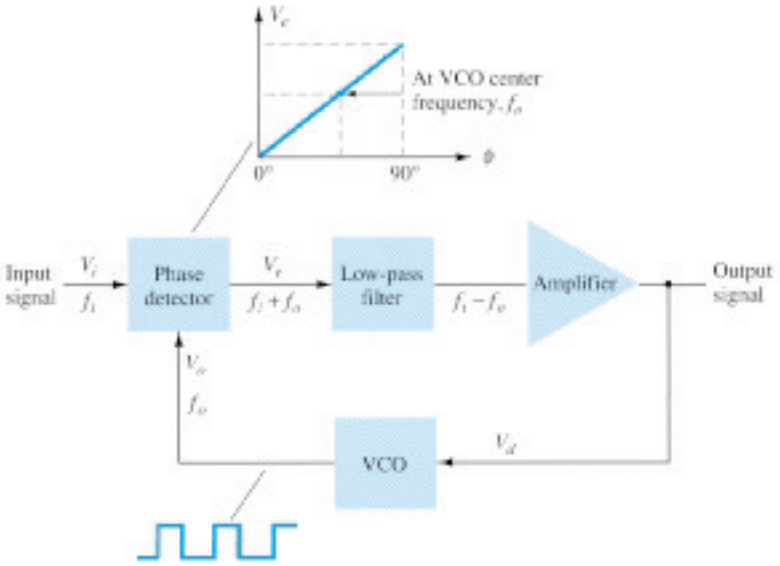


Figure 17.25 Block diagram of basic phase-locked loop (PLL).

vides an output voltage (amplified if necessary) that can be taken as the output voltage from the PLL and is used internally as the voltage to modulate the VCO's frequency. The closed-loop operation of the circuit is to maintain the VCO frequency locked to that of the input signal frequency.

Basic PLL Operation

The basic operation of a PLL circuit can be explained using the circuit of Fig. 17.25 as reference. We will first consider the operation of the various circuits in the phase-locked loop when the loop is operating in lock (the input signal frequency and the VCO frequency are the same). When the input signal frequency is the same as that from the VCO to the comparator, the voltage, V_d, taken as output is the value needed to hold the VCO in lock with the input signal. The VCO then provides output of a fixed-amplitude square-wave signal at the frequency of the input. Best operation is obtained if the VCO center frequency, f_o, is set with the dc bias voltage midway in its linear operating range. The amplifier allows this adjustment in dc voltage from that obtained as output of the filter circuit. When the loop is in lock, the two signals to the comparator are of the same frequency, although not necessarily in phase. A fixed phase difference between the two signals to the comparator results in a fixed dc voltage to the VCO. Changes in the input signal frequency then result in change in the dc voltage to the VCO. Within a capture-and-lock frequency range, the dc voltage will drive the VCO frequency to match that of the input.

While the loop is trying to achieve lock, the output of the phase comparator contains frequency components at the sum and difference of the signals compared. A low-pass filter passes only the lower-frequency component of the signal so that the loop can obtain lock between input and VCO signals.

Owing to the limited operating range of the VCO and the feedback connection of the PLL circuit, there are two important frequency bands specified for a PLL. The capture range of a PLL is the frequency range centered about the VCO free-running frequency, f_o, over which the loop can acquire lock with the input signal. Once the PLL has achieved capture, it can maintain lock with the input signal over a somewhat wider frequency range called the *lock range.*

Applications

The PLL can be used in a wide variety of applications, including (1) frequency demodulation, (2) frequency synthesis, and (3) FSK decoders. Examples of each of these follow.

FREQUENCY DEMODULATION

FM demodulation or detection can be directly achieved using the PLL circuit. If the PLL center frequency is selected or designed at the FM carrier frequency, the filtered or output voltage of the circuit of Fig. 17.25 is the desired demodulated voltage, varying in value proportional to the variation of the signal frequency. The PLL circuit thus operates as a complete intermediate-frequency (IF) strip, limiter, and demodulator as used in FM receivers.

One popular PLL unit is the 565, shown in Fig. 17.26a. The 565 contains a phase detector, amplifier, and voltage-controlled oscillator, which are only partially connected internally. An external resistor and capacitor, R_1 and C_1, are used to set the free-running or center frequency of the VCO. Another external capacitor, C_2, is used to set the low-pass filter passband, and the VCO output must be connected back as input to the phase detector to close the PLL loop. The 565 typically uses two power supplies, V^+ and V^-.

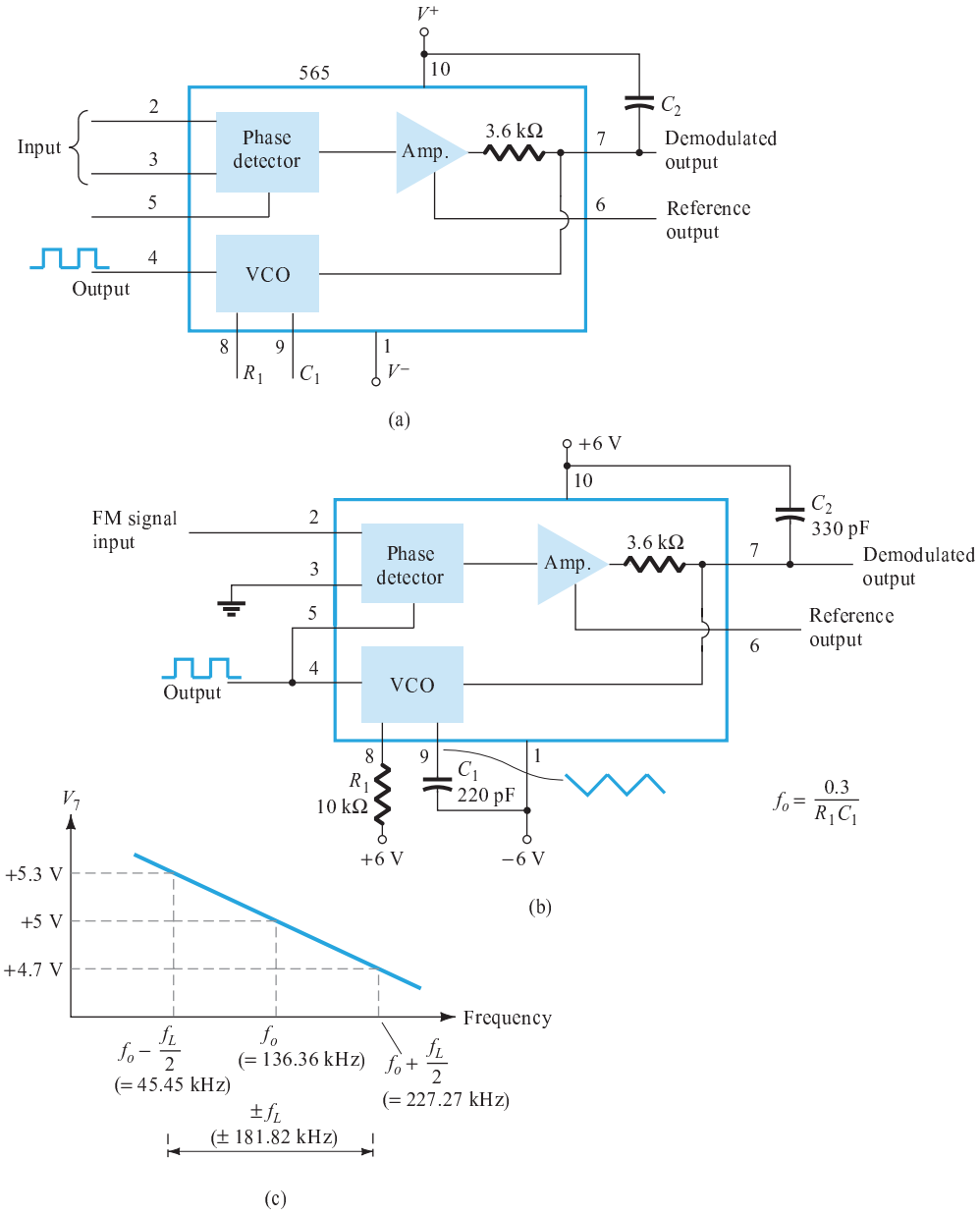


Figure 17.26 Phase-locked loop (PLL): (a) basic block diagram: (b) PLL connected as a frequency demodulator: (c) output voltage vs. frequency plot.

Figure 17.26b shows the PLL connected to work as an FM demodulator. Resistor R_1 and capacitor C_1 set the free-running frequency, f_o,

$$\boxed{f_o = \frac{0.3}{R_1 C_1}} \tag{17.9}$$

$$= \frac{0.3}{(10 \times 10^3)(220 \times 10^{-12})} = 136.36 \text{ kHz}$$

with limitation 2 kΩ ≤ R_1 ≤ 20 kΩ. The lock range is

$$f_L = \pm\frac{8f_o}{V}$$

$$= \pm\frac{8(136.36 \times 10^3)}{6} = \pm 181.8 \text{ kHz}$$

for supply voltages $V = \pm 6$ V. The capture range is

$$f_C = \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{R_2 C_2}}$$

$$= \pm \frac{1}{2\pi}\sqrt{\frac{2\pi(181.8 \times 10^3)}{(3.6 \times 10^3)(330 \times 10^{-12})}} = 156.1 \text{ kHz}$$

The signal at pin 4 is a 136.36-kHz square wave. An input within the lock range of 181.8 kHz will result in the output at pin 7 varying around its dc voltage level set with input signal at f_o. Figure 17.26c shows the output at pin 7 as a function of the input signal frequency. The dc voltage at pin 7 is linearly related to the input signal frequency within the frequency range $f_L = 181.8$ kHz around the center frequency 136.36 kHz. The output voltage is the demodulated signal that varies with frequency within the operating range specified.

FREQUENCY SYNTHESIS

A frequency synthesizer can be built around a PLL as shown in Fig. 17.27. A frequency divider is inserted between the VCO output and the phase comparator so that the loop signal to the comparator is at frequency f_o while the VCO output is Nf_o. This output is a multiple of the input frequency as long as the loop is in lock. The input signal can be stabilized at f_1 with the resulting VCO output at Nf_1 if the loop is set

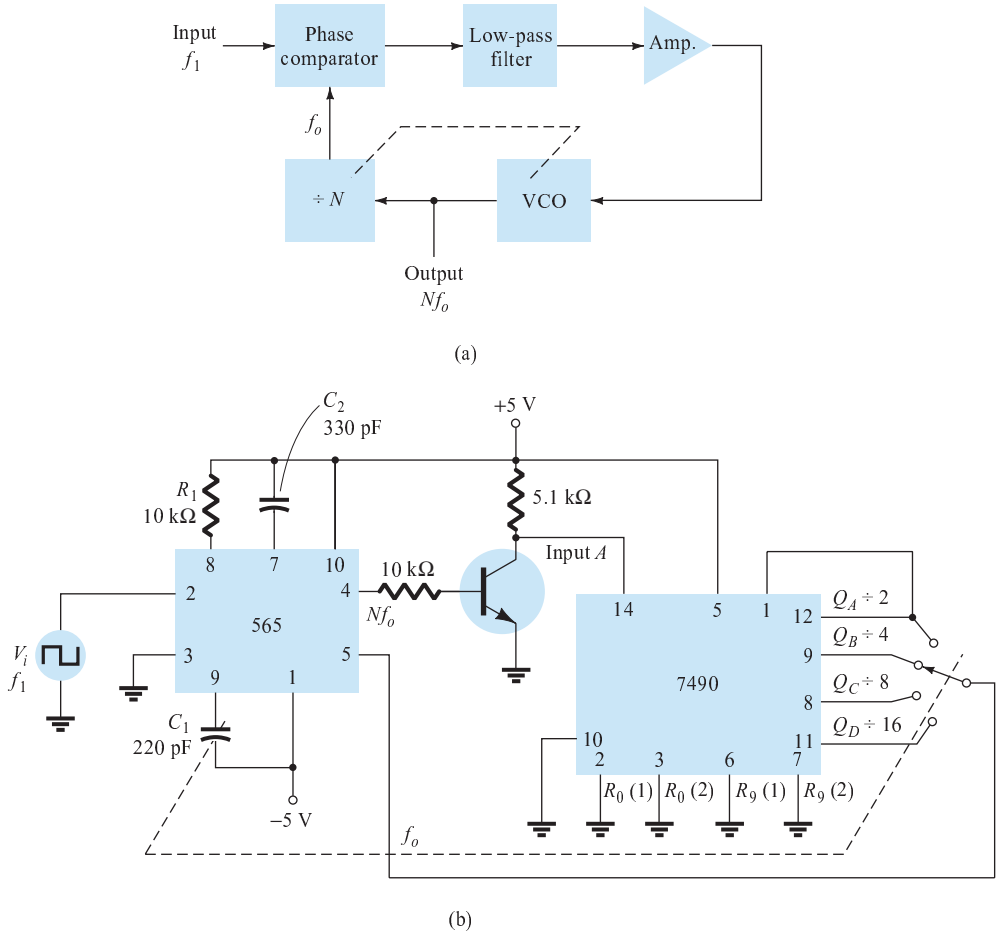


Figure 17.27 Frequency synthesizer: (a) block diagram; (b) implementation using 565 PLL unit.

up to lock at the fundamental frequency (when $f_o = f_1$). Figure 17.27b shows an example using a 565 PLL as frequency multiplier and a 7490 as divider. The input V_i at frequency f_1 is compared to the input (frequency f_o) at pin 5. An output at Nf_o ($4f_o$ in the present example) is connected through an inverter circuit to provide an input at pin 14 of the 7490, which varies between 0 and +5 V. Using the output at pin 9, which is divided by 4 from that at the input to the 7490, the signal at pin 4 of the PLL is four times the input frequency as long as the loop remains in lock. Since the VCO can vary over only a limited range from its center frequency, it may be necessary to change the VCO frequency whenever the divider value is changed. As long as the PLL circuit is in lock, the VCO output frequency will be exactly N times the input frequency. It is only necessary to readjust f_o to be within the capture-and-lock range, the closed loop then resulting in the VCO output becoming exactly Nf_1 at lock.

FSK DECODERS

An FSK (frequency-shift keyed) signal decoder can be built as shown in Fig. 17.28. The decoder receives a signal at one of two distinct carrier frequencies, 1270 Hz or 1070 Hz, representing the RS-232C logic levels or mark (−5 V) or space (+14 V), respectively. As the signal appears at the input, the loop locks to the input frequency and tracks it between two possible frequencies with a corresponding dc shift at the output.

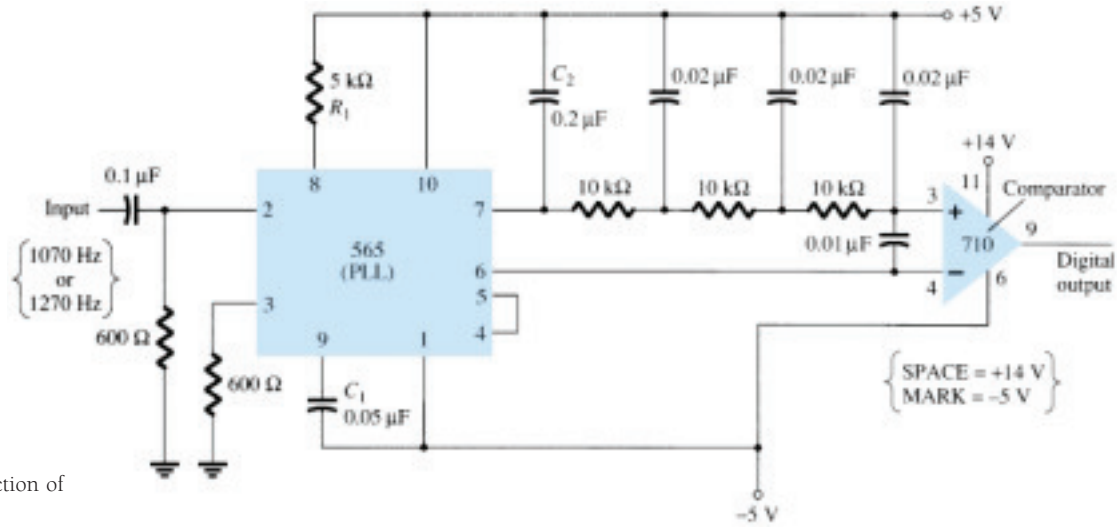


Figure 17.28 Connection of 565 as FSK decoder.

The RC ladder filter (three sections of $C = 0.02\ \mu$F and $R = 10\ \text{k}\Omega$) is used to remove the sum frequency component. The free-running frequency is adjusted with R_1 so that the dc voltage level at the output (pin 7) is the same as that at pin 6. Then an input at frequency 1070 Hz will drive the decoder output voltage to a more positive voltage level, driving the digital output to the high level (space or +14 V). An input at 1270 Hz will correspondingly drive the 565 dc output less positive with the digital output, which then drops to the low level (mark or −5 V).

17.7 INTERFACING CIRCUITRY

Connecting different types of circuits, either in digital or analog circuits, may require some sort of interfacing circuit. An interface circuit may be used to drive a load or to obtain a signal as a receiver circuit. A driver circuit provides the output signal at a

voltage or current level suitable to operate a number of loads, or to operate such devices as relays, displays, or power units. A receiver circuit essentially accepts an input signal, providing high input impedance to minimize loading of the input signal. Furthermore, the interface circuits may include strobing, which provides connecting the interface signals during specific time intervals established by the strobe.

Figure 17.29a shows a dual-line driver, each driver accepting input of TTL signals, providing output capable of driving TTL or MOS device circuits. This type of interface circuit comes in various forms, some as inverting and others as noninverting units. The circuit of Fig. 17.29b shows a dual-line receiver having both inverting and noninverting inputs so that either operating condition can be selected. As an example, connection of an input signal to the inverting input would result in an inverted output from the receiver unit. Connecting the input to the noninverting input would provide the same interfacing except that the output obtained would have the same polarity as the received signal. The driver-receiver unit of Fig. 17.29 provides an output when the strobe signal is present (high in this case).

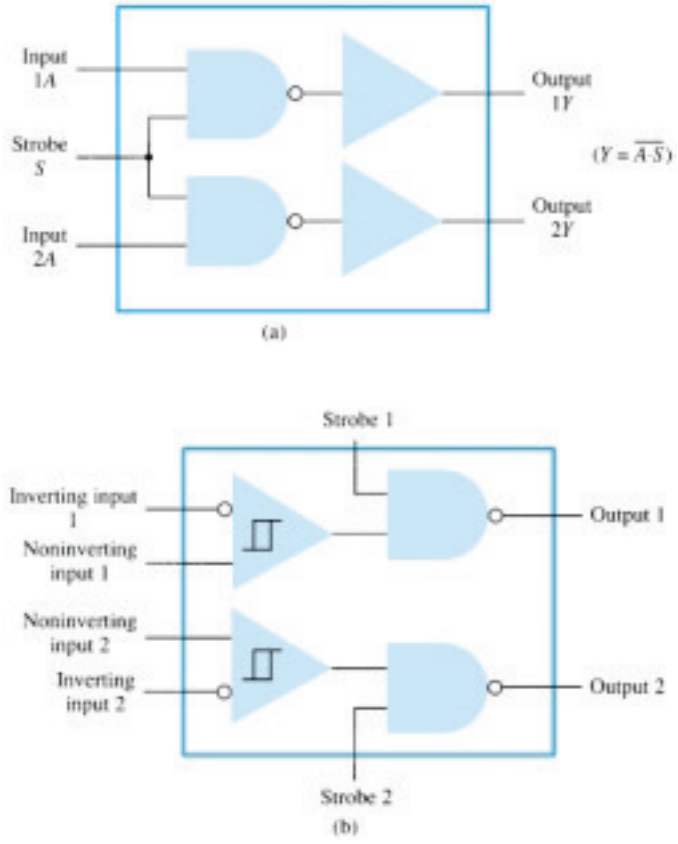


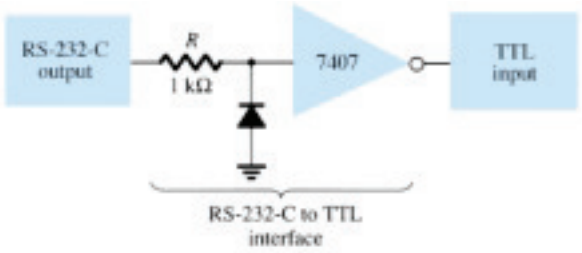
Figure 17.29 Interface units: (a) dual-line drivers (SN75150); (b) dual-line receivers (SN75152).

Another type of interface circuit is that used to connect various digital input and output units, signals with devices such as keyboards, video terminals, and printers. One of the EIA electronic industry standards is referred to as RS-232C. This standard states that a digital signal represents a mark (logic-1) and a space (logic-0). The definitions of mark and space vary with the type of circuit used (although a full reading of the standard will spell out the acceptable limits of mark and space signals).

RS-232C-to-TTL Converter

For TTL circuits, +5 V is a mark and 0 V is a space. For RS-232C, a mark could be −12 V and a space +12 V. Figure 17.30a provides a tabulation of some mark and space definitions. For a unit having outputs defined by RS-232C that is to operate into another unit operating with a TTL signal level, an interface circuit as shown in Fig. 17.30b could be used. A mark output from the driver (at −12 V) would be clipped by the diode so that the input to the inverter circuit is near 0 V, resulting in an output of +5 V (TTL mark). A space output at +12 V would drive the inverter output low for a 0-V output (a space).

	Current Loop	RS-232-C	TTL
MARK	20 mA	−12 V	+5 V
SPACE	0 mA	+12 V	0 V



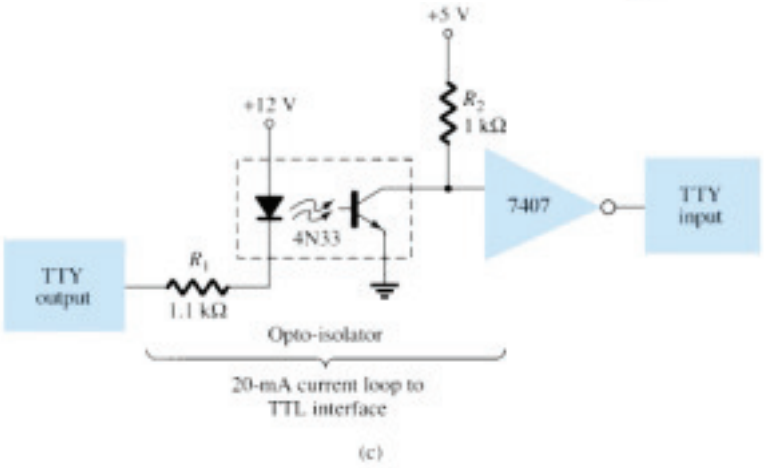


Figure 17.30 Interfacing signal standards and converter circuits.

Another example of an interface circuit converts the signals from a TTY current loop into TTL levels as shown in Fig. 17.30c. An input mark results when 20 mA of current is drawn from the source through the output line of the teletype (TTY). This current then goes through the diode element of an opto-isolator, driving the output transistor on. The input to the inverter going low results in a +5-V signal from the 7407 inverter output so that a mark from the teletype results in a mark to the TTL input. A space from the teletype current loop provides no current, with the opto-isolator transistor remaining off and the inverter output then 0 V, which is a TTL space signal.

Another means of interfacing digital signals is made using open-collector output or tri-state output. When a signal is output from a transistor collector (see Fig. 17.31) that is not connected to any other electronic component, the output is open-collector. This permits connecting a number of signals to the same wire or bus. Any transistor going on then provides a low output voltage, while all transistors remaining off provide a high output voltage.

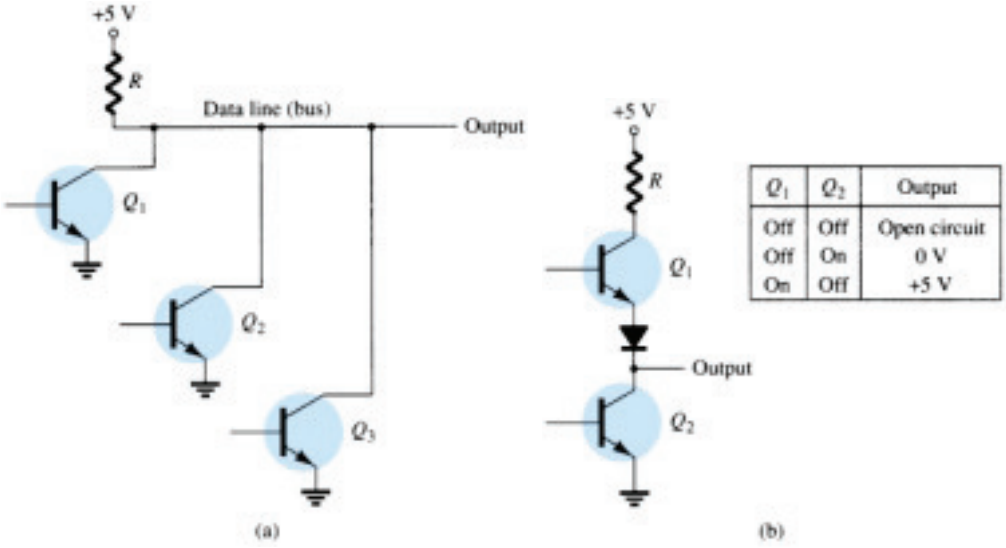


Figure 17.31 Connections to data lines: (a) open-collector output; (b) tri-state output.

17.8 PSPICE WINDOWS

Many of the practical op-amp applications covered in this chapter can be analyzed using PSpice. Analysis of various problems can display the resulting dc bias, or one can use **PROBE** to display resulting waveforms.

Program 17.1—Comparator Circuit Used to Drive an LED

Using Design Center, draw the circuit of a comparator circuit with output driving an LED indicator as shown in Fig. 17.32. To be able to view the magnitude of the dc output voltage, place a **VPRINT1** component at V_o with **DC** and **MAG** selected. To view the dc current through the LED, place an **IPRINT** component in series with the LED current meter as shown in Fig. 17.32. The **Analysis Setup** provides for a dc sweep as shown in Fig. 17.33. The **DC Sweep** is set, as shown, for V_i from 4 to 8 V in 1-V steps. After running the simultation, some of the resulting analysis output obtained is shown in Fig. 17.34.

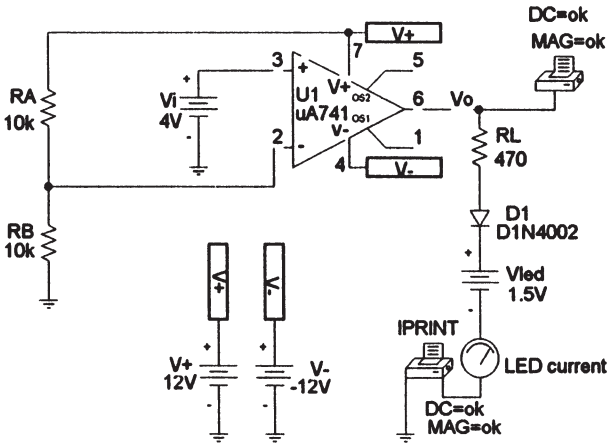


Figure 17.32 Comparator circuit used to drive an LED.

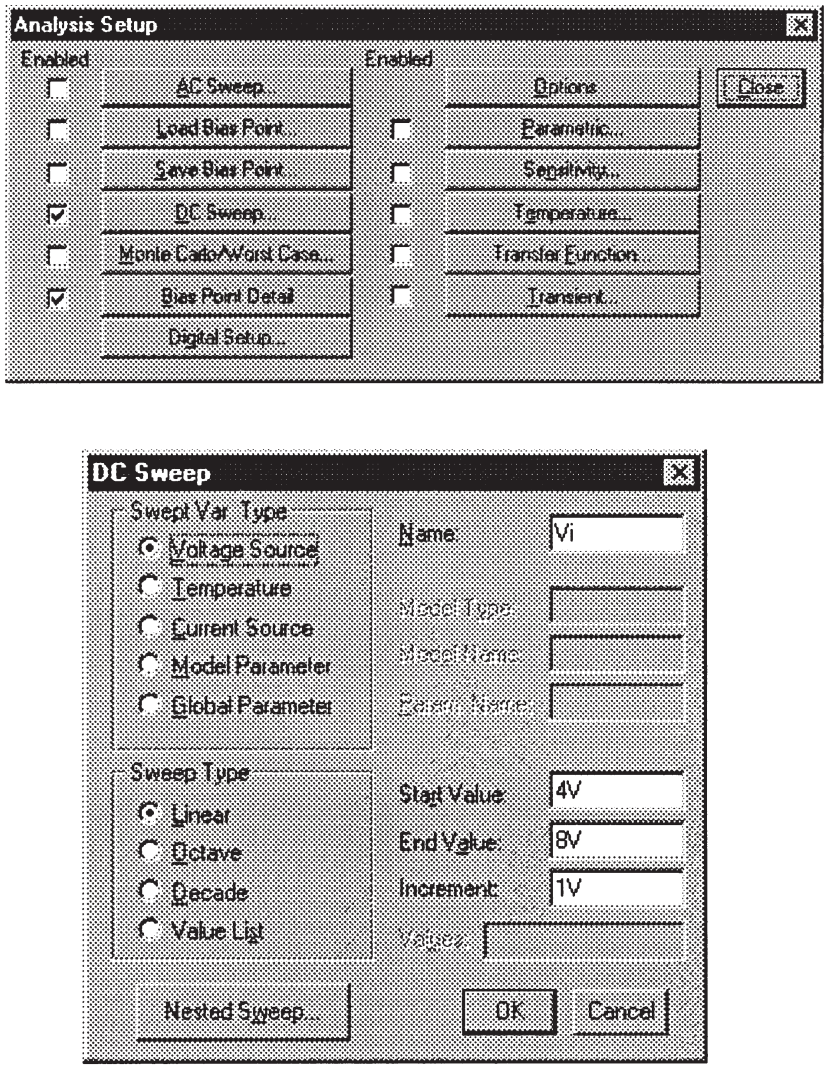


Figure 17.33 Analysis Setup for a dc sweep of the circuit of Fig. 17.32.

The circuit of Fig. 17.32 shows a voltage divider which provides 6 V to the minus input so that any input (V_i) below 6 V will result in the output at the minus saturation voltage (near −10 V). Any input above +6 V results in the output going to the positive saturation level (near +10 V). The LED will therefore be driven *on* by any input above the reference level of +6 V and left *off* by any input below +6 V. The listing of Fig. 17.34 shows a table of the output voltage and a table of the LED current for inputs from 4 to 8 V. The table shows that the LED current is nearly 0 for inputs up to +6 V and that a current of about 20 mA lights the LED for inputs at +6 V or above.

```
Comparator Circuit Driving LED

****     DC TRANSFER CURVES
 V_Vi          V(Vo)
 4.000E+00     -1.161E+01
 5.000E+00     -1.161E+01
 6.000E+00      1.145E+01
 7.000E+00      1.161E+01
 8.000E+00      1.161E+01

****     DC TRANSFER CURVES
 V_Vi          I(V_PRINT3)
 4.000E+00      1.312E-11
 5.000E+00      1.312E-11
 6.000E+00     -1.953E-02
 7.000E+00     -1.987E-02
 8.000E+00     -1.987E-02
```

Figure 17.34 Analysis output (edited) for circuit of Fig. 17.32.

Program 17.2—Comparator Operation

The operation of a comparator IC can be demonstrated using a 741 op-amp as shown in Fig. 17.35. The input is a 5 V, peak sinusoidal signa. The **Analysis Setup** provides for **Transient** analysis with **Print Step** of **20 ns** and **Final Time** of **3 ms.** Since the input signal is applied to the noninverting input, the output is in-phase with the input. When the input goes above 0 V, the output goes to the positive saturation level,

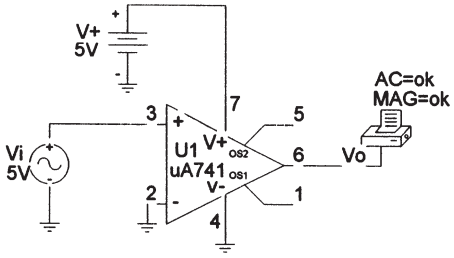


Figure 17.35 Schematic for a comparator.

near +5 V. When the input goes below 0 V, the output goes to the negative saturation level—this being 0 V since the minus voltage input is set to that value. Figure 17.36 shows a **PROBE** output of input and output voltages.

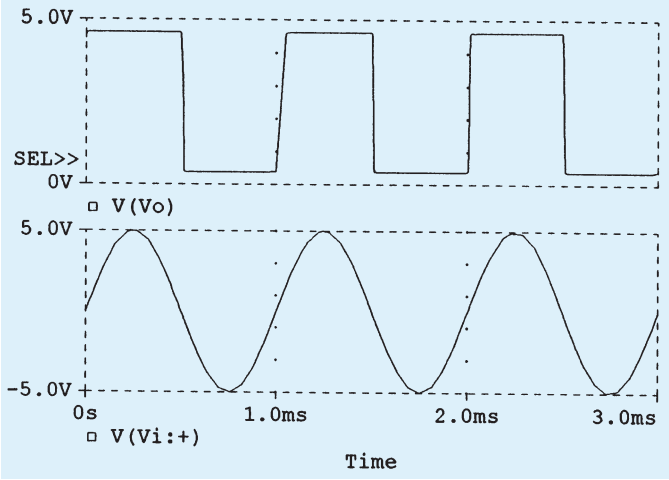


Figure 17.36 Probe output for the comparator of Fig. 17.35.

Program 17.3—Operation of 555 Timer as Oscillator

Figure 17.37 shows a 555 timer connected as an oscillator. Equations (17.3) and (17.4) can be used to calculate the charge and discharge times as follows:

$$T_{\text{high}} = 0.7(R_A + R_B)C = 0.7(7.5\ \text{k}\Omega + 7.15\ \text{k}\Omega)(0.1\ \mu\text{F}) = 1.05\ \text{ms}$$

$$T_{\text{low}} = 0.7R_BC = 0.7(7.5\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.525\ \text{ms}$$

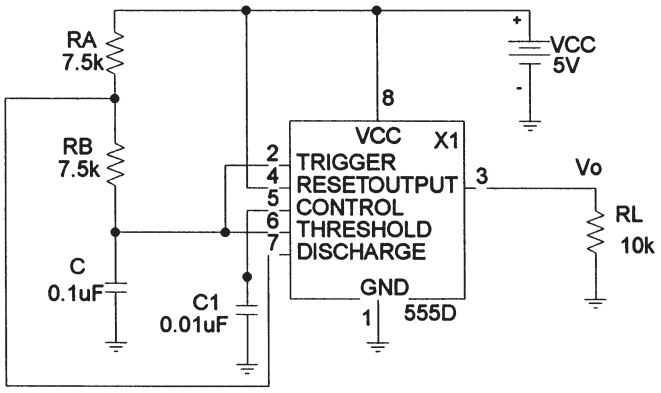


Figure 17.37 Schematic of a 555 timer oscillator.

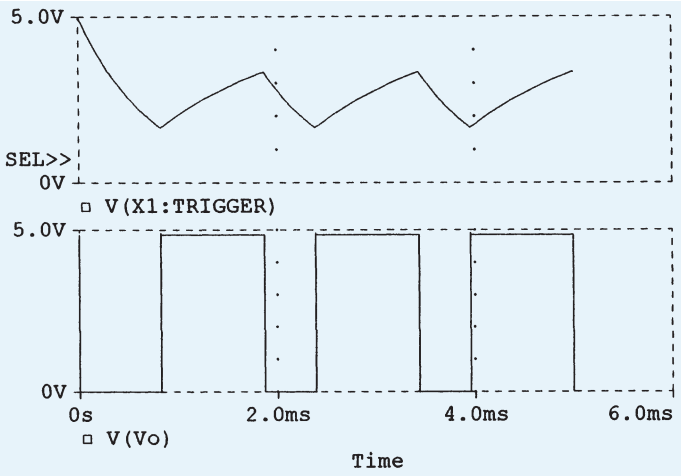


Figure 17.38 Probe output for the 555 oscillator of Fig. 17.37.

The resulting trigger and output waveforms are shown in Fig. 17.38. When the trigger charges to the upper trigger level, the output goes to the low output level of 0 V. The output stays low until the trigger input discharges to the low trigger level, at which time the output goes to the high level of +5 V.

PROBLEMS

§ 17.2 Comparator Unit Operation

1. Draw the diagram of a 741 op-amp operated from ±15-V supplies with $V_i(-) = 0$ V and $V_i(+) = +5$ V. Include terminal pin connections.
2. Sketch the output waveform for the circuit of Fig. 17.39.
3. Draw a circuit diagram of a 311 op-amp showing an input of 10 V rms applied to the inverting input and the plus input to ground. Identify all pin numbers.
4. Draw the resulting output waveform for the circuit of Fig. 17.40.

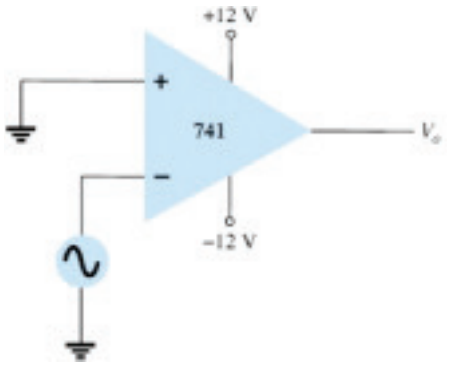


Figure 17.39 Problem 2

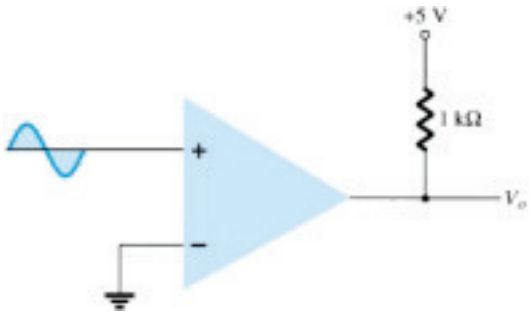


Figure 17.40 Problem 4

5. Draw the circuit diagram of a zero-crossing detector using a 339 comparator stage with ±12-V supplies.

6. Sketch the output waveform for the circuit of Fig. 17.41.

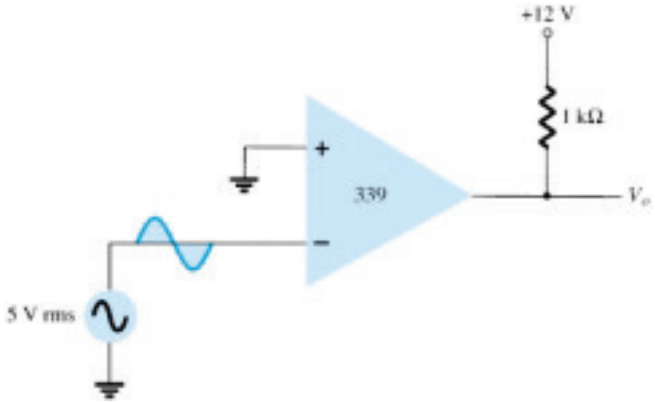


Figure 17.41 Problem 6

* 7. Describe the operation of the circuit in Fig. 17.42.

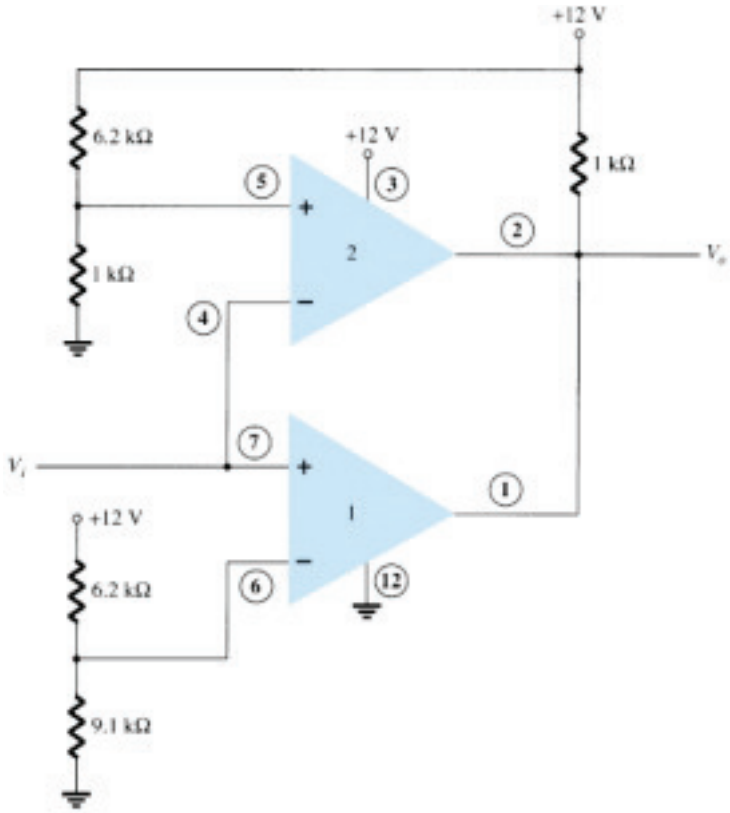


Figure 17.42 Problem 7

§ 17.3 Digital–Analog Converters

8. Sketch a five-stage ladder network using 15-kΩ and 30-kΩ resistors.
9. For a reference voltage of 16 V, calculate the output voltage for an input of 11010 to the circuit of Problem 8.
10. What voltage resolution is possible using a 12-stage ladder network with a 10-V reference voltage?

11. For a dual-slope converter, describe what occurs during the fixed time interval and the count interval.

12. How many count steps occur using a 12-stage digital counter at the output of an ADC?

13. What is the maximum count interval using a 12-stage counter operated at a clock rate of 20 MHz?

§ 17.4 Timer IC Unit Operation

14. Sketch the circuit of a 555 timer connected as an astable multivibrator for operation at 350 kHz. Determine the value of capacitor, C, needed using $R_A = R_B = 7.5\ \text{k}\Omega$.

15. Draw the circuit of a one-shot using a 555 timer to provide one time period of 20 μs. If $R_A = 7.5\ \text{k}\Omega$, what value of C is needed?

16. Sketch the input and output waveforms for a one-shot using a 555 timer triggered by a 10-kHz clock for $R_A = 5.1\ \text{k}\Omega$ and $C = 5$ nF.

§ 17.5 Voltage-Controlled Oscillator

17. Calculate the center frequency of a VCO using a 566 IC as in Fig. 17.22 for $R_1 = 4.7\ \text{k}\Omega$, $R_2 = 1.8\ \text{k}\Omega$, $R_3 = 11\ \text{k}\Omega$, and $C_1 = 0.001\ \mu\text{F}$.

* 18. What frequency range results in the circuit of Fig. 17.23 for $C_1 = 0.001\ \mu\text{F}$?

19. Determine the capacitor needed in the circuit of Fig. 17.22 to obtain a 200-kHz output.

§ 17.6 Phase-Locked Loop

20. Calculate the VCO free-running frequency for the circuit of Fig. 17.26b with $R_1 = 4.7\ \text{k}\Omega$ and $C_1 = 0.001\ \mu\text{F}$.

21. What value of capacitor, C_1, is required in the circuit of Fig. 17.26b to obtain a center frequency of 100 kHz?

22. What is the lock range of the PLL circuit in Fig. 17.26b for $R_1 = 4.7\ \text{k}\Omega$ and $C_1 = 0.001\ \mu\text{F}$?

§ 17.7 Interfacing Circuitry

23. Describe the signal conditions for current-loop and RS-232C interfaces.

24. What is a data bus?

25. What is the difference between open-collector and tri-state output?

§ 17.8 PSpice Windows

* 26. Use Design Center to draw a schematic circuit as in Fig. 17.32, using an LM111 with $V_i = 5$ V rms applied to minus (−) input and +5 V rms applied to plus (+) input. Use Probe to view the output waveform.

* 27. Use Design Center to draw a schematic circuit as in Fig. 17.35. Examine the output listing for the results.

* 28. Use Design Center to draw a 555 oscillator with resulting output with $t_{\text{low}} = 2$ ms, $t_{\text{high}} = 5$ ms.

*Please note: Asterisks indicate more difficult problems.

13

Sinusoidal Alternating Waveforms

13.1 INTRODUCTION

The analysis thus far has been limited to dc networks, networks in which the currents or voltages are fixed in magnitude except for transient effects. We will now turn our attention to the analysis of networks in which the magnitude of the source varies in a set manner. Of particular interest is the time-varying voltage that is commercially available in large quantities and is commonly called the *ac voltage*. (The letters *ac* are an abbreviation for *alternating current*.) To be absolutely rigorous, the terminology *ac voltage* or *ac current* is not sufficient to describe the type of signal we will be analyzing. Each waveform of Fig. 13.1 is an **alternating waveform** available from commercial supplies. The term *alternating* indicates only that the waveform alternates between two prescribed levels in a set time sequence (Fig. 13.1). To be

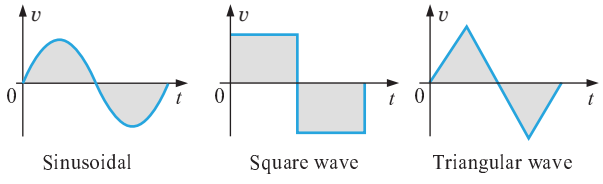


FIG. 13.1
Alternating waveforms.

absolutely correct, the term *sinusoidal, square wave,* or *triangular* must also be applied. The pattern of particular interest is the **sinusoidal ac waveform** for voltage of Fig. 13.1. Since this type of signal is encountered in the vast majority of instances, the abbreviated phrases *ac voltage* and *ac current* are commonly applied without confusion. For the other patterns of Fig. 13.1, the descriptive term is always present, but frequently the *ac* abbreviation is dropped, resulting in the designation *square-wave* or *triangular* waveforms.

One of the important reasons for concentrating on the sinusoidal ac voltage is that it is the voltage generated by utilities throughout the world. Other reasons include its application throughout electrical, electronic, communication, and industrial systems. In addition, the chapters to follow will reveal that the waveform itself has a number of characteristics that will result in a unique response when it is applied to the basic electrical elements. The wide range of theorems and methods introduced for dc networks will also be applied to sinusoidal ac systems. Although the application of sinusoidal signals will raise the required math level, once the notation given in Chapter 14 is understood, most of the concepts introduced in the dc chapters can be applied to ac networks with a minimum of added difficulty.

The increasing number of computer systems used in the industrial community requires, at the very least, a brief introduction to the terminology employed with pulse waveforms and the response of some fundamental configurations to the application of such signals. Chapter 22 will serve such a purpose.

13.2 SINUSOIDAL ac VOLTAGE CHARACTERISTICS AND DEFINITIONS

Generation

Sinusoidal ac voltages are available from a variety of sources. The most common source is the typical home outlet, which provides an ac voltage that originates at a power plant; such a power plant is most commonly fueled by water power, oil, gas, or nuclear fusion. In each case an *ac generator* (also called an *alternator*), as shown in Fig. 13.2(a), is the primary component in the energy-conversion process.

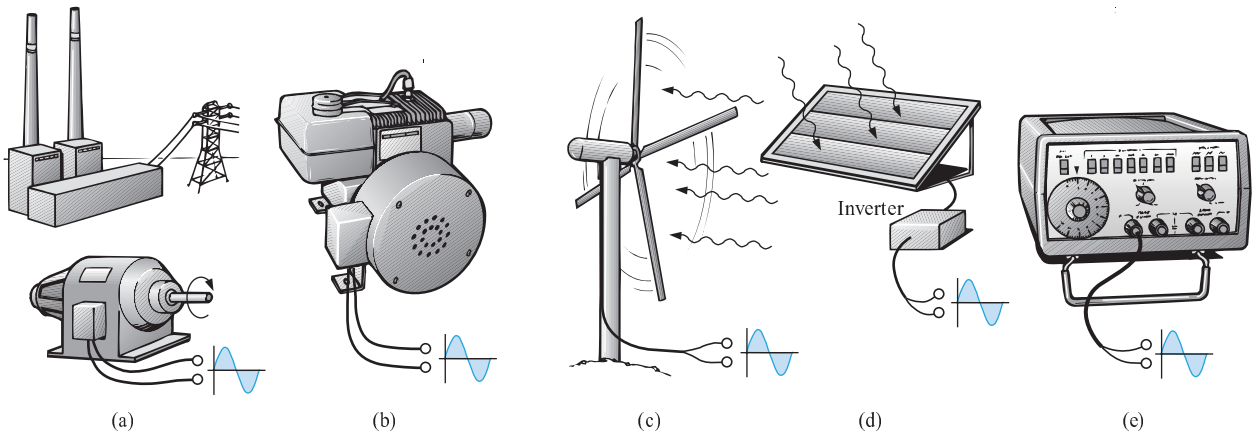


FIG. 13.2

Various sources of ac power: (a) generating plant; (b) portable ac generator; (c) wind-power station; (d) solar panel; (e) function generator.

The power to the shaft developed by one of the energy sources listed will turn a *rotor* (constructed of alternating magnetic poles) inside a set of windings housed in the *stator* (the stationary part of the dynamo) and will induce a voltage across the windings of the stator, as defined by Faraday's law,

$$e = N\frac{d\phi}{dt}$$

Through proper design of the generator, a sinusoidal ac voltage is developed that can be transformed to higher levels for distribution through the power lines to the consumer. For isolated locations where power lines have not been installed, portable ac generators [Fig. 13.2(b)] are available that run on gasoline. As in the larger power plants, however, an ac generator is an integral part of the design.

In an effort to conserve our natural resources, wind power and solar energy are receiving increasing interest from various districts of the world that have such energy sources available in level and duration that make the conversion process viable. The turning propellers of the wind-power station [Fig. 13.2(c)] are connected directly to the shaft of an ac generator to provide the ac voltage described above. Through light energy absorbed in the form of *photons,* solar cells [Fig. 13.2(d)] can generate dc voltages. Through an electronic package called an *inverter,* the dc voltage can be converted to one of a sinusoidal nature. Boats, recreational vehicles (RVs), etc., make frequent use of the inversion process in isolated areas.

Sinusoidal ac voltages with characteristics that can be controlled by the user are available from *function generators,* such as the one in Fig. 13.2(e). By setting the various switches and controlling the position of the knobs on the face of the instrument, one can make available sinusoidal voltages of different peak values and different repetition rates. The function generator plays an integral role in the investigation of the variety of theorems, methods of analysis, and topics to be introduced in the chapters that follow.

Definitions

The sinusoidal waveform of Fig. 13.3 with its additional notation will now be used as a model in defining a few basic terms. These terms can, however, be applied to any alternating waveform. It is important to remember as you proceed through the various definitions that the vertical scaling is in volts or amperes and the horizontal scaling is *always* in units of time.

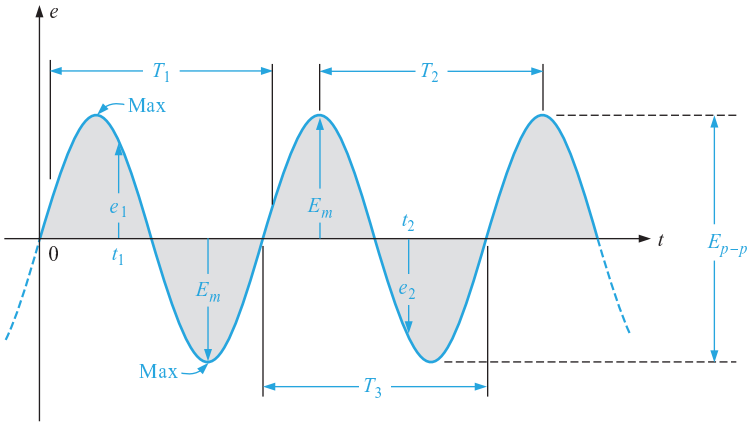


FIG. 13.3
Important parameters for a sinusoidal voltage.

Waveform: The path traced by a quantity, such as the voltage in Fig. 13.3, plotted as a function of some variable such as time (as above), position, degrees, radians, temperature, and so on.

Instantaneous value: The magnitude of a waveform at any instant of time; denoted by lowercase letters (e_1, e_2).

Peak amplitude: The maximum value of a waveform as measured from its *average,* or *mean,* value, denoted by uppercase letters (such as E_m for sources of voltage and V_m for the voltage drop across a load). For the waveform of Fig. 13.3, the average value is zero volts and E_m is as defined by the figure.

Peak value: The maximum instantaneous value of a function as measured from the zero-volt level. For the waveform of Fig. 13.3, the peak amplitude and peak value are the same, since the average value of the function is zero volts.

Peak-to-peak value: Denoted by $E_{p\text{-}p}$ or $V_{p\text{-}p}$, the full voltage between positive and negative peaks of the waveform, that is, the sum of the magnitude of the positive and negative peaks.

Periodic waveform: A waveform that continually repeats itself after the same time interval. The waveform of Fig. 13.3 is a periodic waveform.

Period (T): The time interval between successive repetitions of a periodic waveform (the period $T_1 = T_2 = T_3$ in Fig. 13.3), as long as successive *similar points* of the periodic waveform are used in determining T.

Cycle: The portion of a waveform contained in *one period* of time. The cycles within T_1, T_2, and T_3 of Fig. 13.3 may appear different in Fig. 13.4, but they are all bounded by one period of time and therefore satisfy the definition of a cycle.

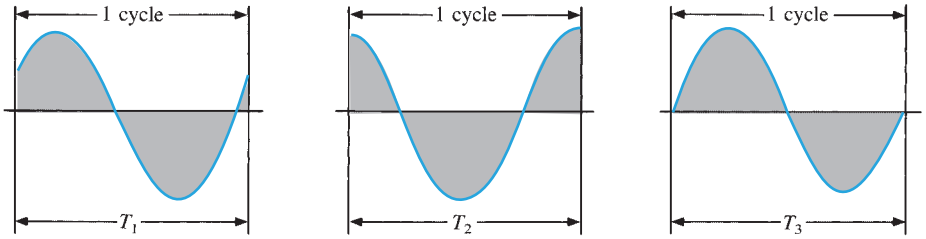


FIG. 13.4
Defining the cycle and period of a sinusoidal waveform.

Frequency (f): The number of cycles that occur in 1 s. The frequency of the waveform of Fig. 13.5(a) is 1 cycle per second, and for Fig. 13.5(b), 2½ cycles per second. If a waveform of similar shape had a period of 0.5 s [Fig. 13.5(c)], the frequency would be 2 cycles per second.

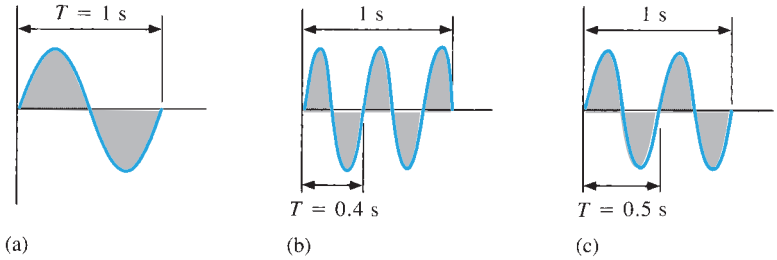


FIG. 13.5
Demonstrating the effect of a changing frequency on the period of a sinusoidal waveform.

The unit of measure for frequency is the *hertz* (Hz), where

$$\boxed{1 \text{ hertz (Hz)} = 1 \text{ cycle per second (c/s)}} \qquad \textbf{(13.1)}$$

The unit hertz is derived from the surname of Heinrich Rudolph Hertz (Fig. 13.6), who did original research in the area of alternating currents and voltages and their effect on the basic *R*, *L*, and *C* elements. The frequency standard for North America is 60 Hz, whereas for Europe it is predominantly 50 Hz.

As with all standards, any variation from the norm will cause difficulties. In 1993, Berlin, Germany, received all its power from eastern plants, whose output frequency was varying between 50.03 and 51 Hz. The result was that clocks were gaining as much as 4 minutes a day. Alarms went off too soon, VCRs clicked off before the end of the program, etc., requiring that clocks be continually reset. In 1994, however, when power was linked with the rest of Europe, the precise standard of 50 Hz was reestablished and everyone was on time again.

Using a log scale (described in detail in Chapter 21), a frequency spectrum from 1 GHz to 1000 GHz can be scaled off on the same axis, as shown in Fig. 13.7. A number of terms in the various spectrums are probably familiar to the reader from everyday experiences. Note that the audio range (human ear) extends from only 15 Hz to 20 kHz, but the transmission of radio signals can occur between 3 kHz and 300 GHz. The uniform process of defining the intervals of the radio-frequency spectrum from VLF to EHF is quite evident from the length of the bars in the figure (although keep in mind that it is a log scale, so the frequencies encompassed within each segment are quite different). Other frequencies of particular interest (TV, CB, microwave, etc.) are also included for reference purposes. Although it is numerically easy to talk about frequencies in the megahertz and gigahertz range, keep in mind that a frequency of 100 MHz, for instance, represents a sinusoidal waveform that passes through 100,000,000 cycles in only 1 s—an incredible number when we compare it to the 60 Hz of our conventional power sources The new Pentium II chip manufactured by Intel can run at speeds up to 450 MHz. Imagine a product able to handle 450,000,000 instructions per second—an incredible achievement.

Since the frequency is inversely related to the period—that is, as one increases, the other decreases by an equal amount—the two can be related by the following equation:

$$\boxed{f = \frac{1}{T}} \qquad \begin{array}{l} f = \text{Hz} \\ T = \text{seconds (s)} \end{array} \qquad \textbf{(13.2)}$$

or

$$\boxed{T = \frac{1}{f}} \qquad \textbf{(13.3)}$$

German (Hamburg, Berlin, Karlsruhe)
(1857–94)
Physicist
Professor of Physics, Karlsruhe Polytechnic and University of Bonn

Courtesy of the Smithsonian Institution Photo No. 66,606

Spurred on by the earlier predictions of the English physicist James Clerk Maxwell, Heinrich Hertz produced *electromagnetic waves* in his laboratory at the Karlsruhe Polytechnic while in his early 30s. The rudimentary *transmitter* and *receiver* were in essence the first to broadcast and receive radio waves. He was able to measure the *wavelength* of the electromagnetic waves and confirmed that the *velocity of propagation* is in the same order of magnitude as light. In addition, he demonstrated that the *reflective* and *refractive* properties of electromagnetic waves are the same as those for heat and light waves. It was indeed unfortunate that such an ingenious, industrious individual should pass away at the very early age of 37 due to a bone disease.

FIG. 13.6
Heinrich Rudolph Hertz.

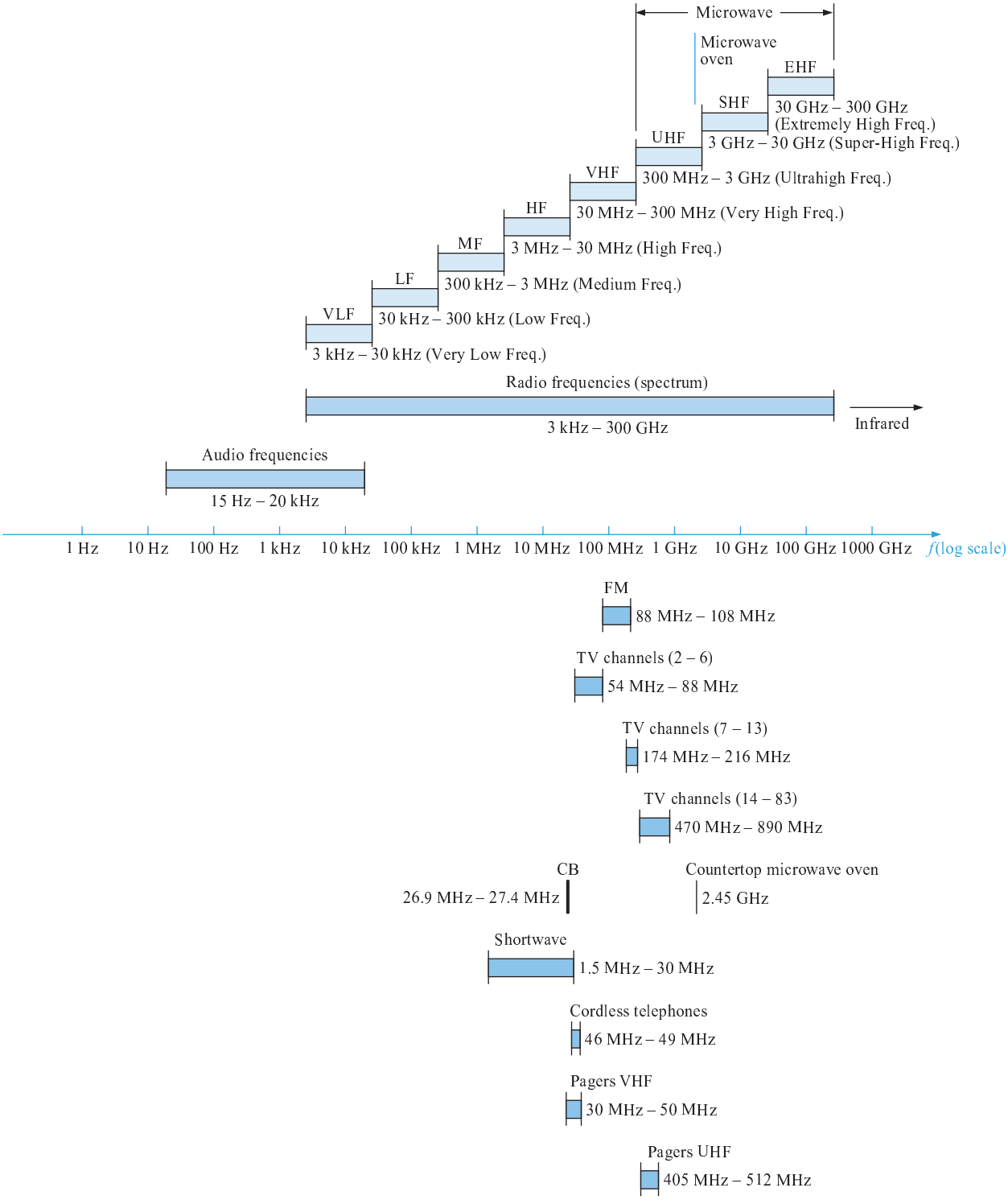


FIG. 13.7
Areas of application for specific frequency bands.

EXAMPLE 13.1 Find the period of a periodic waveform with a frequency of
a. 60 Hz.
b. 1000 Hz.

Solutions:

a. $T = \frac{1}{f} = \frac{1}{60\ \text{Hz}} \cong 0.01667\ \text{s}$ or **16.67 ms**

(a recurring value since 60 Hz is so prevalent)

b. $T = \frac{1}{f} = \frac{1}{1000\ \text{Hz}} = 10^{-3}\ \text{s} = \mathbf{1\ ms}$

EXAMPLE 13.2 Determine the frequency of the waveform of Fig. 13.8.

Solution: From the figure, $T = (25\ \text{ms} - 5\ \text{ms}) = 20\ \text{ms}$, and

$$f = \frac{1}{T} = \frac{1}{20 \times 10^{-3}\ \text{s}} = \mathbf{50\ Hz}$$

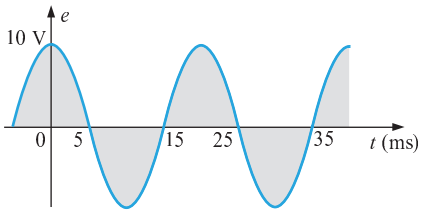


FIG. 13.8
Example 13.2.

EXAMPLE 13.3 The **oscilloscope** is an instrument that will display alternating waveforms such as those described above. A sinusoidal pattern appears on the oscilloscope of Fig. 13.9 with the indicated vertical and horizontal sensitivities. The vertical sensitivity defines the voltage associated with each vertical division of the display. Virtually all oscilloscope screens are cut into a crosshatch pattern of lines separated by 1 cm in the vertical and horizontal directions. The horizontal sensitivity defines the time period associated with each horizontal division of the display.

For the pattern of Fig. 13.9 and the indicated sensitivities, determine the period, frequency, and peak value of the waveform.

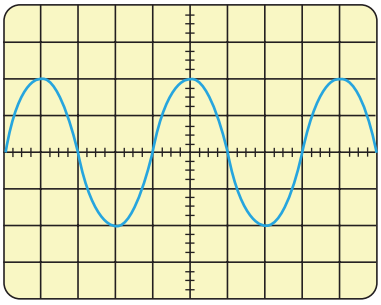


FIG. 13.9
Example 13.3.

Solution: One cycle spans 4 divisions. The period is therefore

$$T = 4\ \text{div.}\left(\frac{50\ \mu\text{s}}{\text{div.}}\right) = \mathbf{200\ \mu s}$$

and the frequency is

$$f = \frac{1}{T} = \frac{1}{200 \times 10^{-6}\ \text{s}} = \mathbf{5\ kHz}$$

The vertical height above the horizontal axis encompasses 2 divisions. Therefore,

$$V_m = 2\ \text{div.}\left(\frac{0.1\ \text{V}}{\text{div.}}\right) = \mathbf{0.2\ V}$$

Defined Polarities and Direction

In the following analysis, we will find it necessary to establish a set of polarities for the sinusoidal ac voltage and a direction for the sinusoidal ac current. In each case, the polarity and current direction will be for an instant of time in the positive portion of the sinusoidal waveform. This is shown in Fig. 13.10 with the symbols for the sinusoidal ac voltage and current. A lowercase letter is employed for each to indicate that the quantity is time dependent; that is, its magnitude will change with time.

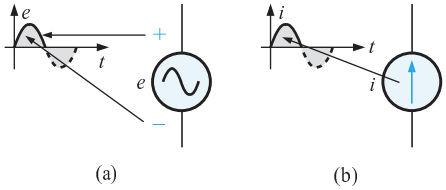


FIG. 13.10
(a) Sinusoidal ac voltage sources; (b) sinusoidal current sources.

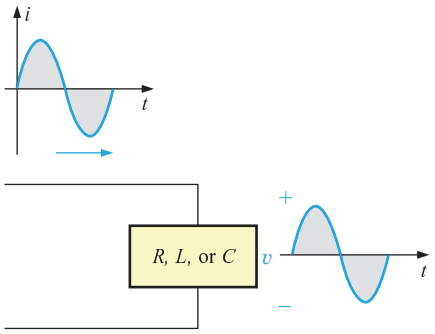


FIG. 13.11
The sine wave is the only alternating waveform whose shape is not altered by the response characteristics of a pure resistor, inductor, or capacitor.

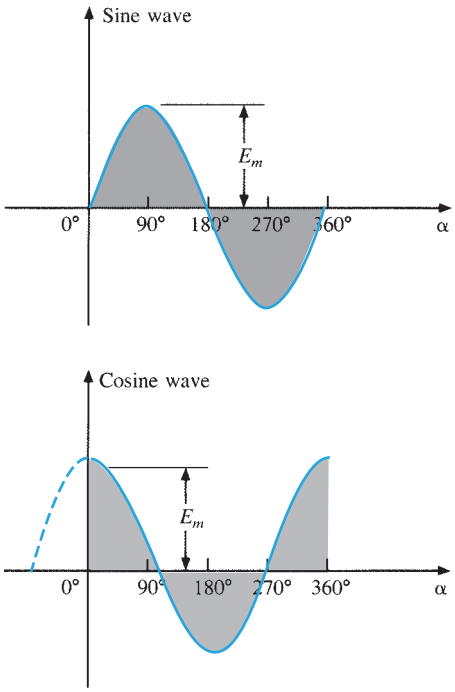


FIG. 13.12
Sine wave and cosine wave with the horizontal axis in degrees.

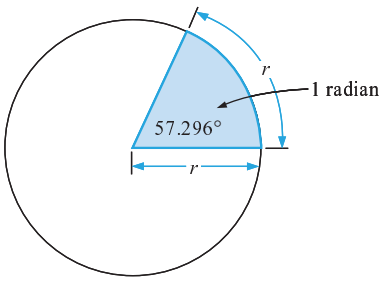


FIG. 13.13
Defining the radian.

The need for defining polarities and current direction will become quite obvious when we consider multisource ac networks. Note in the last sentence the absence of the term *sinusoidal* before the phrase *ac networks*. This phrase will be used to an increasing degree as we progress; *sinusoidal* is to be understood unless otherwise indicated.

13.3 THE SINE WAVE

The terms defined in the previous section can be applied to any type of periodic waveform, whether smooth or discontinuous. The sinusoidal waveform is of particular importance, however, since it lends itself readily to the mathematics and the physical phenomena associated with electric circuits. Consider the power of the following statement:

The sine wave is the only alternating waveform whose shape is unaffected by the response characteristics of R, L, and C elements.

In other words, if the voltage across (or current through) a resistor, coil, or capacitor is sinusoidal in nature, the resulting current (or voltage, respectively) for each will also have sinusoidal characteristics, as shown in Fig. 13.11. If a square wave or a triangular wave were applied, such would not be the case. It must be pointed out that the above statement is also applicable to the cosine wave, since the waves differ only by a 90° shift on the horizontal axis, as shown in Fig. 13.12.

The unit of measurement for the horizontal axis of Fig. 13.12 is the *degree*. A second unit of measurement frequently used is the **radian** (rad). It is defined by a quadrant of a circle such as in Fig. 13.13 where the distance subtended on the circumference equals the radius of the circle.

If we define x as the number of intervals of r (the radius) around the circumference of the circle, then

$$C = 2\pi r = x \cdot r$$

and we find

$$x = 2\pi$$

Therefore, there are 2π rad around a 360° circle, as shown in Fig. 13.14, and

$$2\pi \text{ rad} = 360° \tag{13.4}$$

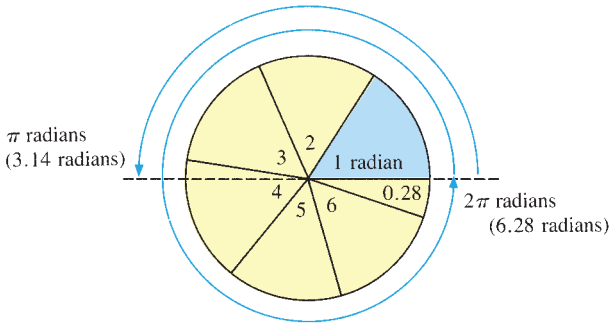


FIG. 13.14
There are 2π radians in one full circle of 360°.

with $$\boxed{1 \text{ rad} = 57.296^\circ \cong 57.3^\circ} \qquad (13.5)$$

A number of electrical formulas contain a multiplier of π. For this reason, it is sometimes preferable to measure angles in radians rather than in degrees.

The quantity π is the ratio of the circumference of a circle to its diameter.

π has been determined to an extended number of places primarily in an attempt to see if a repetitive sequence of numbers appears. It does not. A sampling of the effort appears below:

$$\pi = 3.14159\ \ 26535\ \ 89793\ \ 23846\ \ 26433\ldots$$

Although the approximation $\pi \cong 3.14$ is often applied, all the calculations in this text will use the π function as provided on all scientific calculators.

For 180° and 360°, the two units of measurement are related as shown in Fig. 13.14. The conversion equations between the two are the following:

$$\boxed{\text{Radians} = \left(\frac{\pi}{180^\circ}\right) \times (\text{degrees})} \qquad (13.6)$$

$$\boxed{\text{Degrees} = \left(\frac{180^\circ}{\pi}\right) \times (\text{radians})} \qquad (13.7)$$

Applying these equations, we find

$$\textbf{90°:}\quad \text{Radians} = \frac{\pi}{180^\circ}(90^\circ) = \frac{\pi}{2}\ \textbf{rad}$$

$$\textbf{30°:}\quad \text{Radians} = \frac{\pi}{180^\circ}(30^\circ) = \frac{\pi}{6}\ \textbf{rad}$$

$$\frac{\pi}{3}\ \textbf{rad:}\quad \text{Degrees} = \frac{180^\circ}{\pi}\left(\frac{\pi}{3}\right) = \textbf{60°}$$

$$\frac{3\pi}{2}\ \textbf{rad:}\quad \text{Degrees} = \frac{180^\circ}{\pi}\left(\frac{3\pi}{2}\right) = \textbf{270°}$$

Using the radian as the unit of measurement for the abscissa, we would obtain a sine wave, as shown in Fig. 13.15.

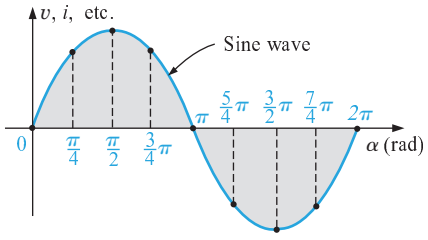


FIG. 13.15
Plotting a sine wave versus radians.

It is of particular interest that the sinusoidal waveform can be derived from the length of the *vertical projection* of a radius vector rotating in a uniform circular motion about a fixed point. Starting as shown in Fig. 13.16(a) and plotting the amplitude (above and below zero) on the coordinates drawn to the right [Figs. 13.16(b) through (i)], we will trace a complete sinusoidal waveform after the radius vector has completed a 360° rotation about the center.

The velocity with which the radius vector rotates about the center, called the **angular velocity,** can be determined from the following equation:

$$\boxed{\text{Angular velocity} = \frac{\text{distance (degrees or radians)}}{\text{time (seconds)}}} \qquad (13.8)$$

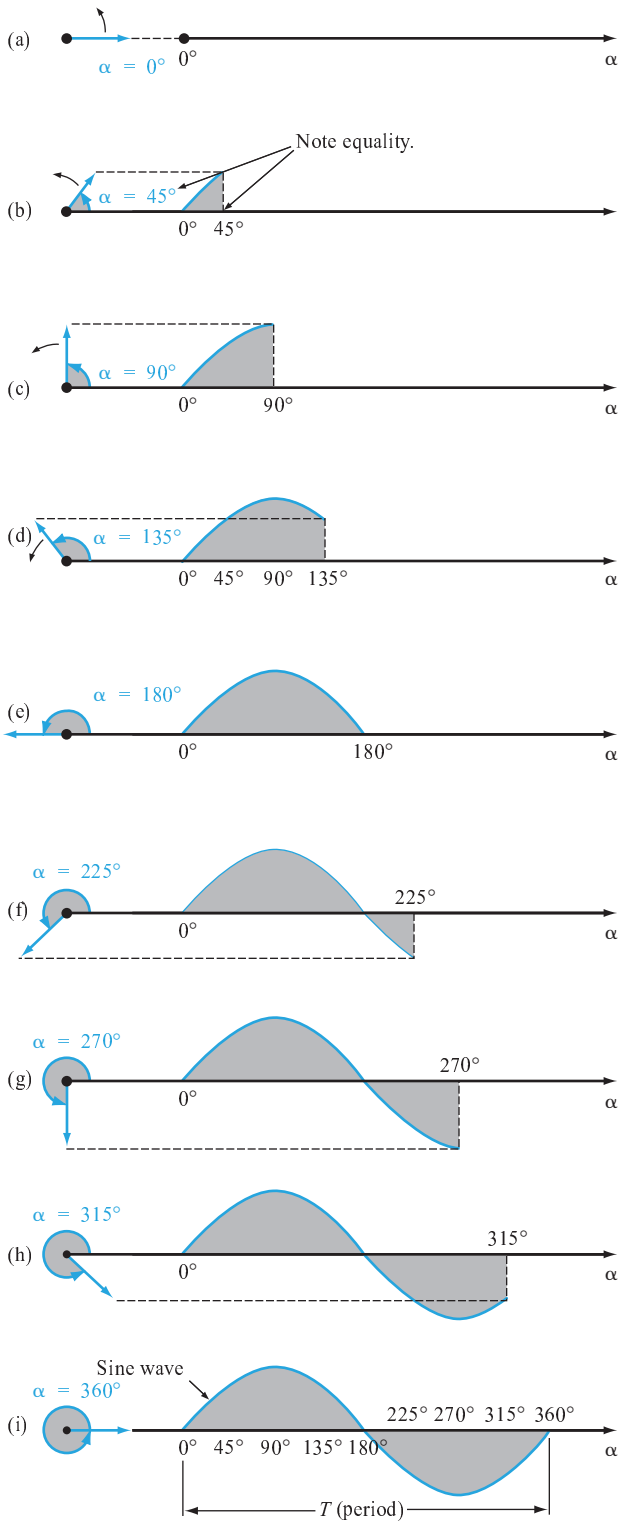


FIG. 13.16
Generating a sinusoidal waveform through the vertical projection of a rotating vector.

Substituting into Eq. (13.8) and assigning the Greek letter omega (ω) to the angular velocity, we have

$$\boxed{\omega = \frac{\alpha}{t}} \qquad \textbf{(13.9)}$$

and

$$\boxed{\alpha = \omega t} \qquad \textbf{(13.10)}$$

Since ω is typically provided in radians per second, the angle α obtained using Eq. (13.10) is usually in radians. If α is required in degrees, Equation (13.7) must be applied. The importance of remembering the above will become obvious in the examples to follow.

In Fig. 13.16, the time required to complete one revolution is equal to the period (T) of the sinusoidal waveform of Fig. 13.16(i). The radians subtended in this time interval are 2π. Substituting, we have

$$\boxed{\omega = \frac{2\pi}{T}} \quad \text{(rad/s)} \qquad \textbf{(13.11)}$$

In words, this equation states that the smaller the period of the sinusoidal waveform of Fig. 13.16(i), or the smaller the time interval before one complete cycle is generated, the greater must be the angular velocity of the rotating radius vector. Certainly this statement agrees with what we have learned thus far. We can now go one step further and apply the fact that the frequency of the generated waveform is inversely related to the period of the waveform; that is, $f = 1/T$. Thus,

$$\boxed{\omega = 2\pi f} \quad \text{(rad/s)} \qquad \textbf{(13.12)}$$

This equation states that the higher the frequency of the generated sinusoidal waveform, the higher must be the angular velocity. Equations (13.11) and (13.12) are verified somewhat by Fig. 13.17, where for the same radius vector, $\omega = 100$ rad/s and 500 rad/s.

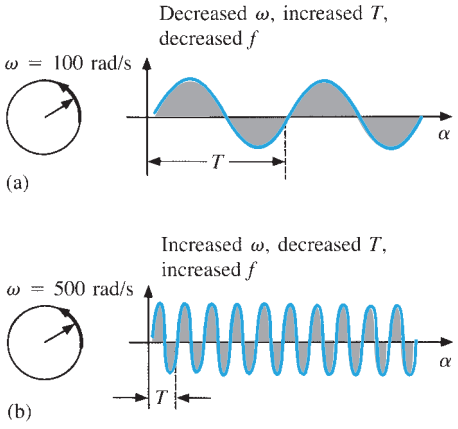


FIG. 13.17
Demonstrating the effect of ω on the frequency and period.

EXAMPLE 13.4 Determine the angular velocity of a sine wave having a frequency of 60 Hz.

Solution:

$$\omega = 2\pi f = (2\pi)(60 \text{ Hz}) \cong \mathbf{377 \text{ rad/s}}$$

(a recurring value due to 60-Hz predominance)

EXAMPLE 13.5 Determine the frequency and period of the sine wave of Fig. 13.17(b).

Solution: Since $\omega = 2\pi/T$,

$$T = \frac{2\pi}{\omega} = \frac{2\pi \text{ rad}}{500 \text{ rad/s}} = \frac{2\pi \text{ rad}}{500 \text{ rad/s}} = \mathbf{12.57 \text{ ms}}$$

and

$$f = \frac{1}{T} = \frac{1}{12.57 \times 10^{-3} \text{ s}} = \mathbf{79.58 \text{ Hz}}$$

EXAMPLE 13.6 Given $\omega = 200$ rad/s, determine how long it will take the sinusoidal waveform to pass through an angle of 90°.

Solution: Eq. (13.10): $\alpha = \omega t$, and

$$t = \frac{\alpha}{\omega}$$

However, α must be substituted as $\pi/2$ (= 90°) since ω is in radians per second:

$$t = \frac{\alpha}{\omega} = \frac{\pi/2 \text{ rad}}{200 \text{ rad/s}} = \frac{\pi}{400 \text{ s}} = \mathbf{7.85 \text{ ms}}$$

EXAMPLE 13.7 Find the angle through which a sinusoidal waveform of 60 Hz will pass in a period of 5 ms.

Solution: Eq. (13.11): $\alpha = \omega t$, or

$$\alpha = 2\pi ft = (2\pi)(60 \text{ Hz})(5 \times 10^{-3} \text{ s}) = \mathbf{1.885 \text{ rad}}$$

If not careful, one might be tempted to interpret the answer as 1.885°. However,

$$\alpha\,(^\circ) = \frac{180^\circ}{\pi \text{ rad}}(1.885 \text{ rad}) = \mathbf{108^\circ}$$

13.4 GENERAL FORMAT FOR THE SINUSOIDAL VOLTAGE OR CURRENT

The basic mathematical format for the sinusoidal waveform is

$$\boxed{A_m \sin \alpha} \qquad \textbf{(13.13)}$$

where A_m is the peak value of the waveform and α is the unit of measure for the horizontal axis, as shown in Fig. 13.18.

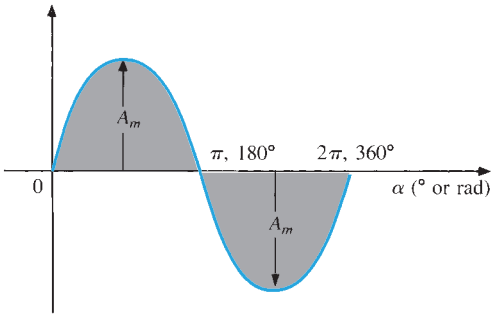


FIG. 13.18
Basic sinusoidal function.

The equation $\alpha = \omega t$ states that the angle α through which the rotating vector of Fig. 13.16 will pass is determined by the angular velocity of the rotating vector and the length of time the vector rotates. For example, for a particular angular velocity (fixed ω), the longer the radius vector is permitted to rotate (that is, the greater the value of t), the greater will be the number of degrees or radians through which the vector will pass. Relating this statement to the sinusoidal waveform, for a particular angular velocity, the longer the time, the greater the num-

ber of cycles shown. For a fixed time interval, the greater the angular velocity, the greater the number of cycles generated.

Due to Eq. (13.10), the general format of a sine wave can also be written

$$\boxed{A_m \sin \omega t} \tag{13.14}$$

with ωt as the horizontal unit of measure.

For electrical quantities such as current and voltage, the general format is

$$i = I_m \sin \omega t = I_m \sin \alpha$$
$$e = E_m \sin \omega t = E_m \sin \alpha$$

where the capital letters with the subscript m represent the amplitude, and the lowercase letters i and e represent the instantaneous value of current or voltage, respectively, at any time t. This format is particularly important since it presents the sinusoidal voltage or current as a function of time, which is the horizontal scale for the oscilloscope. Recall that the horizontal sensitivity of a scope is in time per division and not degrees per centimeter.

EXAMPLE 13.8 Given $e = 5 \sin \alpha$, determine e at $\alpha = 40°$ and $\alpha = 0.8\pi$.

Solution: For $\alpha = 40°$,

$$e = 5 \sin 40° = 5(0.6428) = \mathbf{3.214\ V}$$

For $\alpha = 0.8\pi$,

$$\alpha\,(°) = \frac{180°}{\pi}(0.8\pi) = 144°$$

and

$$e = 5 \sin 144° = 5(0.5878) = \mathbf{2.939\ V}$$

The conversion to degrees will not be required for most modern-day scientific calculators since they can perform the function directly. First, be sure that the calculator is in the RAD mode. Then simply enter the radian measure and use the appropriate trigonometric key (sin, cos, tan, etc.).

The angle at which a particular voltage level is attained can be determined by rearranging the equation

$$e = E_m \sin \alpha$$

in the following manner:

$$\sin \alpha = \frac{e}{E_m}$$

which can be written

$$\boxed{\alpha = \sin^{-1} \frac{e}{E_m}} \tag{13.15}$$

Similarly, for a particular current level,

$$\boxed{\alpha = \sin^{-1} \frac{i}{I_m}} \tag{13.16}$$

The function $\sin^{-1}$ is available on all scientific calculators.

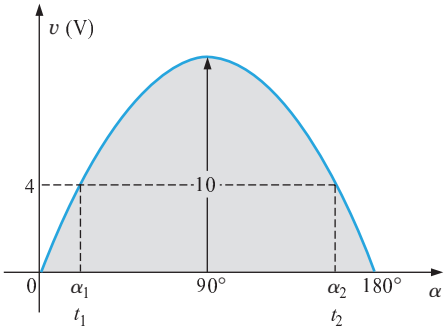


FIG. 13.19
Example 13.9.

EXAMPLE 13.9

a. Determine the angle at which the magnitude of the sinusoidal function $v = 10 \sin 377t$ is 4 V.
b. Determine the time at which the magnitude is attained.

Solutions:

a. Eq. (13.15):

$$\alpha_1 = \sin^{-1}\frac{v}{E_m} = \sin^{-1}\frac{4\text{ V}}{10\text{ V}} = \sin^{-1} 0.4 = \mathbf{23.578°}$$

However, Figure 13.19 reveals that the magnitude of 4 V (positive) will be attained at two points between 0° and 180°. The second intersection is determined by

$$\alpha_2 = 180° - 23.578° = \mathbf{156.422°}$$

In general, therefore, keep in mind that Equations (13.15) and (13.16) will provide an angle with a magnitude between 0° and 90°.

b. Eq. (13.10): $\alpha = \omega t$, and so $t = \alpha/\omega$. However, α must be in radians. Thus,

$$\alpha\text{ (rad)} = \frac{\pi}{180°}(23.578°) = 0.411\text{ rad}$$

and

$$t_1 = \frac{\alpha}{\omega} = \frac{0.411\text{ rad}}{377\text{ rad/s}} = \mathbf{1.09\text{ ms}}$$

For the second intersection,

$$\alpha\text{ (rad)} = \frac{\pi}{180°}(156.422°) = 2.73\text{ rad}$$

$$t_2 = \frac{\alpha}{\omega} = \frac{2.73\text{ rad}}{377\text{ rad/s}} = \mathbf{7.24\text{ ms}}$$

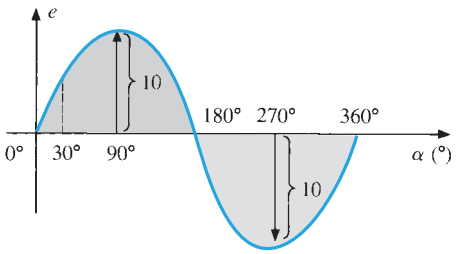


FIG. 13.20
Example 13.10, horizontal axis in degrees.

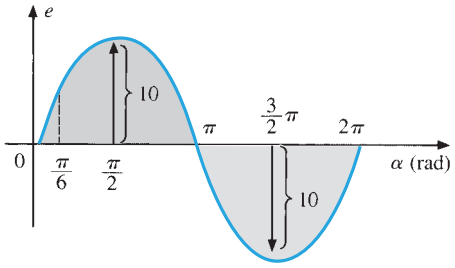


FIG. 13.21
Example 13.10, horizontal axis in radians.

The sine wave can also be plotted against *time* on the horizontal axis. The time period for each interval can be determined from $t = \alpha/\omega$, but the most direct route is simply to find the period T from $T = 1/f$ and break it up into the required intervals. This latter technique will be demonstrated in Example 13.10.

Before reviewing the example, take special note of the relative simplicity of the mathematical equation that can represent a sinusoidal waveform. Any alternating waveform whose characteristics differ from those of the sine wave cannot be represented by a single term, but may require two, four, six, or perhaps an infinite number of terms to be represented accurately. Additional description of nonsinusoidal waveforms can be found in Chapter 24.

EXAMPLE 13.10

Sketch $e = 10 \sin 314t$ with the abscissa
a. angle (α) in degrees.
b. angle (α) in radians.
c. time (t) in seconds.

Solutions:

a. See Fig 13.20. (Note that no calculations are required.)
b. See Fig. 13.21. (Once the relationship between degrees and radians is understood, there is again no need for calculations.)

c. 360°: $T = \dfrac{2\pi}{\omega} = \dfrac{2\pi}{314} = 20 \text{ ms}$

180°: $\dfrac{T}{2} = \dfrac{20 \text{ ms}}{2} = 10 \text{ ms}$

90°: $\dfrac{T}{4} = \dfrac{20 \text{ ms}}{4} = 5 \text{ ms}$

30°: $\dfrac{T}{12} = \dfrac{20 \text{ ms}}{12} = 1.67 \text{ ms}$

See Fig. 13.22.

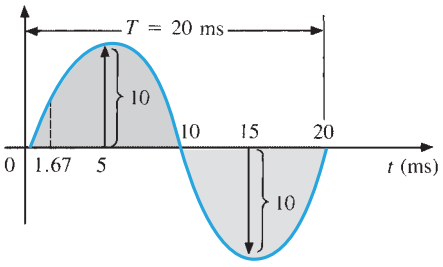


FIG. 13.22
Example 13.10, horizontal axis in milliseconds.

EXAMPLE 13.11 Given $i = 6 \times 10^{-3} \sin 1000t$, determine i at $t = 2$ ms.

Solution:

$$\alpha = \omega t = 1000t = (1000 \text{ rad/s})(2 \times 10^{-3} \text{ s}) = 2 \text{ rad}$$

$$\alpha\,(^\circ) = \frac{180^\circ}{\pi \text{ rad}}(2 \text{ rad}) = 114.59^\circ$$

$$i = (6 \times 10^{-3})(\sin 114.59^\circ)$$
$$= (6 \text{ mA})(0.9093) = \mathbf{5.46 \text{ mA}}$$

13.5 PHASE RELATIONS

Thus far, we have considered only sine waves that have maxima at $\pi/2$ and $3\pi/2$, with a zero value at 0, π, and 2π, as shown in Fig. 13.21. If the waveform is shifted to the right or left of 0°, the expression becomes

$$A_m \sin(\omega t \pm \theta) \qquad \textbf{(13.17)}$$

where θ is the angle in degrees or radians that the waveform has been shifted.

If the waveform passes through the horizontal axis with a *positive-going* (increasing with time) slope *before* 0°, as shown in Fig. 13.23, the expression is

$$A_m \sin(\omega t + \theta) \qquad \textbf{(13.18)}$$

At $\omega t = \alpha = 0°$, the magnitude is determined by $A_m \sin \theta$. If the waveform passes through the horizontal axis with a positive-going slope *after* 0°, as shown in Fig. 13.24, the expression is

$$A_m \sin(\omega t - \theta) \qquad \textbf{(13.19)}$$

And at $\omega t = \alpha = 0°$, the magnitude is $A_m \sin(-\theta)$, which, by a trigonometric identity, is $-A_m \sin \theta$.

If the waveform crosses the horizontal axis with a positive-going slope 90° ($\pi/2$) sooner, as shown in Fig. 13.25, it is called a *cosine wave;* that is,

$$\sin(\omega t + 90^\circ) = \sin\left(\omega t + \frac{\pi}{2}\right) = \cos \omega t \qquad \textbf{(13.20)}$$

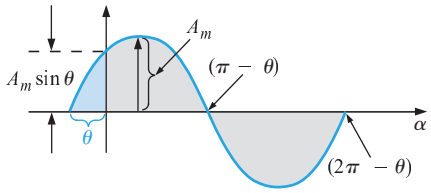


FIG. 13.23
Defining the phase shift for a sinusoidal function that crosses the horizontal axis with a positive slope before 0°.

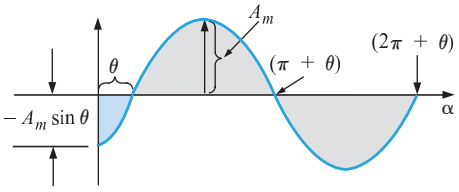


FIG. 13.24
Defining the phase shift for a sinusoidal function that crosses the horizontal axis with a positive slope after 0°.

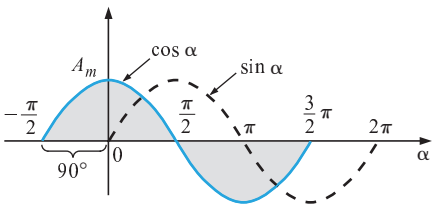


FIG. 13.25
Phase relationship between a sine wave and a cosine wave.

or
$$\sin \omega t = \cos(\omega t - 90°) = \cos\left(\omega t - \frac{\pi}{2}\right) \tag{13.21}$$

The terms *lead* and *lag* are used to indicate the relationship between two sinusoidal waveforms of the *same frequency* plotted on the same set of axes. In Fig. 13.25, the cosine curve is said to *lead* the sine curve by 90°, and the sine curve is said to *lag* the cosine curve by 90°. The 90° is referred to as the phase angle between the two waveforms. In language commonly applied, the waveforms are *out of phase* by 90°. Note that the phase angle between the two waveforms is measured between those two points on the horizontal axis through which each passes with the *same slope*. If both waveforms cross the axis at the same point with the same slope, they are *in phase*.

The geometric relationship between various forms of the sine and cosine functions can be derived from Fig. 13.26. For instance, starting at the sin α position, we find that cos α is an additional 90° in the counterclockwise direction. Therefore, cos α = sin(α + 90°). For −sin α we must travel 180° in the counterclockwise (or clockwise) direction so that −sin α = sin($\alpha \pm 180°$), and so on, as listed below:

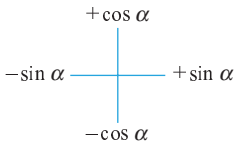


FIG. 13.26
Graphic tool for finding the relationship between specific sine and cosine functions.

$$\begin{aligned} \cos \alpha &= \sin(\alpha + 90°) \\ \sin \alpha &= \cos(\alpha - 90°) \\ -\sin \alpha &= \sin(\alpha \pm 180°) \\ -\cos \alpha &= \sin(\alpha + 270°) = \sin(\alpha - 90°) \\ &\text{etc.} \end{aligned} \tag{13.22}$$

In addition, one should be aware that

$$\begin{aligned} \sin(-\alpha) &= -\sin \alpha \\ \cos(-\alpha) &= \cos \alpha \end{aligned} \tag{13.23}$$

If a sinusoidal expression should appear as

$$e = -E_m \sin \omega t$$

the negative sign is associated with the sine portion of the expression, not the peak value E_m. In other words, the expression, if not for convenience, would be written

$$e = E_m(-\sin \omega t)$$

Since

$$-\sin \omega t = \sin(\omega t \pm 180°)$$

the expression can also be written

$$e = E_m \sin(\omega t \pm 180°)$$

revealing that a negative sign can be replaced by a 180° change in phase angle (+ or −); that is,

$$\begin{aligned} e &= E_m \sin \omega t = E_m \sin(\omega t + 180°) \\ &= E_m \sin(\omega t - 180°) \end{aligned}$$

A plot of each will clearly show their equivalence. There are, therefore, two correct mathematical representations for the functions.