The **phase relationship** between two waveforms indicates which one leads or lags, and by how many degrees or radians.

EXAMPLE 13.12 What is the phase relationship between the sinusoidal waveforms of each of the following sets?

a. $v = 10 \sin(\omega t + 30°)$
   $i = 5 \sin(\omega t + 70°)$
b. $i = 15 \sin(\omega t + 60°)$
   $v = 10 \sin(\omega t - 20°)$
c. $i = 2 \cos(\omega t + 10°)$
   $v = 3 \sin(\omega t - 10°)$
d. $i = -\sin(\omega t + 30°)$
   $v = 2 \sin(\omega t + 10°)$
e. $i = -2 \cos(\omega t - 60°)$
   $v = 3 \sin(\omega t - 150°)$

Solutions:

a. See Fig. 13.27.
   ***i* leads *v* by 40°, or *v* lags *i* by 40°.**

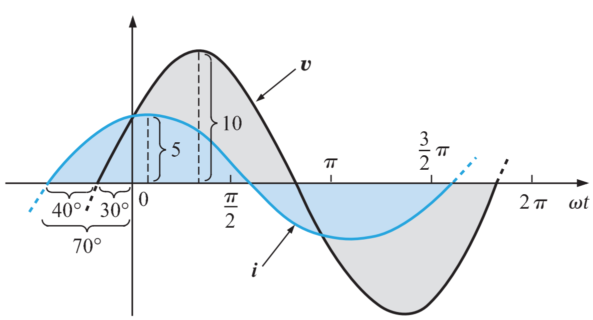


FIG. 13.27
Example 13.12; i leads v by 40°.

b. See Fig. 13.28.
   ***i* leads *v* by 80°, or *v* lags *i* by 80°.**

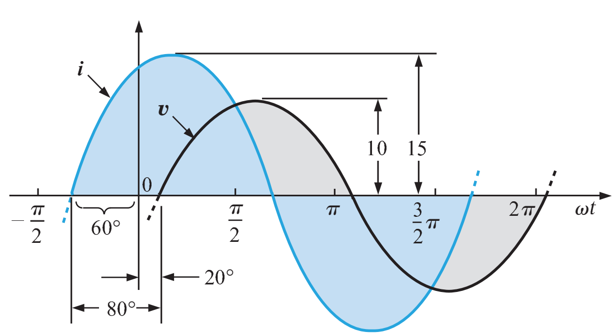


FIG. 13.28
Example 13.12; i leads v by 80°.

c. See Fig. 13.29.

$$i = 2\cos(\omega t + 10°) = 2\sin(\omega t + 10° + 90°)$$
$$= 2\sin(\omega t + 100°)$$

***i* leads *v* by 110°, or *v* lags *i* by 110°.**

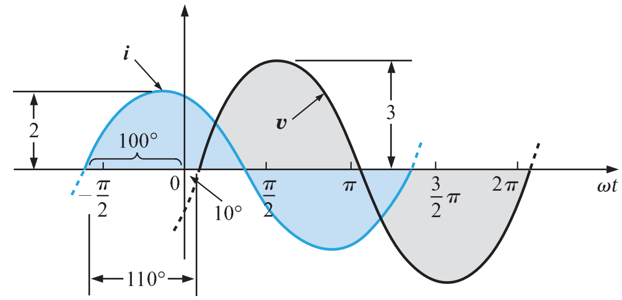


FIG. 13.29
Example 13.12; i leads v by 110°.

d. See Fig. 13.30.

$$-\sin(\omega t + 30°) = \sin(\omega t + 30° - 180°)$$ (Note)
$$= \sin(\omega t - 150°)$$

***v* leads *i* by 160°, or *i* lags *v* by 160°.**

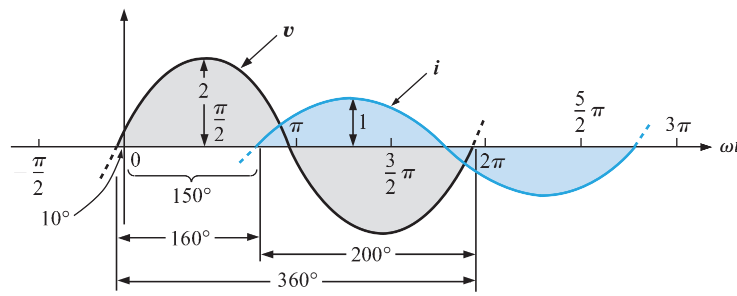


FIG. 13.30
Example 13.12; v leads i by 160°.

Or using

$$-\sin(\omega t + 30°) = \sin(\omega t + 30° + 180°)$$ (Note)
$$= \sin(\omega t + 210°)$$

***i* leads *v* by 200°, or *v* lags *i* by 200°.**

e. See Fig. 13.31.

$$i = -2\cos(\omega t - 60°) = 2\cos(\omega t - 60° - 180°)$$ (By choice)
$$= 2\cos(\omega t - 240°)$$

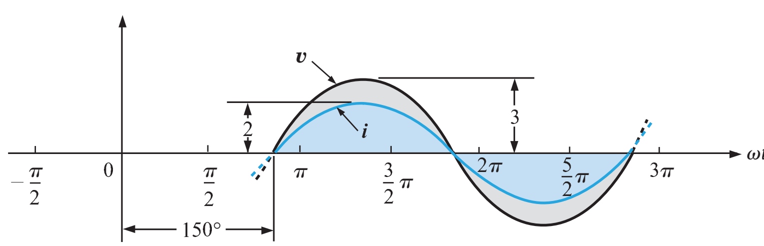


FIG. 13.31
Example 13.12; v and i are in phase.

However, $\cos \alpha = \sin(\alpha + 90°)$

so that $2\cos(\omega t - 240°) = 2\sin(\omega t - 240° + 90°)$
$= 2\sin(\omega t - 150°)$

***v* and *i* are in phase.**

Phase Measurements

The hookup procedure for using an oscilloscope to measure phase angles is covered in detail in Section 15.13. However, the equation for determining the phase angle can be introduced using Fig. 13.32. First, note that each sinusoidal function has the same frequency, permitting the use of either waveform to determine the period. For the waveform chosen in Fig. 13.32, the period encompasses 5 divisions at 0.2 ms/div. The phase shift between the waveforms (irrespective of which is leading or lagging) is 2 divisions. Since the full period represents a cycle of 360°, the following ratio [from which Equation (13.24) can be derived] can be formed:

$$\frac{360°}{T\text{ (no. of div.)}} = \frac{\theta}{\text{phase shift (no. of div.)}}$$

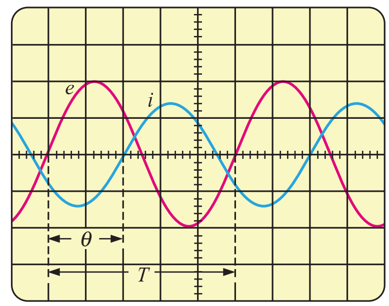
and

$$\theta = \frac{\text{phase shift (no. of div.)}}{T\text{ (no. of div.)}} \times 360° \qquad \textbf{(13.24)}$$

Substituting into Eq. (13.24) will result in

$$\theta = \frac{(2\text{ div.})}{(5\text{ div.})} \times 360° = 144°$$

and *e* leads *i* by 144°.



Vertical sensitivity = 2 V/div.
Horizontal sensitivity = 0.2 ms/div.

FIG. 13.32
Finding the phase angle between waveforms using a dual-trace oscilloscope.

13.6 AVERAGE VALUE

Even though the concept of the **average value** is an important one in most technical fields, its true meaning is often misunderstood. In Fig. 13.33(a), for example, the average height of the sand may be required to determine the volume of sand available. The average height of the sand is that height obtained if the distance from one end to the other is maintained while the sand is leveled off, as shown in Fig. 13.33(b). The area under the mound of Fig. 13.33(a) will then equal the area under the rectangular shape of Fig. 13.33(b) as determined by $A = b \times h$. Of course, the depth (into the page) of the sand must be the same for Fig. 13.33(a) and (b) for the preceding conclusions to have any meaning.

In Fig. 13.33 the distance was measured from one end to the other. In Fig. 13.34(a) the distance extends beyond the end of the original pile of Fig. 13.33. The situation could be one where a landscaper would like to know the average height of the sand if spread out over a distance such as defined in Fig. 13.34(a). The result of an increased distance is as shown in Fig. 13.34(b). The average height has decreased compared to Fig. 13.33. Quite obviously, therefore, the longer the distance, the lower is the average value.

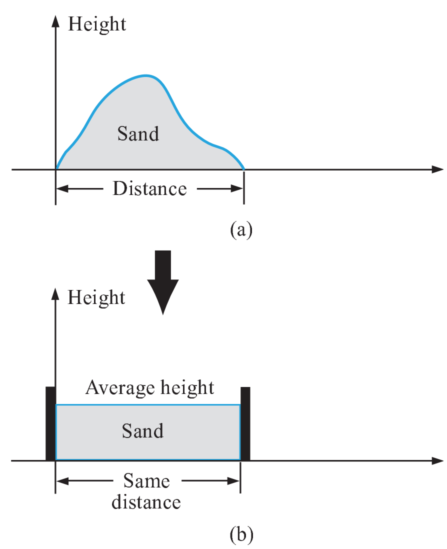


FIG. 13.33
Defining average value.

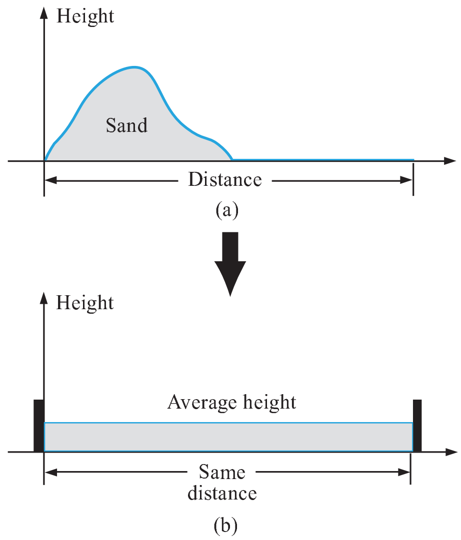


FIG. 13.34
Effect of distance (length) on average value.

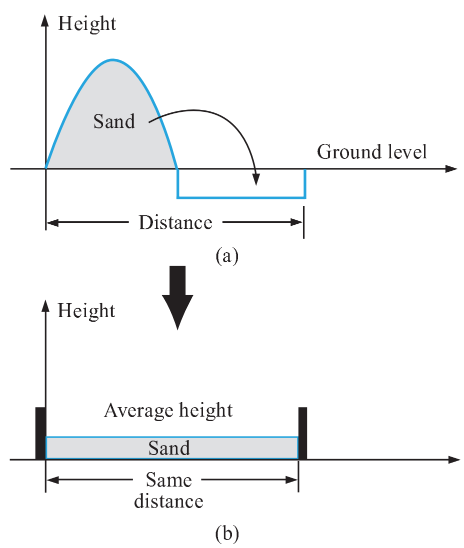


FIG. 13.35
Effect of depressions (negative excursions) on average value.

If the distance parameter includes a depression, as shown in Fig. 13.35(a), some of the sand will be used to fill the depression, resulting in an even lower average value for the landscaper, as shown in Fig. 13.35(b). For a sinusoidal waveform, the depression would have the same shape as the mound of sand (over one full cycle), resulting in an average value at ground level (or zero volts for a sinusoidal voltage over one full period).

After traveling a considerable distance by car, some drivers like to calculate their average speed for the entire trip. This is usually done by dividing the miles traveled by the hours required to drive that distance. For example, if a person traveled 225 mi in 5 h, the average speed was 225 mi/5 h, or 45 mi/h. This same distance may have been traveled at various speeds for various intervals of time, as shown in Fig. 13.36.

By finding the total area under the curve for the 5 h and then dividing the area by 5 h (the total time for the trip), we obtain the same result of 45 mi/h; that is,

$$\text{Average speed} = \frac{\text{area under curve}}{\text{length of curve}} \tag{13.25}$$

$$\begin{aligned}\text{Average speed} &= \frac{A_1 + A_2}{5\text{ h}} \\ &= \frac{(60\text{ mi/h})(2\text{ h}) + (50\text{ mi/h})(2.5\text{ h})}{5\text{ h}} \\ &= \frac{225}{5}\text{ mi/h} \\ &= \mathbf{45\ mi/h}\end{aligned}$$

Equation (13.25) can be extended to include any variable quantity, such as current or voltage, if we let G denote the average value, as follows:

$$G\ \text{(average value)} = \frac{\text{algebraic sum of areas}}{\text{length of curve}} \tag{13.26}$$

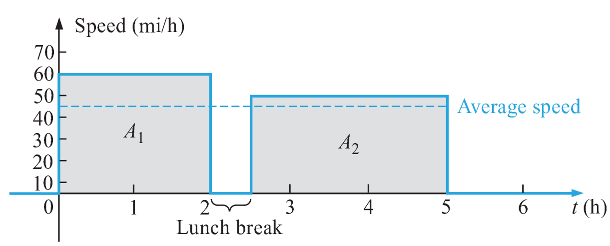


FIG. 13.36
Plotting speed versus time for an automobile excursion.

The *algebraic* sum of the areas must be determined, since some area contributions will be from below the horizontal axis. Areas above the axis will be assigned a positive sign, and those below, a negative sign. A positive average value will then be above the axis, and a negative value, below.

The average value of *any* current or voltage is the value indicated on a dc meter. In other words, over a complete cycle, the average value is the equivalent dc value. In the analysis of electronic circuits to be considered in a later course, both dc and ac sources of voltage will be applied to the same network. It will then be necessary to know or determine the dc (or average value) and ac components of the voltage or current in various parts of the system.

EXAMPLE 13.13 Determine the average value of the waveforms of Fig. 13.37.

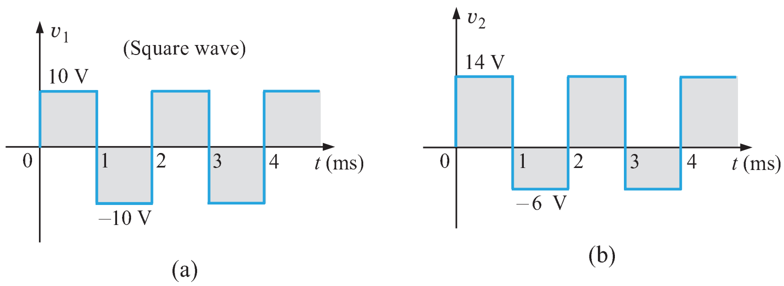


FIG. 13.37
Example 13.13.

Solutions:

a. By inspection, the area above the axis equals the area below over one cycle, resulting in an average value of zero volts. Using Eq. (13.26):

$$G = \frac{(10\text{ V})(1\text{ ms}) - (10\text{ V})(1\text{ ms})}{2\text{ ms}}$$

$$= \frac{0}{2\text{ ms}} = \mathbf{0\ V}$$

b. Using Eq. (13.26):

$$G = \frac{(14\text{ V})(1\text{ ms}) - (6\text{ V})(1\text{ ms})}{2\text{ ms}}$$

$$= \frac{14\text{ V} - 6\text{ V}}{2} = \frac{8\text{ V}}{2} = \mathbf{4\ V}$$

as shown in Fig. 13.38.

In reality, the waveform of Fig. 13.37(b) is simply the square wave of Fig. 13.37(a) with a dc shift of 4 V; that is,

$$v_2 = v_1 + 4\text{ V}$$

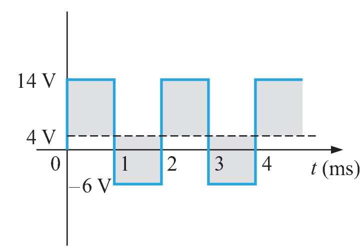


FIG. 13.38
Defining the average value for the waveform of Fig. 13.37(b).

EXAMPLE 13.14 Find the average values of the following waveforms over one full cycle:

a. Fig. 13.39.
b. Fig. 13.40.

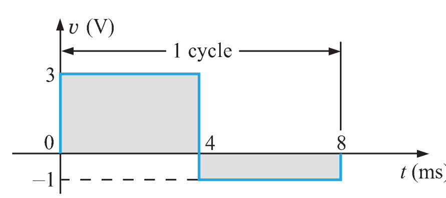


FIG. 13.39
Example 13.14, part (a).

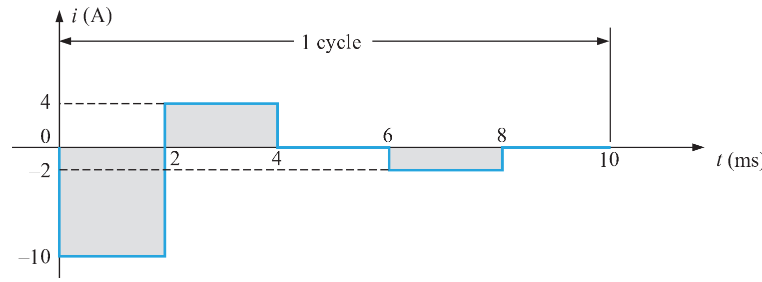


FIG. 13.40
Example 13.14, part (b).

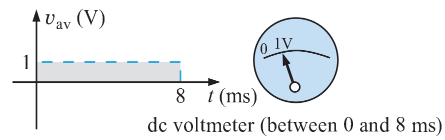


FIG. 13.41
The response of a dc meter to the waveform of Fig. 13.39.

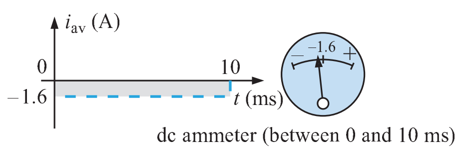


FIG. 13.42
The response of a dc meter to the waveform of Fig. 13.40.

Solutions:

a. $$G = \frac{+(3\text{ V})(4\text{ ms}) - (1\text{ V})(4\text{ ms})}{8\text{ ms}} = \frac{12\text{ V} - 4\text{ V}}{8} = \mathbf{1\ V}$$

Note Fig. 13.41.

b. $$G = \frac{-(10\text{ V})(2\text{ ms}) + (4\text{ V})(2\text{ ms}) - (2\text{ V})(2\text{ ms})}{10\text{ ms}}$$

$$= \frac{-20\text{ V} + 8\text{ V} - 4\text{ V}}{10} = -\frac{16\text{ V}}{10} = \mathbf{-1.6\ V}$$

Note Fig. 13.42.

We found the areas under the curves in the preceding example by using a simple geometric formula. If we should encounter a sine wave or any other unusual shape, however, we must find the area by some other means. We can obtain a good approximation of the area by attempting to reproduce the original wave shape using a number of small rectangles or other familiar shapes, the area of which we already know through simple geometric formulas. For example,

the area of the positive (or negative) pulse of a sine wave is $2A_m$.

Approximating this waveform by two triangles (Fig. 13.43), we obtain (using *area* = 1/2 *base* × *height* for the area of a triangle) a rough idea of the actual area:

$$\text{Area shaded} = 2\left(\frac{1}{2}bh\right) = 2\left[\left(\frac{1}{2}\right)\overbrace{\left(\frac{\pi}{2}\right)}^{b}\overbrace{(A_m)}^{h}\right] = \frac{\pi}{2}A_m$$
$$\cong 1.58A_m$$

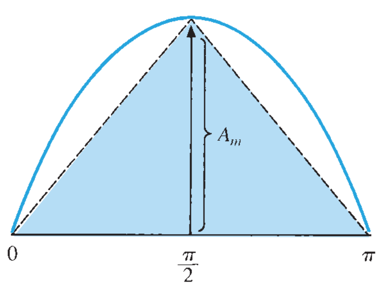


FIG. 13.43
Approximating the shape of the positive pulse of a sinusoidal waveform with two right triangles.

A closer approximation might be a rectangle with two similar triangles (Fig. 13.44):

$$\text{Area} = A_m\frac{\pi}{3} + 2\left(\frac{1}{2}\ bh\right) = A_m\frac{\pi}{3} + \frac{\pi}{3}\ A_m = \frac{2}{3}\pi A_m$$
$$= 2.094A_m$$

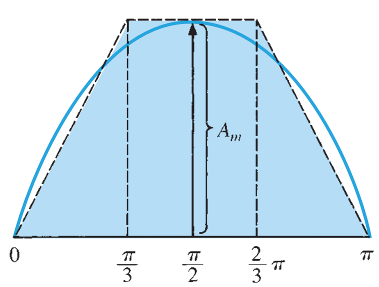


FIG. 13.44
A better approximation for the shape of the positive pulse of a sinusoidal waveform.

which is certainly close to the actual area. If an infinite number of forms were used, an exact answer of $2A_m$ could be obtained. For irregular waveforms, this method can be especially useful if data such as the average value are desired.

The procedure of calculus that gives the exact solution $2A_m$ is known as *integration*. Integration is presented here only to make the method recognizable to the reader; it is not necessary to be proficient in its use to continue with this text. It is a useful mathematical tool, however, and should be learned. Finding the area under the positive pulse of a sine wave using integration, we have

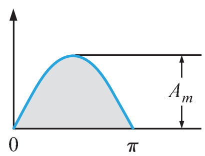
$$\text{Area} = \int_0^{\pi} A_m \sin \alpha \, d\alpha$$

where $\int$ is the sign of integration, 0 and π are the limits of integration, $A_m \sin \alpha$ is the function to be integrated, and $d\alpha$ indicates that we are integrating with respect to α.

Integrating, we obtain

$$\begin{aligned}\text{Area} &= A_m[-\cos \alpha]_0^{\pi} \\ &= -A_m(\cos \pi - \cos 0°) \\ &= -A_m[-1 - (+1)] = -A_m(-2)\end{aligned}$$

$$\boxed{\text{Area} = 2A_m} \qquad \textbf{(13.27)}$$

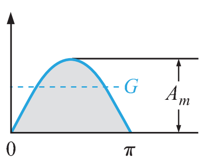


Since we know the area under the positive (or negative) pulse, we can easily determine the average value of the positive (or negative) region of a sine wave pulse by applying Eq. (13.26):

$$G = \frac{2A_m}{\pi}$$

and

$$\boxed{G = 0.637A_m} \qquad \textbf{(13.28)}$$



For the waveform of Fig. 13.45,

$$G = \frac{(2A_m/2)}{\pi/2} = \frac{2A_m}{\pi} \qquad \text{(average the same as for a full pulse)}$$

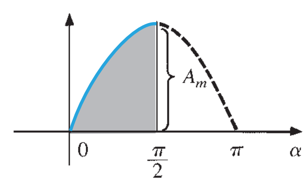


FIG. 13.45
Finding the average value of one-half the positive pulse of a sinusoidal waveform.

EXAMPLE 13.15 Determine the average value of the sinusoidal waveform of Fig. 13.46.

Solution: By inspection it is fairly obvious that

the average value of a pure sinusoidal waveform over one full cycle is zero.

Eq. (13.26):

$$G = \frac{+2A_m - 2A_m}{2\pi} = \mathbf{0\ V}$$

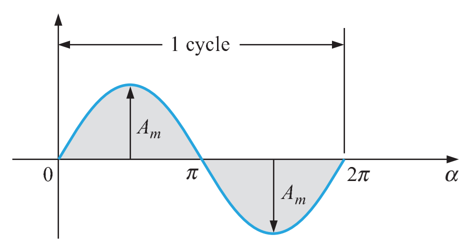


FIG. 13.46
Example 13.15.

EXAMPLE 13.16 Determine the average value of the waveform of Fig. 13.47.

Solution: The peak-to-peak value of the sinusoidal function is 16 mV + 2 mV = 18 mV. The peak amplitude of the sinusoidal waveform is, therefore, 18 mV/2 = 9 mV. Counting down 9 mV from 2 mV (or 9 mV up from −16 mV) results in an average or dc level of −7 mV, as noted by the dashed line of Fig. 13.47.

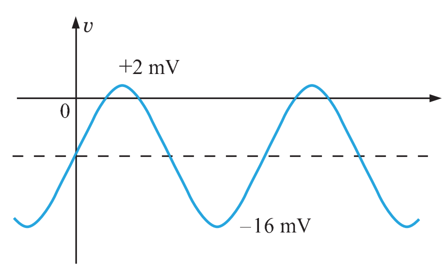


FIG. 13.47
Example 13.16.

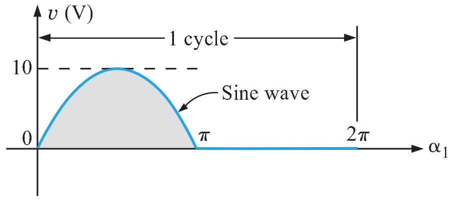


FIG. 13.48
Example 13.17.

EXAMPLE 13.17 Determine the average value of the waveform of Fig. 13.48.

Solution:

$$G = \frac{2A_m + 0}{2\pi} = \frac{2(10\text{ V})}{2\pi} \cong \mathbf{3.18\text{ V}}$$

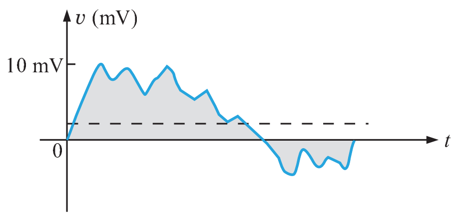


FIG. 13.49
Example 13.18.

EXAMPLE 13.18 For the waveform of Fig. 13.49, determine whether the average value is positive or negative, and determine its approximate value.

Solution: From the appearance of the waveform, the average value is positive and in the vicinity of 2 mV. Occasionally, judgments of this type will have to be made.

Instrumentation

The dc level or average value of any waveform can be found using a digital multimeter (DMM) or an **oscilloscope.** For purely dc circuits, simply set the DMM on dc, and read the voltage or current levels. Oscilloscopes are limited to voltage levels using the sequence of steps listed below:

1. First choose GND from the DC-GND-AC option list associated with each vertical channel. The GND option blocks any signal to which the oscilloscope probe may be connected from entering the oscilloscope and responds with just a horizontal line. Set the resulting line in the middle of the vertical axis on the horizontal axis, as shown in Fig. 13.50(a).

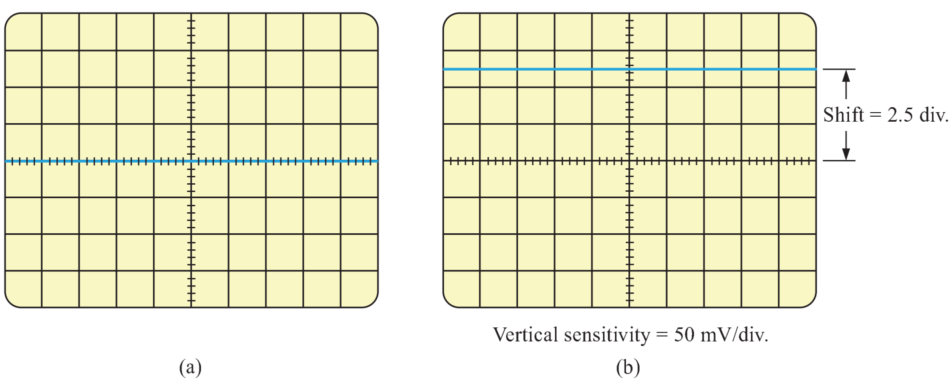


FIG. 13.50
Using the oscilloscope to measure dc voltages: (a) setting the GND condition; (b) the vertical shift resulting from a dc voltage when shifted to the DC option.

2. Apply the oscilloscope probe to the voltage to be measured (if not already connected), and switch to the DC option. If a dc voltage is present, the horizontal line will shift up or down, as demonstrated in Fig. 13.50(b). Multiplying the shift by the vertical sensitivity will result in the dc voltage. An upward shift is a positive voltage (higher potential at the red or positive lead of the oscilloscope), while a downward shift is a negative voltage (lower potential at the red or positive lead of the oscilloscope).

In general,

$$V_{dc} = (\text{vertical shift in div.}) \times (\text{vertical sensitivity in V/div.}) \quad \textbf{(13.29)}$$

For the waveform of Fig. 13.50(b),

$$V_{dc} = (2.5 \text{ div.})(50 \text{ mV/div.}) = \mathbf{125\ mV}$$

The oscilloscope can also be used to measure the dc or average level of any waveform using the following sequence:

1. Using the GND option, reset the horizontal line to the middle of the screen.
2. Switch to AC (all dc components of the signal to which the probe is connected will be blocked from entering the oscilloscope—only the alternating, or changing, components will be displayed). Note the location of some definitive point on the waveform, such as the bottom of the half-wave rectified waveform of Fig. 13.51(a); that is, note its position on the vertical scale. For the future, whenever you use the AC option, keep in mind that the computer will distribute the waveform above and below the horizontal axis such that the average value is zero; that is, the area above the axis will equal the area below.
3. Then switch to DC (to permit both the dc and the ac components of the waveform to enter the oscilloscope), and note the shift in the chosen level of part 2, as shown in Fig. 13.51(b). Equation (13.29) can then be used to determine the dc or average value of the waveform. For the waveform of Fig. 13.51(b), the average value is about

$$V_{av} = V_{dc} = (0.9 \text{ div.})(5 \text{ V/div.}) = \mathbf{4.5\ V}$$

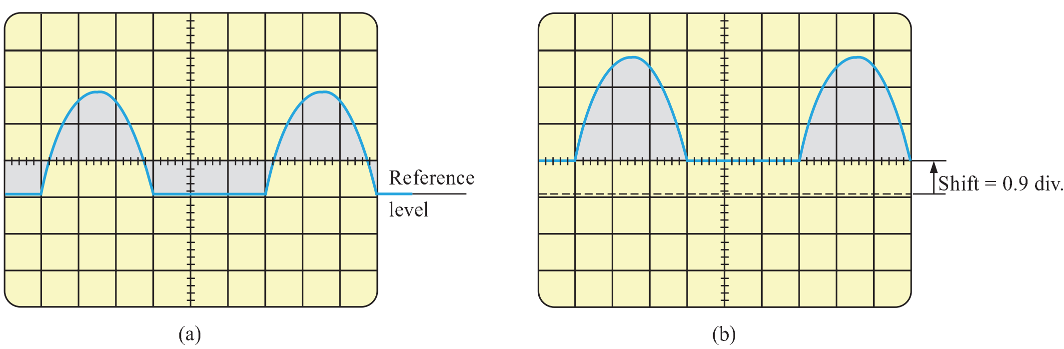


FIG. 13.51

Determining the average value of a nonsinusoidal waveform using the oscilloscope: (a) vertical channel on the ac mode; (b) vertical channel on the dc mode.

The procedure outlined above can be applied to any alternating waveform such as the one in Fig. 13.49. In some cases the average value may require moving the starting position of the waveform under the AC option to a different region of the screen or choosing a higher voltage scale. DMMs can read the average or dc level of any waveform by simply choosing the appropriate scale.

13.7 EFFECTIVE VALUES

This section will begin to relate dc and ac quantities with respect to the power delivered to a load. It will help us determine the amplitude of a sinusoidal ac current required to deliver the same power as a particular dc current. The question frequently arises, How is it possible for a sinusoidal ac quantity to deliver a net power if, over a full cycle, the net current in any one direction is zero (average value = 0)? It would almost appear that the power delivered during the positive portion of the sinusoidal waveform is withdrawn during the negative portion, and since the two are equal in magnitude, the net power delivered is zero. However, understand that *irrespective of direction,* current of any magnitude through a resistor will deliver power *to that resistor.* In other words, during the positive or negative portions of a sinusoidal ac current, power is being delivered at *each instant of time* to the resistor. The power delivered at each instant will, of course, vary with the magnitude of the sinusoidal ac current, but there will be a net flow during either the positive or the negative pulses with a net flow over the full cycle. The net power flow will equal twice that delivered by either the positive or the negative regions of sinusoidal quantity.

A fixed relationship between ac and dc voltages and currents can be derived from the experimental setup shown in Fig. 13.52. A resistor in a water bath is connected by switches to a dc and an ac supply. If switch 1 is closed, a dc current I, determined by the resistance R and battery voltage E, will be established through the resistor R. The temperature reached by the water is determined by the dc power dissipated in the form of heat by the resistor.

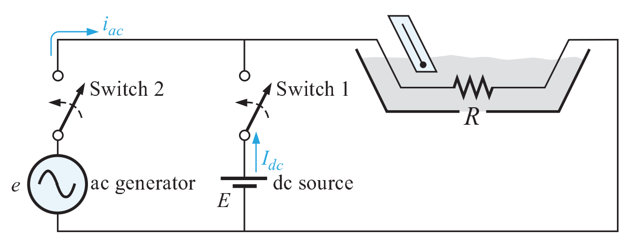


FIG. 13.52
An experimental setup to establish a relationship between dc and ac quantities.

If switch 2 is closed and switch 1 left open, the ac current through the resistor will have a peak value of I_m. The temperature reached by the water is now determined by the ac power dissipated in the form of heat by the resistor. The ac input is varied until the temperature is the same as that reached with the dc input. When this is accomplished, the average electrical power delivered to the resistor R by the ac source is the same as that delivered by the dc source.

The power delivered by the ac supply at any instant of time is

$$P_{ac} = (i_{ac})^2R = (I_m \sin \omega t)^2R = (I_m^2 \sin^2 \omega t)R$$

but

$$\sin^2 \omega t = \frac{1}{2}(1 - \cos 2\omega t) \qquad \text{(trigonometric identity)}$$

Therefore,

$$P_{ac} = I_m^2\left[\frac{1}{2}(1 - \cos 2\omega t)\right]R$$

and

$$P_{ac} = \frac{I_m^2 R}{2} - \frac{I_m^2 R}{2}\cos 2\omega t \tag{13.30}$$

The *average power* delivered by the ac source is just the first term, since the average value of a cosine wave is zero even though the wave may have twice the frequency of the original input current waveform. Equating the average power delivered by the ac generator to that delivered by the dc source,

$$P_{av(ac)} = P_{dc}$$

$$\frac{I_m^2 R}{2} = I_{dc}^2 R \quad \text{and} \quad I_m = \sqrt{2}I_{dc}$$

or

$$I_{dc} = \frac{I_m}{\sqrt{2}} = 0.707I_m$$

which, in words, states that

the equivalent dc value of a sinusoidal current or voltage is $1/\sqrt{2}$ or 0.707 of its maximum value.

The equivalent dc value is called the **effective value** of the sinusoidal quantity.

In summary,

$$I_{eq(dc)} = I_{eff} = 0.707I_m \tag{13.31}$$

or

$$I_m = \sqrt{2}I_{eff} = 1.414I_{eff} \tag{13.32}$$

and

$$E_{eff} = 0.707E_m \tag{13.33}$$

or

$$E_m = \sqrt{2}E_{eff} = 1.414E_{eff} \tag{13.34}$$

As a simple numerical example, it would require an ac current with a peak value of $\sqrt{2}(10) = 14.14$ A to deliver the same power to the resistor in Fig. 13.52 as a dc current of 10 A. The effective value of any quantity plotted as a function of time can be found by using the following equation derived from the experiment just described:

$$I_{eff} = \sqrt{\frac{\int_0^T i^2(t)\,dt}{T}} \tag{13.35}$$

or

$$I_{eff} = \sqrt{\frac{\text{area } (i^2(t))}{T}} \tag{13.36}$$

which, in words, states that to find the effective value, the function $i(t)$ must first be squared. After $i(t)$ is squared, the area under the curve is found by integration. It is then divided by T, the length of the cycle or the period of the waveform, to obtain the average or *mean* value of the squared waveform. The final step is to take the *square root* of the mean value. This procedure gives us another designation for the effective value, the **root-mean-square (rms) value.**

EXAMPLE 13.19 Find the effective values of the sinusoidal waveform in each part of Fig. 13.53.

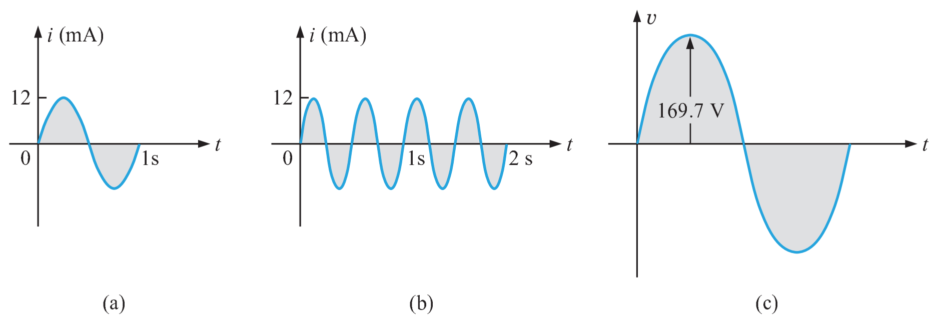


FIG. 13.53
Example 13.19.

Solution: For part (a), $I_{\text{eff}} = 0.707(12 \times 10^{-3}\text{ A}) =$ **8.484 mA.** For part (b), again $I_{\text{eff}} =$ **8.484 mA.** Note that frequency did not change the effective value in (b) above as compared to (a). For part (c), $V_{\text{eff}} = 0.707(169.73\text{ V}) \cong$ **120 V,** the same as available from a home outlet.

EXAMPLE 13.20 The 120-V dc source of Fig. 13.54(a) delivers 3.6 W to the load. Determine the peak value of the applied voltage (E_m) and the current (I_m) if the ac source [Fig. 13.54(b)] is to deliver the same power to the load.

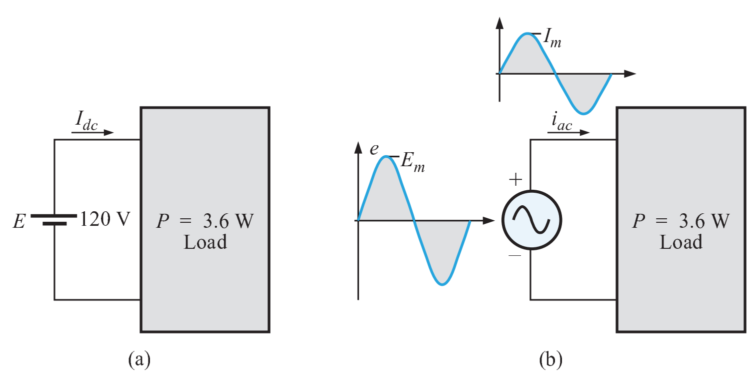


FIG. 13.54
Example 13.20.

Solution:

$$P_{dc} = V_{dc}I_{dc}$$

and $$I_{dc} = \frac{P_{dc}}{V_{dc}} = \frac{3.6\text{ W}}{120\text{ V}} = 30\text{ mA}$$

$$I_m = \sqrt{2}I_{dc} = (1.414)(30\text{ mA}) = \mathbf{42.42\ mA}$$

$$E_m = \sqrt{2}E_{dc} = (1.414)(120\text{ V}) = \mathbf{169.68\ V}$$

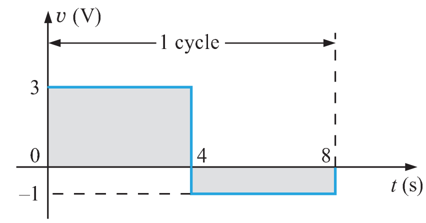


FIG. 13.55
Example 13.21.

EXAMPLE 13.21 Find the effective or rms value of the waveform of Fig. 13.55.

Solution:
v^2 (Fig. 13.56):

$$V_{eff} = \sqrt{\frac{(9)(4) + (1)(4)}{8}} = \sqrt{\frac{40}{8}} = \mathbf{2.236\ V}$$

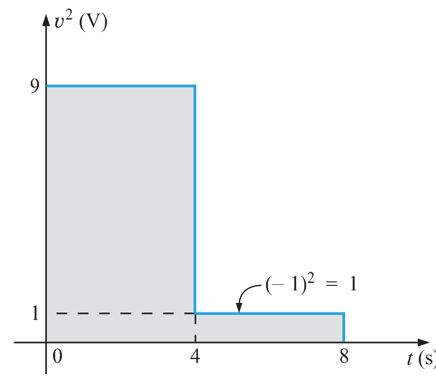


FIG. 13.56
The squared waveform of Fig. 13.55.

EXAMPLE 13.22 Calculate the effective value of the voltage of Fig. 13.57.

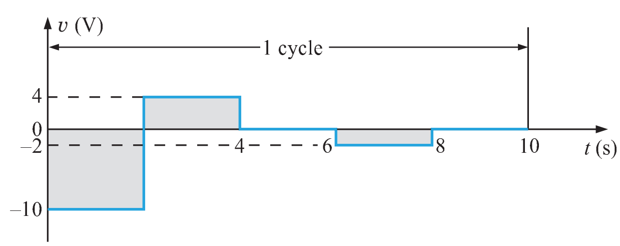


FIG. 13.57
Example 13.22.

Solution:
v^2 (Fig. 13.58):

$$V_{eff} = \sqrt{\frac{(100)(2) + (16)(2) + (4)(2)}{10}} = \sqrt{\frac{240}{10}}$$

$$= \mathbf{4.899\ V}$$

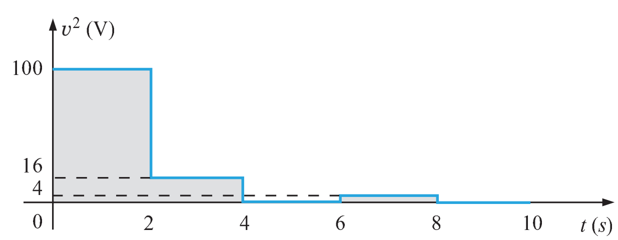


FIG. 13.58
The squared waveform of Fig. 13.57.

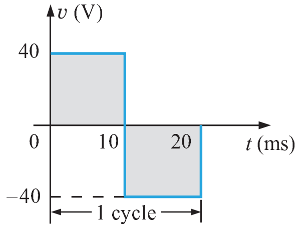


FIG. 13.59
Example 13.23.

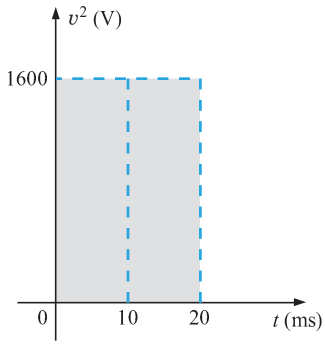


FIG. 13.60
The squared waveform of Fig. 13.59.

EXAMPLE 13.23 Determine the average and effective values of the square wave of Fig. 13.59.

Solution: By inspection, the average value is zero.

v^2 (Fig. 13.60):

$$V_{\text{eff}} = \sqrt{\frac{(1600)(10 \times 10^{-3}) + (1600)(10 \times 10^{-3})}{20 \times 10^{-3}}}$$

$$= \sqrt{\frac{32{,}000 \times 10^{-3}}{20 \times 10^{-3}}} = \sqrt{1600}$$

$$V_{\text{eff}} = \mathbf{40\ V}$$

(the maximum value of the waveform of Fig. 13.60)

The waveforms appearing in these examples are the same as those used in the examples on the average value. It might prove interesting to compare the effective and average values of these waveforms.

The effective values of sinusoidal quantities such as voltage or current will be represented by E and I. These symbols are the same as those used for dc voltages and currents. To avoid confusion, the peak value of a waveform will always have a subscript m associated with it: $I_m \sin \omega t$. *Caution:* When finding the effective value of the positive pulse of a sine wave, note that the squared area is *not* simply $(2A_m)^2 = 4A_m^2$; it must be found by a completely new integration. This will always be the case for any waveform that is not rectangular.

A unique situation arises if a waveform has both a dc and an ac component that may be due to a source such as the one in Fig. 13.61. The combination appears frequently in the analysis of electronic networks where both dc and ac levels are present in the same system.

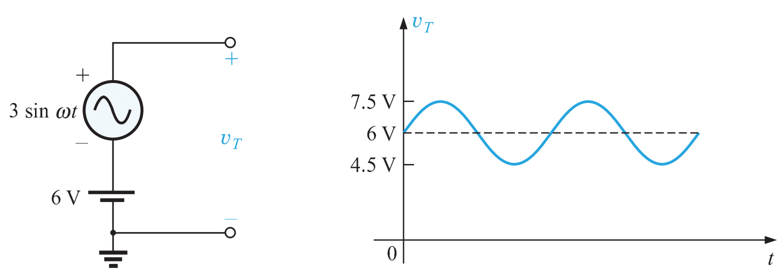


FIG. 13.61
Generation and display of a waveform having a dc and an ac component.

The question arises, What is the effective value of the voltage v_T? One might be tempted to simply assume that it is the sum of the effective values of each component of the waveform; that is, $V_T(\text{eff}) = 0.7071(1.5\ \text{V}) + 6\ \text{V} = 1.06\ \text{V} + 6\ \text{V} = 7.06\ \text{V}$. However, the rms value is actually determined by

$$V_{\text{eff}} = \sqrt{V_{\text{dc}}^2 + V_{\text{ac(rms)}}^2} \qquad \textbf{(13.37)}$$

which for the above example is

$$V_{\text{eff}} = \sqrt{(6\ \text{V})^2 + (1.06\ \text{V})^2}$$
$$= \sqrt{37.124}\ \text{V}$$
$$\cong \mathbf{6.1\ V}$$

This result is noticeably less than the above solution. The development of Eq. (13.37) can be found in Chapter 24.

Instrumentation

It is important to note whether the DMM in use is a *true rms* meter or simply a meter where the average value is calibrated (as described in the next section) to indicate the rms level. A *true rms* meter will read the effective value of any waveform (such as Figs. 13.49 and 13.61) and is not limited to only sinusoidal waveforms. Since the label *true rms* is normally not placed on the face of the meter, it is prudent to check the manual if waveforms other than purely sinusoidal are to be encountered.

13.8 ac METERS AND INSTRUMENTS

The d'Arsonval movement employed in dc meters can also be used to measure sinusoidal voltages and currents if the *bridge rectifier* of Fig. 13.62 is placed between the signal to be measured and the average reading movement.

The bridge rectifier, composed of four diodes (electronic switches), will convert the input signal of zero average value to one having an average value sensitive to the peak value of the input signal. The conversion process is well described in most basic electronics texts. Fundamentally, conduction is permitted through the diodes in such a manner as to convert the sinusoidal input of Fig. 13.63(a) to one having the appearance of Fig. 13.63(b). The negative portion of the input has been effectively "flipped over" by the bridge configuration. The resulting waveform of Fig. 13.63(b) is called a *full-wave rectified waveform.*

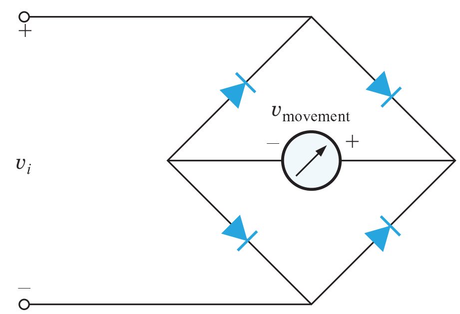


FIG. 13.62
Full-wave bridge rectifier.

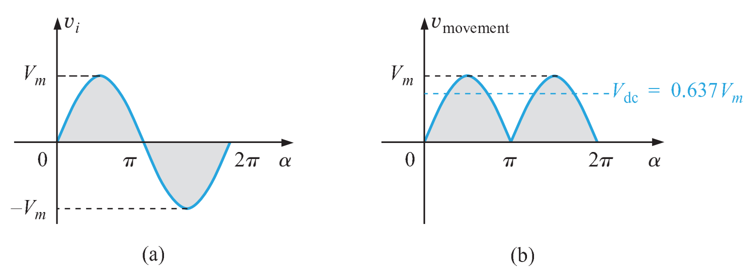


FIG. 13.63
(a) Sinusoidal input; (b) full-wave rectified signal.

The zero average value of Fig. 13.63(a) has been replaced by a pattern having an average value determined by

$$G = \frac{2V_m + 2V_m}{2\pi} = \frac{4V_m}{2\pi} = \frac{2V_m}{\pi} = 0.637V_m$$

The movement of the pointer will therefore be directly related to the peak value of the signal by the factor 0.637.

Forming the ratio between the rms and dc levels will result in

$$\frac{V_{rms}}{V_{dc}} = \frac{0.707V_m}{0.637V_m} \cong 1.11$$

revealing that the scale indication is 1.11 times the dc level measured by the movement; that is,

$$\boxed{\text{Meter indication} = 1.11 \text{ (dc or average value)}} \quad \textit{full-wave} \qquad \textbf{(13.38)}$$

Some ac meters use a half-wave rectifier arrangement that results in the waveform of Fig. 13.64, which has half the average value of Fig. 13.63(b) over one full cycle. The result is

$$\boxed{\text{Meter indication} = 2.22 \text{ (dc or average value)}} \quad \textit{half-wave} \qquad \textbf{(13.39)}$$

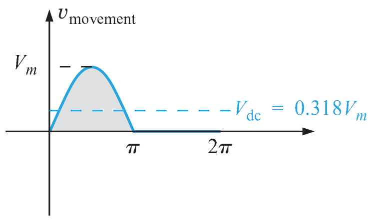


FIG. 13.64
Half-wave rectified signal.

A second movement, called the **electrodynamometer movement** (Fig. 13.65), can measure both ac and dc quantities without a change in internal circuitry. The movement can, in fact, read the effective value of any periodic or nonperiodic waveform because a reversal in current direction reverses the fields of both the stationary and the movable coils, so the deflection of the pointer is always up-scale.

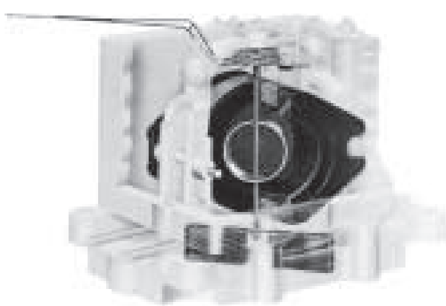


FIG. 13.65
Electrodynamometer movement. (Courtesy of Weston Instruments, Inc.)

The **VOM,** introduced in Chapter 2, can be used to measure both dc and ac voltages using a d'Arsonval movement and the proper switching networks. That is, when the meter is used for dc measurements, the dial setting will establish the proper series resistance for the chosen scale and will permit the appropriate dc level to pass directly to the movement. For ac measurements, the dial setting will introduce a network that employs a full- or half-wave rectifier to establish a dc level. As discussed above, each setting is properly calibrated to indicate the desired quantity on the face of the instrument.

EXAMPLE 13.24 Determine the reading of each meter for each situation of Fig. 13.66(a) and (b).

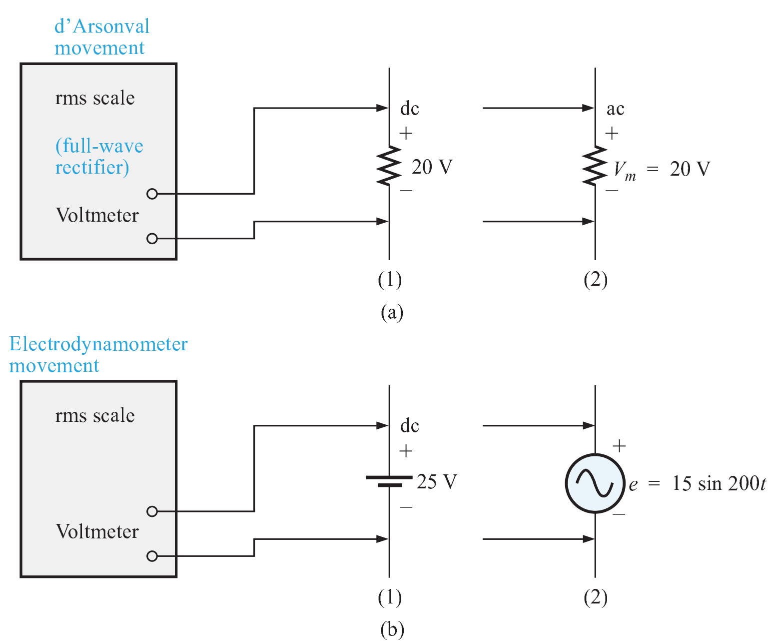


FIG. 13.66
Example 13.24.

Solution: For Fig. 13.66(a), situation (1): By Eq. (13.38),

$$\text{Meter indication} = 1.11(20 \text{ V}) = \mathbf{22.2 \text{ V}}$$

For Fig. 13.66(a), situation (2):

$$V_{\text{rms}} = 0.707V_m = 0.707(20 \text{ V}) = \mathbf{14.14 \text{ V}}$$

For Fig. 13.66(b), situation (1):

$$V_{\text{rms}} = V_{\text{dc}} = \mathbf{25 \text{ V}}$$

For Fig. 13.66(b), situation (2):

$$V_{\text{rms}} = 0.707V_m = 0.707(15 \text{ V}) \cong \mathbf{10.6 \text{ V}}$$

Most DMMs employ a full-wave rectification system to convert the input ac signal to one with an average value. In fact, for the DMM of Fig. 2.27, the same scale factor of Eq. (13.38) is employed; that is, the average value is scaled up by a factor of 1.11 to obtain the rms value. In digital meters, however, there are no moving parts such as in the d'Arsonval or electrodynamometer movements to display the signal level. Rather, the average value is sensed by a multiprocessor integrated circuit (IC), which in turn determines which digits should appear on the digital display.

Digital meters can also be used to measure nonsinusoidal signals, but the scale factor of each input waveform must first be known (normally provided by the manufacturer in the operator's manual). For instance, the scale factor for an average responding DMM on the ac rms scale will produce an indication for a square-wave input that is 1.11 times the peak value. For a triangular input, the response is 0.555 times the peak value. Obviously, for a sine wave input, the response is 0.707 times the peak value.

For any instrument, it is always good practice to read (if only briefly) the operator's manual if it appears that you will use the instrument on a regular basis.

For frequency measurements, the **frequency counter** of Fig. 13.67 provides a digital readout of sine, square, and triangular waves from 5 Hz to 100 MHz at input levels from 30 mV to 42 V. Note the relative simplicity of the panel and the high degree of accuracy available.

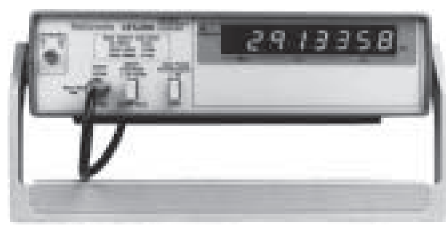


FIG. 13.67
Frequency counter. (Courtesy of Tektronix, Inc.)

The **Amp-Clamp®** of Fig. 13.68 is an instrument that can measure alternating current in the ampere range without having to open the circuit. The loop is opened by squeezing the "trigger"; then it is placed around the current-carrying conductor. Through transformer action, the level of current in rms units will appear on the appropriate scale. The accuracy of this instrument is ±3% of full scale at 60 Hz, and its scales have maximum values ranging from 6 A to 300 A. The addition of two leads, as indicated in the figure, permits its use as both a voltmeter and an ohmmeter.

FIG. 13.68
Amp-Clamp®. (Courtesy of Simpson Instruments, Inc.)

One of the most versatile and important instruments in the electronics industry is the **oscilloscope,** which has already been introduced in this chapter. It provides a display of the waveform on a cathode-ray tube to permit the detection of irregularities and the determination of quantities such as magnitude, frequency, period, dc component, and so on. The analog oscilloscope of Fig. 13.69 can display two waveforms at the same time (dual-channel) using an innovative interface (front panel). It employs menu buttons to set the vertical and horizontal scales by choosing from selections appearing on the screen. One can also store up to four measurement setups for future use.

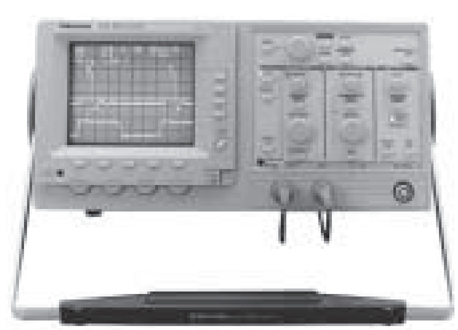


FIG. 13.69
Dual-channel oscilloscope. (Courtesy of Tektronix, Inc.)

A student accustomed to watching TV might be confused when first introduced to an oscilloscope. There is, at least initially, an assumption that the oscilloscope is generating the waveform on the screen—much like a TV broadcast. However, it is important to clearly understand that

an oscilloscope displays only those signals generated elsewhere and connected to the input terminals of the oscilloscope. The absence of an external signal will simply result in a horizontal line on the screen of the scope.

On most modern-day oscilloscopes, there is a switch or knob with the choice DC/GND/AC, as shown in Fig. 13.70(a), that is often ignored or treated too lightly in the early stages of scope utilization. The effect of each position is fundamentally as shown in Fig. 13.70(b). In the DC mode the dc and ac components of the input signal can pass directly to the display. In the AC position the dc input is blocked by the capacitor, but the ac portion of the signal can pass through to the screen. In the GND position the input signal is prevented from reaching the scope display by a direct ground connection, which reduces the scope display to a single horizontal line.

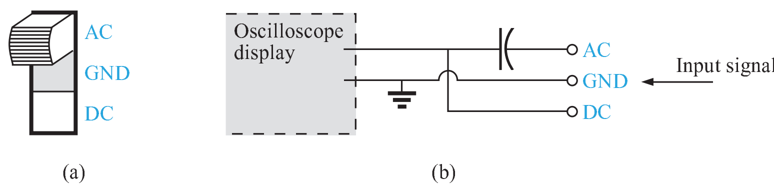


FIG. 13.70
AC-GND-DC switch for the vertical channel of an oscilloscope.

13.9 APPLICATIONS

(120 V at 60 Hz) versus (220 V at 50 Hz)

In North and South America the most common available ac supply is 120 V at 60 Hz, while in Europe and the Eastern countries it is 220 V at 50 Hz. The choices of rms value and frequency were obviously made carefully because they have such an important impact on the design and operation of so many systems.

The fact that the frequency difference is only 10 Hz reveals that there was agreement on the general frequency range that should be used for power generation and distribution. History suggests that the question of frequency selection was originally focused on that frequency that would not exhibit *flicker in the incandescent lamps* available in those days. Technically, however, there really wouldn't be a noticeable difference between 50 and 60 cycles per second based on this criterion. Another important factor in the early design stages was the effect of frequency on the size of transformers, which play a major role in power generation and distribution. Working through the fundamental equations for transformer design, you will find that *the size of a transformer is inversely proportional to frequency.* The result is that transformers operating at 50 Hz must be larger (on a purely mathematical basis about 17% larger) than those operating at 60 Hz. You will therefore find that transformers designed for the international market where they can operate on 50 Hz or 60 Hz are designed around the 50-Hz frequency. On the other side of the coin, however, higher frequencies result in increased concerns about arcing, increased losses in the transformer core due to eddy current and hysteresis losses (Chapter 19), and skin effect phenomena (Chapter 19). Somewhere in the discussion we must consider the fact that 60 Hz is an exact multiple of 60 seconds in a minute and 60 minutes in an hour. Since accurate timing is such a critical part of our technological design, was this a significant motive in the final choice? There is also the question about whether the 50 Hz is a result of the close affinity of this value to the metric system. Keep in mind that powers of 10 are all powerful in the metric system, with 100 cm in a meter, 100°C the boiling point of water, and so on. Note that 50 Hz is exactly half of this special number. All in all, it would seem that both sides have an argument that would be worth defending. However, in the final analysis, we must also wonder whether the difference is simply political in nature.

The difference in voltage between North America and Europe is a different matter entirely in the sense that the difference is close to 100%. Again, however, there are valid arguments for both sides. There is no question that larger voltages such as 220 V *raise safety issues* beyond those raised by voltages of 120 V. However, when higher voltages are supplied, there is less current in the wire for the same power demand, permitting the use of smaller conductors—a real money saver. In addition, motors, compressors, and so on, found in common home appliances and throughout the industrial community *can be smaller in size.* Higher voltages, however, also bring back the concern about arcing effects, insulation requirements, and, due to real safety concerns, higher installation costs. In general, however, international travelers are prepared for most situations if they have a transformer that can convert from their home level to that of the country they plan to visit. Most equipment (not clocks, of course) can run quite well on 50 Hz or 60 Hz for most travel periods. For any unit not operating at its design frequency, it will simply have to "work a little harder" to perform the given task. The major problem for the traveler is not the transformer itself but the wide variety of plugs used from one country to another. Each country has its own design for the "female" plug in the wall. For the three-week tour, this could mean as many as 6 to 10 different plugs of the type shown in Fig. 13.71. For a 120-V, 60-Hz supply, the plug is quite standard in appearance with its two spade leads (and possible ground connection).

In any event, both the 120 V at 60 Hz and the 220 V at 50 Hz are obviously meeting the needs of the consumer. It is a debate that could go on at length without an ultimate victor.

FIG. 13.71
Variety of plugs for a 220-V, 50-Hz connection.

Safety Concerns (High Voltages and dc versus ac)

Be aware that any "live" network should be treated with a calculated level of respect. Electricity in its various forms is not to be feared but should be employed with some awareness of its potentially dangerous side effects. It is common knowledge that electricity and water do not mix (never use extension cords or plug in TVs or radios in the bathroom) because a full 120 V in a layer of water of any height (from a shallow puddle to a full bath) can be *lethal.* However, other effects of dc and ac voltages are less known. In general, as the voltage and current increase, your concern about safety should increase exponentially.

For instance, under dry conditions, most human beings can survive a 120-V ac shock such as obtained when changing a light bulb, turning on a switch, and so on. Most electricians have experienced such a jolt many times in their careers. However, ask an electrician to relate how it feels to hit 220 V, and the response (if he or she has been unfortunate to have had such an experience) will be totally different. How often have you heard of a back-hoe operator hitting a 220-V line and having a fatal heart attack? Remember, the operator is sitting in a metal container on a damp ground which provides an excellent path for the resulting current to flow from the line to ground. If only for a short period of time, with the best environment (rubber-sole shoes, etc.), in a situation where you can quickly escape the situation, most human beings can also survive a 220-V shock. However, as mentioned above, it is one you will not quickly forget. For voltages beyond 220 V rms, the chances of survival go down exponentially with increase in voltage. It takes only about 10 mA of steady current through the heart to put it in defibrillation. In general, therefore, always be sure that the power is disconnected when working on the repair of electrical equipment. Don't assume that throwing a wall switch will disconnect the power. Throw the main circuit breaker and test the lines with a voltmeter before working on the system. Since voltage is a two-point phenomenon, don't be a hero and work with one line at at time—accidents happen!

You should also be aware that the reaction to dc voltages is quite different from that to ac voltages. You have probably seen in movies or comic strips that people are often unable to let go of a *hot* wire. This is evidence of the most important difference between the two types of voltages. As mentioned above, if you happen to touch a "hot" 120-V ac line, you will probably get a good sting, but *you can let go.* If it happens to be a "hot" 120-V dc line, you will probably not be able to let go, and a fatality could occur. Time plays an important role when this happens, because the longer you are subjected to the dc voltage, the more the resistance in the body decreases until a fatal current can be established. The reason that we can let go of an ac line is best demonstrated by carefully examining the 120-V rms, 60-Hz voltage in Fig. 13.72. Since the voltage is oscillating, there is a period of time when the voltage is near zero or less than, say, 20 V, and is reversing in direction. Although this time interval is very short, it appears every 8.3 ms and provides a window to *let go.*

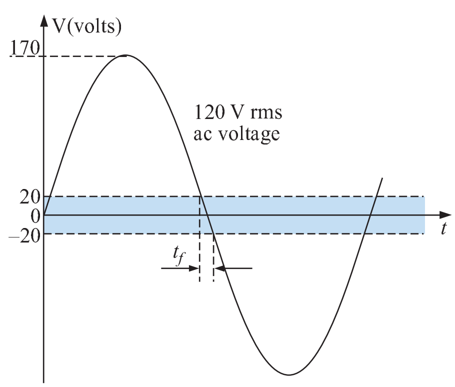


FIG 13.72
Interval of time when sinusoidal voltage is near zero volts.

Now that we are aware of the additional dangers of dc voltages, it is important to mention that under the wrong conditions, dc voltages as low as 12 V such as from a car battery can be quite dangerous. If you happen to be working on a car under wet conditions, or if you are sweating badly for some reason or, worse yet, wearing a wedding ring that may have moisture and body salt underneath, touching the positive terminal may initiate the process whereby the body resistance begins to drop and serious injury could take place. It is one of the reasons you seldom see a professional electrician wearing any rings or jewelry—it is just not worth the risk.

Before leaving this topic of safety concerns, you should also be aware of the dangers of high-frequency supplies. We are all aware of what 2.45 GHz at 120 V can do to a meat product in a microwave oven. As discussed in Chapter 5, it is therefore very important that the seal around the oven be as tight as possible. However, don't ever assume that anything is absolutely perfect in design—so don't make it a habit to view the cooking process in the microwave 6 in. from the door on a continuing basis. Find something else to do, and check the food only when the cooking process is complete. If you ever visit the Empire State Building, you will notice that you are unable to get close to the antenna on the dome due to the high-frequency signals being emitted with a great deal of power. Also note the large KEEP OUT signs near radio transmission towers for local radio stations. Standing within 10 ft of an AM transmitter working at 540 kHz would bring on disaster. Simply holding (not to be tried!) a fluorescent bulb near the tower could make it light up due to the excitation of the molecules inside the bulb.

In total, therefore, treat any situation with high ac voltages or currents, high-energy dc levels, and high frequencies with added care.

Bulb Savers

Ever since the invention of the light bulb, consumers have clamored for ways to extend the life of a bulb. I can remember the days when I was taught to always turn a light off when leaving a room and not to play with a light switch because it cost us a penny (at a time when a penny had some real value) every time I turned the switch on and off. Through advanced design we now have bulbs that are guaranteed to last a number of years. They cost more, but there is no need to replace the bulb as often, and over time there is a financial savings. For some of us it is simply a matter of having to pay so much for a single bulb.

For interest sake, I measured the cold dc resistance of a standard 60-W bulb and found it to be about 14 Ω. Forgetting any inductive effects due to the filament and wire, this would mean a current of 120 V/14 Ω = 8.6 A when the light is first turned on. This is a fairly heavy current for the filament to absorb when you consider that the normal operating current is 60 W/120 V = 0.5 A. Fortunately, it lasts for only a few milliseconds, as shown in Fig. 13.73(a), before the bulb heats up, causing the filament resistance to quickly increase and cut the current down to reasonable levels. However, over time, hitting the bulb with 8.6 A every time you turn the switch on will take its toll on the filament, and eventually the filament will simply surrender its natural characteristics and open up. You can easily tell if a bulb is bad by simply shaking it and listening for the clinking sound of the broken filament hitting the bulb. Assuming an initial current of 8.6 A for a single bulb, if the light switch controlled four 60-W bulbs in the same room, the surge current through the switch could be as high as 4(8.6 A) = 34.4 A as shown in Fig. 13.73(b), which probably exceeds the rating of the breaker (typically 20 A) for the circuit. However, the saving grace is that it lasts for only a few milliseconds, and circuit breakers are not designed to react that quickly. Even the GFI safety breakers in the bathroom are typically rated at a 5-ms response time. However, when you look at the big picture and imagine all these spikes on the line generated throughout a residential community, it is certainly a problem that the power company has to deal with on a continuing basis.

One way to suppress this surge current is to place an inductor in series with the bulb to choke out the spikes down the line. This method, in fact, leads to one way of extending the life of a light bulb through the use of dimmers. Any well-designed dimmer (such as the one described in Chapter 12) has an inductor in the line to suppress current surges. The results are both an extended life for the bulb and the ability to control the power level. Left on in the full voltage position, the switch could be used as a regular switch and the life of the bulb could be

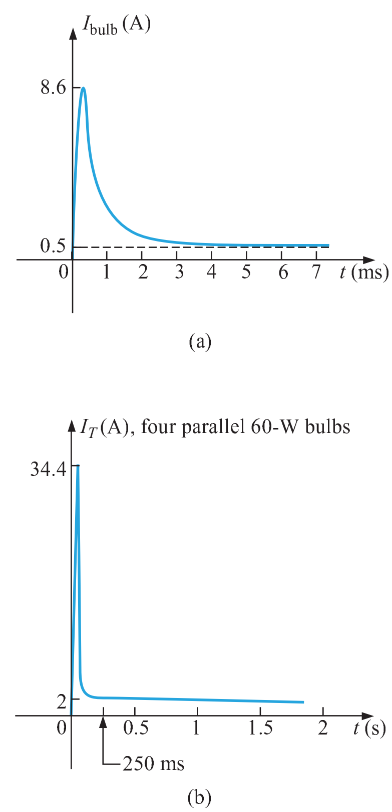


FIG 13.73
Surge currents: (a) single 60-W bulb; (b) four parallel 60-W bulbs.

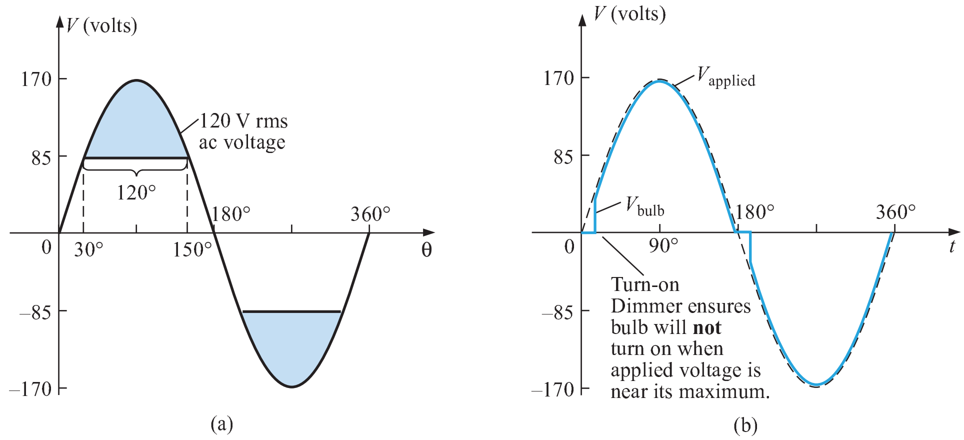


FIG. 13.74

Turn-on voltage: (a) equal to or greater than one-half the peak value; (b) when a dimmer is used.

extended. In fact, many dimmers now use triacs designed to turn on only when the applied voltage passes through zero. If we look at the full sine wave of Fig. 13.74(a), we find that the voltage is at least half of its maximum value of 85 V for a full two-thirds of each cycle, or about 67% of the time. The chances, therefore, of your turning on a light bulb with at least 85 V on the line is far better than 2 to 1, so you can expect the current for a 60-W light bulb to be at least 85 V/14 Ω = 6 A 67% of the time, which exceeds the rated 0.5-A rated value by 1100%. If we use a dimmer with a triac designed to turn on only when the applied voltage passes through zero or shortly thereafter, as shown in Fig.

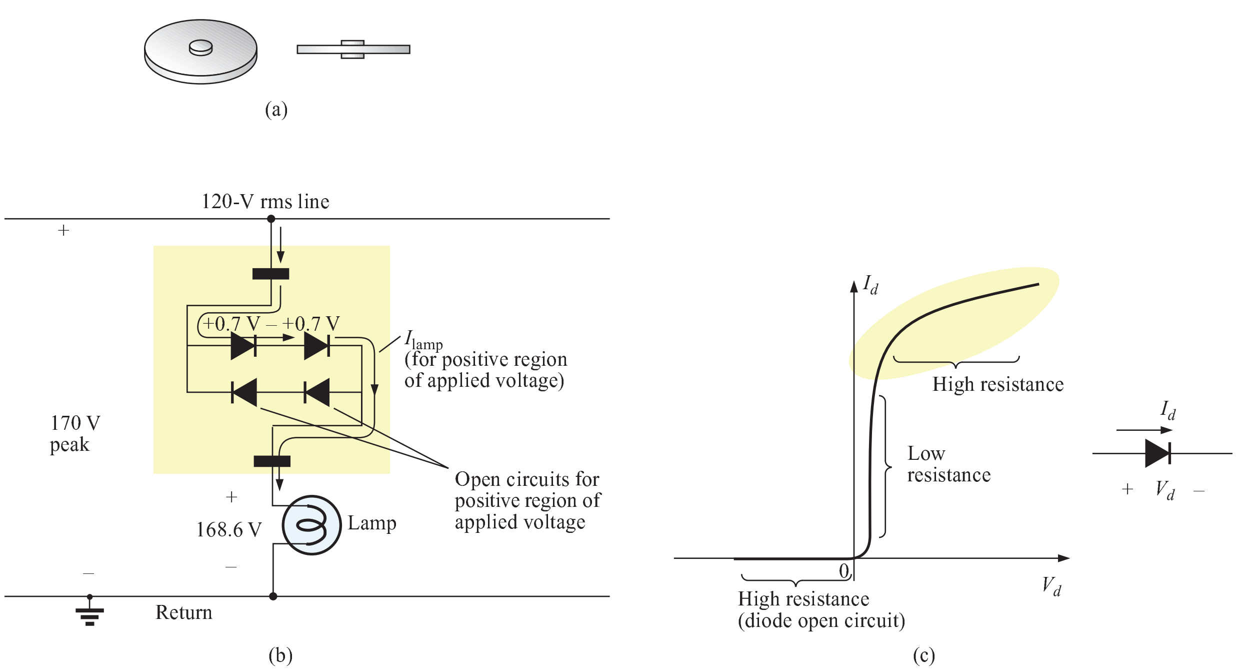


FIG. 13.75

Bulb saver: (a) external appearance; (b) basic operation; (c) diode characteristics at high current levels.

13.74(b), the applied voltage will increase from about zero volts, giving the bulb time to warm up before the full voltage is applied.

Another commercial offering to extend the life of light bulbs is the smaller circular disc shown in Fig. 13.75(a) which is inserted between the bulb and the holder. Contacts are provided on both sides to permit conduction through the simple diode network shown in Fig. 13.75(b). You may recall from an earlier chapter that the voltage across diodes in the on state is 0.7 V as shown for each diode in Fig. 13.75(b) for the positive portion of the input voltage. The result is that the voltage to the bulb is reduced by about 1.4 V throughout the cycle, reducing the power delivered to the bulb. For most situations the reduced lighting is not a problem, and the bulb will last longer simply because it is not pressed to work at full output. However, the real saving in the device is the manner in which it could help suppress the surge currents through the light bulb. The true characteristics of a diode are shown in Fig. 13.75(c) for the full range of currents through the diode. For most applications in electronic circuits, the vertical region is employed. For excessive currents the diode characteristics flatten out as shown. This region is characterized as having a large resistance (compared to very small resistance of the vertical region) which will come into play when the bulb is first turned on. In other words, when the bulb is first turned on, the current will be so high that the diode will enter its high resistance region and by Ohm's law will limit the surge current—thereby extending the life of the bulb. The two diodes facing the other way are for the negative portion of the supply voltage.

New methods of extending the life of bulbs hit the marketplace every day. All in all, however, one guaranteed way to extend the life of your bulbs is to return to the old philosophy of turning lights off when you leave a room, and "Don't play with the light switch!"

13.10 COMPUTER ANALYSIS

PSpice (Windows)

Schematics offer a variety of ac voltage and current sources. However, for the purposes of this text, the voltage source **VSIN** and the current source **ISIN** are the most appropriate because they have a list of attributes that will cover most areas of normal interest for sinusoidal networks. Under the library, **SOURCE.slb,** a number of others are listed, but they don't have the full range of the above or they are dedicated to only one type of analysis. On occasion, **ISRC** will be used because it has an arrow symbol like that appearing in the text, and it can be used for dc, ac, and some transient analyses. The symbol for **ISIN** is simply a sine wave which utilizes the plus-and-minus sign to indicate direction. The sources **VAC, IAC, VSRC,** and **ISRC** are fine if the magnitude and phase of a specific quantity are desired or if a transient plot is against frequency. However, they will not provide a transient response against time even if the frequency and transient information are provided under **Analysis.**

For all of the sinusoidal sources, the magnitude entered and read is the peak value of the waveform and not the rms value. This will become clear when a plot of a quantity is desired and the magnitude calculated by PSpice (Windows) is the peak value of the transient response. However, for a purely steady-state ac response, the magnitude provided can be the rms value, and the output read as the rms value. Only when a plot is desired will it be clear that PSpice is accepting every ac magnitude as the peak value of the waveform. Of course, the phase angle is the same whether the magnitude is the peak or the rms value.

A number of default values are set by PSpice if values are entered for specific attributes of the source. If not specified, **DC** and **AC** values are defaulted to 0, and **Transient** values default to the **DC** value. When using **VSIN,** always specify **VOFF** as 0 V (unless a specific value is part of the analysis), provide both the **AC** and the **VAMPL** values at the same level, and provide the **PHASE** angle associated with the source. The **TD** (time delay), **DF** (damping factor), and **DC** value will all default to 0 if not specified. Similar statements apply to **ISIN.** Additional information about the various types of sources can be found in the *Circuit Analysis User's Guide* or from **Help.**

Each source can be obtained from the **SOURCE.slb** library using the same procedure introduced in previous chapters. To set the attributes of the source, double-click on the source, and double-click on each attribute to be defined. The **Value** of each can then be entered directly in the box provided. For each entry, be sure to **Save Attr** which will place the value alongside the attribute in the listing below. If you would like an attribute displayed, select **Change Display,** and when the **Change Attribute** dialog box appears, choose what you would like to display. The name and value listed in the choice appear in the boxes at the top of the dialog box. To change the assigned name appearing with the symbol on the schematic, simply choose **PKGREF** (package reference) and enter the desired name. It will not appear on the schematic, however, unless you follow through with the correct **Change Display** sequence.

C++

The absence of any network configurations to analyze in this chapter severely limits the content with respect to packaged computer programs. However, the door is still wide open for the application of a language to write programs that can be helpful in the application of some of the concepts introduced in the chapter. In particular, let us examine the C++ program of Fig. 13.76, designed to calculate the average value of a pulse waveform having up to 5 different levels.

The program begins with a heading and preprocessor directive. Recall that the *iostream.h* header file sets up the input-output path between the program and the disk operating system. Note that the *main* ( ) part of the program extends all the way down to the bottom, as identified by the braces { }. Within this region all the calculations will be performed, and the results will be displayed.

Within the *main* ( ) part of the program, all the variables to be employed in the calculations are defined as floating point (decimal values) or integer (whole numbers). The comments on the right identify each variable. This is followed by a display of the question about how many levels will be encountered in the waveform using *cout* (comment out). The *cin* (comment in) statement permits a response from the user.

Next, the loop statement *for* is employed to establish a fixed number of repetitions of the sequence appearing within the parentheses ( ) for a number of loops defined by the variable *levels.* The format of this *for* statement is such that the first entry within the parentheses ( ) is the initial value of the variable *count* (1 in this case), followed by a semicolon and then a test expression determining how many times the sequence to follow will be repeated. In other words, if *levels* is 5, then the first pass

Heading | Preprocessor directive | Body of program | Define form and name of variables | Obtain # of levels | Iterative for statement | Calculate V_{ave} | Display results

```
//C++ Average Waveform Voltage Calculation

#include <iostream.h>          //needed for input/output

main()
{
        float Vave;             //average value of waveform
        float Vlevel;           //voltage level during time Tlevel
        float VTsum = 0;        //used for adding voltage-time products
        float T = 0;            //total waveform time
        float Tlevel;           //time duration of Vlevel
        int levels;             //the number of levels in the waveform
        int count;              //loop counter

        cout << "How many levels do you wish to enter (1..5) ? ";
        cin >> levels;          //get number of levels from user

        for(count = 1; count <= levels; count++)    //begin loop
        {
                cout << "\n";
                cout << "Enter voltage level " << count << ": ";
                cin >> Vlevel;      //get voltage from user
                cout << "Enter time for level " << count << ": ";
                cin >> Tlevel;      //get time from user
                VTsum += Vlevel * Tlevel;      //add product to VTsum
                T += Tlevel;        //add Tlevel to total waveform time
        }
        Vave = VTsum / T;           //calculate average value
        cout << "\n";
        cout << "The average value of the waveform is ";
        cout << Vave << " volts.\n";
}
```

FIG. 13.76

C++ program designed to calculate the average value of a waveform with up to five positive or negative pulses.

through the *for* statement will result in 1 being compared to 5, and the test expression will be satisfied because 5 is greater than or equal to 1 (< =). On the next pass, *count* will be increased to 2, and the same test will be performed. Eventually *count* will equal 5, the test expression will not be satisfied, and the program will move to its next statement, which is *Vave* = *VT sum*/*T*. The last entry *count*++ of the *for* statement simply increments the variable *count* after each iteration. The first line within the *for* statement calls for a line to be skipped, followed by a question on the display about the level of voltage for the first time interval. The question will include the current state of the *count* variable followed by a colon. In C++ all character outputs must be displayed in quotes (not required for numerical values). However, note the absence of the quotes for *count* since it will be a numerical value. Next the user enters the first voltage level through *cin,* followed by a request for the time interval. In this case units are not provided but simply measured as an increment of the whole; that is, if the total period is 5 μs and the first interval is 2 μs, then just a 2 is entered.

The area under the pulse is then calculated to establish the variable *VTsum,* which was initially set at 0. On the next pass the value of *VTsum* will be the value obtained by the first run plus the new area. In other words, *VTsum* is a storage for the total accumulated area. Similarly, *T* is the accumulated sum of the time intervals.

Following a FALSE response from the test expression of the *for* statement, the program will move to calculate the average value of the waveform using the accumulated values of the area and time. A line is

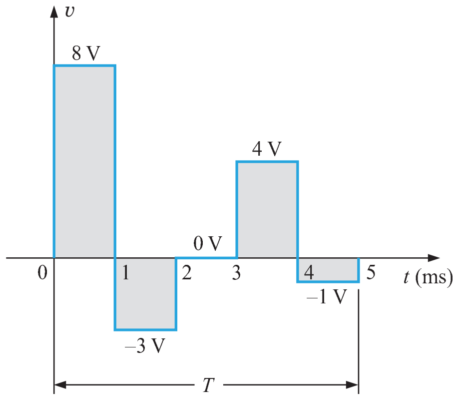


FIG. 13.77
Waveform with five pulses to be analyzed by the C++ program of Fig. 13.76.

then skipped and the average value is displayed with the remaining *cout* statements. Brackets have been added along the edge of the program to help identify the various components of the program.

A program is now available that can find the average value of any pulse waveform having up to five positive or negative pulses. It can be placed in storage and simply called for when needed. Operations such as the above are not available in either form of PSpice or in any commercially available software package. It took the knowledge of a language and a few minutes of time to generate a short program of lifetime value.

Two runs will clearly reveal what will be displayed and how the output will appear. The waveform of Fig. 13.77 has five levels, entered as shown in the output file of Fig. 13.78. As indicated the average value is 1.6 V. The waveform of Fig. 13.79 has only three pulses, and the time interval for each is different. Note the manner in which the time intervals were entered. Each is entered as a multiplier of the standard unit of measure for the horizontal axis. The variable *levels* will be only 3, requiring only three iterations of the *for* statement. The result is a negative value of -0.933 V, as shown in the output file of Fig. 13.80.

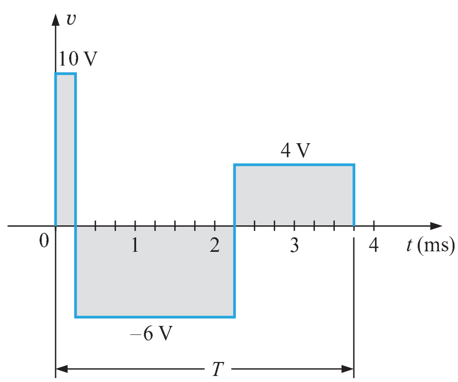


FIG. 13.79
Waveform with three pulses to be analyzed by the C++ program of Fig. 13.76.

```
How many levels do you wish to enter (1..5) ? 5

Enter voltage level 1: 8
Enter time for level 1: 1

Enter voltage level 2: -3
Enter time for level 2: 1

Enter voltage level 3: 0
Enter time for level 3: 1

Enter voltage level 4: 4
Enter time for level 4: 1

Enter voltage level 5: -1
Enter time for level 5: 1

The average value of the waveform is 1.6 volts.
```

FIG. 13.78
Output results for the waveform of Fig. 13.77.

```
How many levels do you wish to enter (1..5) ? 3

Enter voltage level 1: 10
Enter time for level 1: .25

Enter voltage level 2: -6
Enter time for level 2: 2

Enter voltage level 3: 4
Enter time for level 3: 1.5

The average value of the waveform is -0.933333 volts.
```

FIG. 13.80
Output results for the waveform of Fig. 13.79.

PROBLEMS

SECTION 13.2 Sinusoidal ac Voltage Characteristics and Definitions

1. For the periodic waveform of Fig. 13.81:
   a. Find the period *T*.
   b. How many cycles are shown?
   c. What is the frequency?
   ***d.** Determine the positive amplitude and peak-to-peak value (think!).

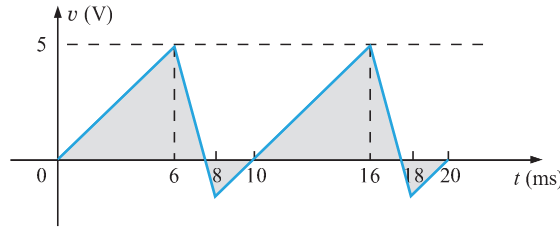


FIG. 13.81
Problem 1.

2. Repeat Problem 1 for the periodic waveform of Fig. 13.82.

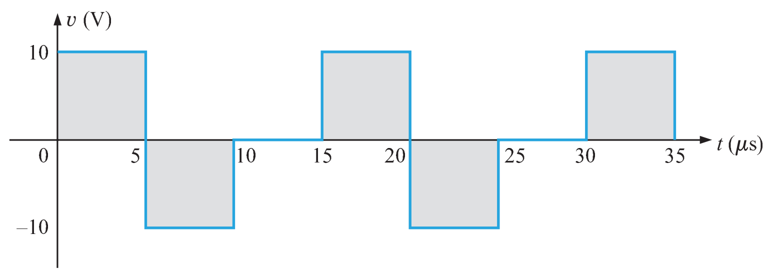


FIG. 13.82
Problems 2, 9, and 47.

3. Determine the period and frequency of the sawtooth waveform of Fig. 13.83.

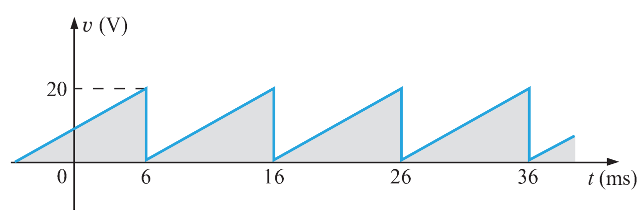
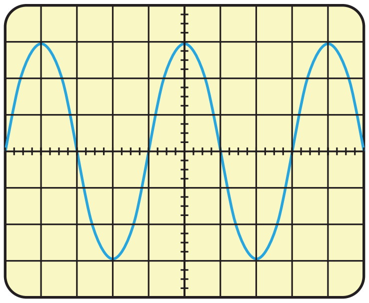


FIG. 13.83
Problems 3 and 48.

4. Find the period of a periodic waveform whose frequency is
   a. 25 Hz. **b.** 35 MHz.
   c. 55 kHz. **d.** 1 Hz.
5. Find the frequency of a repeating waveform whose period is
   a. 1/60 s. **b.** 0.01 s.
   c. 34 ms. **d.** 25 μs.
6. Find the period of a sinusoidal waveform that completes 80 cycles in 24 ms.
7. If a periodic waveform has a frequency of 20 Hz, how long (in seconds) will it take to complete five cycles?
8. What is the frequency of a periodic waveform that completes 42 cycles in 6 s?
9. Sketch a periodic square wave like that appearing in Fig. 13.82 with a frequency of 20,000 Hz and a peak value of 10 mV.



Vertical sensitivity = 50 mV/div.
Horizontal sensitivity = 10 μs/div.

FIG. 13.84
Problem 10.

10. For the oscilloscope pattern of Fig. 13.84:
  a. Determine the peak amplitude.
  b. Find the period.
  c. Calculate the frequency.
  Redraw the oscilloscope pattern if a +25-mV dc level were added to the input waveform.

SECTION 13.3 The Sine Wave

11. Convert the following degrees to radians:
  a. 45° **b.** 60°
  c. 120° **d.** 270°
  e. 178° **f.** 221°

12. Convert the following radians to degrees:
  a. $\pi/4$ **b.** $\pi/6$
  c. $\frac{1}{10}\pi$ **d.** $\frac{7}{6}\pi$
  e. 3π **f.** 0.55π

13. Find the angular velocity of a waveform with a period of
  a. 2 s. **b.** 0.3 ms.
  c. 4 μs. **d.** $\frac{1}{26}$ s.

14. Find the angular velocity of a waveform with a frequency of
  a. 50 Hz. **b.** 600 Hz.
  c. 2 kHz. **d.** 0.004 MHz.

15. Find the frequency and period of sine waves having an angular velocity of
  a. 754 rad/s. **b.** 8.4 rad/s.
  c. 6000 rad/s. **d.** $\frac{1}{16}$ rad/s.

16. Given $f = 60$ Hz, determine how long it will take the sinusoidal waveform to pass through an angle of 45°.

17. If a sinusoidal waveform passes through an angle of 30° in 5 ms, determine the angular velocity of the waveform.

SECTION 13.4 General Format for the Sinusoidal Voltage or Current

18. Find the amplitude and frequency of the following waves:
  a. $20 \sin 377t$ **b.** $5 \sin 754t$
  c. $10^6 \sin 10{,}000t$ **d.** $0.001 \sin 942t$
  e. $-7.6 \sin 43.6t$ **f.** $(\frac{1}{42}) \sin 6.283t$

19. Sketch $5 \sin 754t$ with the abscissa
  a. angle in degrees.
  b. angle in radians.
  c. time in seconds.

20. Sketch $10^6 \sin 10{,}000t$ with the abscissa
  a. angle in degrees.
  b. angle in radians.
  c. time in seconds.

21. Sketch $-7.6 \sin 43.6t$ with the abscissa
  a. angle in degrees.
  b. angle in radians.
  c. time in seconds.

22. If $e = 300 \sin 157t$, how long (in seconds) does it take this waveform to complete 1/2 cycle?

23. Given $i = 0.5 \sin \alpha$, determine i at $\alpha = 72°$.

24. Given $v = 20 \sin \alpha$, determine v at $\alpha = 1.2\pi$.

***25.** Given $v = 30 \times 10^{-3} \sin \alpha$, determine the angles at which v will be 6 mV.

***26.** If $v = 40$ V at $\alpha = 30°$ and $t = 1$ ms, determine the mathematical expression for the sinusoidal voltage.

SECTION 13.5 Phase Relations

27. Sketch $\sin(377t + 60°)$ with the abscissa
- **a.** angle in degrees.
- **b.** angle in radians.
- **c.** time in seconds.

28. Sketch the following waveforms:
- **a.** $50 \sin(\omega t + 0°)$
- **b.** $-20 \sin(\omega t + 2°)$
- **c.** $5 \sin(\omega t + 60°)$
- **d.** $4 \cos \omega t$
- **e.** $2 \cos(\omega t + 10°)$
- **f.** $-5 \cos(\omega t + 20°)$

29. Find the phase relationship between the waveforms of each set:
- **a.** $v = 4 \sin(\omega t + 50°)$
  $i = 6 \sin(\omega t + 40°)$
- **b.** $v = 25 \sin(\omega t - 80°)$
  $i = 5 \times 10^{-3} \sin(\omega t - 10°)$
- **c.** $v = 0.2 \sin(\omega t - 60°)$
  $i = 0.1 \sin(\omega t + 20°)$
- **d.** $v = 200 \sin(\omega t - 210°)$
  $i = 25 \sin(\omega t - 60°)$

***30.** Repeat Problem 29 for the following sets:
- **a.** $v = 2 \cos(\omega t - 30°)$
  $i = 5 \sin(\omega t + 60°)$
- **b.** $v = -1 \sin(\omega t + 20°)$
  $i = 10 \sin(\omega t - 70°)$
- **c.** $v = -4 \cos(\omega t + 90°)$
  $i = -2 \sin(\omega t + 10°)$

31. Write the analytical expression for the waveforms of Fig. 13.85 with the phase angle in degrees.

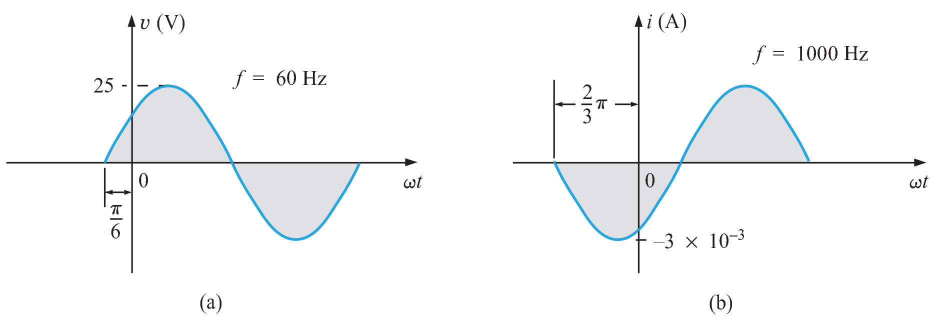


FIG. 13.85
Problem 31.

32. Repeat Problem 31 for the waveforms of Fig. 13.86.

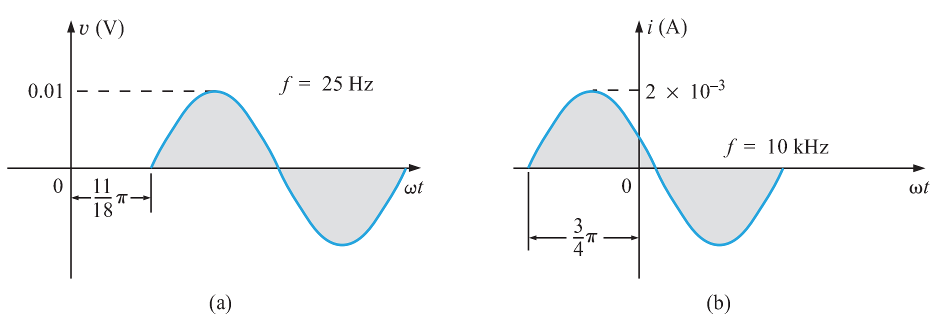


FIG. 13.86
Problem 32.

***33.** The sinusoidal voltage $v = 200 \sin(2\pi 1000t + 60°)$ is plotted in Fig. 13.87. Determine the time t_1.

***34.** The sinusoidal current $i = 4 \sin(50{,}000t - 40°)$ is plotted in Fig. 13.88. Determine the time t_1.

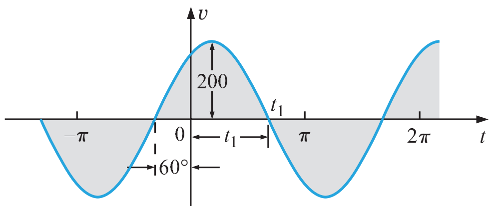


FIG. 13.87
Problem 33.

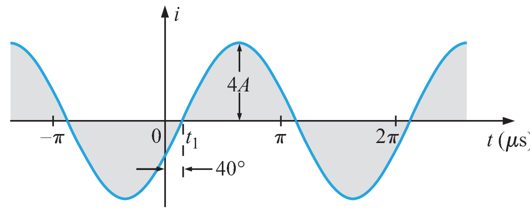
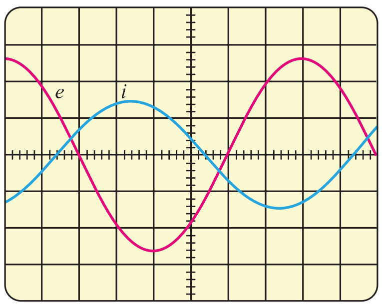


FIG. 13.88
Problem 34.

***35.** Determine the phase delay in milliseconds between the following two waveforms:

$$v = 60 \sin(1800t + 20°)$$
$$i = 1.2 \sin(1800t - 20°)$$

36. For the oscilloscope display of Fig. 13.89:
- **a.** Determine the period of each waveform.
- **b.** Determine the frequency of each waveform.
- **c.** Find the rms value of each waveform.
- **d.** Determine the phase shift between the two waveforms and which leads or lags.

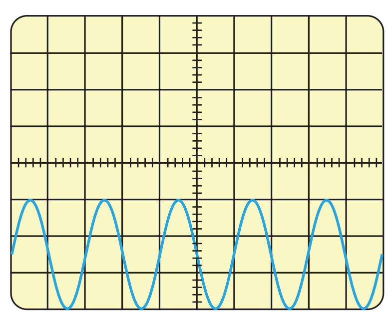


Vertical sensitivity = 0.5 V/div.
Horizontal sensitivity = 1 ms/div.

FIG. 13.89
Problem 36.

SECTION 13.6 Average Value

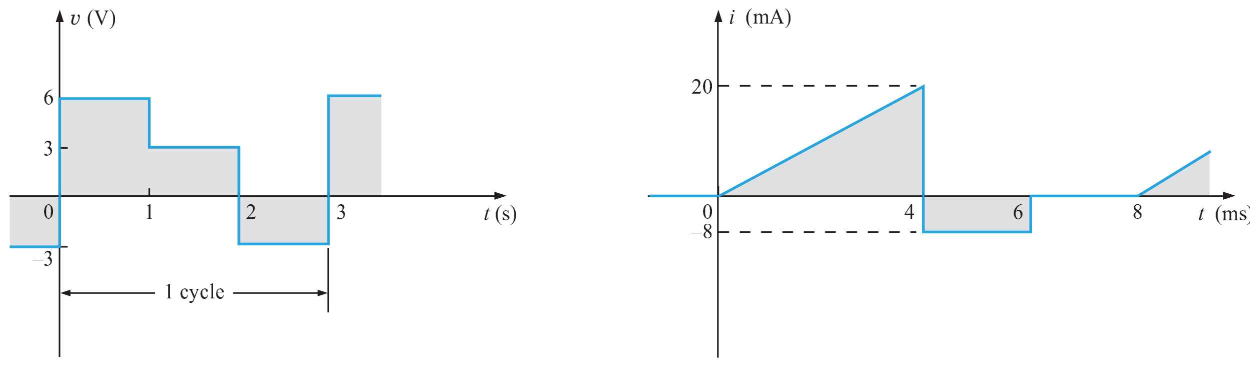
37. For the waveform of Fig. 13.90:
- **a.** Determine the period.
- **b.** Find the frequency.
- **c.** Determine the average value.
- **d.** Sketch the resulting oscilloscope display if the vertical channel is switched from DC to AC.



Vertical sensitivity = 10 mV/div.
Horizontal sensitivity = 0.2 ms/div.

FIG. 13.90
Problem 37.

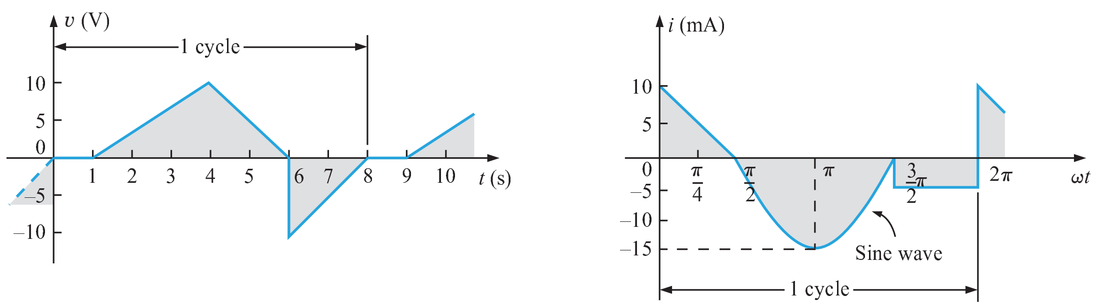
38. Find the average value of the periodic waveforms of Fig. 13.91 over one full cycle.



(a) (b)

FIG. 13.91
Problem 38.

39. Find the average value of the periodic waveforms of Fig. 13.92 over one full cycle.



(a) (b)

FIG. 13.92
Problem 39.

***40.** **a.** By the method of approximation, using familiar geometric shapes, find the area under the curve of Fig. 13.93 from zero to 10 s. Compare your solution with the actual area of 5 volt-seconds (V•s).

b. Find the average value of the waveform from zero to 10 s.

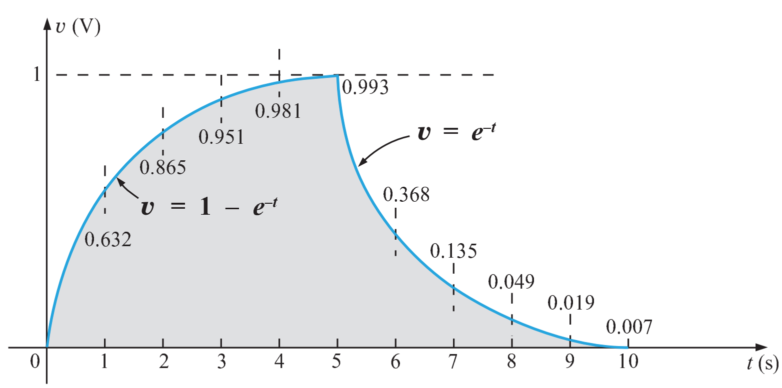
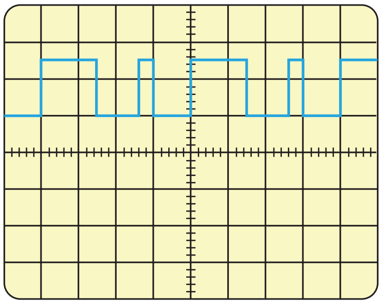


FIG. 13.93
Problem 40.



Vertical sensitivity = 10 mV/div.
Horizontal sensitivity = 10 μs/div.

FIG. 13.94
Problem 41.

***41.** For the waveform of Fig. 13.94:
   a. Determine the period.
   b. Find the frequency.
   c. Determine the average value.
   d. Sketch the resulting oscilloscope display if the vertical channel is switched from DC to AC.

SECTION 13.7 Effective Values

42. Find the effective values of the following sinusoidal waveforms:
   a. $v = 20 \sin 754t$
   b. $v = 7.07 \sin 377t$
   c. $i = 0.006 \sin(400t + 20°)$
   d. $i = 16 \times 10^{-3} \sin(377t - 10°)$

43. Write the sinusoidal expressions for voltages and currents having the following effective values at a frequency of 60 Hz with zero phase shift:
   a. 1.414 V   **b.** 70.7 V
   c. 0.06 A   **d.** 24 μA

44. Find the effective value of the periodic waveform of Fig. 13.95 over one full cycle.

45. Find the effective value of the periodic waveform of Fig. 13.96 over one full cycle.

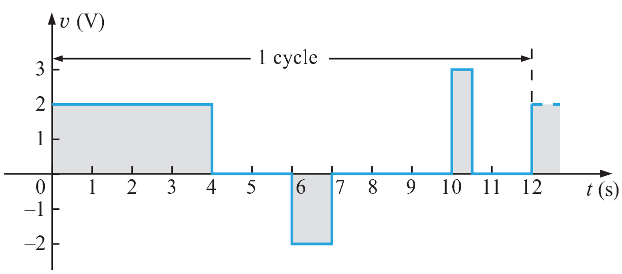


FIG. 13.95
Problem 44.

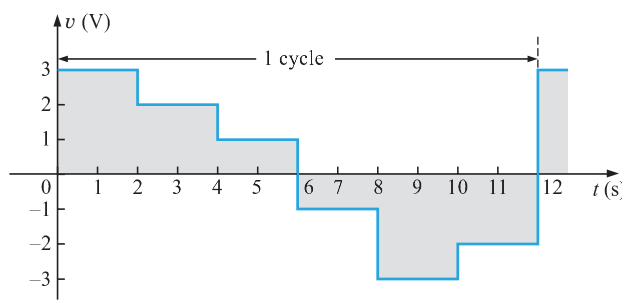


FIG. 13.96
Problem 45.

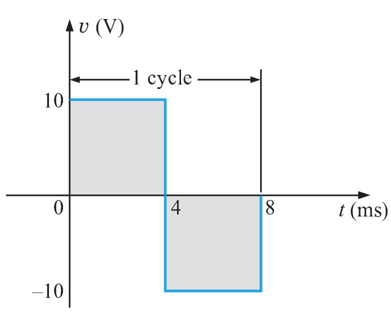


FIG. 13.97
Problem 46.

46. What are the average and effective values of the square wave of Fig. 13.97?

47. What are the average and effective values of the waveform of Fig. 13.82?

48. What is the average value of the waveform of Fig. 13.83?

49. For each waveform of Fig. 13.98, determine the period, frequency, average value, and effective value.

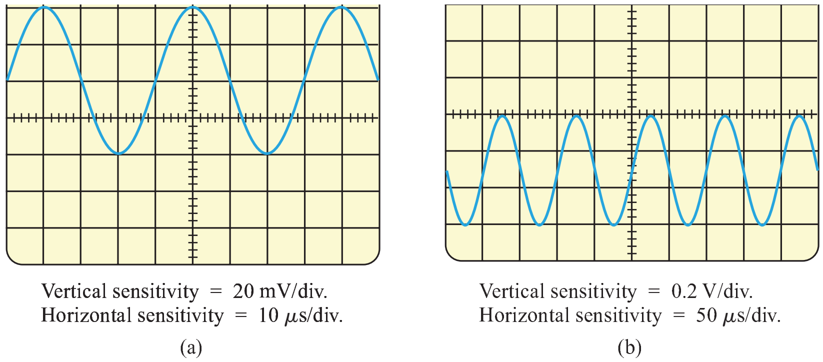


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FIG. 13.98
Problem 49.

SECTION 13.8 ac Meters and Instruments

50. Determine the reading of the meter for each situation of Fig. 13.99.

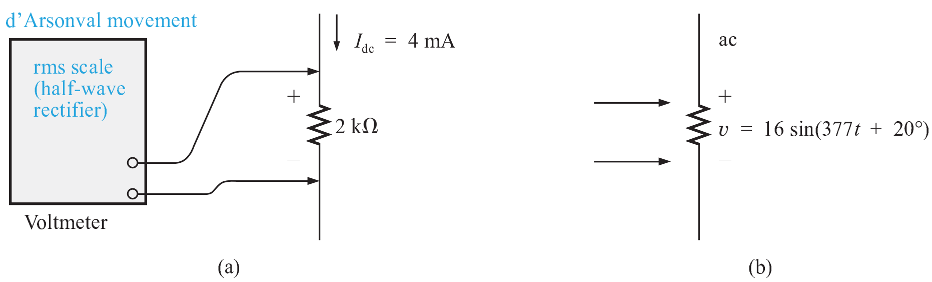


FIG. 13.99
Problem 50.

SECTION 13.10 Computer Analysis

Programming Language (C++, BASIC, Pascal, etc.)

51. Given a sinusoidal function, write a program to determine the effective value, frequency, and period.

52. Given two sinusoidal functions, write a program to determine the phase shift between the two waveforms, and indicate which is leading or lagging.

53. Given an alternating pulse waveform, write a program to determine the average and effective values of the waveform over one complete cycle.

GLOSSARY

Alternating waveform A waveform that oscillates above and below a defined reference level.

Amp-Clamp® A clamp-type instrument that will permit non-invasive current measurements and that can be used as a conventional voltmeter or ohmmeter.

Angular velocity The velocity with which a radius vector projecting a sinusoidal function rotates about its center.

Average value The level of a waveform defined by the condition that the area enclosed by the curve above this level is exactly equal to the area enclosed by the curve below this level.

Cycle A portion of a waveform contained in one period of time.

Effective value The equivalent dc value of any alternating voltage or current.

Electrodynamometer meters Instruments that can measure both ac and dc quantities without a change in internal circuitry.

Frequency (f) The number of cycles of a periodic waveform that occur in 1 second.

Frequency counter An instrument that will provide a digital display of the frequency or period of a periodic time-varying signal.

Instantaneous value The magnitude of a waveform at any instant of time, denoted by lowercase letters.

Oscilloscope An instrument that will display, through the use of a cathode-ray tube, the characteristics of a time-varying signal.

Peak amplitude The maximum value of a waveform as measured from its average, or mean, value, denoted by uppercase letters.

Peak-to-peak value The magnitude of the total swing of a signal from positive to negative peaks. The sum of the absolute values of the positive and negative peak values.

Peak value The maximum value of a waveform, denoted by uppercase letters.

Period (T) The time interval between successive repetitions of a periodic waveform.

Periodic waveform A waveform that continually repeats itself after a defined time interval.

Phase relationship An indication of which of two waveforms leads or lags the other, and by how many degrees or radians.

Radian (rad) A unit of measure used to define a particular segment of a circle. One radian is approximately equal to 57.3°; 2π rad are equal to 360°.

Root-mean-square (rms) value The root-mean-square or effective value of a waveform.

Sinusoidal ac waveform An alternating waveform of unique characteristics that oscillates with equal amplitude above and below a given axis.

VOM A multimeter with the capability to measure resistance and both ac and dc levels of current and voltage.

Waveform The path traced by a quantity, plotted as a function of some variable such as position, time, degrees, temperature, and so on.

CHAPTER 14

Operational Amplifiers

14.1 INTRODUCTION

An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

Figure 14.1 shows a basic op-amp with two inputs and one output as would result using a differential amplifier input stage. Recall from Chapter 12 that each input results in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the plus (+) or the minus (−) input.

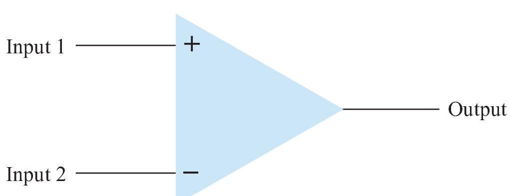
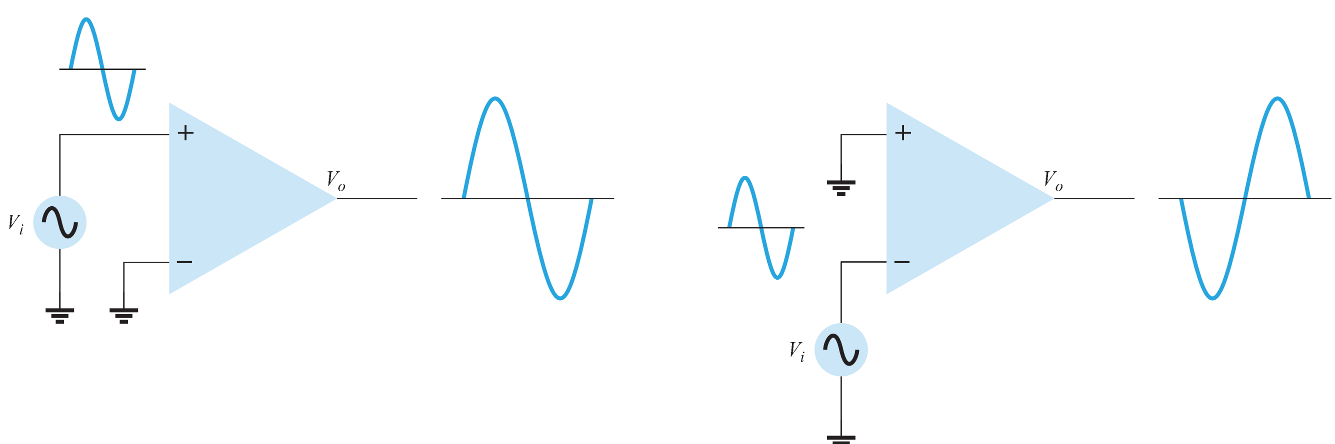


Figure 14.1 Basic op-amp.

Single-Ended Input

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Figure 14.2 shows the signals connected



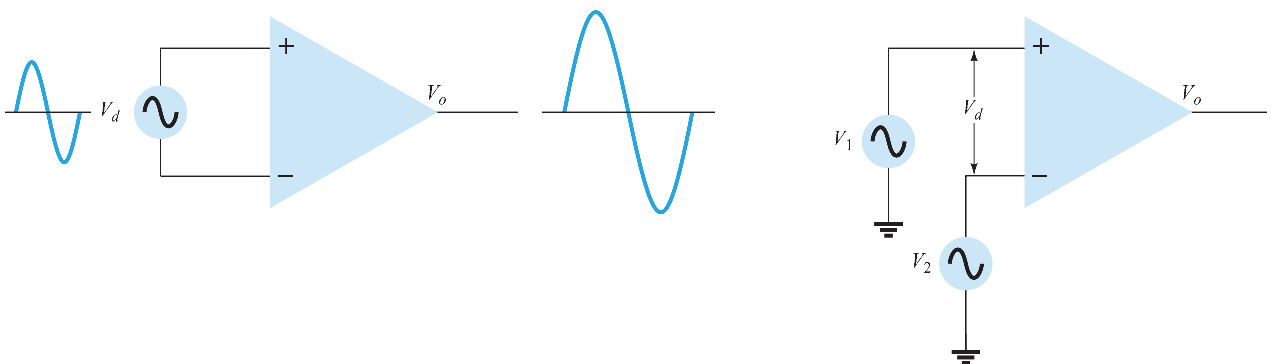
(a) (b)

Figure 14.2 Single-ended operation.

for this operation. In Fig. 14.2a, the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Figure 14.2b shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.

Double-Ended (Differential) Input

In addition to using only one input, it is possible to apply signals at each input—this being a double-ended operation. Figure 14.3a shows an input, V_d, applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Figure 14.3b shows the same action resulting when two separate signals are applied to the inputs, the difference signal being $V_{i_1} - V_{i_2}$.



(a) (b)

Figure 14.3 Double-ended (differential) operation.

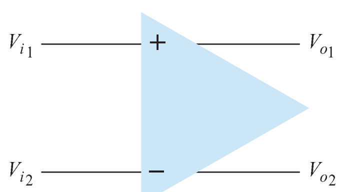


Figure 14.4 Double-ended output.

Double-Ended Output

While the operation discussed so far had a single output, the op-amp can also be operated with opposite outputs, as shown in Fig. 14.4. An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Figure 14.5 shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Figure 14.6 shows the same operation with a single output measured

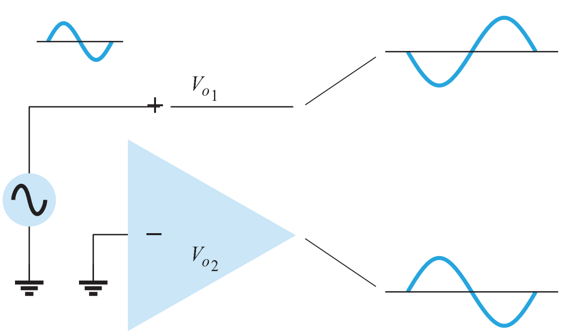


Figure 14.5 Double-ended output with single-ended input.

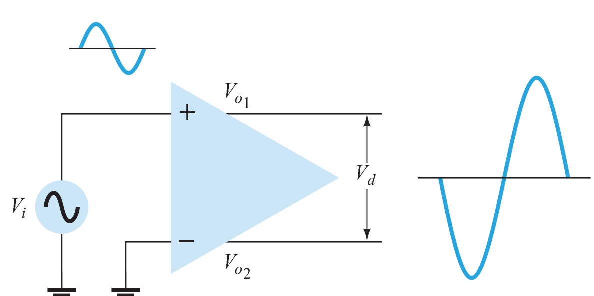


Figure 14.6 Double-ended output.

between output terminals (not with respect to ground). This difference output signal is $V_{o_1} - V_{o_2}$. The difference output is also referred to as a *floating signal* since neither output terminal is the ground (reference) terminal. Notice that the difference output is twice as large as either V_{o_1} or V_{o_2} since they are of opposite polarity and subtracting them results in twice their amplitude [i.e., 10 V − (−10 V) = 20 V]. Figure 14.7 shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.

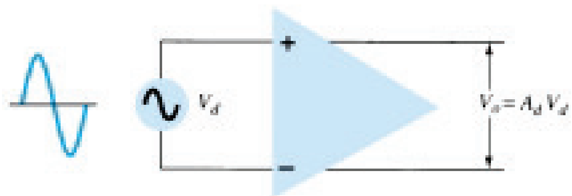


Figure 14.7 Differential-input, differential-output operation.

Common-Mode Operation

When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 14.8. Ideally, the two inputs are equally amplified, and since they result in opposite polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

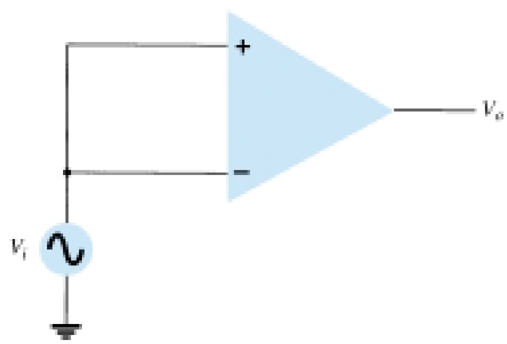


Figure 14.8 Common-mode operation.

Common-Mode Rejection

A significant feature of a differential connection is that the signals which are opposite at the inputs are highly amplified, while those which are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature, referred to as common-mode rejection, is discussed more fully in the next section.

14.2 DIFFERENTIAL AND COMMON-MODE OPERATION

One of the more important features of a differential circuit connection, as provided in an op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs, while only slightly amplifying signals that are common to both inputs. An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs. Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common-mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs

When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$V_d = V_{i_1} - V_{i_2} \tag{14.1}$$

Common Inputs

When both input signals are the same, a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) \tag{14.2}$$

Output Voltage

Since any signals applied to an op-amp in general have both in-phase and out-of-phase components, the resulting output can be expressed as

$$V_o = A_d V_d + A_c V_c \tag{14.3}$$

where V_d = difference voltage given by Eq. (14.1)
V_c = common voltage given by Eq. (14.2)
A_d = differential gain of the amplifier
A_c = common-mode gain of the amplifier

Opposite Polarity Inputs

If opposite polarity inputs applied to an op-amp are ideally opposite signals, $V_{i_1} = -V_{i_2} = V_s$, the resulting difference voltage is

$$\text{Eq. (14.1): } V_d = V_{i_1} - V_{i_2} = V_s - (-V_s) = 2V_s$$

while the resulting common voltage is

$$\text{Eq. (14.2): } V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}[V_s + (-V_s)] = 0$$

so that the resulting output voltage is

$$\text{Eq. (14.3): } V_o = A_d V_d + A_c V_c = A_d\,(2V_s) + 0 = 2\,A_d V_s$$

This shows that when the inputs are an ideal opposite signal (no common element), the output is the differential gain times twice the input signal applied to one of the inputs.

Same Polarity Inputs

If the same polarity inputs are applied to an op-amp, $V_{i_1} = V_{i_2} = V_s$, the resulting difference voltage is

$$\text{Eq. (14.1): } V_d = V_{i_1} - V_{i_2} = V_s - V_s = 0$$

while the resulting common voltage is

$$\text{Eq. (14.2):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}(V_s + V_s) = V_s$$

so that the resulting output voltage is

$$\text{Eq. (14.3):} \quad V_o = A_d V_d + A_c V_c = A_d(0) + A_c V_s = A_c V_s$$

This shows that when the inputs are ideal in-phase signals (no difference signal), the output is the common-mode gain times the input signal, V_s, which shows that only common-mode operation occurs.

Common-Mode Rejection

The solutions above provide the relationships that can be used to measure A_d and A_c in op-amp circuits.

1. *To measure* A_d: Set $V_{i_1} = -V_{i_2} = V_s = 0.5$ V, so that

$$\text{Eq. (14.1):} \quad V_d = (V_{i_1} - V_{i_2}) = (0.5\text{ V} - (-0.5\text{ V}) = 1\text{ V}$$

   and $$\text{Eq. (14.2):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}[0.5\text{ V} + (-0.5\text{ V})] = 0\text{ V}$$

   Under these conditions the output voltage is

$$\text{Eq. (14.3):} \quad V_o = A_d V_d + A_c V_c = A_d(1\text{ V}) + A_c(0) = A_d$$

   Thus, setting the input voltages $V_{i_1} = -V_{i_2} = 0.5$ V results in an output voltage numerically equal to the value of A_d.
2. *To measure* A_c: Set $V_{i_1} = V_{i_2} = V_s = 1$ V, so that

$$\text{Eq. (14.1):} \quad V_d = (V_{i_1} - V_{i_2}) = (1\text{ V} - 1\text{ V}) = 0\text{ V}$$

   and $$\text{Eq. (14.2):} \quad V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2}) = \tfrac{1}{2}(1\text{ V} + 1\text{ V}) = 1\text{ V}$$

   Under these conditions the output voltage is

$$\text{Eq. (14.3):} \quad V_o = A_d V_d + A_c V_c = A_d(0\text{ V}) + A_c(1\text{ V}) = A_c$$

   Thus, setting the input voltages $V_{i_1} = V_{i_2} = 1$ V results in an output voltage numerically equal to the value of A_c.

Common-Mode Rejection Ratio

Having obtained A_d and A_c (as in the measurement procedure discussed above), we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\text{CMRR} = \frac{A_d}{A_c} \tag{14.4}$$

The value of CMRR can also be expressed in logarithmic terms as

$$\text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c} \quad \text{(dB)} \tag{14.5}$$

EXAMPLE 14.1 Calculate the CMRR for the circuit measurements shown in Fig. 14.9.

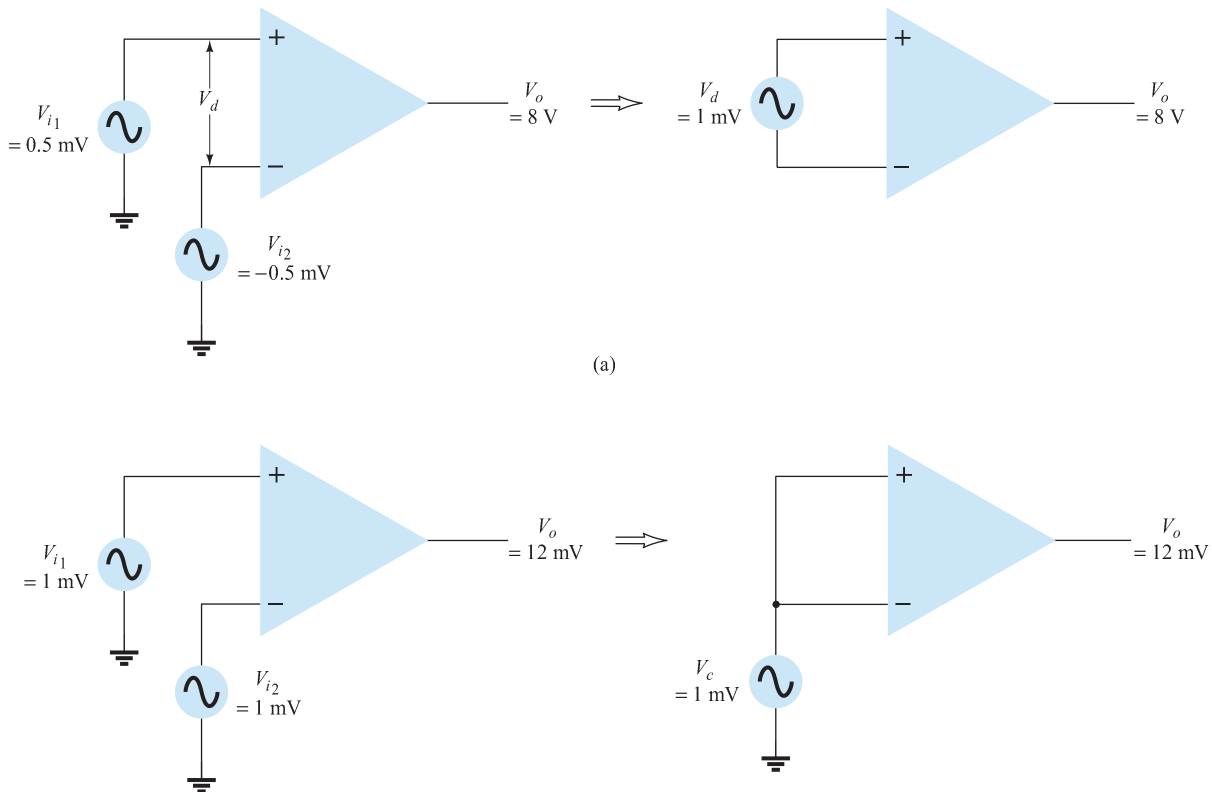


Figure 14.9 Differential and common-mode operation: (a) differential-mode; (b) common-mode.

Solution

From the measurement shown in Fig. 14.9a, using the procedure in step 1 above, we obtain

$$A_d = \frac{V_o}{V_d} = \frac{8\text{ V}}{1\text{ mV}} = 8000$$

The measurement shown in Fig. 14.9b, using the procedure in step 2 above, gives us

$$A_c = \frac{V_o}{V_c} = \frac{12\text{ mV}}{1\text{ mV}} = 12$$

Using Eq. (14.4), the value of CMRR is

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{8000}{12} = \mathbf{666.7}$$

which can also be expressed as

$$\text{CMRR} = 20\log_{10}\frac{A_d}{A_c} = 20\log_{10} 666.7 = \mathbf{56.48\ dB}$$

It should be clear that the desired operation will have A_d very large with A_c very small. That is, the signal components of opposite polarity will appear greatly amplified at the output, whereas the signal components that are in phase will mostly cancel out so that the common-mode gain, A_c, is very small. Ideally, the value of the CMRR is infinite. Practically, the larger the value of CMRR, the better the circuit operation.

We can express the output voltage in terms of the value of CMRR as follows:

$$\text{Eq. (14.3):} \quad V_o = A_d V_d + A_c V_c = A_d V_d\left(1 + \frac{A_c V_c}{A_d V_d}\right)$$

Using Eq. (14.4), we can write the above as

$$\boxed{V_o = A_d V_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)} \tag{14.6}$$

Even when both V_d and V_c components of signal are present, Eq. (14.6) shows that for large values of CMRR, the output voltage will be due mostly to the difference signal, with the common-mode component greatly reduced or rejected. Some practical examples should help clarify this idea.

EXAMPLE 14.2

Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 150\ \mu\text{V}$, $V_{i_2} = 140\ \mu\text{V}$. The amplifier has a differential gain of $A_d = 4000$ and the value of CMRR is:
(a) 100.
(b) 10^5.

Solution

$$\text{Eq. (14.1):} \quad V_d = V_{i_1} - V_{i_2} = (150 - 140)\ \mu\text{V} = 10\ \mu\text{V}$$

$$\text{Eq. (14.2):} \quad V_c = \frac{1}{2}(V_{i_1} + V_{i_2}) = \frac{150\ \mu\text{V} + 140\ \mu\text{V}}{2} = 145\ \mu\text{V}$$

(a) $$\text{Eq. (14.6):} \quad V_o = A_d V_d\left(1 + \frac{1}{\text{CMRR}}\frac{V_c}{V_d}\right)$$
$$= (4000)(10\ \mu\text{V})\left(1 + \frac{1}{100}\frac{145\ \mu\text{V}}{10\ \mu\text{V}}\right)$$
$$= 40\text{ mV}(1.145) = \mathbf{45.8\ mV}$$

(b) $$V_o = (4000)(10\ \mu\text{V})\left(1 + \frac{1}{10^5}\frac{145\ \mu\text{V}}{10\ \mu\text{V}}\right) = 40\text{ mV}(1.000145) = \mathbf{40.006\ mV}$$

Example 14.2 shows that the larger the value of CMRR, the closer the output voltage is to the difference input times the difference gain with the common-mode signal being rejected.

14.3 OP-AMP BASICS

An operational amplifier is a very high gain amplifier having very high input impedance (typically a few megohms) and low output impedance (less than 100 Ω). The basic circuit is made using a difference amplifier having two inputs (plus and minus) and at least one output. Figure 14.10 shows a basic op-amp unit. As discussed ear-

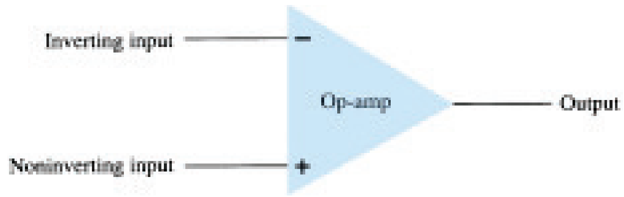


Figure 14.10 Basic op-amp.

lier, the plus (+) input produces an output that is in phase with the signal applied, while an input to the minus (−) input results in an opposite polarity output. The ac equivalent circuit of the op-amp is shown in Fig. 14.11a. As shown, the input signal applied between input terminals sees an input impedance, R_i, typically very high. The output voltage is shown to be the amplifier gain times the input signal taken through an output impedance, R_o, which is typically very low. An ideal op-amp circuit, as shown in Fig. 14.11b, would have infinite input impedance, zero output impedance, and an infinite voltage gain.

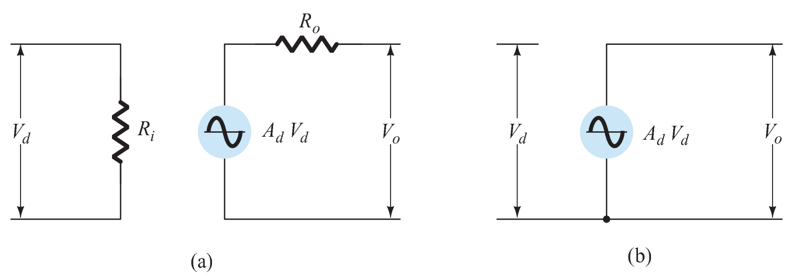


Figure 14.11 Ac equivalent of op-amp circuit: (a) practical; (b) ideal.

Basic Op-Amp

The basic circuit connection using an op-amp is shown in Fig. 14.12. The circuit shown provides operation as a constant-gain multiplier. An input signal, V_1, is applied through resistor R_1 to the minus input. The output is then connected back to the same minus input through resistor R_f. The plus input is connected to ground. Since the signal V_1 is essentially applied to the minus input, the resulting output is opposite in phase to the input signal. Figure 14.13a shows the op-amp replaced by its ac equivalent circuit. If we use the ideal op-amp equivalent circuit, replacing R_i by an infinite resistance and R_o by zero resistance, the ac equivalent circuit is that shown in Fig. 14.13b. The circuit is then redrawn, as shown in Fig. 14.13c, from which circuit analysis is carried out.

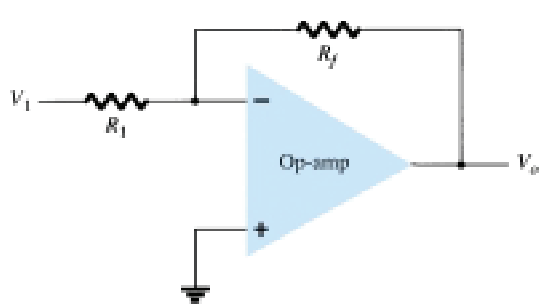


Figure 14.12 Basic op-amp connection.

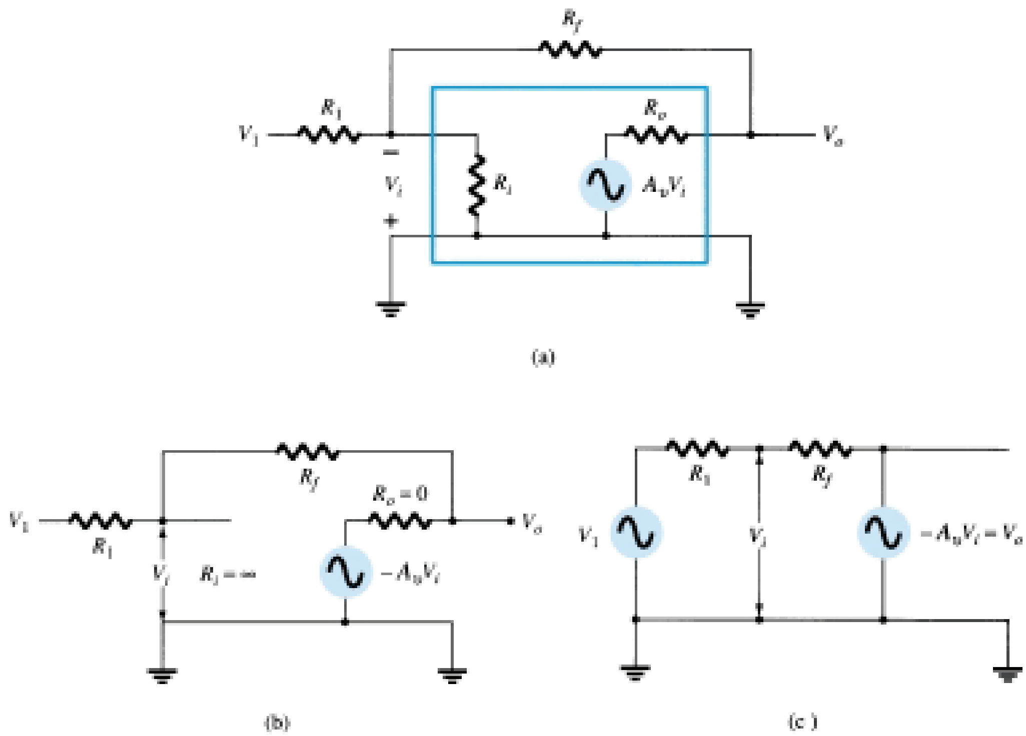


Figure 14.13 Operation of op-amp as constant-gain multiplier: (a) op-amp ac equivalent circuit; (b) ideal op-amp equivalent circuit; (c) redrawn equivalent circuit.

Using superposition, we can solve for the voltage V_1 in terms of the components due to each of the sources. For source V_1 only ($-A_v V_i$ set to zero),

$$V_{i_1} = \frac{R_f}{R_1 + R_f} V_1$$

For source $-A_v V_i$ only (V_1 set to zero),

$$V_{i_2} = \frac{R_1}{R_1 + R_f} (-A_v V_i)$$

The total voltage V_i is then

$$V_i = V_{i_1} + V_{i_2} = \frac{R_f}{R_1 + R_f} V_1 + \frac{R_1}{R_1 + R_f} (-A_v V_i)$$

which can be solved for V_i as

$$V_i = \frac{R_f}{R_f + (1 + A_v)R_1} V_1 \qquad (14.7)$$

If $A_v \gg 1$ and $A_v R_1 \gg R_f$, as is usually true, then

$$V_i = \frac{R_f}{A_v R_1} V_1$$

Solving for V_o/V_i, we get

$$\frac{V_o}{V_i} = \frac{-A_v V_i}{V_i} = \frac{-A_v}{V_i} \frac{R_f V_1}{A_v R_1} = -\frac{R_f}{R_1} \frac{V_1}{V_i}$$

so that

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1} \tag{14.8}$$

The result, in Eq. (14.8), shows that the ratio of overall output to input voltage is dependent only on the values of resistors R_1 and R_f —provided that A_v is very large.

Unity Gain

If $R_f = R_1$, the gain is

$$\text{voltage gain} = -\frac{R_f}{R_1} = -1$$

so that the circuit provides a unity voltage gain with 180° phase inversion. If R_f is exactly R_1, the voltage gain is exactly 1.

Constant Magnitude Gain

If R_f is some multiple of R_1, the overall amplifier gain is a constant. For example, if $R_f = 10R_1$, then

$$\text{voltage gain} = -\frac{R_f}{R_1} = -10$$

and the circuit provides a voltage gain of exactly 10 along with an 180° phase inversion from the input signal. If we select precise resistor values for R_f and R_1, we can obtain a wide range of gains, the gain being as accurate as the resistors used and is only slightly affected by temperature and other circuit factors.

Virtual Ground

The output voltage is limited by the supply voltage of, typically, a few volts. As stated before, voltage gains are very high. If, for example, $V_o = -10$ V and $A_v = 20{,}000$, the input voltage would then be

$$V_i = \frac{-V_o}{A_v} = \frac{10\text{ V}}{20{,}000} = 0.5\text{ mV}$$

If the circuit has an overall gain (V_o/V_1) of, say, 1, the value of V_1 would then be 10 V. Compared to all other input and output voltages, the value of V_i is then small and may be considered 0 V.

Note that although $V_i \approx 0$ V, it is not exactly 0 V. (The output voltage is a few volts due to the very small input V_i times a very large gain A_v.) The fact that $V_i \approx 0$ V leads to the concept that at the amplifier input there exists a virtual short circuit or virtual ground.

The concept of a virtual short implies that although the voltage is nearly 0 V, there is no current through the amplifier input to ground. Figure 14.14 depicts the virtual ground concept. The heavy line is used to indicate that we may consider that a short

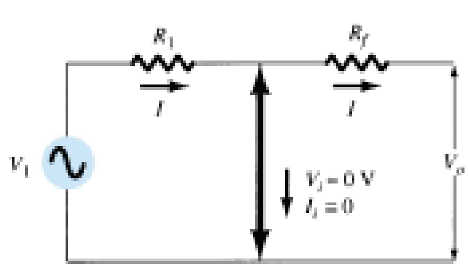


Figure 14.14 Virtual ground in an op-amp.

exists with $V_i \approx 0$ V but that this is a virtual short so that no current goes through the short to ground. Current goes only through resistors R_1 and R_f as shown.

Using the virtual ground concept, we can write equations for the current I as follows:

$$I = \frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

which can be solved for V_o/V_1:

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

The virtual ground concept, which depends on A_v being very large, allowed a simple solution to determine the overall voltage gain. It should be understood that although the circuit of Fig. 14.14 is not physically correct, it does allow an easy means for determining the overall voltage gain.

14.4 PRACTICAL OP-AMP CIRCUITS

The op-amp can be connected in a large number of circuits to provide various operating characteristics. In this section, we cover a few of the most common of these circuit connections.

Inverting Amplifier

The most widely used constant-gain amplifier circuit is the inverting amplifier, as shown in Fig. 14.15. The output is obtained by multiplying the input by a fixed or constant gain, set by the input resistor (R_1) and feedback resistor (R_f)—this output also being inverted from the input. Using Eq. (14.8) we can write

$$V_o = -\frac{R_f}{R_1} V_1$$

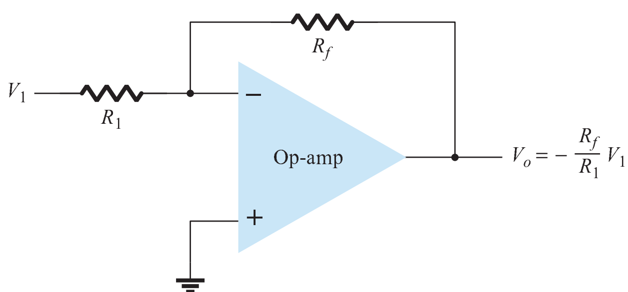


Figure 14.15 Inverting constant-gain multiplier.

EXAMPLE 14.3

If the circuit of Fig. 14.15 has $R_1 = 100$ kΩ and $R_f = 500$ kΩ, what output voltage results for an input of $V_1 = 2$ V?

Solution

$$\text{Eq. (14.8): } V_o = -\frac{R_f}{R_1} V_1 = -\frac{500\text{ k}\Omega}{100\text{ k}\Omega}(2\text{ V}) = \mathbf{-10\ V}$$

Noninverting Amplifier

The connection of Fig. 14.16a shows an op-amp circuit that works as a noninverting amplifier or constant-gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability (discussed later). To determine the voltage gain of the circuit, we can use the equivalent representation shown in Fig. 14.16b. Note that the voltage across R_1 is V_1 since $V_i \approx 0$ V. This must be equal to the output voltage, through a voltage divider of R_1 and R_f, so that

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

which results in

$$\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \tag{14.9}$$

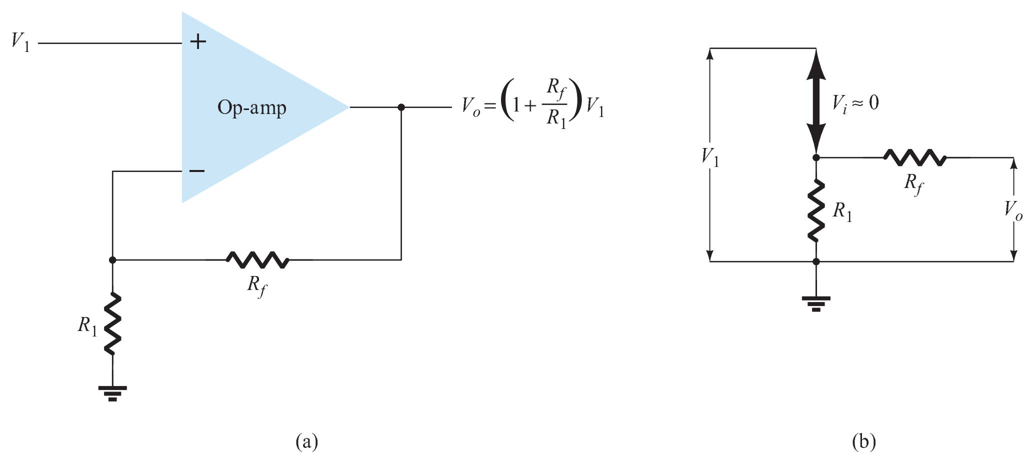


Figure 14.16 Noninverting constant-gain multiplier.

EXAMPLE 14.4

Calculate the output voltage of a noninverting amplifier (as in Fig. 14.16) for values of $V_1 = 2$ V, $R_f = 500$ kΩ, and $R_1 = 100$ kΩ.

Solution

$$\text{Eq. (14.9): } V_o = \left(1 + \frac{R_f}{R_1}\right)V_1 = \left(1 + \frac{500\text{ k}\Omega}{100\text{ k}\Omega}\right)(2\text{ V}) = 6(2\text{ V}) = \mathbf{+12\ V}$$

Unity Follower

The unity-follower circuit, as shown in Fig. 14.17a, provides a gain of unity (1) with no polarity or phase reversal. From the equivalent circuit (see Fig. 14.17b) it is clear that

$$V_o = V_1 \tag{14.10}$$

and that the output is the same polarity and magnitude as the input. The circuit operates like an emitter- or source-follower circuit except that the gain is exactly unity.

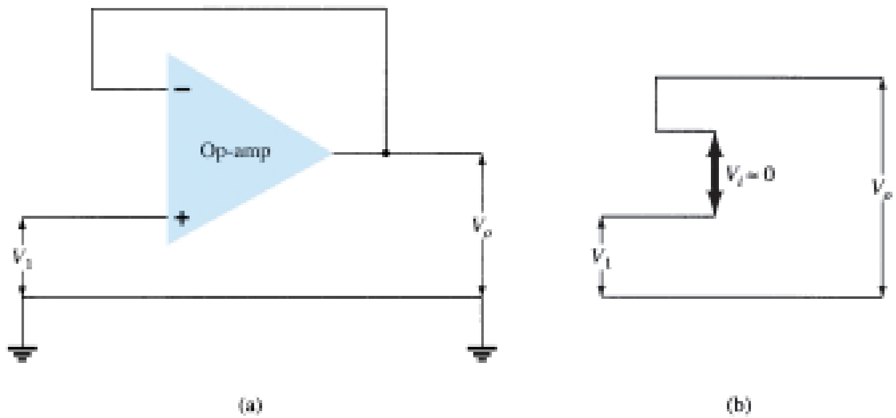


Figure 14.17 (a) Unity follower; (b) virtual-ground equivalent circuit.

Summing Amplifier

Probably the most used of the op-amp circuits is the summing amplifier circuit shown in Fig. 14.18a. The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain factor. Using the equivalent representation shown in Fig. 14.18b, the output voltage can be expressed in terms of the inputs as

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \tag{14.11}$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.

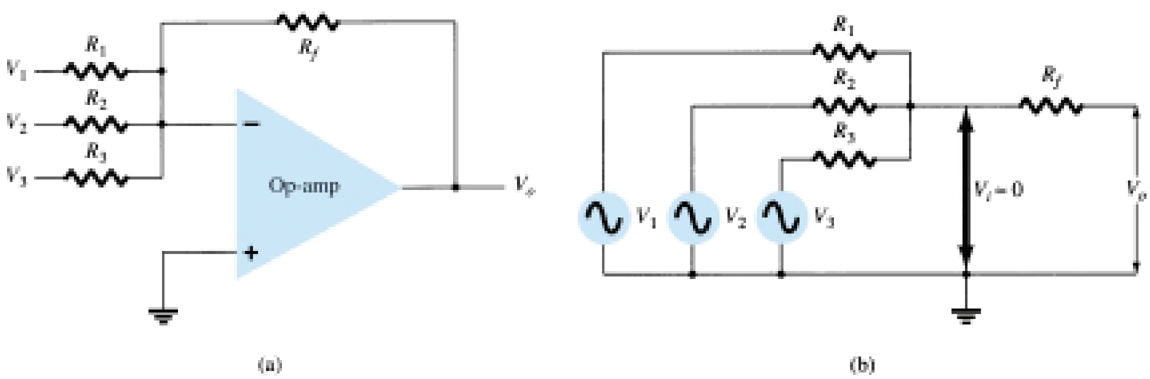


Figure 14.18 (a) Summing amplifier; (b) virtual-ground equivalent circuit.

EXAMPLE 14.5

Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use $R_f = 1\ \text{M}\Omega$ in all cases.

(a) $V_1 = +1$ V, $V_2 = +2$ V, $V_3 = +3$ V, $R_1 = 500$ kΩ, $R_2 = 1$ MΩ, $R_3 = 1$ MΩ.
(b) $V_1 = -2$ V, $V_2 = +3$ V, $V_3 = +1$ V, $R_1 = 200$ kΩ, $R_2 = 500$ kΩ, $R_3 = 1$ MΩ.

Solution

Using Eq. (14.11):

$$\text{(a)}\quad V_o = -\left[\frac{1000\text{ k}\Omega}{500\text{ k}\Omega}(+1\text{ V}) + \frac{1000\text{ k}\Omega}{1000\text{ k}\Omega}(+2\text{ V}) + \frac{1000\text{ k}\Omega}{1000\text{ k}\Omega}(+3\text{ V})\right]$$

$$= -[2(1\text{ V}) + 1(2\text{ V}) + 1(3\text{ V})] = \mathbf{-7\text{ V}}$$

$$\text{(b)}\quad V_o = -\left[\frac{1000\text{ k}\Omega}{200\text{ k}\Omega}(-2\text{ V}) + \frac{1000\text{ k}\Omega}{500\text{ k}\Omega}(+3\text{ V}) + \frac{1000\text{ k}\Omega}{1000\text{ k}\Omega}(+1\text{ V})\right]$$

$$= -[5(-2\text{ V}) + 2(3\text{ V}) + 1(1\text{ V})] = \mathbf{+3\text{ V}}$$

Integrator

So far, the input and feedback components have been resistors. If the feedback component used is a capacitor, as shown in Fig. 14.19a, the resulting connection is called an *integrator*. The virtual-ground equivalent circuit (Fig. 14.19b) shows that an expression for the voltage between input and output can be derived in terms of the current I, from input to output. Recall that virtual ground means that we can consider the voltage at the junction of R and X_C to be ground (since $V_i \approx 0$ V) but that no current goes into ground at that point. The capacitive impedance can be expressed as

$$X_C = \frac{1}{j\omega C} = \frac{1}{sC}$$

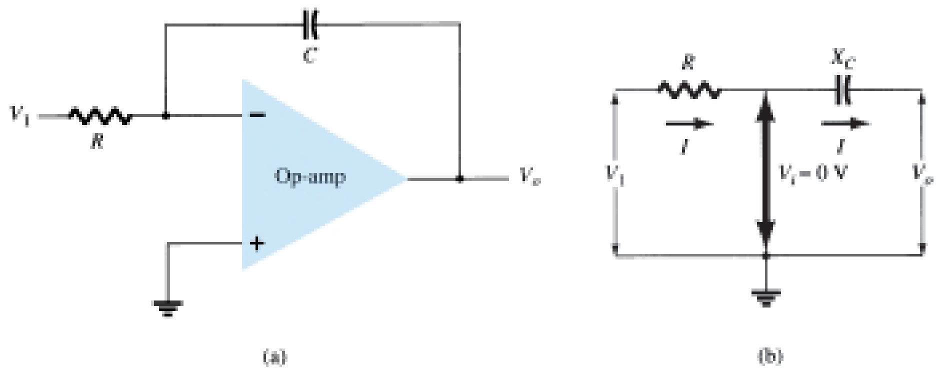


Figure 14.19 Integrator.

where $s = j\omega$ is in the Laplace notation.[*] Solving for V_o/V_1 yields

$$I = \frac{V_1}{R} = -\frac{V_o}{X_C} = \frac{-V_o}{1/sC} = -sCV_o$$

$$\frac{V_o}{V_1} = \frac{-1}{sCR} \tag{14.12}$$

The expression above can be rewritten in the time domain as

$$v_o(t) = -\frac{1}{RC}\int v_1(t)\, dt \tag{14.13}$$

*Laplace notation allows expressing differential or integral operations which are part of calculus in algebraic form using the operator **s**. Readers unfamiliar with calculus should ignore the steps leading to Eq. (14.13) and follow the physical meaning used thereafter.

Equation (14.13) shows that the output is the integral of the input, with an inversion and scale multiplier of $1/RC$. The ability to integrate a given signal provides the analog computer with the ability to solve differential equations and therefore provides the ability to electrically solve analogs of physical system operation.

The integration operation is one of summation, summing the area under a waveform or curve over a period of time. If a fixed voltage is applied as input to an integrator circuit, Eq. (14.13) shows that the output voltage grows over a period of time, providing a ramp voltage. Equation (14.13) can thus be understood to show that the output voltage ramp (for a fixed input voltage) is opposite in polarity to the input voltage and is multiplied by the factor $1/RC$. While the circuit of Fig. 14.19 can operate on many varied types of input signals, the following examples will use only a fixed input voltage, resulting in a ramp output voltage.

As an example, consider an input voltage, $V_1 = 1$ V, to the integrator circuit of Fig. 14.20a. The scale factor of $1/RC$ is

$$-\frac{1}{RC} = \frac{1}{(1\ \text{M}\Omega)(1\ \mu\text{F})} = -1$$

so that the output is a negative ramp voltage as shown in Fig. 14.20b. If the scale factor is changed by making $R = 100$ kΩ, for example, then

$$-\frac{1}{RC} = \frac{1}{(100\ \text{k}\Omega)(1\ \mu\text{F})} = -10$$

and the output is then a steeper ramp voltage, as shown in Fig. 14.20c.

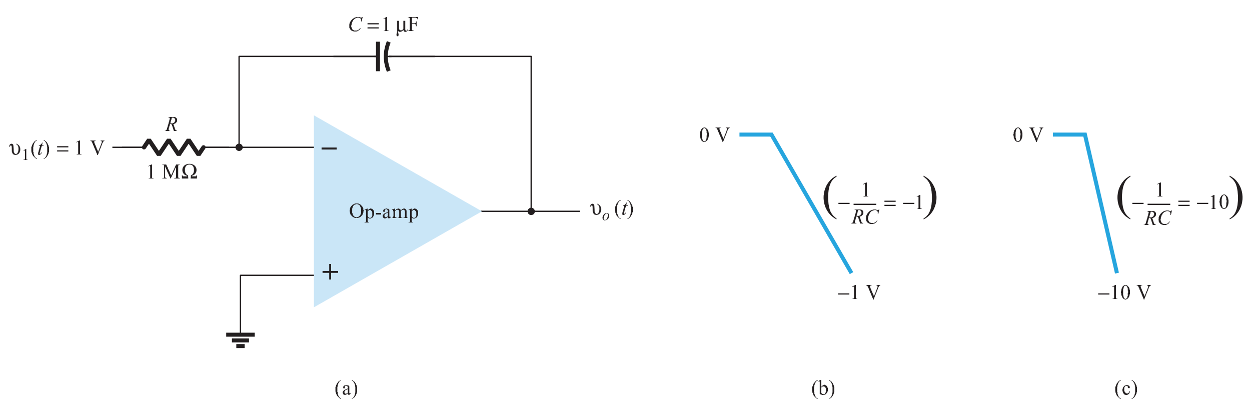


Figure 14.20 Operation of integrator with step input.

More than one input may be applied to an integrator, as shown in Fig. 14.21, with the resulting operation given by

$$v_o(t) = -\left[\frac{1}{R_1C}\int v_1(t)\,dt + \frac{1}{R_2C}\int v_2(t)\,dt + \frac{1}{R_3C}\int v_3(t)\,dt\right] \quad (14.14)$$

An example of a summing integrator as used in an analog computer is given in Fig. 14.21. The actual circuit is shown with input resistors and feedback capacitor, whereas the analog-computer representation indicates only the scale factor for each input.

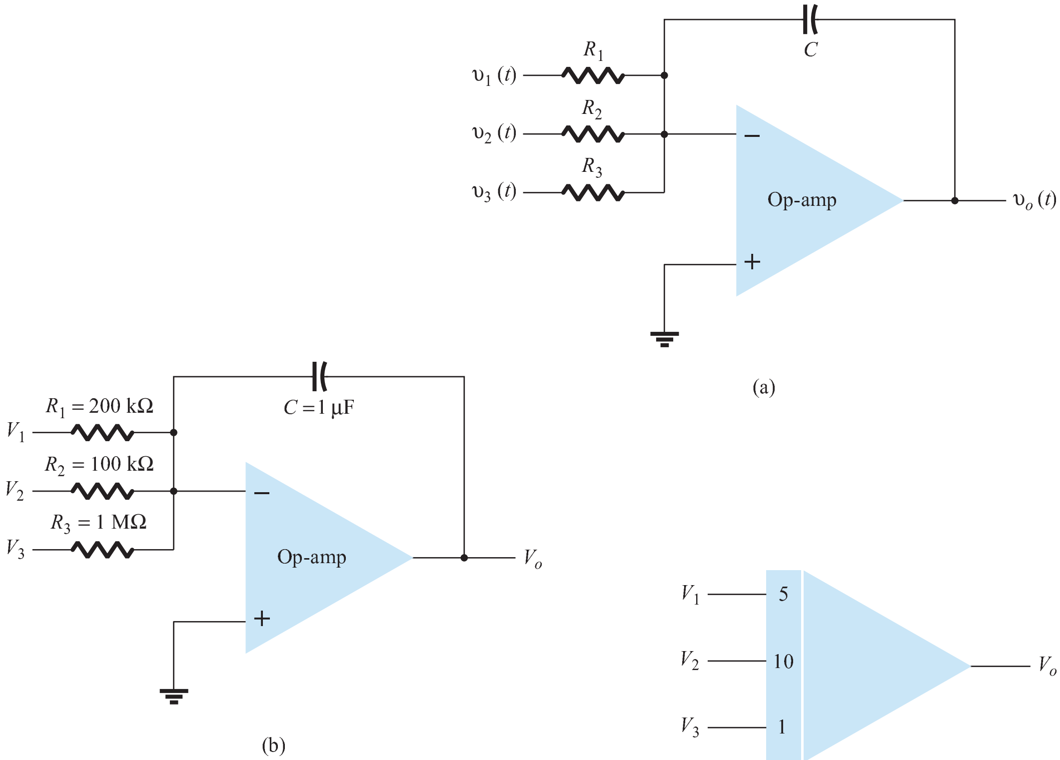


Figure 14.21 (a) Summing-integrator circuit; (b) component values; (c) analog-computer, integrator-circuit representation.

Differentiator

A differentiator circuit is shown in Fig. 14.22. While not as useful as the circuit forms covered above, the differentiator does provide a useful operation, the resulting relation for the circuit being

$$v_o(t) = -RC\,\frac{dv_1(t)}{dt} \tag{14.15}$$

where the scale factor is $-RC$.

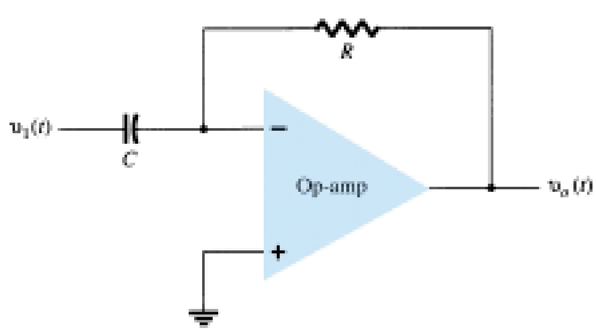


Figure 14.22 Differentiator circuit.

14.5 OP-AMP SPECIFICATIONS—DC OFFSET PARAMETERS

Before going into various practical applications using op-amps, we should become familiar with some of the parameters used to define the operation of the unit. These specifications include both dc and transient or frequency operating features, as covered next.

Offset Currents and Voltages

While the op-amp output should be 0 V when the input is 0 V, in actual operation there is some offset voltage at the output. For example, if one connected 0 V to both op-amp inputs and then measured 26 mV(dc) at the output, this would represent 26 mV of unwanted voltage generated by the circuit and not by the input signal. Since the user may connect the amplifier circuit for various gain and polarity operations, however, the manufacturer specifies an input offset voltage for the op-amp. The output offset voltage is then determined by the input offset voltage and the gain of the amplifier, as connected by the user.

The output offset voltage can be shown to be affected by two separate circuit conditions. These are: (1) an input offset voltage, V_{IO}, and (2) an offset current due to the difference in currents resulting at the plus (+) and minus (−) inputs.

INPUT OFFSET VOLTAGE, V_{IO}

The manufacturer's specification sheet provides a value of V_{IO} for the op-amp. To determine the effect of this input voltage on the output, consider the connection shown in Fig. 14.23. Using $V_o = AV_i$, we can write

$$V_o = AV_i = A\left(V_{IO} - V_o \frac{R_1}{R_1 + R_f}\right)$$

Solving for V_o, we get

$$V_o = V_{IO} \frac{A}{1 + A[R_1/(R_1 + R_f)]} \approx V_{IO} \frac{A}{A[R_1/(R_1 + R_f)]}$$

from which we can write

$$V_o(\text{offset}) = V_{IO} \frac{R_1 + R_f}{R_1} \qquad (14.16)$$

Equation (14.16) shows how the output offset voltage results from a specified input offset voltage for a typical amplifier connection of the op-amp.

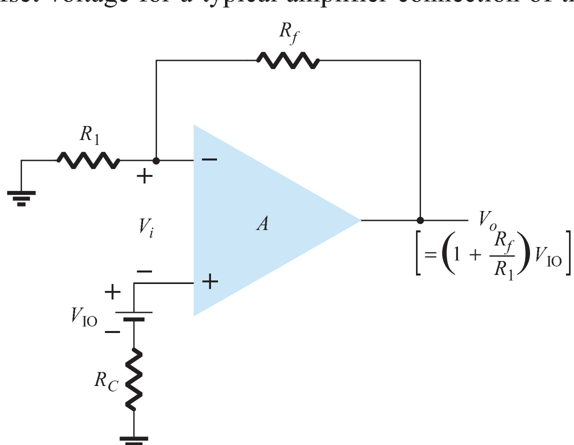


Figure 14.23 Operation showing effect of input offset voltage, V_{IO}.

EXAMPLE 14.6 Calculate the output offset voltage of the circuit in Fig. 14.24. The op-amp spec lists $V_{IO} = 1.2$ mV.

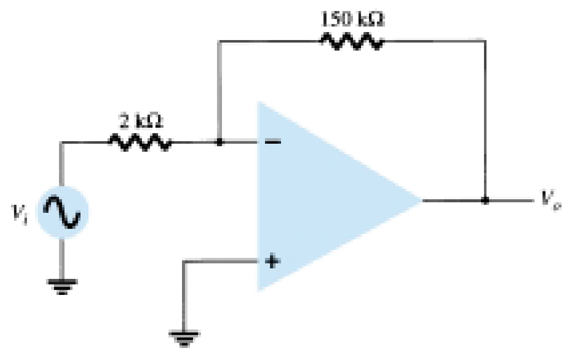


Figure 14.24 Op-amp connection for Examples 14.6 and 14.7.

Solution

Eq. (14.16): $$V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1} = (1.2 \text{ mV})\left(\frac{2 \text{ k}\Omega + 150 \text{ k}\Omega}{2 \text{ k}\Omega}\right) = \mathbf{91.2 \text{ mV}}$$

OUTPUT OFFSET VOLTAGE DUE TO INPUT OFFSET CURRENT, I_{IO}

An output offset voltage will also result due to any difference in dc bias currents at both inputs. Since the two input transistors are never exactly matched, each will operate at a slightly different current. For a typical op-amp connection, such as that shown in Fig. 14.25, an output offset voltage can be determined as follows. Replacing the bias currents through the input resistors by the voltage drop that each develops, as shown in Fig. 14.26, we can determine the expression for the resulting output voltage. Using superposition, the output voltage due to input bias current I_{IB}^+, denoted by V_o^+, is

$$V_o^+ = I_{IB}^+ R_C\left(1 + \frac{R_f}{R_1}\right)$$

while the output voltage due to only I_{IB}^-, denoted by V_o^-, is

$$V_o^- = I_{IB}^- R_1\left(-\frac{R_f}{R_1}\right)$$

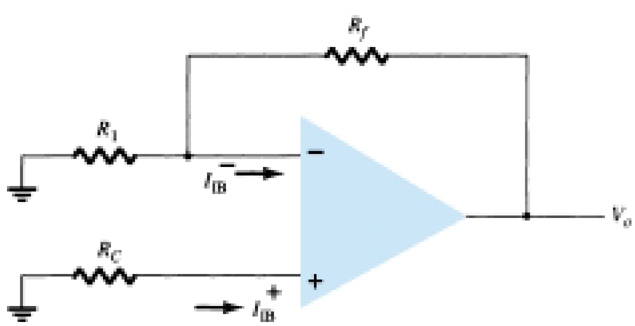


Figure 14.25 Op-amp connection showing input bias currents.

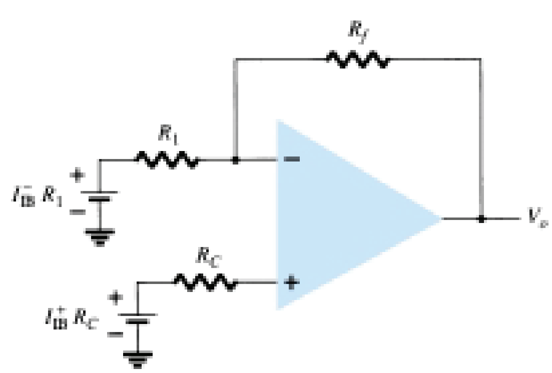


Figure 14.26 Redrawn circuit of Fig. 14.25.

for a total output offset voltage of

$$V_o(\text{offset due to } I_{IB}^+ \text{ and } I_{IB}^-) = I_{IB}^+ R_C\left(1 + \frac{R_f}{R_1}\right) - I_{IB}^- R_1\frac{R_f}{R_1} \qquad (14.17)$$

Since the main consideration is the difference between the input bias currents rather than each value, we define the offset current I_{IO} by

$$I_{IO} = I_{IB}^+ - I_{IB}^-$$

Since the compensating resistance R_C is usually approximately equal to the value of R_1, using $R_C = R_1$ in Eq. (14.17) we can write

$$V_o(\text{offset}) = I_{IB}^+(R_1 + R_f) - I_{IB}^- R_f$$

$$= I_{IB}^+ R_f - I_{IB}^- R_f = R_f(I_{IB}^+ - I_{IB}^-)$$

resulting in

$$\boxed{V_o(\text{offset due to } I_{IO}) = I_{IO} R_f} \qquad (14.18)$$

EXAMPLE 14.7

Calculate the offset voltage for the circuit of Fig. 14.24 for op-amp specification listing $I_{IO} = 100$ nA.

Solution

Eq. (14.18): $V_o = I_{IO} R_f = (100 \text{ nA})(150 \text{ k}\Omega) = \mathbf{15\ mV}$

TOTAL OFFSET DUE TO V_{IO} AND I_{IO}

Since the op-amp output may have an output offset voltage due to both factors covered above, the total output offset voltage can be expressed as

$$|V_o(\text{offset})| = |V_o(\text{offset due to } V_{IO})| + |V_o(\text{offset due to } I_{IO})| \qquad (14.19)$$

The absolute magnitude is used to accommodate the fact that the offset polarity may be either positive or negative.

EXAMPLE 14.8

Calculate the total offset voltage for the circuit of Fig. 14.27 for an op-amp with specified values of input offset voltage, $V_{IO} = 4$ mV and input offset current $I_{IO} = 150$ nA.

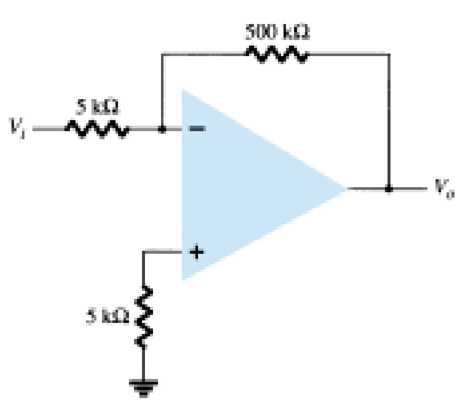


Figure 14.27 Op-amp circuit for Example 14.8.

Solution

The offset due to V_{IO} is

$$\text{Eq. (14.16):}\quad V_o(\text{offset due to } V_{IO}) = V_{IO}\frac{R_1 + R_f}{R_1} = (4\text{ mV})\left(\frac{5\text{ k}\Omega + 500\text{ k}\Omega}{5\text{ k}\Omega}\right)$$

$$= 404\text{ mV}$$

$$\text{Eq. (14.18):}\quad V_o(\text{offset due to } I_{IO}) = I_{IO}R_f = (150\text{ nA})(500\text{ k}\Omega) = 75\text{ mV}$$

resulting in a total offset

$$\text{Eq. (14.19):}\quad V_o(\text{total offset}) = V_o(\text{offset due to } V_{IO}) + V_o(\text{offset due to } I_{IO})$$

$$= 404\text{ mV} + 75\text{ mV} = \mathbf{479\text{ mV}}$$

INPUT BIAS CURRENT, I_{IB}

A parameter related to I_{IO} and the separate input bias currents I_{IB}^{+} and I_{IB}^{-} is the average bias current defined as

$$I_{IB} = \frac{I_{IB}^{+} + I_{IB}^{-}}{2} \tag{14.20}$$

One could determine the separate input bias currents using the specified values I_{IO} and I_{IB}. It can be shown that for $I_{IB}^{+} > I_{IB}^{-}$

$$I_{IB}^{+} = I_{IB} + \frac{I_{IO}}{2} \tag{14.21}$$

$$I_{IB}^{-} = I_{IB} - \frac{I_{IO}}{2} \qquad (14.21)$$

EXAMPLE 14.9

Calculate the input bias currents at each input of an op-amp having specified values of $I_{IO} = 5$ nA and $I_{IB} = 30$ nA.

Solution

Using Eq. (14.21):

$$I_{IB}^{+} = I_{IB} + \frac{I_{IO}}{2} = 30\text{ nA} + \frac{5\text{ nA}}{2} = \mathbf{32.5\text{ nA}}$$

$$I_{IB}^{-} = I_{IB} - \frac{I_{IO}}{2} = 30\text{ nA} - \frac{5\text{ nA}}{2} = \mathbf{27.5\text{ nA}}$$

14.6 OP-AMP SPECIFICATIONS—FREQUENCY PARAMETERS

An op-amp is designed to be a high-gain, wide-bandwidth amplifier. This operation tends to be unstable (oscillate) due to positive feedback (see Chapter 18). To ensure stable operation, op-amps are built with internal compensation circuitry, which also causes the very high open-loop gain to diminish with increasing frequency. This gain reduction is referred to as *roll-off*. In most op-amps, roll-off occurs at a rate of 20 dB per decade (-20 dB/decade) or 6 dB per octave (-6 dB/octave). (Refer to Chapter 11 for introductory coverage of dB and frequency response.)

Note that while op-amp specifications list an open-loop voltage gain (A_{VD}), the user typically connects the op-amp using feedback resistors to reduce the circuit voltage gain to a much smaller value (closed-loop voltage gain, A_{CL}). A number of circuit improvements result from this gain reduction. First, the amplifier voltage gain is a more stable, precise value set by the external resistors; second, the input impedance of the circuit is increased over that of the op-amp alone; third, the circuit output impedance is reduced from that of the op-amp alone; and finally, the frequency response of the circuit is increased over that of the op-amp alone.

Gain–Bandwidth

Because of the internal compensation circuitry included in an op-amp, the voltage gain drops off as frequency increases. Op-amp specifications provide a description of the gain versus bandwidth. Figure 14.28 provides a plot of gain versus frequency for a typical op-amp. At low frequency down to dc operation the gain is that value listed by the manufacturer's specification A_{VD} (voltage differential gain) and is typically a very large value. As the frequency of the input signal increases the open-loop gain drops off until it finally reaches the value of 1 (unity). The frequency at this gain value is specified by the manufacturer as the unity-gain bandwidth, B_1. While this value is a frequency (see Fig. 14.28) at which the gain becomes 1, it can be considered a bandwidth, since the frequency band from 0 Hz to the unity-gain frequency is also a bandwidth. One could therefore refer to the point at which the gain reduces to 1 as the unity-gain frequency (f_1) or unity-gain bandwidth (B_1).

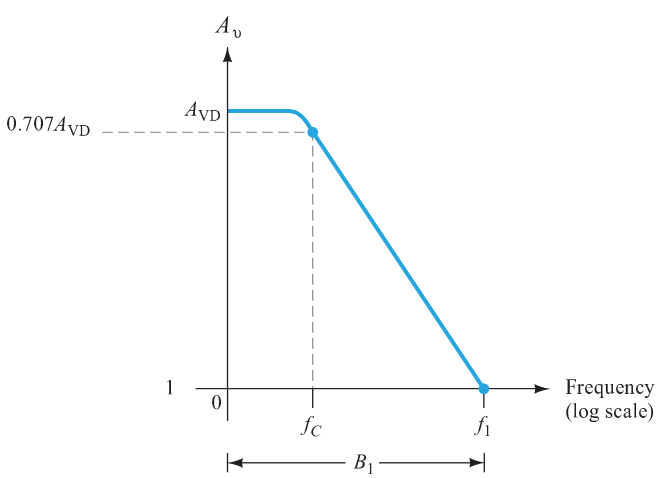


Figure 14.28 Gain versus frequency plot.

Another frequency of interest is that shown in Fig. 14.28, at which the gain drops by 3 dB (or to 0.707 the dc gain, A_{VD}), this being the cutoff frequency of the op-amp, f_C. In fact, the unity-gain frequency and cutoff frequency are related by

$$f_1 = A_{VD} f_C \tag{14.22}$$

Equation (14.22) shows that the unity-gain frequency may also be called the gain–bandwidth product of the op-amp.

EXAMPLE 14.10 Determine the cutoff frequency of an op-amp having specified values $B_1 = 1$ MHz and $A_{VD} = 200$ V/mV.

Solution

Since $f_1 = B_1 = 1$ MHz, we can use Eq. (14.22) to calculate

$$f_C = \frac{f_1}{A_{VD}} = \frac{1 \text{ MHz}}{200 \text{ V/mV}} = \frac{1 \times 10^6}{200 \times 10^3} = \mathbf{5\ Hz}$$

Slew Rate, SR

Another parameter reflecting the op-amp's ability to handling varying signals is slew rate, defined as

slew rate = maximum rate at which amplifier output can change in volts per microsecond (V/μs)

$$\text{SR} = \frac{\Delta V_o}{\Delta t} \quad \text{V}/\mu\text{s} \quad \text{with } t \text{ in } \mu\text{s} \tag{14.23}$$

The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal.* If one tried to drive the output at a rate of voltage change greater than the slew rate, the output would not be able to change fast enough and would not vary over the full range expected, resulting in signal clipping or distortion. In any case, the output would not be an amplified duplicate of the input signal if the op-amp slew rate is exceeded.

EXAMPLE 14.11 For an op-amp having a slew rate of SR = 2 V/μs, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.5 V in 10 μs?

Solution

Since $V_o = A_{CL} V_i$, we can use

$$\frac{\Delta V_o}{\Delta t} = A_{CL} \frac{\Delta V_i}{\Delta t}$$

from which we get

$$A_{CL} = \frac{\Delta V_o/\Delta t}{\Delta V_i/\Delta t} = \frac{\text{SR}}{\Delta V_i/\Delta t} = \frac{2 \text{ V}/\mu\text{s}}{0.5 \text{ V}/10\ \mu\text{s}} = \mathbf{40}$$

Any closed-loop voltage gain of magnitude greater than 40 would drive the output at a rate greater than the slew rate allows, so the maximum closed-loop gain is 40.

*The closed-loop gain is that obtained with the output connected back to the input in some way.

Maximum Signal Frequency

The maximum frequency that an op-amp may operate at depends on both the bandwidth (BW) and slew rate (SR) parameters of the op-amp. For a sinusoidal signal of general form

$$v_o = K \sin(2\pi f t)$$

the maximum voltage rate of change can be shown to be

$$\text{signal maximum rate of change} = 2\pi f K \qquad \text{V/s}$$

To prevent distortion at the output, the rate of change must also be less than the slew rate, that is,

$$2\pi f K \leq \text{SR}$$

$$\omega K \leq \text{SR}$$

so that

$$f \leq \frac{\text{SR}}{2\pi K} \qquad \text{Hz}$$

$$\omega \leq \frac{\text{SR}}{K} \qquad \text{rad/s} \tag{14.24}$$

Additionally, the maximum frequency, f, in Eq. (14.24), is also limited by the unity-gain bandwidth.

EXAMPLE 14.12

For the signal and circuit of Fig. 14.29, determine the maximum frequency that may be used. Op-amp slew rate is SR = 0.5 V/μs.

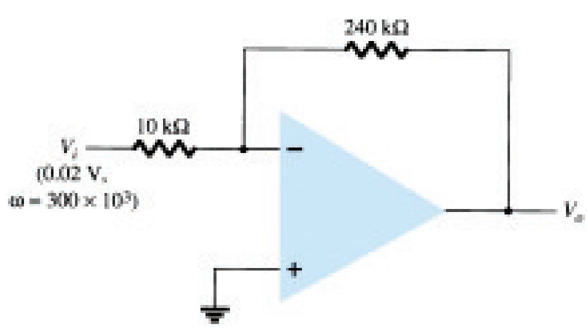


Figure 14.29 Op-amp circuit for Example 14.12.

Solution

For a gain of magnitude

$$A_{CL} = \left|\frac{R_f}{R_1}\right| = \frac{240\ \text{k}\Omega}{10\ \text{k}\Omega} = 24$$

the output voltage provides

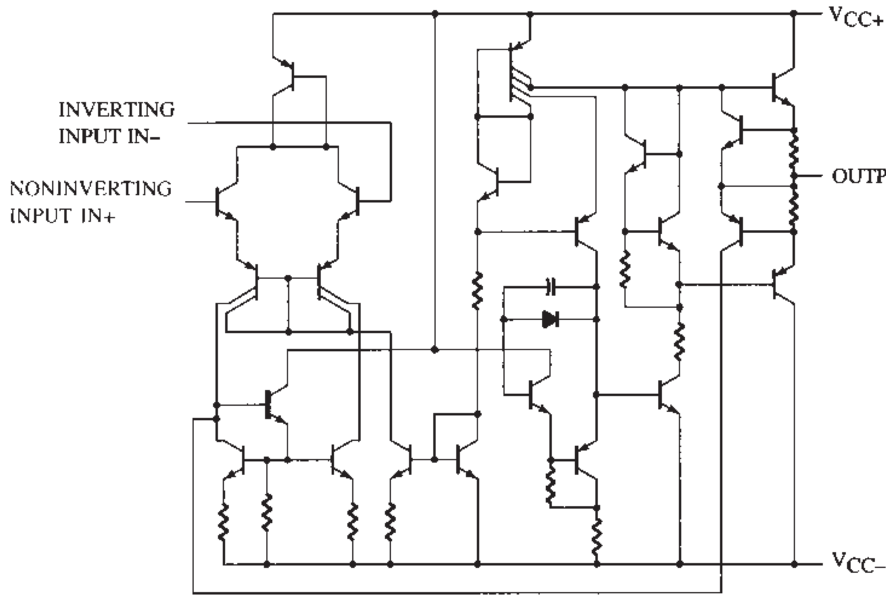
$$K = A_{CL} V_i = 24(0.02\ \text{V}) = 0.48\ \text{V}$$

$$\text{Eq. (14.24):} \quad \omega \leq \frac{\text{SR}}{K} = \frac{0.5\ \text{V}/\mu\text{s}}{0.48\ \text{V}} = \mathbf{1.1 \times 10^6\ rad/s}$$

Since the signal's frequency, $\omega = 300 \times 10^3$ rad/s, is less than the maximum value determined above, no output distortion will result.

14.7 OP-AMP UNIT SPECIFICATIONS

In this section, we discuss how the manufacturer's specifications are read for a typical op-amp unit. A popular bipolar op-amp IC is the 741 described by the information provided in Fig. 14.30. The op-amp is available in a number of packages, an 8-pin DIP and a 10-pin flatpack being among the more usual forms.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA741M	uA741C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		– 22	– 18	V
Differential input voltage (see Note 2)		± 30	± 30	V
Input voltage any input (see Notes 1 and 3)		± 15	± 15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		± 0.5	± 0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 5)		500	500	mW
Operating free-air temperature range		– 55 to 125	0 to 70	°C
Storage temperature range		– 65 to 150	– 65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	FH, FK, J, JG, or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	°C

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the uA741M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J and JG packages, uA741M chips are alloy mounted; uA741C chips are glass mounted.

Figure 14.30 741 op-amp specifications.

electrical characteristics at specified free-air temperature, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V

PARAMETER		TEST CONDITIONS†		uA741M MIN	uA741M TYP	uA741M MAX	uA741C MIN	uA741C TYP	uA741C MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$	25°C		± 15			± 15		mV
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	± 12	± 13		± 12	± 13		V
			Full range	± 12			± 12			
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	25°C	± 12	± 14		± 12	± 14		V
		$R_L \geq 10\ k\Omega$	Full range	± 12			± 12			
		$R_L = 2\ k\Omega$	25°C	± 10	± 13		± 10	± 13		
		$R_L \geq 2\ k\Omega$	Full range	± 10			± 10			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$	25°C	50	200		20	200		V/mV
		$V_O = \pm 10$ V	Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	VO = 0 See note 6	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity $(\Delta V_{IO}/\Delta V_{CC})$	$V_{CC} = \pm 9$ V to ± 15 V	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		± 25	± 40		± 25	± 40	mA
I_{CC}	Supply current	No load, $V_O = 0$	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, $V_O = 0$	25°C		50	85		50	85	mW
			Full range			100			100	

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	uA741M MIN	uA741M TYP	uA741M MAX	uA741C MIN	uA741C TYP	uA741C MAX	UNIT
t_r	Rise time	$V_I = 20$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.3			0.3		μs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.5			0.5		V/μs

Figure 14.30 Continued.

Absolute Maximum Ratings

The absolute maximum ratings provide information on what largest voltage supplies may be used, how large the input signal swing may be, and at how much power the device is capable of operating. Depending on the particular version of 741 used, the largest supply voltage is a dual supply of ±18 V or ±22 V. In addition, the IC can internally dissipate from 310 to 570 mW, depending on the IC package used. Table 14.1 summarizes some typical values to use in examples and problems.

TABLE 14.1 Absolute Maximum Ratings

Supply voltage	±22 V
Internal power dissipation	500 mW
Differential input voltage	±30 V
Input voltage	±15 V

EXAMPLE 14.13

Determine the current draw from a dual power supply of ±12 V if the IC dissipates 500 mW.

Solution

If we assume that each supply provides half the total power to the IC, then

$$P = VI$$

$$250 \text{ mW} = 12 \text{ V}(I)$$

so that each supply must provide a current of

$$I = \frac{250 \text{ mW}}{12 \text{ V}} = \mathbf{20.83 \text{ mA}}$$

Electrical Characteristics

Electrical characteristics include many of the parameters covered earlier in this chapter. The manufacturer provides some combination of typical, minimum, or maximum values for various parameters as deemed most useful to the user. A summary is provided in Table 14.2.

TABLE 14.2 μA741 Electrical Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°$C

Characteristic	*MIN*	*TYP*	*MAX*	*Unit*
V_{IO} Input offset voltage		1	6	mV
I_{IO} Input offset current		20	200	nA
I_{IB} Input bias current		80	500	nA
V_{ICR} Common-mode input voltage range	±12	±13		V
V_{OM} Maximum peak output voltage swing	±12	±14		V
A_{VD} Large-signal differential voltage amplification	20	200		V/mV
r_i Input resistance	0.3	2		MΩ
r_o Output resistance		75		Ω
C_i Input capacitance		1.4		pF
CMRR Common-mode rejection ratio	70	90		dB
I_{CC} Supply current		1.7	2.8	mA
P_D Total power dissipation		50	85	mW

V_{IO} **Input offset voltage:** The input offset voltage is seen to be typically 1 mV, but can go as high as 6 mV. The output offset voltage is then computed based on the circuit used. If the worst condition possible is of interest, the maximum value should be used. Typical values are those more commonly expected when using the op-amp.

I_{IO} **Input offset current:** The input offset current is listed to be typically 20 nA, while the largest value expected is 200 nA.

I_{IB} **Input bias current:** The input bias current is typically 80 nA and may be as large as 500 nA.

V_{ICR} **Common-mode input voltage range:** This parameter lists the range that the input voltage may vary over (using a supply of ±15 V), about ±12 to ±13 V. Inputs larger in amplitude than this value will probably result in output distortion and should be avoided.

V_{OM} **Maximum peak output voltage swing:** This parameter lists the largest value the output may vary (using a ±15-V supply). Depending on the circuit closed-loop gain, the input signal should be limited to keep the output from varying by an amount no larger than ±12 V, in the worst case, or by ±14 V, typically.

$\boldsymbol{A_{VD}}$ **Large-signal differential voltage amplification:** This is the open-loop voltage gain of the op-amp. While a minimum value of 20 V/mV or 20,000 V/V is listed, the manufacturer also lists a typical value of 200 V/mV or 200,000 V/V.

$\boldsymbol{r_i}$ **Input resistance:** The input resistance of the op-amp when measured under open-loop is typically 2 MΩ but could be as little as 0.3 MΩ or 300 kΩ. In a closed-loop circuit, this input impedance can be much larger, as discussed previously.

$\boldsymbol{r_o}$ **Output resistance:** The op-amp output resistance is listed as typically 75 Ω. No minimum or maximum value is given by the manufacturer for this op-amp. Again, in a closed-loop circuit, the output impedance can be lower, depending on the circuit gain.

$\boldsymbol{C_i}$ **Input capacitance:** For high-frequency considerations, it is helpful to know that the input to the op-amp has typically 1.4 pF of capacitance, a generally small value compared even to stray wiring.

CMRR Common-mode rejection ratio: The op-amp parameter is seen to be typically 90 dB but could go as low as 70 dB. Since 90 dB is equivalent to 31622.78, the op-amp amplifies noise (common inputs) by over 30,000 times less than difference inputs.

$\boldsymbol{I_{CC}}$ **Supply current:** The op-amp draws a total of 2.8 mA, typically from the dual voltage supply, but the current drawn could be as little as 1.7 mA. This parameter helps the user determine the size of the voltage supply to use. It also can be used to calculate the power dissipated by the IC ($P_D = 2V_{CC}I_{CC}$).

$\boldsymbol{P_D}$ **Total power dissipation:** The total power dissipated by the op-amp is typically 50 mW but could go as high as 85 mW. Referring to the previous parameter, the op-amp will dissipate about 50 mW when drawing about 1.7 mA using a dual 15-V supply. At smaller supply voltages, the current drawn will be less and the total power dissipated will also be less.

EXAMPLE 14.14

Using the specifications listed in Table 14.2, calculate the typical output offset voltage for the circuit connection of Fig. 14.31.

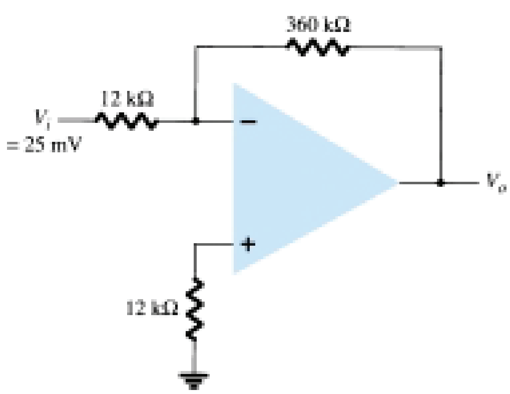


Figure 14.31 Op-amp circuit for Examples 14.14, 14.15, and 14.17.

Solution

The output offset due to V_{IO} is calculated to be

$$\text{Eq. (14.16):}\quad V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1} = (1\text{ mV})\left(\frac{12\text{ k}\Omega + 360\text{ k}\Omega}{12\text{ k}\Omega}\right) = 31\text{ mV}$$

The output voltage due to I_{IO} is calculated to be

$$\text{Eq. (14.18):} \quad V_o(\text{offset}) = I_{IO}R_f = 20 \text{ nA}(360 \text{ k}\Omega) = 7.2 \text{ mV}$$

Assuming that these two offsets are the same polarity at the output, the total output offset voltage is then

$$V_o(\text{offset}) = 31 \text{ mV} + 7.2 \text{ mV} = \mathbf{38.2\ mV}$$

EXAMPLE 14.15

For the typical characteristics of the 741 op-amp ($r_o = 75\ \Omega$, $A = 200\ \text{k}\Omega$), calculate the following values for the circuit of Fig. 14.31.

(a) A_{CL}.
(b) Z_i.
(c) Z_o.

Solution

(a) Eq. (14.8): $\dfrac{V_o}{V_i} = -\dfrac{R_f}{R_1} = -\dfrac{360\ \text{k}\Omega}{12\ \text{k}\Omega} = \mathbf{-30} \cong \dfrac{1}{\beta}$

(b) $Z_i = R_1 = \mathbf{12\ k\Omega}$

(c) $Z_o = \dfrac{r_o}{(1 + \beta A)} = \dfrac{75\ \Omega}{1 + \left(\dfrac{1}{30}\right)(200\ \text{k}\Omega)} = \mathbf{0.011\ \Omega}$

Operating Characteristics

Another group of values used to describe the operation of the op-amp over varying signals are provided in Table 14.3.

TABLE 14.3 Operating Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°$C

Parameter	*MIN*	*TYP*	*MAX*	*Unit*
B_1 Unity gain bandwidth		1		MHz
t_r Rise time		0.3		μs

EXAMPLE 14.16

Calculate the cutoff frequency of an op-amp having characteristics given in Tables 14.2 and 14.3.

Solution

$$\text{Eq. (14.22):}\ f_C = \frac{f_1}{A_{VD}} = \frac{B_1}{A_{VD}} = \frac{1 \text{ MHz}}{20{,}000} = \mathbf{50\ Hz}$$

EXAMPLE 14.17

Calculate the maximum frequency of the input signal for the circuit in Fig. 14.31, with an input of $V_i = 25$ mV.

Solution

For a closed-loop gain of $A_{CL} = 30$ and an input of $V_i = 25$ mV, the output gain factor is calculated to be

$$K = A_{CL}V_i = 30(25 \text{ mV}) = 750 \text{ mV} = 0.750 \text{ V}$$

Using Eq. (14.24), the maximum signal frequency, f_{max}, is

$$f_{\text{max}} = \frac{\text{SR}}{2\pi K} = \frac{0.5\ \text{V}/\mu\text{s}}{2\pi(0.750\ \text{V})} = \mathbf{106\ kHz}$$

Op-Amp Performance

The manufacturer provides a number of graphical descriptions to describe the performance of the op-amp. Figure 14.32 includes some typical performance curves comparing various characteristics as a function of supply voltage. The open-loop voltage gain is seen to get larger with a larger supply voltage value. While the previous tabular information provided information at a particular supply voltage, the performance curve shows how the voltage gain is affected by using a range of supply voltage values.

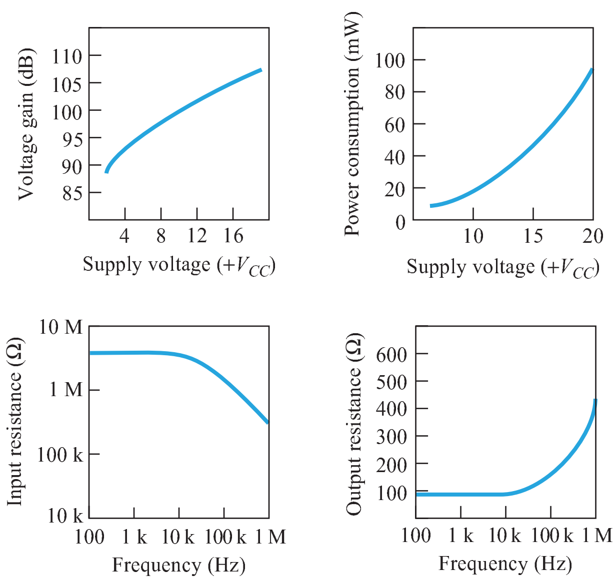


Figure 14.32 Performance curves.

EXAMPLE 14.18

Using Fig. 14.32, determine the open-loop voltage gain for a supply voltage of $V_{CC} = \pm 12$ V.

Solution

From the curve in Fig. 14.32, $A_{\text{VD}} \approx 104$ dB. This is a linear voltage gain of

$$A_{\text{VD}}\ (\text{dB}) = 20 \log_{10} A_{\text{VD}}$$

$$104\ \text{dB} = 20 \log A_{\text{VD}}$$

$$A_{\text{VD}} = \text{antilog}\ \frac{104}{20} = 158.5 \times 10^3$$

Another performance curve in Fig. 14.32 shows how power consumption varies as a function of supply voltage. As shown, the power consumption increases with larger values of supply voltage. For example, while the power dissipation is about 50 mW at $V_{CC} = \pm 15$ V, it drops to about 5 mW with $V_{CC} = \pm 5$ V. Two other curves show how the input and output resistances are affected by frequency, the input impedance dropping and the output resistance increasing at higher frequency.

14.8 PSPICE WINDOWS

The evaluation version of PSpice has only four op-amp units. These are defined by the subcircuit made up of various transistors, resistors, capacitors, and so on. These are models of four of the more common op-amp units and have their unit specifications. One can model an op-amp to provide a more ideal unit—this being helpful when describing theoretical circuit connections. Lets start by describing an op-amp model that can be used to analyze circuits.

PSpice Op-Amp Model

An op-amp can be described by a schematic circuit having an input impedance, R_i, an output impedance, R_O, and a voltage gain, A_v. Figure 14.33 shows this basic circuit, using the typical values of a 741 op-amp:

$$R_i = 2\text{ M}\Omega, \qquad R_O = 75\Omega, \qquad A_v = 200{,}000 = 200\text{ V/mV}$$

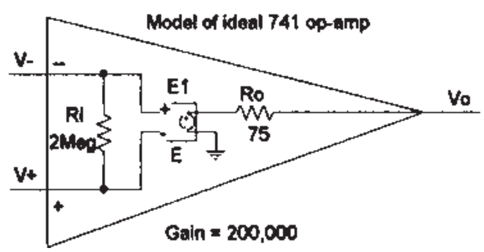


Figure 14.33 PSpice ideal op-amp model.

The values of input and output resistance are provided by resistor components with desired values. The gain of the op-amp is provided using a voltage-controlled voltage source, schematic device part labeled **E.** Figure 14.34 shows setting the E device for a gain of 200,000 (the device parameter **GAIN** is set to a value of 200,000). The schematic circuit of Fig. 14.33 thus represents a 741 op-amp with typical specs listed above.

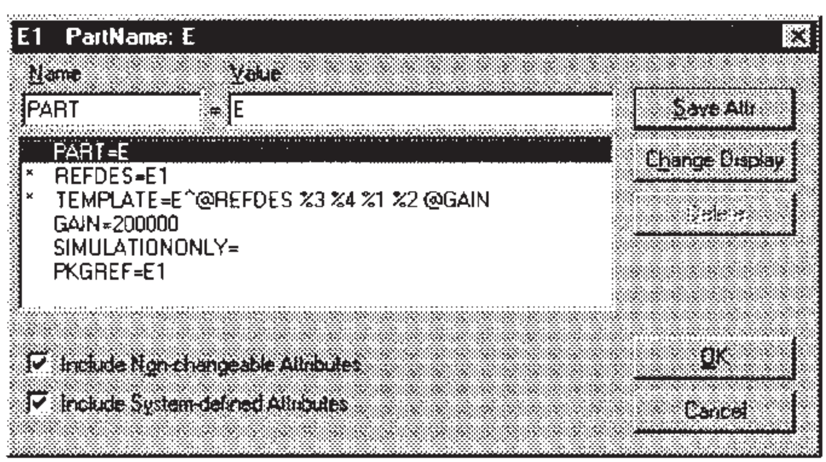


Figure 14.34 Setting gain of part E.

Program 14.1—Inverting Op-Amp

An inverting op-amp of the type described in Example 14.3 and shown in Fig. 14.15 is considered first. Using the ideal model of Fig. 14.33, an inverting op-amp circuit is drawn as in Fig. 14.35. With the dc voltage display turned on, the result after running an analysis shows that for an input of 2 V and a circuit gain of −5.

$$A_v = -R_F/R_1 = -500\ \text{k}\Omega/100\ \text{k}\Omega = -5$$

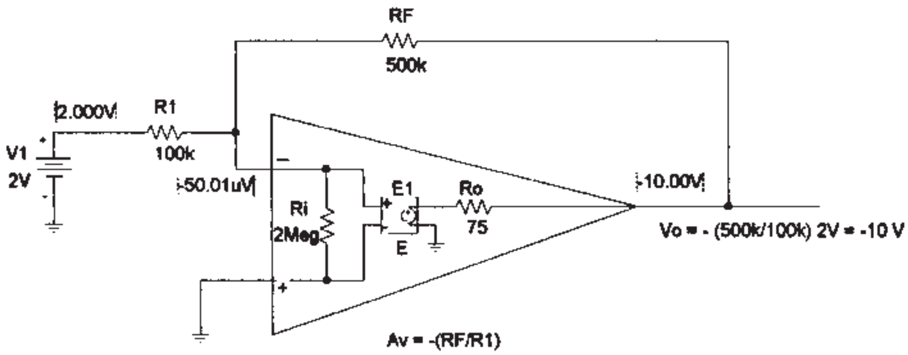


Figure 14.35 Inverting op-amp using ideal model.

The output is exactly −10 V

$$V_O = A_v V_i = -5(2\ \text{V}) = -10\ \text{V}$$

The input to the minus terminal is −50.01 μV, which is virtually ground or 0 V.

A practical inverting op-amp circuit is drawn in Fig. 14.36. Using the same resistor values as in Fig. 14.35 with a practical op-amp unit, the μA741, the resulting output is −9.96 V, near the ideal value of −10 V. This slight difference from the ideal is due to the actual gain and input impedance of the μA741 op-amp unit. Fig. 14.36 shows dc voltages because the **Enable Bias Voltage Display** was set on. Notice the minus input is 69.26 μV for this op-amp circuit—slightly different from that using the op-amp model of Fig. 14.33.

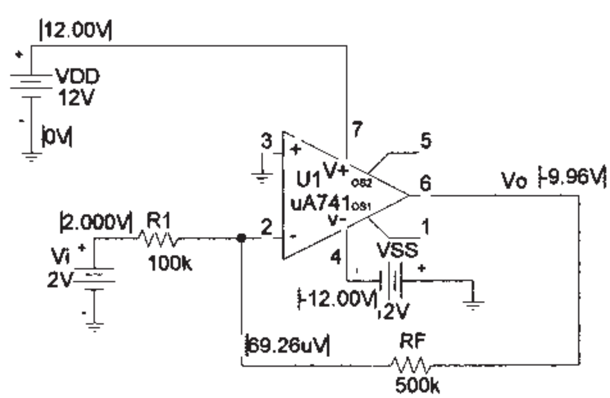


Figure 14.36 Practical inverting op-amp circuit.

An output listing from the analysis of Fig. 14.36 is shown in Fig. 14.37. Before the analysis is done, selecting **Analysis Setup, Transfer Function,** and then **Output** of **V(RF:2)** and **Input Source** of V_i will provide the small-signal characteristics in the output listing. The circuit gain is seen to be

```
Inverting op-amp circuit

****    SMALL-SIGNAL CHARACTERISTICS
    V(Vo)/V_Vi = -5.000E+00
    INPUT RESISTANCE AT V_Vi = 1.000E+05
    OUTPUT RESISTANCE AT V(Vo) = 4.950E-03
```

Figure 14.37 PSpice output for inverting op-amp (edited).

$$V_O/V_i = -5$$

Input resistance at $V_i = 1 \times 10^5$

Output resistance at $V_O = 4.95 \times 10^{-3}$

Program 14.2—Noninverting Op-Amp

Fig. 14.38 shows a noninverting op-amp circuit. The bias voltages are displayed on the figure. The theoretical gain of the amplifier circuit should be

$$A_v = (1 + RF/R1) = 1 + 500\text{ k}\Omega/100\text{ k}\Omega = 6$$

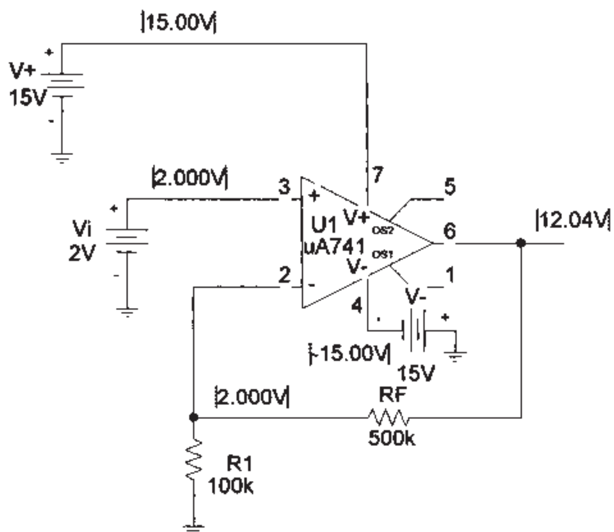


Figure 14.38 Design Center schematic for noninverting op-amp circuit.

For an input of 2 V, the resulting output will be

$$V_O = A_v V_i = 5(2\text{ V}) = 10\text{ V}$$

The output is noninverted from the input.

Program 14.3—Summing Op-Amp Circuit

A summing op-amp circuit such as that in Example 14.5 is shown in Fig. 14.39. Bias voltages also are displayed in Fig. 14.39, showing the resulting output at 3 V, as was

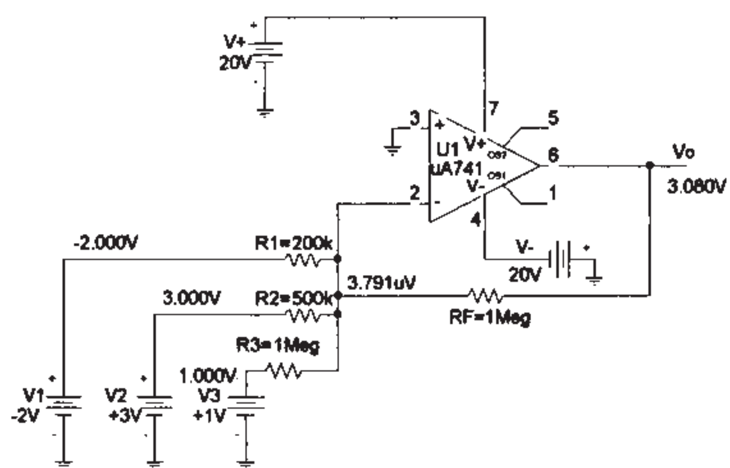


Figure 14.39 Summing amplifier for Program 14.3.

calculated in Example 14.5. Notice how well the virtual ground concept works with the minus input being only 3.791 μV.

Program 14.4—Unity-Gain Op-Amp Circuit

Figure 14.40 shows a unity-gain op-amp circuit with bias voltages displayed. For an input of +2 V, the output is exactly +2 V.

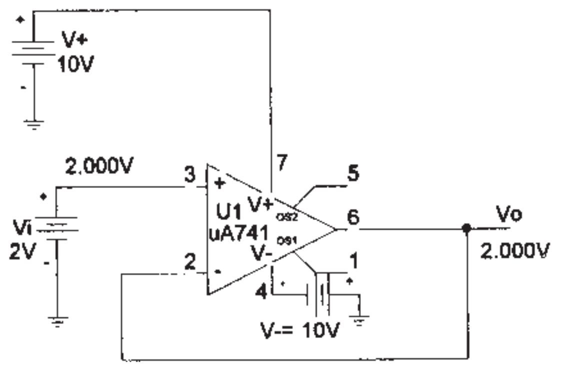


Figure 14.40 Unity-gain amplifier.

Program 14.5—Op-Amp Integrator Circuit

An op-amp integrator circuit is shown in Fig. 14.41. The input is selected as **VPULSE,** which is set to be a step input as follows:

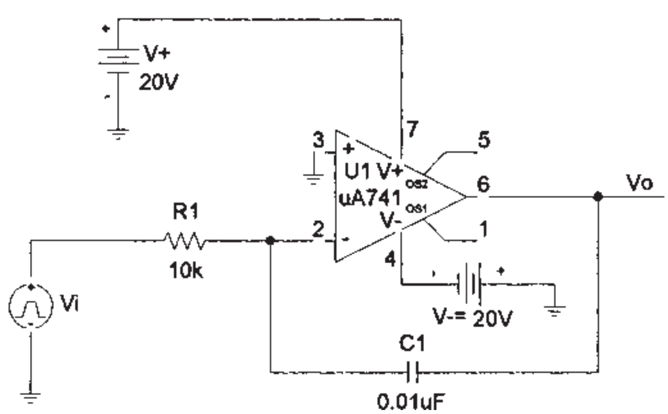


Figure 14.41 Op-amp integrator circuit.

Set **ac** = 0, **dc** = 0, **V1** = 0 V, **V2** = 2 V, **TD** = 0, **TR** = 0, **TF** = 0, **PW** = 10 ms, and **PER** = 20 ms. This provides a step from 0 to 2 V, with no time delay, rise time or fall time, having a period of 10 ms and repeating after a period of 20 ms. For this problem, the voltage rises instantly to 2 V, then stays there for a sufficiently long time for the output to drop as a ramp voltage from the maximum supply level of +20 V to the lowest level of −20 V. Theoretically, the output for the circuit of Fig. 14.41 is

$$v_O(t) = -1/RC \int v_i(t)\, dt$$

$$v_O(t) = -1/(10\text{ k}\Omega)(0.01\ \mu\text{F}) \int 2\, dt = -10{,}000 \int 2\, dt = -20{,}000t$$

This is a negative ramp voltage dropping at a rate (slope) of −20,000 V/s. This ramp voltage will drop from +20 V to −20 V in

$$40 \text{ V}/20{,}000 = 2 \times 10^{-3} = 2 \text{ ms}$$

Fig. 14.42 shows the input step waveform and the resulting output ramp waveform obtained using **PROBE.**

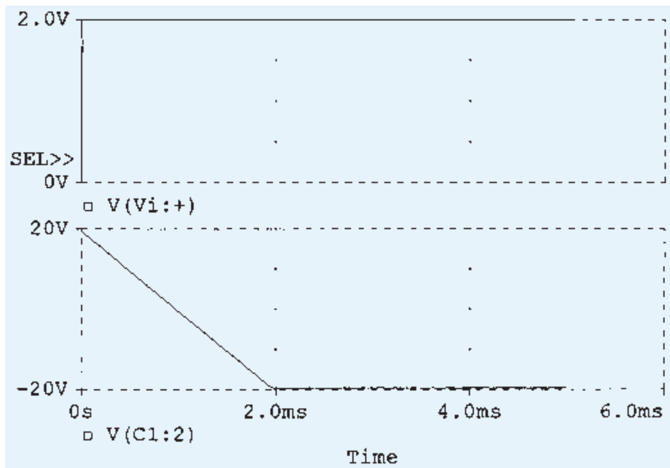


Figure 14.42 Probe waveform for integrator circuit.

Program 14.6—Multistage Op-Amp Circuit

A multistage op-amp circuit is shown in Fig. 14.43. The input to stage 1 of 200 mV provides an output of 200 mV to stages 2 and 3. Stage 2 is an inverting amplifier with

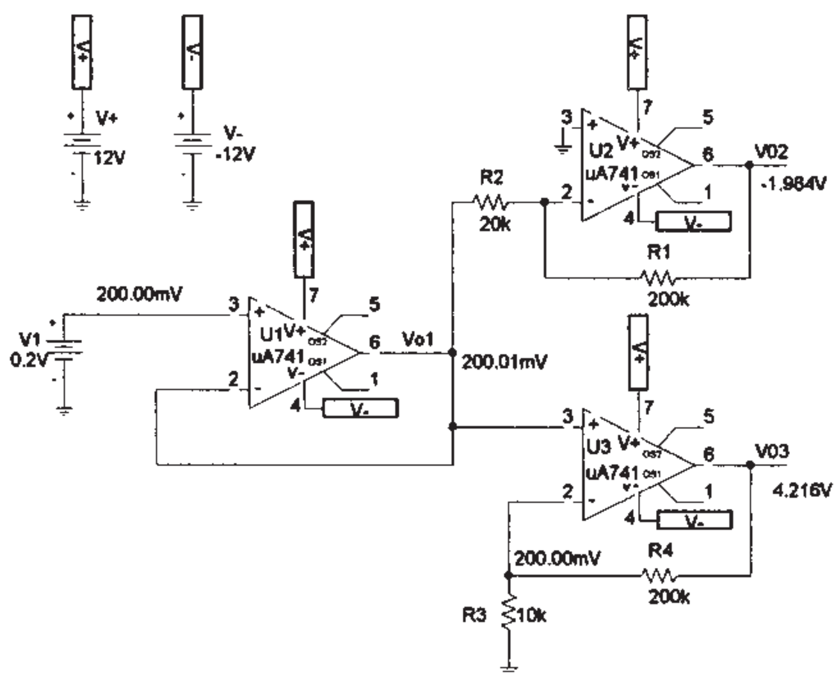


Figure 14.43 Multistage op-amp circuit.

gain -200 kΩ/20 kΩ $= -10$, with an output from stage 2 of $-10(200$ mV$) = -2$ V. State 3 is a non-inverting amplifier with gain of (1 + 200 kΩ/10 kΩ = 21), resulting in an output of 21(200 mV) = 4.2 V.

PROBLEMS

§ 14.2 Differential and Common-Mode Operation

1. Calculate the CMRR (in dB) for the circuit measurements of $V_d = 1$ mV, $V_o = 120$ mV, and $V_C = 1$ mV, $V_o = 20$ μV.

2. Determine the output voltage of an op-amp for input voltages of $V_{i_1} = 200$ μV and $V_{i_2} = 140$ μV. The amplifier has a differential gain of $A_d = 6000$ and the value of CMRR is:
(a) 200.
(b) 10^5.

§ 14.4 Practical Op-Amp Circuits

3. What is the output voltage in the circuit of Fig. 14.44?

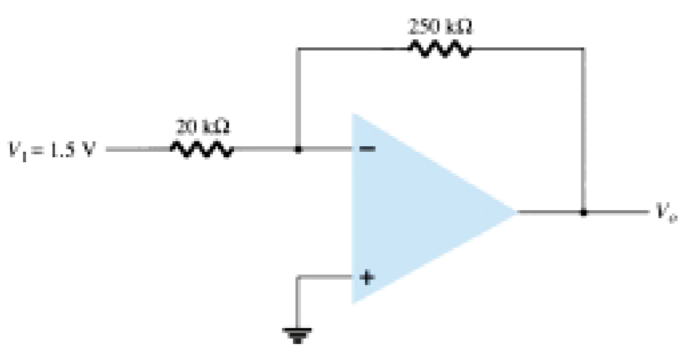


Figure 14.44 Problems 3 and 25

4. What is the range of the voltage-gain adjustment in the circuit of Fig. 14.45?

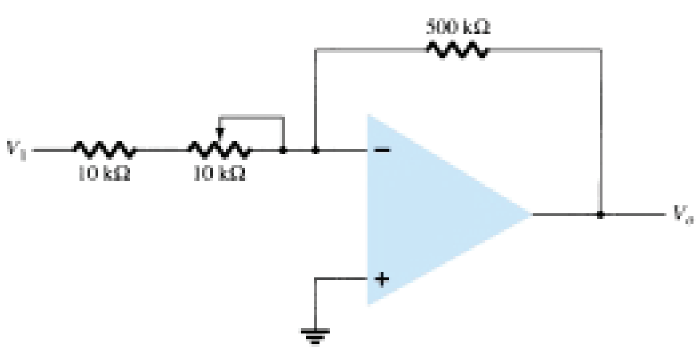


Figure 14.45 Problem 4

5. What input voltage results in an output of 2 V in the circuit of Fig. 14.46?

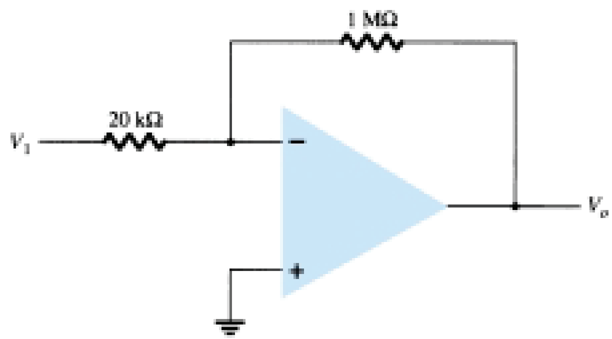


Figure 14.46 Problem 5

6. What is the range of the output voltage in the circuit of Fig. 14.47 if the input can vary from 0.1 to 0.5 V?
7. What output voltage results in the circuit of Fig. 14.48 for an input of $V_1 = -0.3$ V?

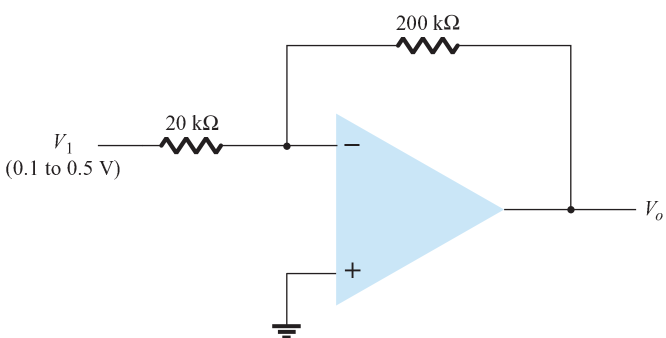


Figure 14.47 Problem 6

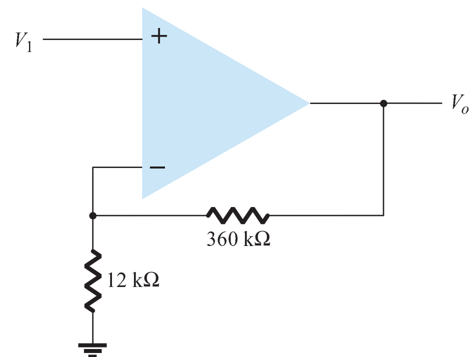


Figure 14.48 Problems 7, 8, and 26

8. What input must be applied to the input of Fig. 14.48 to result in an output of 2.4 V?
9. What range of output voltage is developed in the circuit of Fig. 14.49?
10. Calculate the output voltage developed by the circuit of Fig. 14.50 for $R_f = 330$ kΩ.
11. Calculate the output voltage of the circuit in Fig. 14.50 for $R_f = 68$ kΩ.

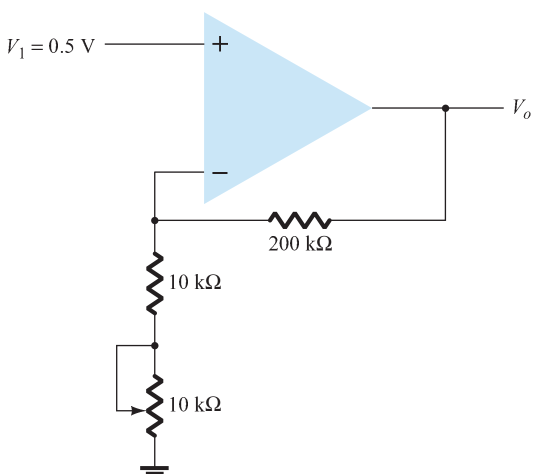


Figure 14.49 Problem 9

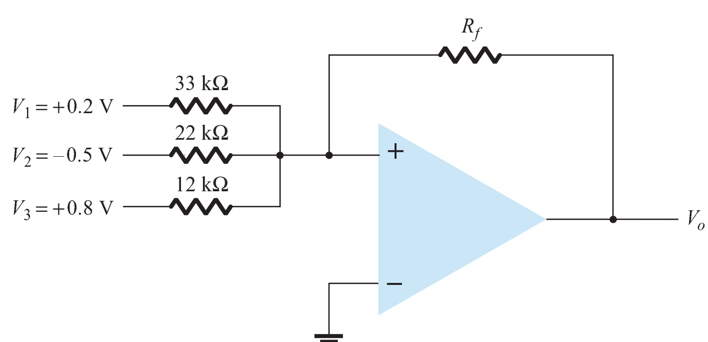


Figure 14.50 Problems 10, 11, and 27

12. Sketch the output waveform resulting in Fig. 14.51.

13. What output voltage results in the circuit of Fig. 14.52 for $V_1 = +0.5$ V?

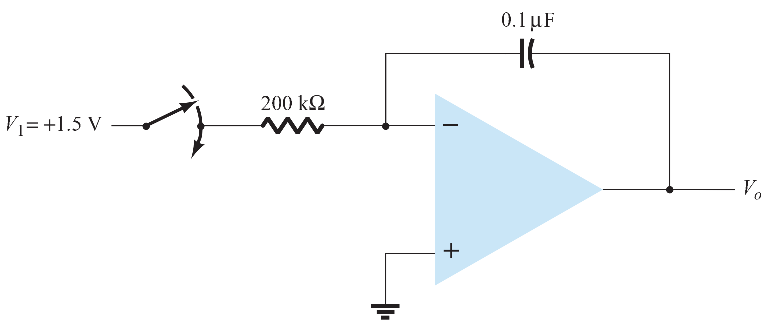


Figure 14.51 Problem 12

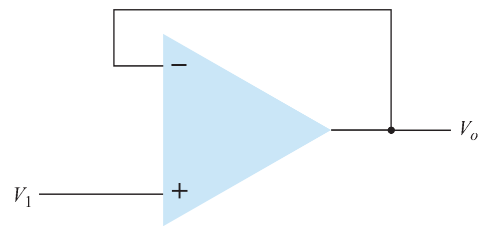


Figure 14.52 Problem 13

14. Calculate the output voltage for the circuit of Fig. 14.53.

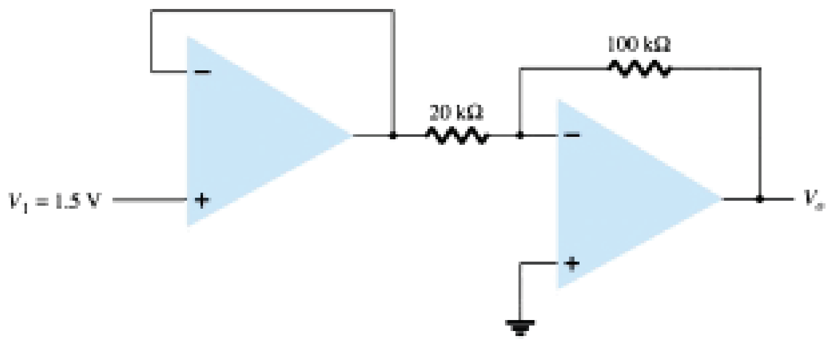


Figure 14.53 Problems 14 and 28

15. Calculate the output voltages V_2 and V_3 in the circuit of Fig. 14.54.

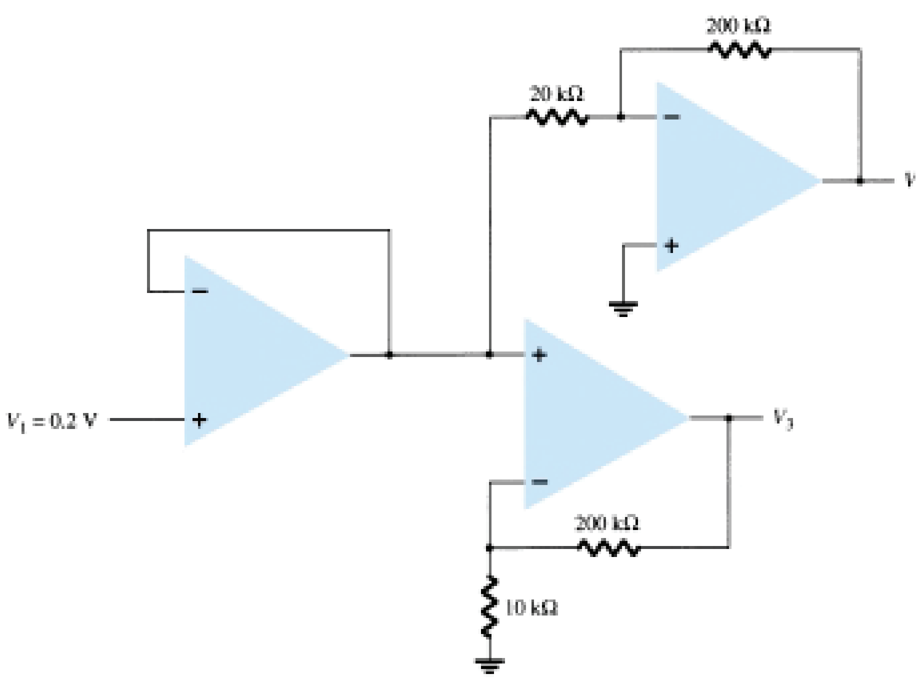


Figure 14.54 Problem 15

16. Calculate the output voltage, V_o, in the circuit of Fig. 14.55.

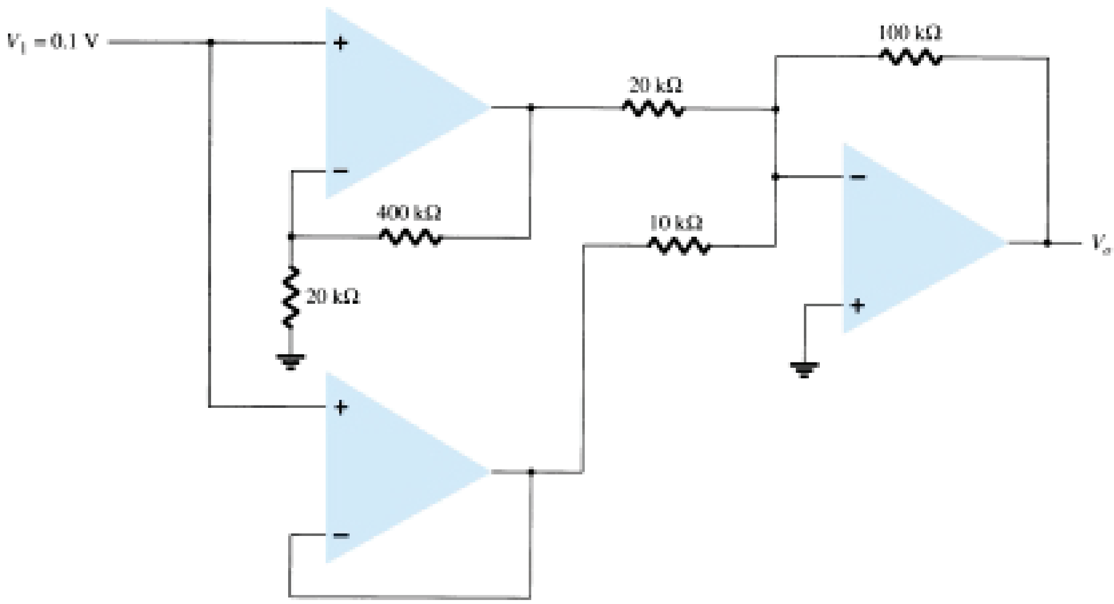


Figure 14.55 Problems 16 and 29

17. Calculate V_o in the circuit of Fig. 14.56.

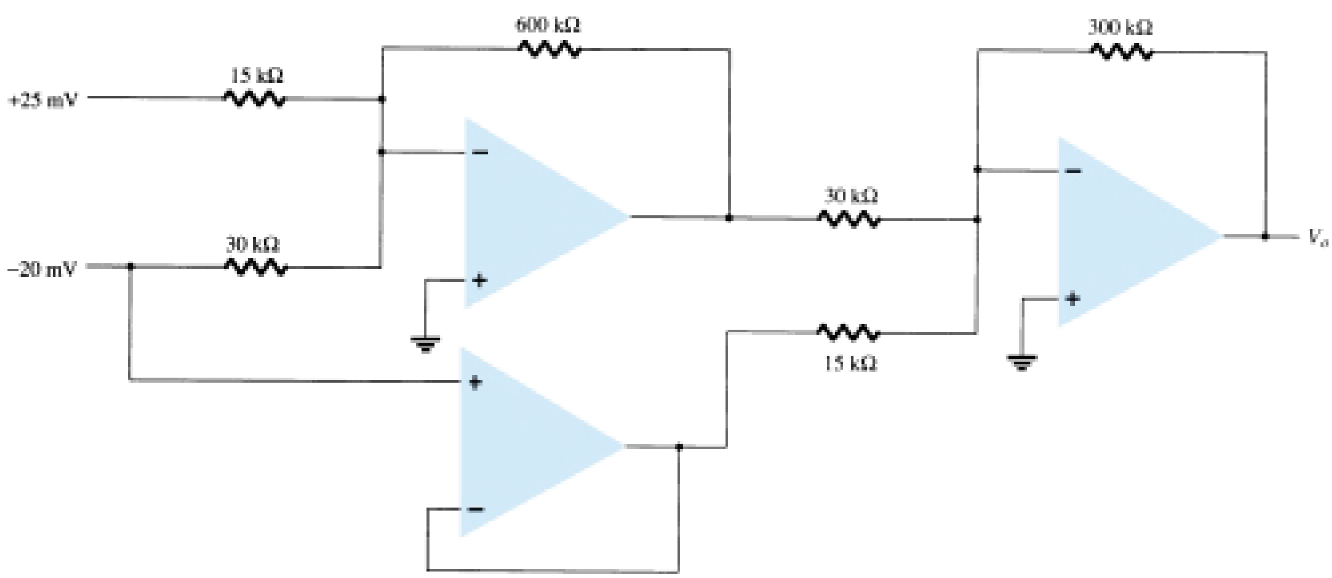


Figure 14.56 Problem 17

§ 14.5 Op-Amp Specifications—DC Offset Parameters

* **18.** Calculate the total offset voltage for the circuit of Fig. 14.57 for an op-amp with specified values of input offset voltage $V_{IO} = 6$ mV and input offset current $I_{IO} = 120$ nA.

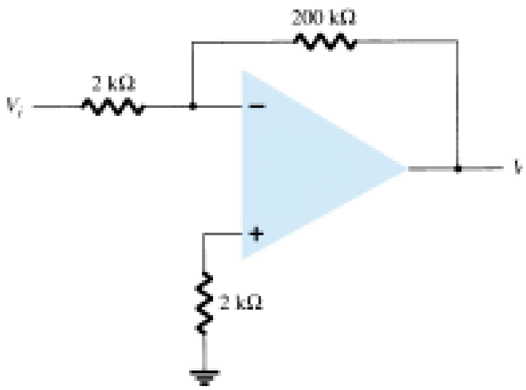


Figure 14.57 Problems 18, 22, 23, and 24

*19. Calculate the input bias current at each input of an op-amp having specified values of $I_{IO} = 4$ nA and $I_{IB} = 20$ nA.

§ 14.6 Op-Amp Specifications—Frequency Parameters

20. Determine the cutoff frequency of an op-amp having specified values $B_1 = 800$ kHz and $A_{VD} = 150$ V/mV.

*21. For an op-amp having a slew rate of SR = 2.4 V/μs, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.3 V in 10 μs?

*22. For an input of $V_1 = 50$ mV in the circuit of Fig. 14.57, determine the maximum frequency that may be used. The op-amp slew rate SR = 0.4 V/μs.

23. Using the specifications listed in Table 14.2, calculate the typical offset voltage for the circuit connection of Fig. 14.57.

*24. For the typical characteristics of the 741 op-amp, calculate the following values for the circuit of Fig. 14.57.
(a) A_{CL}.
(b) Z_i.
(c) Z_o.

§ 14.8 PSpice Windows

*25. Use Schematic Capture to draw a circuit to determine the output voltage in the circuit of Fig. 14.44.

*26. Use Schematic Capture to calculate the output voltage in the circuit of Fig. 14.48 for the input of $V_i = 0.5$ V.

*27. Use Schematic Capture to calculate the output voltage in the circuit of Fig. 14.50 for $R_f = 68$ kΩ.

*28. Use Schematic Capture to calculate the output voltage in the circuit of Fig. 14.53.

*29. Use Schematic Capture to calculate the output voltage in the circuit of Fig. 14.55.

*30. Use Schematic Capture to calculate the output voltage in the circuit of Fig. 14.56.

*31. Use Schematic Capture to obtain the output waveform for a 2 V step input to an integrator circuit, as shown in Fig. 14.20, with values of $R = 40$ kΩ and $C = 0.003$ μF.

*Please Note: Asterisks indicate more difficult problems.

CHAPTER

15 Op-Amp Applications

15.1 CONSTANT-GAIN MULTIPLIER

One of the most common op-amp circuits is the inverting constant-gain multiplier, which provides a precise gain or amplification. Figure 15.1 shows a standard circuit connection with the resulting gain being given by

$$A = -\frac{R_f}{R_1} \tag{15.1}$$

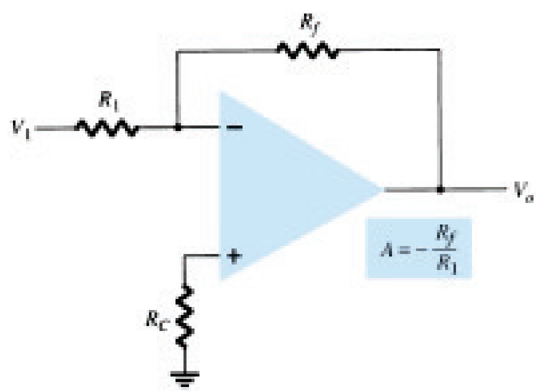


Figure 15.1 Fixed-gain amplifier.

EXAMPLE 15.1 Determine the output voltage for the circuit of Fig. 15.2 with a sinusoidal input of 2.5 mV.

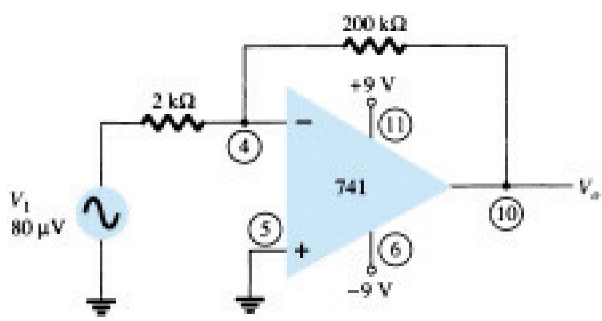


Figure 15.2 Circuit for Example 15.1.

Solution

The circuit of Fig. 15.2 uses a 741 op-amp to provide a constant or fixed gain, calculated from Eq. (15.1) to be

$$A = -\frac{R_f}{R_1} = -\frac{200\text{ k}\Omega}{2\text{ k}\Omega} = -100$$

The output voltage is then

$$V_o = AV_i = -100(2.5\text{ mV}) = -250\text{ mV} = \mathbf{-0.25\ V}$$

A noninverting constant-gain multiplier is provided by the circuit of Fig. 15.3, with the gain given by

$$\boxed{A = 1 + \frac{R_f}{R_1}} \qquad (15.2)$$

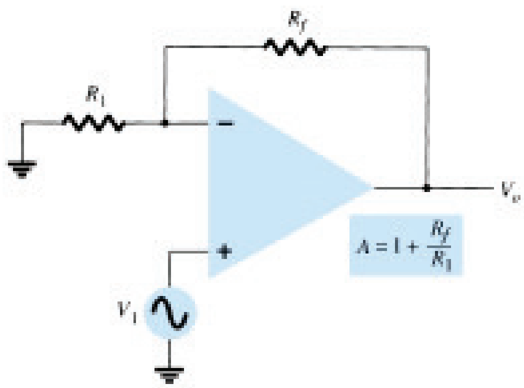


Figure 15.3 Noninverting fixed-gain amplifier.

EXAMPLE 15.2

Calculate the output voltage from the circuit of Fig. 15.4 for an input of 120 μV.

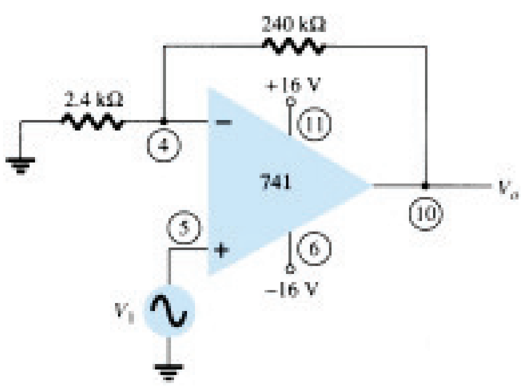


Figure 15.4 Circuit for Example 15.2.

Solution

The gain of the op-amp circuit is calculated using Eq. (15.2) to be

$$A = 1 + \frac{R_f}{R_1} = 1 + \frac{240\text{ k}\Omega}{2.4\text{ k}\Omega} = 1 + 100 = 101$$

The output voltage is then

$$V_o = AV_i = 101(120\ \mu\text{V}) = \mathbf{12.12\ mV}$$

Multiple-Stage Gains

When a number of stages are connected in series, the overall gain is the product of the individual stage gains. Figure 15.5 shows a connection of three stages. The first stage is connected to provide noninverting gain as given by Eq. (15.2). The next two stages provide an inverting gain given by Eq. (15.1). The overall circuit gain is then noninverting and calculated by

$$A = A_1 A_2 A_3$$

where $A_1 = 1 + R_f/R_1$, $A_2 = -R_f/R_2$, and $A_3 = -R_f/R_3$.

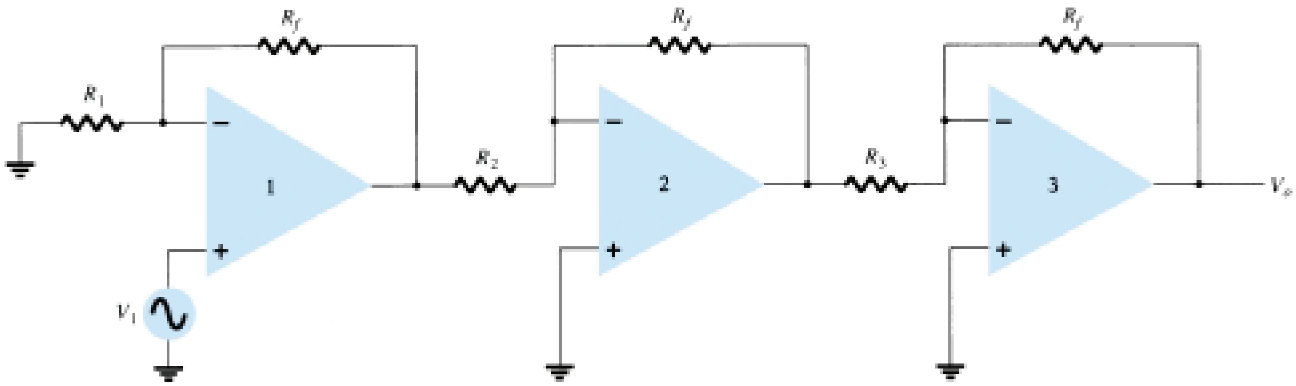


Figure 15.5 Constant-gain connection with multiple stages.

EXAMPLE 15.3

Calculate the output voltage using the circuit of Fig. 15.5 for resistor components of value $R_f = 470$ kΩ, $R_1 = 4.3$ kΩ, $R_2 = 33$ kΩ, and $R_3 = 33$ kΩ for an input of 80 μV.

Solution

The amplifier gain is calculated to be

$$A = A_1 A_2 A_3 = \left(1 + \frac{R_f}{R_1}\right)\left(-\frac{R_f}{R_2}\right)\left(-\frac{R_f}{R_3}\right)$$

$$= \left(1 + \frac{470\text{ k}\Omega}{4.3\text{ k}\Omega}\right)\left(-\frac{470\text{ k}\Omega}{33\text{ k}\Omega}\right)\left(-\frac{470\text{ k}\Omega}{33\text{ k}\Omega}\right)$$

$$= (110.3)(-14.2)(-14.2) = 22.2 \times 10^3$$

so that

$$V_o = AV_i = 22.2 \times 10^3(80\ \mu\text{V}) = \mathbf{1.78\ V}$$

EXAMPLE 15.4

Show the connection of an LM124 quad op-amp as a three-stage amplifier with gains of +10, −18, and −27. Use a 270-kΩ feedback resistor for all three circuits. What output voltage will result for an input of 150 μV?

Solution

For the gain of +10:

$$A_1 = 1 + \frac{R_f}{R_1} = +10$$

$$\frac{R_f}{R_1} = 10 - 1 = 9$$

$$R_1 = \frac{R_f}{9} = \frac{270\ \text{k}\Omega}{9} = 30\ \text{k}\Omega$$

For the gain of −18:

$$A_2 = -\frac{R_f}{R_2} = -18$$

$$R_2 = \frac{R_f}{18} = \frac{270\ \text{k}\Omega}{18} = 15\ \text{k}\Omega$$

For the gain of −27:

$$A_3 = -\frac{R_f}{R_3} = -27$$

$$R_3 = \frac{R_f}{27} = \frac{270\ \text{k}\Omega}{27} = 10\ \text{k}\Omega$$

The circuit showing the pin connections and all components used is in Fig. 15.6. For an input of $V_1 = 150\ \mu\text{V}$, the output voltage will be

$$V_o = A_1 A_2 A_3 V_1 = (10)(-18)(-27)(150\ \mu\text{V}) = 4860(150\ \mu\text{V})$$
$$= \mathbf{0.729\ V}$$

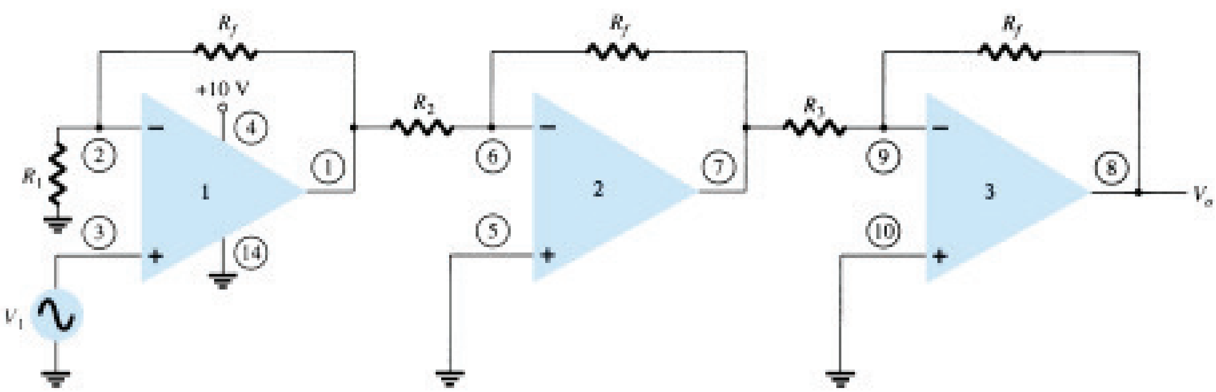


Figure 15.6 Circuit for Example 15.4 (using LM124).

A number of op-amp stages could also be used to provide separate gains, as demonstrated in the next example.

EXAMPLE 15.5

Show the connection of three op-amp stages using an LM348 IC to provide outputs that are 10, 20, and 50 times larger than the input. Use a feedback resistor of $R_f =$ 500 kΩ in all stages.

Solution

The resistor component for each stage is calculated to be

$$R_1 = -\frac{R_f}{A_2} = -\frac{500\ \text{k}\Omega}{-10} = 50\ \text{k}\Omega$$

$$R_2 = -\frac{R_f}{A_2} = -\frac{500\ \text{k}\Omega}{-20} = 25\ \text{k}\Omega$$

$$R_3 = -\frac{R_f}{A_3} = -\frac{500\ \text{k}\Omega}{-50} = 10\ \text{k}\Omega$$

The resulting circuit is drawn in Fig. 15.7.

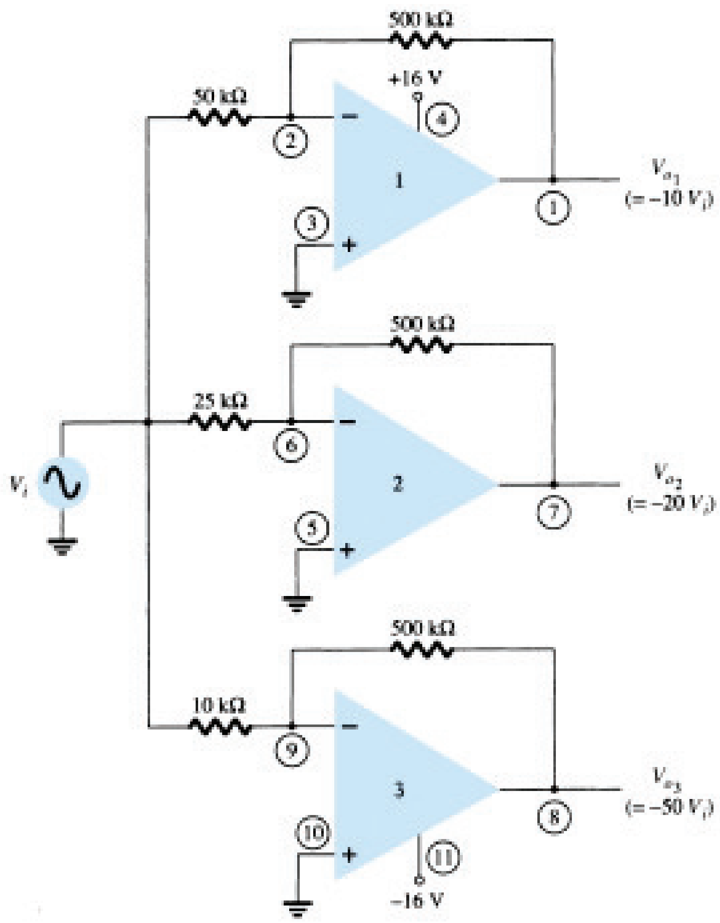


Figure 15.7 Circuit for Example 15.5 (using LM348).

15.2 VOLTAGE SUMMING

Another popular use of an op-amp is as a summing amplifier. Figure 15.8 shows the connection with the output being the sum of the three inputs, each multiplied by a different gain. The output voltage is

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right) \tag{15.3}$$

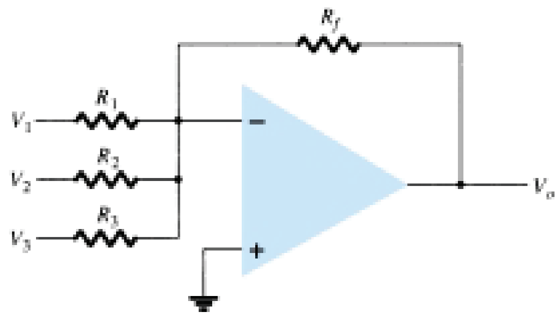


Figure 15.8 Summing amplifier.

Calculate the output voltage for the circuit of Fig. 15.9. The inputs are $V_1 = 50$ mV sin(1000t) and $V_2 = 10$ mV sin(3000t).

EXAMPLE 15.6

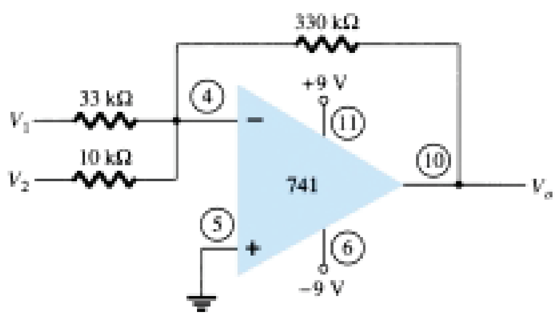


Figure 15.9 Circuit for Example 15.6.

Solution

The output voltage is

$$V_o = -\left(\frac{330\text{ k}\Omega}{33\text{ k}\Omega} V_1 + \frac{330\text{ k}\Omega}{10\text{ k}\Omega} V_2\right) = -(10V_1 + 33V_2)$$

$$= -[10(50\text{ mV})\sin(1000t) + 33(10\text{ mV})\sin(3000t)]$$

$$= \mathbf{-[0.5\sin(1000t) + 0.33\sin(3000t)]}$$

Voltage Subtraction

Two signals can be subtracted, one from the other, in a number of ways. Figure 15.10 shows two op-amp stages used to provide subtraction of input signals. The resulting output is given by

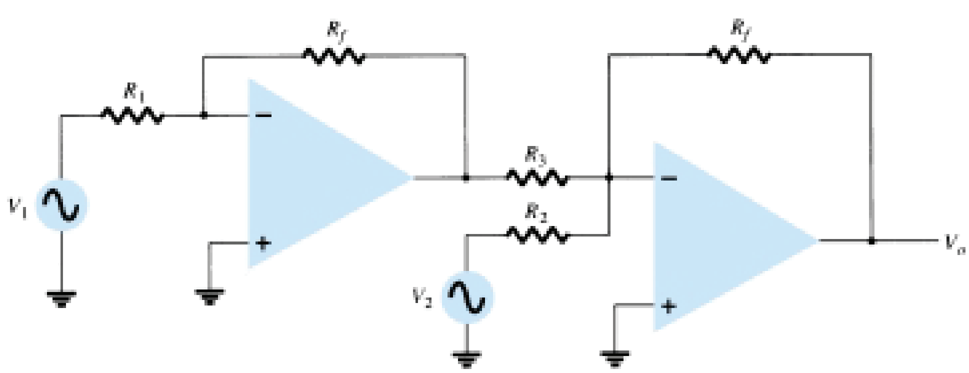


Figure 15.10 Circuit to subtract two signals.

$$V_o = -\left[\frac{R_f}{R_3}\left(-\frac{R_f}{R_1}V_1\right) + \frac{R_f}{R_2}V_2\right]$$

$$\boxed{V_o = -\left(\frac{R_f}{R_2}V_2 - \frac{R_f}{R_3}\frac{R_f}{R_1}V_1\right)} \tag{15.4}$$

EXAMPLE 15.7

Determine the output for the circuit of Fig. 15.10 with components $R_f = 1\ \text{M}\Omega$, $R_1 = 100\ \text{k}\Omega$, $R_2 = 50\ \text{k}\Omega$, and $R_3 = 500\ \text{k}\Omega$.

Solution

The output voltage is calculated to be

$$V_o = -\left(\frac{1\ \text{M}\Omega}{50\ \text{k}\Omega}V_2 - \frac{1\ \text{M}\Omega}{500\ \text{k}\Omega}\,\frac{1\ \text{M}\Omega}{100\ \text{k}\Omega}V_1\right) = -(20V_2 - 20V_1) = \mathbf{-20(V_2 - V_1)}$$

The output is seen to be the difference of V_2 and V_1 multiplied by a gain factor of -20.

Another connection to provide subtraction of two signals is shown in Fig. 15.11. This connection uses only one op-amp stage to provide subtracting two input signals. Using superposition the output can be shown to be

$$\boxed{V_o = \frac{R_3}{R_1 + R_3}\,\frac{R_2 + R_4}{R_2}V_1 - \frac{R_4}{R_2}V_2} \tag{15.5}$$

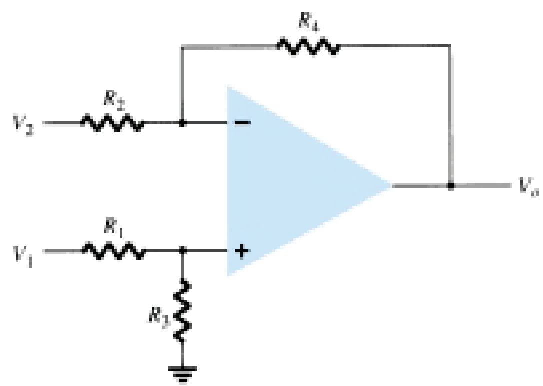


Figure 15.11 Subtraction circuit.

EXAMPLE 15.8

Determine the output voltage for the circuit of Fig. 15.12.

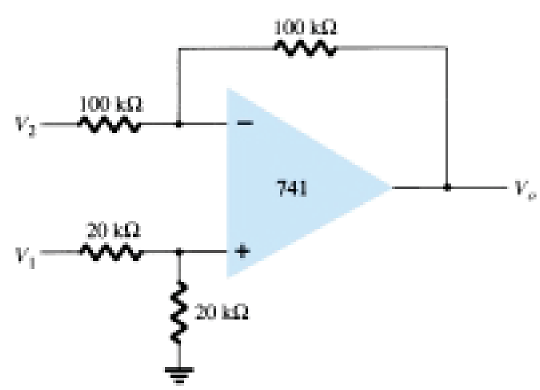


Figure 15.12 Circuit for Example 15.8.

Solution

The resulting output voltage can be expressed as

$$V_o = \left(\frac{20\ \text{k}\Omega}{20\ \text{k}\Omega + 20\ \text{k}\Omega}\right)\left(\frac{100\ \text{k}\Omega + 100\ \text{k}\Omega}{100\ \text{k}\Omega}\right) V_1 - \frac{100\ \text{k}\Omega}{100\ \text{k}\Omega} V_2$$

$$= \boldsymbol{V_1 - V_2}$$

The resulting output voltage is seen to be the difference of the two input voltages.

15.3 VOLTAGE BUFFER

A voltage buffer circuit provides a means of isolating an input signal from a load by using a stage having unity voltage gain, with no phase or polarity inversion, and acting as an ideal circuit with very high input impedance and low output impedance. Figure 15.13 shows an op-amp connected to provide this buffer amplifier operation. The output voltage is determined by

$$\boxed{V_o = V_1} \tag{15.6}$$

Figure 15.14 shows how an input signal can be provided to two separate outputs. The advantage of this connection is that the load connected across one output has no (or little) effect on the other output. In effect, the outputs are buffered or isolated from each other.

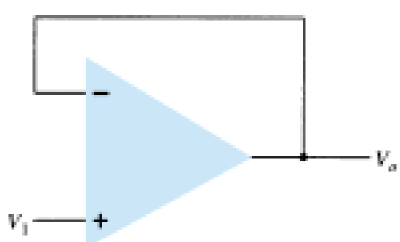


Figure 15.13 Unity-gain (buffer) amplifier.

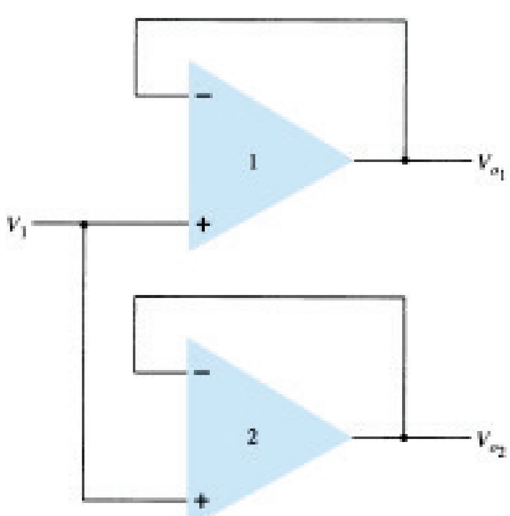


Figure 15.14 Use of buffer amplifier to provide output signals.

EXAMPLE 15.9

Show the connection of a 741 as a unity-gain circuit.

Solution

The connection is shown in Fig. 15.15.

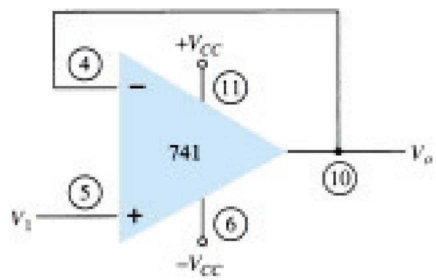


Figure 15.15 Connection for Example 15.9.

15.4 CONTROLLED SOURCES

Operational amplifiers can be used to form various types of controlled sources. An input voltage can be used to control an output voltage or current, or an input current can be used to control an output voltage or current. These types of connections are suitable for use in various instrumentation circuits. A form of each type of controlled source is provided next.

Voltage-Controlled Voltage Source

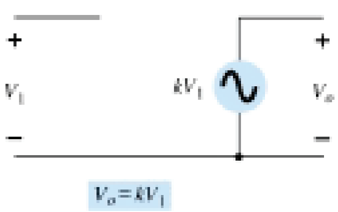


Figure 15.16 Ideal voltage-controlled voltage source.

An ideal form of a voltage source whose output V_o is controlled by an input voltage V_1 is shown in Fig. 15.16. The output voltage is seen to be dependent on the input voltage (times a scale factor k). This type of circuit can be built using an op-amp as shown in Fig. 15.17. Two versions of the circuit are shown, one using the inverting input, the other the noninverting input. For the connection of Fig. 15.17a, the output voltage is

$$V_o = -\frac{R_f}{R_1} V_1 = kV_1 \tag{15.7}$$

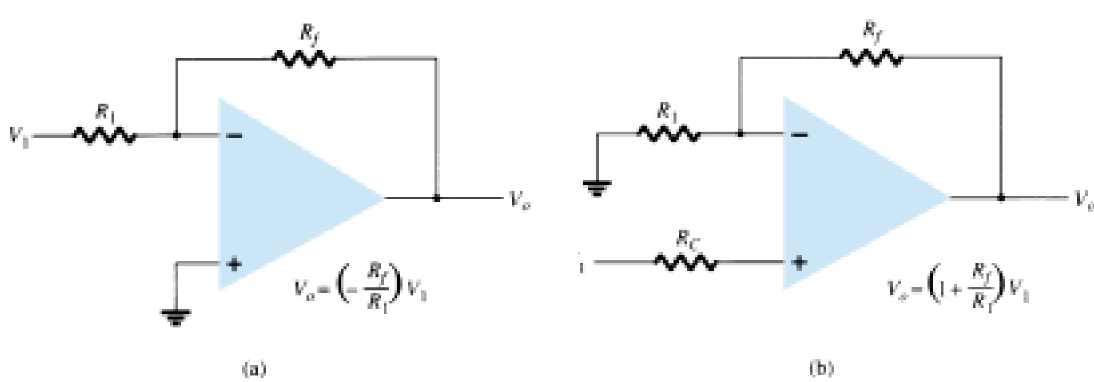


Figure 15.17 Practical voltage-controlled voltage source circuits.

while that of Fig. 15.17b results in

$$V_o = \left(1 + \frac{R_f}{R_1}\right)V_1 = kV_1 \tag{15.8}$$

Voltage-Controlled Current Source

An ideal form of circuit providing an output current controlled by an input voltage is that of Fig. 15.18. The output current is dependent on the input voltage. A practical circuit can be built, as in Fig. 15.19, with the output current through load resistor R_L controlled by the input voltage V_1. The current through load resistor R_L can be seen to be

$$I_o = \frac{V_1}{R_1} = kV_1 \tag{15.9}$$

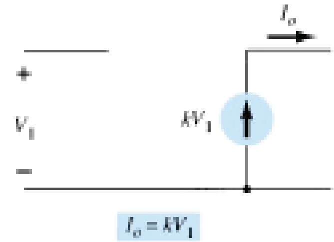


Figure 15.18 Ideal voltage-controlled current source.

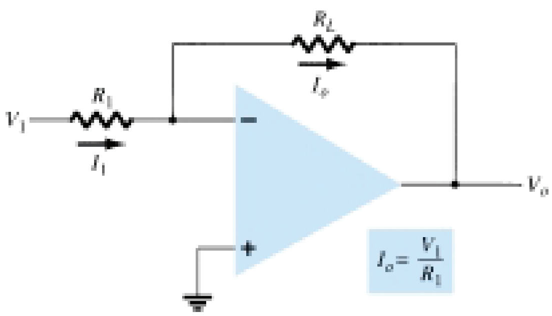


Figure 15.19 Practical voltage-controlled current source.

Current-Controlled Voltage Source

An ideal form of a voltage source controlled by an input current is shown in Fig. 15.20. The output voltage is dependent on the input current. A practical form of the circuit is built using an op-amp as shown in Fig. 15.21. The output voltage is seen to be

$$V_o = -I_1R_L = kI_1 \tag{15.10}$$

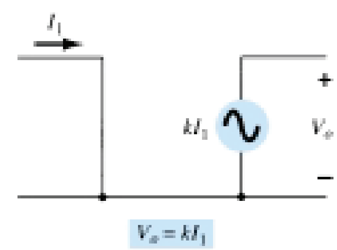


Figure 15.20 Ideal current-controlled voltage source.

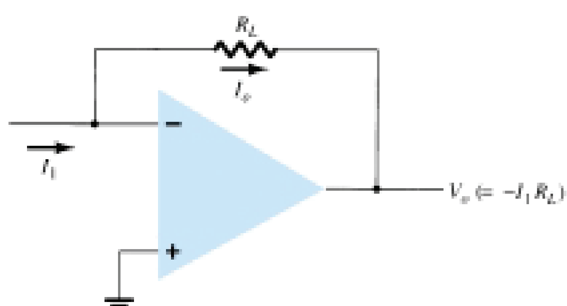


Figure 15.21 Practical form of current-controlled voltage source.

Current-Controlled Current Source

An ideal form of a circuit providing an output current dependent on an input current is shown in Fig. 15.22. In this type of circuit, an output current is provided dependent on the input current. A practical form of the circuit is shown in Fig. 15.23. The input current I_1 can be shown to result in the output current I_o so that

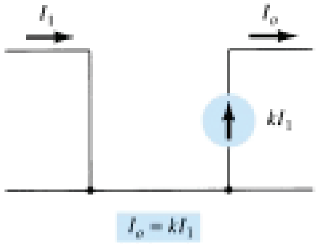


Figure 15.22 Ideal current-controlled current source.

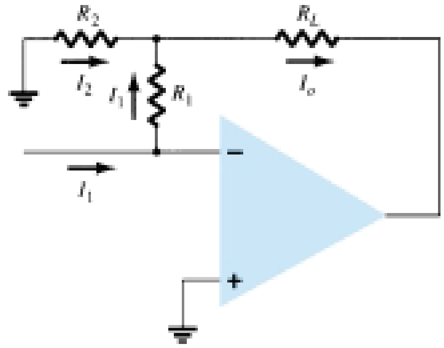


Figure 15.23 Practical form of current-controlled current source.

$$I_o = I_1 + I_2 = I_1 + \frac{I_1 R_1}{R_2} = \left(1 + \frac{R_1}{R_2}\right) I_1 = kI_1 \tag{15.11}$$

EXAMPLE 15.10

(a) For the circuit of Fig. 15.24a, calculate I_L.

(b) For the circuit of Fig. 15.24b, calculate V_o.

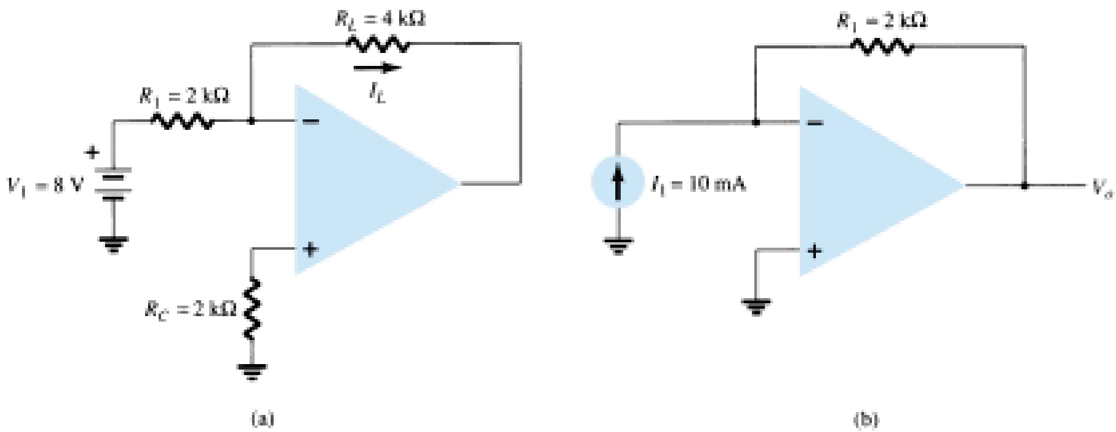


Figure 15.24 Circuits for Example 15.10.

Solution

(a) For the circuit of Fig. 15.24a,

$$I_L = \frac{V_1}{R_1} = \frac{8\ \text{V}}{2\ \text{k}\Omega} = \mathbf{4\ mA}$$

(b) For the circuit of Fig. 15.24b,

$$V_o = -I_1 R_1 = -(10\ \text{mA})(2\ \text{k}\Omega) = \mathbf{-20\ V}$$

15.5 INSTRUMENTATION CIRCUITS

A popular area of op-amp application is in instrumentation circuits such as dc or ac voltmeters. A few typical circuits will demonstrate how op-amps can be used.

DC Millivoltmeter

Figure 15.25 shows a 741 op-amp used as the basic amplifier in a dc millivoltmeter. The amplifier provides a meter with high input impedance and scale factors dependent only on resistor value and accuracy. Notice that the meter reading represents millivolts of signal at the circuit input. An analysis of the op-amp circuit provides the circuit transfer function

$$\left|\frac{I_o}{V_1}\right| = \frac{R_f}{R_1}\left(\frac{1}{R_S}\right) = \left(\frac{100\text{ k}\Omega}{100\text{ k}\Omega}\right)\left(\frac{1}{10\ \Omega}\right) = \frac{1\text{ mA}}{10\text{ mV}}$$

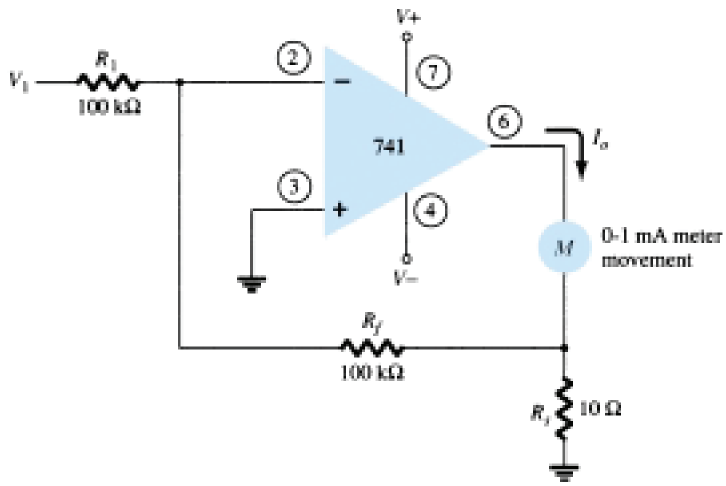


Figure 15.25 Op-amp dc millivoltmeter.

Thus, an input of 10 mV will result in a current through the meter of 1 mA. If the input is 5 mV, the current through the meter will be 0.5 mA, which is half-scale deflection. Changing R_f to 200 kΩ, for example, would result in a circuit scale factor of

$$\left|\frac{I_o}{V_1}\right| = \left(\frac{200\text{ k}\Omega}{100\text{ k}\Omega}\right)\left(\frac{1}{10\ \Omega}\right) = \frac{1\text{ mA}}{5\text{ mV}}$$

showing that the meter now reads 5 mV, full scale. It should be kept in mind that building such a millivoltmeter requires purchasing an op-amp, a few resistors, diodes, capacitors, and a meter movement.

AC Millivoltmeter

Another example of an instrumentation circuit is the ac millivoltmeter shown in Fig. 15.26. The circuit transfer function is

$$\left|\frac{I_o}{V_1}\right| = \frac{R_f}{R_1}\left(\frac{1}{R_S}\right) = \left(\frac{100\text{ k}\Omega}{100\text{ k}\Omega}\right)\left(\frac{1}{10\ \Omega}\right) = \frac{1\text{ mA}}{10\text{ mV}}$$

which appears the same as the dc millivoltmeter, except that in this case the signal handled is an ac signal. The meter indication provides a full-scale deflection for an ac input voltage of 10 mV, while an ac input of 5 mV will result in half-scale deflection with the meter reading interpreted in millivolt units.

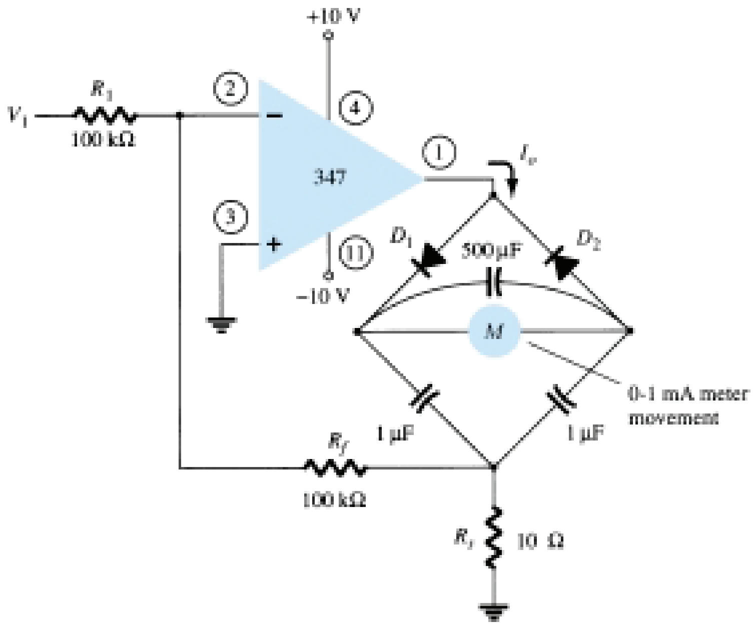


Figure 15.26 Ac millivoltmeter using op-amp.

Display Driver

Figure 15.27 shows op-amp circuits that can be used to drive a lamp display or LED display. When the noninverting input to the circuit in Fig. 15.27a goes above the inverting input, the output at terminal 1 goes to the positive saturation level (near +5 V in this example) and the lamp is driven on when transistor Q_1 conducts. As shown in the circuit, the output of the op-amp provides 30 mA of current to the base of transistor Q_1, which then drives 600 mA through a suitably selected transistor (with $\beta > 20$) capable of handling that amount of current. Figure 15.27b shows an op-amp circuit that can supply 20 mA to drive an LED display when the noninverting input goes positive compared to the inverting input.

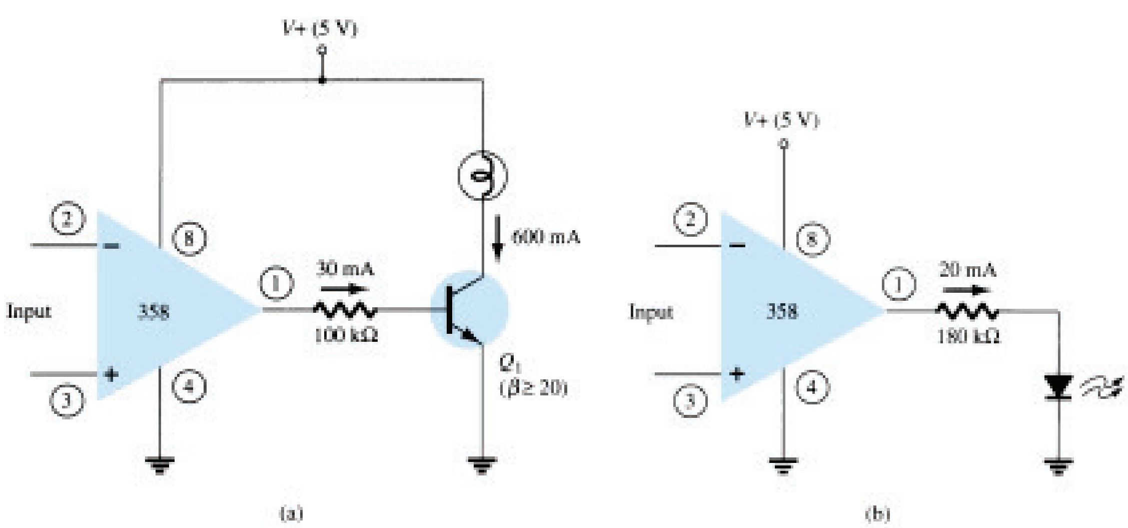


Figure 15.27 Display driver circuits: (a) lamp driver; (b) LED driver.

Instrumentation Amplifier

A circuit providing an output based on the difference between two inputs (times a scale factor) is shown in Fig. 15.28. A potentiometer is provided to permit adjusting the scale factor of the circuit. While three op-amps are used, a single-quad op-amp IC is all that is necessary (other than the resistor components). The output voltage can be shown to be

$$\frac{V_o}{V_1 - V_2} = 1 + \frac{2R}{R_P}$$

so that the output can be obtained from

$$V_o = \left(1 + \frac{2R}{R_P}\right)(V_1 - V_2) = k(V_1 - V_2) \qquad (15.12)$$

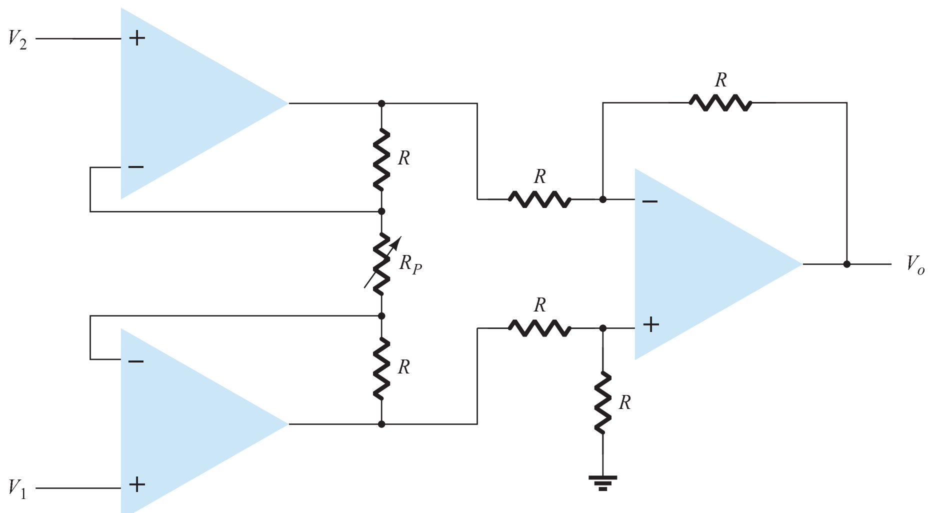


Figure 15.28 Instrumentation amplifier.

EXAMPLE 15.11

Calculate the output voltage expression for the circuit of Fig. 15.29.

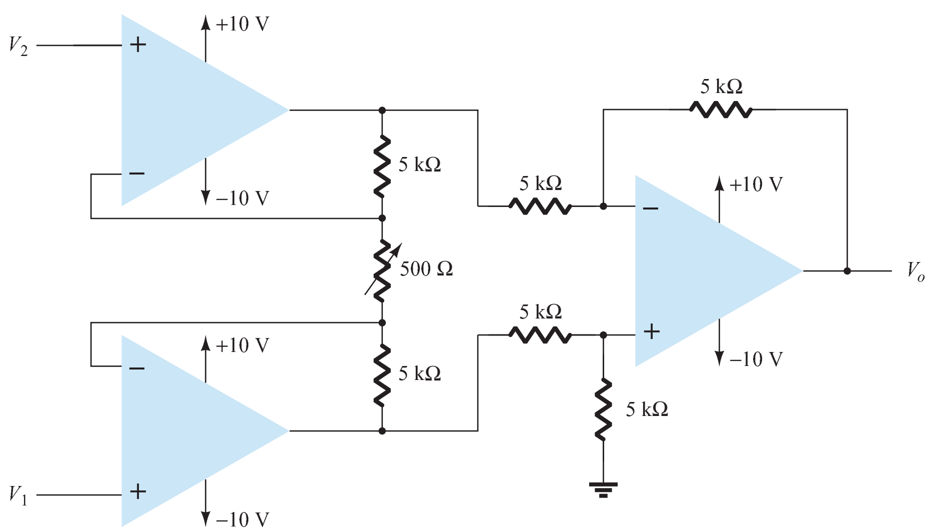


Figure 15.29 Circuit for Example 15.11.

Solution

The output voltage can then be expressed using Eq. (15.12) as

$$V_o = \left(1 + \frac{2R}{R_P}\right)(V_1 - V_2) = \left[1 + \frac{2(5000)}{500}\right](V_1 - V_2)$$
$$= \mathbf{21(V_1 - V_2)}$$

15.6 ACTIVE FILTERS

A popular application uses op-amps to build active filter circuits. A filter circuit can be constructed using passive components: resistors and capacitors. An active filter additionally uses an amplifier to provide voltage amplification and signal isolation or buffering.

A filter that provides a constant output from dc up to a cutoff frequency f_{OH} and then passes no signal above that frequency is called an ideal low-pass filter. The ideal response of a low-pass filter is shown in Fig. 15.30a. A filter that provides or passes signals above a cutoff frequency f_{OL} is a high-pass filter, as idealized in Fig. 15.30b. When the filter circuit passes signals that are above one ideal cutoff frequency and below a second cutoff frequency, it is called a bandpass filter, as idealized in Fig. 15.30c.

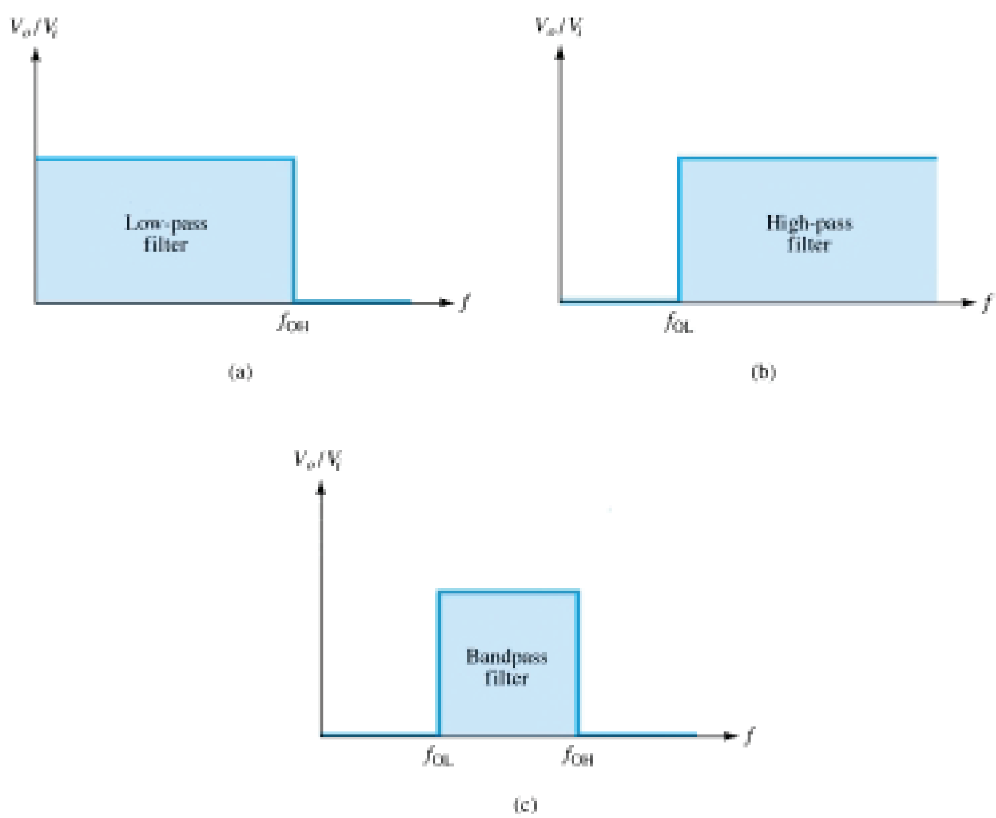


Figure 15.30 Ideal filter response: (a) low-pass; (b) high-pass; (c) bandpass.

Low-Pass Filter

A first-order, low-pass filter using a single resistor and capacitor as in Fig. 15.31a has a practical slope of −20 dB per decade, as shown in Fig. 15.31b (rather than the ideal response of Fig. 15.30a). The voltage gain below the cutoff frequency is constant at

$$A_v = 1 + \frac{R_f}{R_1} \tag{15.13}$$

at a cutoff frequency of

$$f_{OH} = \frac{1}{2\pi R_1 C_1} \tag{15.14}$$

Connecting two sections of filter as in Fig. 15.32 results in a second-order low-pass filter with cutoff at −40 dB per decade—closer to the ideal characteristic of Fig.

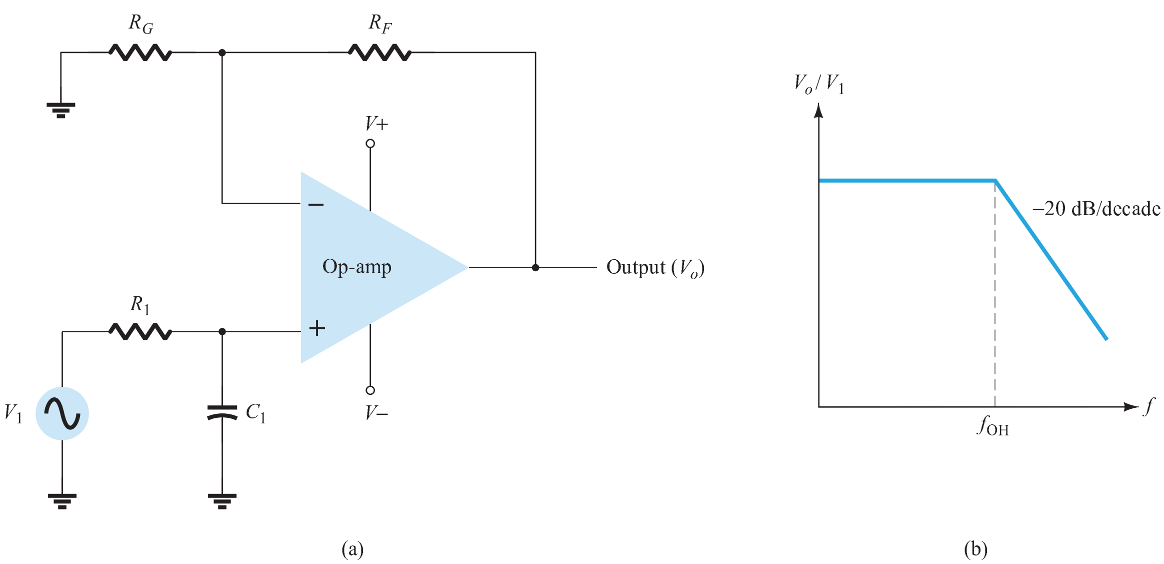


Figure 15.31 First-order low-pass active filter.

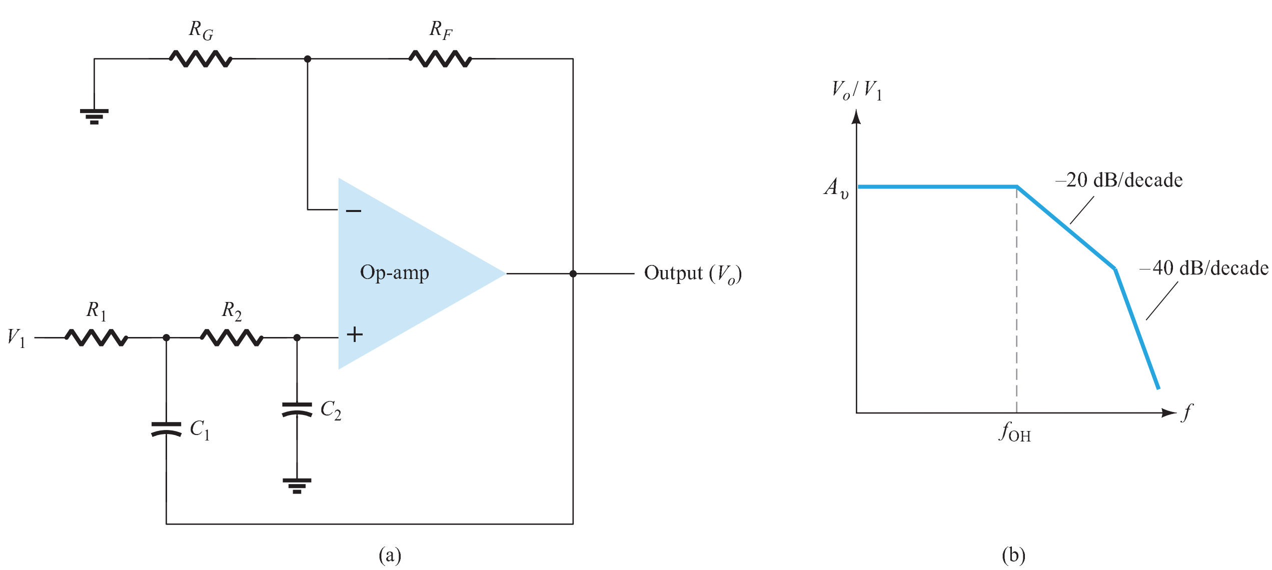


Figure 15.32 Second-order low-pass active filter.

15.30a. The circuit voltage gain and cutoff frequency are the same for the second-order circuit as for the first-order filter circuit, except that the filter response drops at a faster rate for a second-order filter circuit.

EXAMPLE 15.12 Calculate the cutoff frequency of a first-order low-pass filter for $R_1 = 1.2\ \text{k}\Omega$ and $C_1 = 0.02\ \mu\text{F}$.

Solution

$$f_{\text{OH}} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(1.2 \times 10^3)(0.02 \times 10^{-6})} = \mathbf{6.63\ kHz}$$

High-Pass Active Filter

First- and second-order high-pass active filters can be built as shown in Fig. 15.33. The amplifier gain is calculated using Eq. (15.13). The amplifier cutoff frequency is

$$f_{\text{OL}} = \frac{1}{2\pi R_1 C_1} \tag{15.15}$$

with a second-order filter $R_1 = R_2$, and $C_1 = C_2$ results in the same cutoff frequency as in Eq. (15.15).

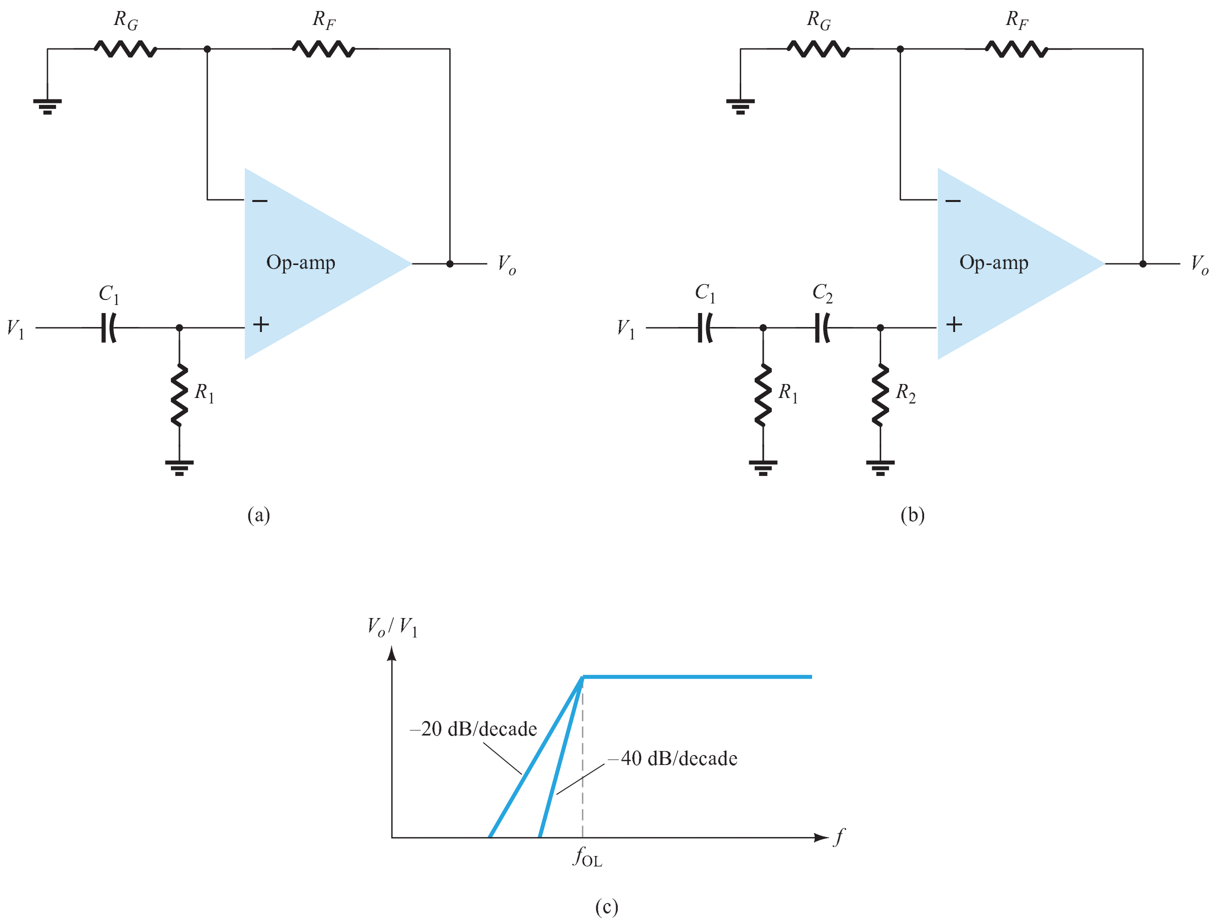


Figure 15.33 High-pass filter: (a) first order; (b) second order; (c) response plot.

Calculate the cutoff frequency of a second-order high-pass filter as in Fig. 15.33b for R1 5 R2 5 2.1 kV, C1 5 C2 5 0.05 mF, and Ro1 5 10 kV, Rof 5 50 kV.

EXAMPLE 15.13

Solution

$$\text{Eq. (15.13):}\quad A_v = 1 + \frac{R_{of}}{R_{o1}} = 1 + \frac{50\text{ k}\Omega}{10\text{ k}\Omega} = 6$$

The cutoff frequency is then

$$\text{Eq. (15.15):}\quad f_{\text{OL}} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(2.1 \times 10^3)(0.05 \times 10^{-6})} \approx \mathbf{1.5\text{ kHz}}$$

Bandpass Filter

Figure 15.34 shows a bandpass filter using two stages, the first a high-pass filter and the second a low-pass filter, the combined operation being the desired bandpass response.

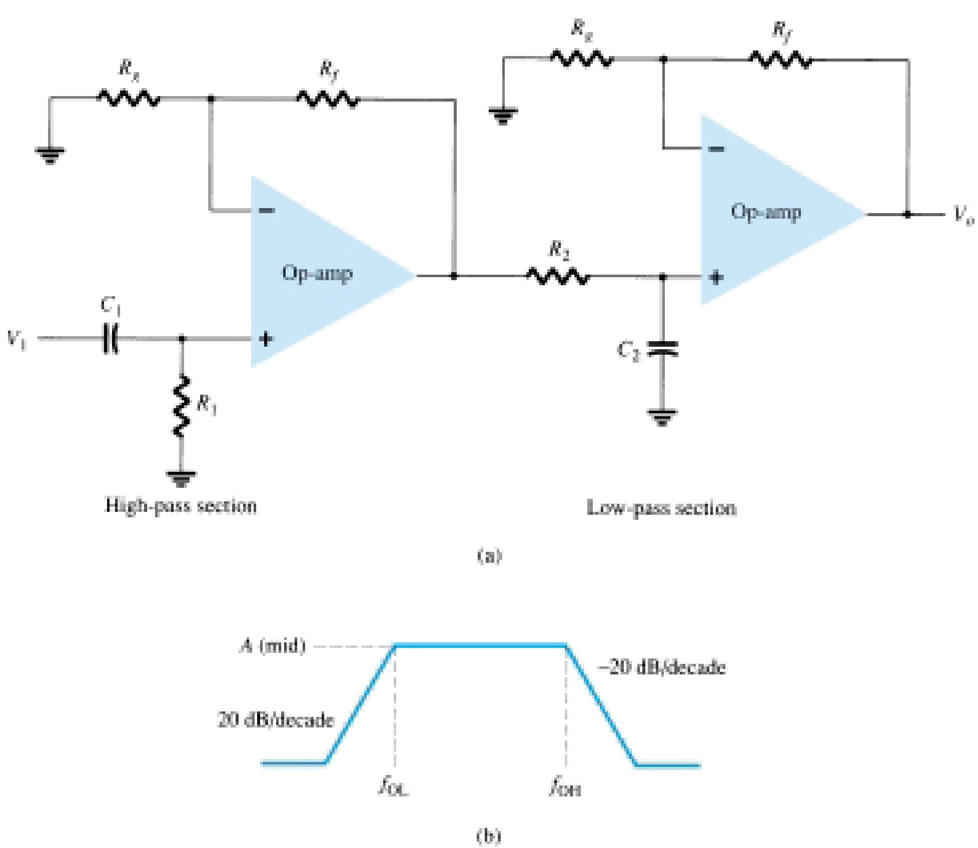


Figure 15.34 Bandpass active filter.

EXAMPLE 15.14 Calculate the cutoff frequencies of the bandpass filter circuit of Fig. 15.34 with $R_1 = R_2 = 10\ \text{k}\Omega$, $C_1 = 0.1\ \mu\text{F}$, and $C_2 = 0.002\ \mu\text{F}$.

Solution

$$f_{OL} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(10 \times 10^3)(0.1 \times 10^{-6})} = \mathbf{159.15\ Hz}$$

$$f_{OH} = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi(10 \times 10^3)(0.002 \times 10^{-6})} = \mathbf{7.96\ kHz}$$

15.7 PSPICE WINDOWS

Many of the practical op-amp applications covered in this chapter can be analyzed using PSpice. Analysis of various problems will be used to display the resulting dc bias or, using **PROBE,** to display resulting waveforms. As always, first use **Schematic** drawing to draw the circuit diagram and set the desired analysis, then use **Simulation** to analyze the circuit. Finally, examine the resulting **Output** or use **PROBE** to view various waveforms.

Program 15.1—Summing Op-Amp

A summing op-amp using a 741 IC is shown in Fig. 15.35. Three dc voltage inputs are summed, with a resulting output dc voltage determined as follows:

$$V_O = -[(100\ \text{k}\Omega/20\ \text{k}\Omega)(+2\ \text{V}) + (100\ \text{k}\Omega/50\ \text{k}\Omega)(-3\ \text{V}) + (100\ \text{k}\Omega/10\ \text{k}\Omega)(+1\ \text{V})]$$

$$= -[(10\ \text{V}) + (-6\ \text{V}) + (10\ \text{V})] = -[20\ \text{V} - 6\ \text{V}] = -14\ \text{V}$$

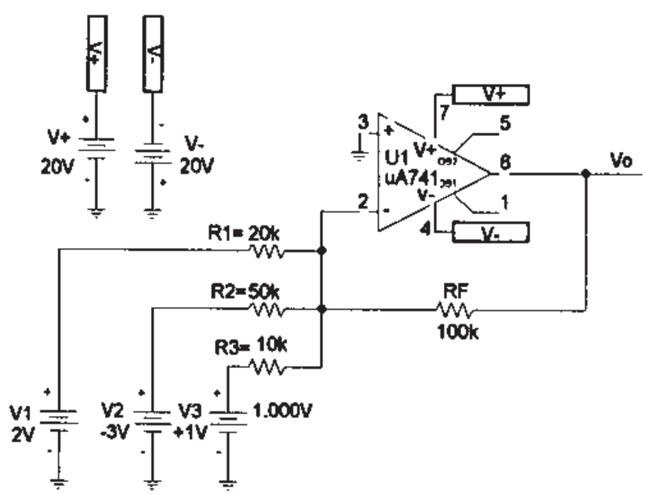


Figure 15.35 Summing amplifier using μA741 op-amp.

The steps in drawing the circuit and doing the analysis are as follows. Using **Get New Part:**

Select **uA741.**

Select **R** and repeatedly place three input resistors and feedback resistor; set resistor values and change resistor names, if desired.

Select **VDC** and place three input voltages and two supply voltages; set voltage values and change voltage names, if desired.

Select **GLOBAL** (global connector) and use to identify supply voltages and make connection to op-amp power input terminals (4 and 7)

Now that the circuit is drawn and all part names and values set as in Fig. 15.35, press the **Simulation** button to have PSpice analyze the circuit. Since no specific analysis has been chosen, only the dc bias will be carried out.

Press the **Enable Bias Voltage Display** button to see the dc voltages at various points in the circuit. The bias voltages displayed in Fig. 15.35 shows the output to be −13.99 V (compared to the calculated value of −14 V above).

Program 15.2—Op-Amp DC Voltmeter

A dc voltmeter built using a μA741 op-amp is provided by the schematic of Fig. 15.36. From the material presented in Section 15.5, the transfer function of the circuit is

$$I_O/V_1 = (R_F/R_1)(1/R_S) = (1\ \text{M}\Omega/1\ \text{M}\Omega)(1/10\ \text{k}\Omega)$$

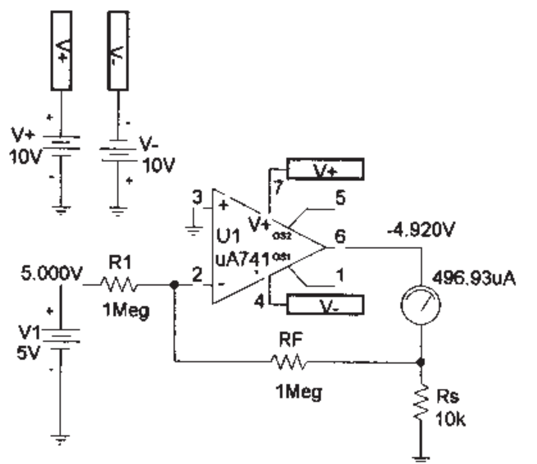


Figure 15.36 Op-amp dc voltmeter.

The full-scale setting of this voltmeter (for I_O full scale at 1 mA) is then

$$V_1(\text{full scale}) = (10\ \text{k}\Omega)(1\ \text{mA}) = 10\ \text{V}$$

Thus, an input of 10 V will result in a meter current of 1 mA—the full-scale deflection of the meter. Any input less then 10 V will result is a proportionately smaller meter deflection.

The steps in drawing the circuit and doing the analysis are as follows. Using **Get New Part:**

Select **μA741.**

Select **R** and repeatedly place input resistor, feedback resistor; and meter setting resistor; set resistor values and change resistor names, if desired.

Select **VDC** and place input voltage and two supply voltages; set voltage values and change voltage names, if desired.

Select **GLOBAL** (global connector) and use to identify supply voltages and make connection to op-amp power input terminals (4 and 7)

Select **IPROBE** and use as meter movement.

Now that the circuit is drawn and all part names and values set as in Fig. 15.36, press the **Simulation** button to have PSpice analyze the circuit. Since no specific analysis has been chosen, only the dc bias will be carried out.

Figure 15.36 shows that an input of 5 V will result in a current of 0.5 mA, with the meter reading of 0.5 being read as 5 V (since 1 mA full scale will occur for 10 V input).

Program 15.3—Low-Pass Active Filter

Figure 15.37 shows the schematic of a low-pass active filter. This first-order filter circuit passes frequencies from dc up to the cutoff frequency determined by resistor R_1 and capacitor C_1 using

$$f_{OH} = 1/(2\pi R_1 C_1)$$

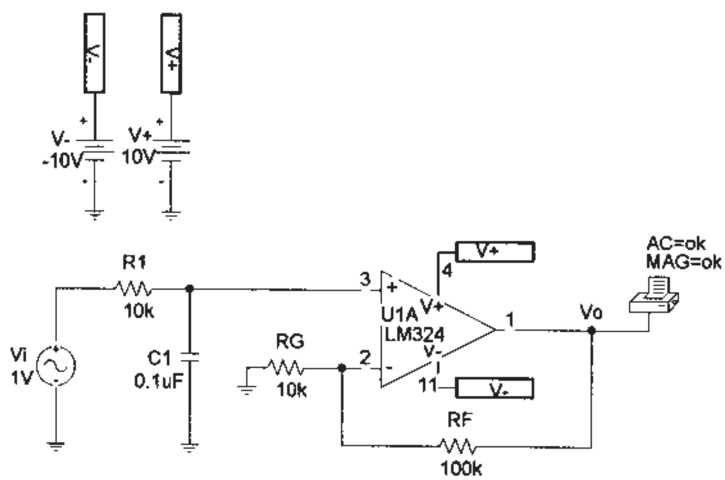


Figure 15.37 Low-pass active filter.

For the circuit of Fig. 15.37, this is

$$f_{OH} = 1/(2\pi R_1 C_1) = 1/(2\pi \cdot 10\ \text{k}\Omega \cdot 0.1\ \mu\text{F}) = 159\ \text{Hz}$$

Figure 15.38 shows the **Analysis Setup**—choosing an ac sweep of 10 points per decade from 1 Hz to 10 kHz. After running the analysis, a **PROBE** output showing the output voltage, V_O, is that shown in Fig. 15.39. The cutoff frequency obtained using **PROBE** is seen to be fh = 159.5 Hz, very close to that calculated above.

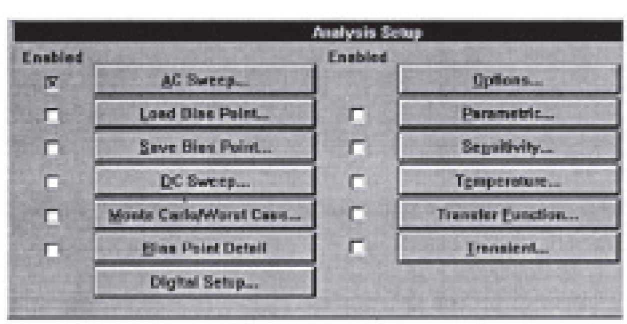


Figure 15.38 Analysis Setup for schematic of Fig. 15.37.

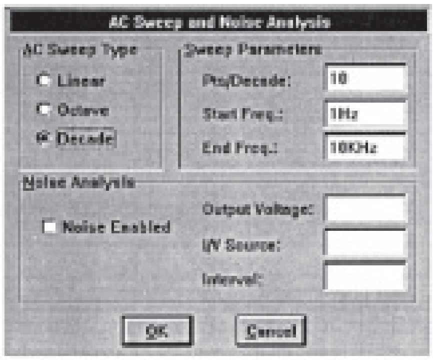


Figure 15.38 Continued.

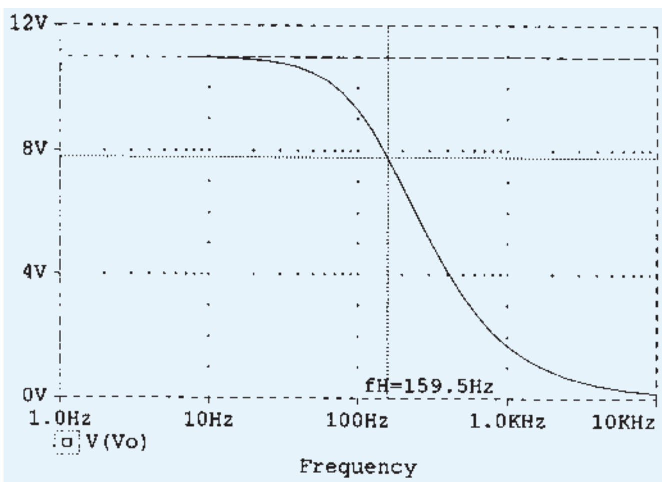


Figure 15.39 Waveform V_O for the circuit in Fig. 15.37.

Program 15.4—High-Pass Active Filter

Figure 15.40 shows the schematic of a high-pass active filter. This first-order filter circuit passes frequencies above a cutoff frequency determined by resistor R_1 and capacitor C_1 using

$$f_{\mathrm{OL}} = 1/(2\pi R_1 C_1)$$

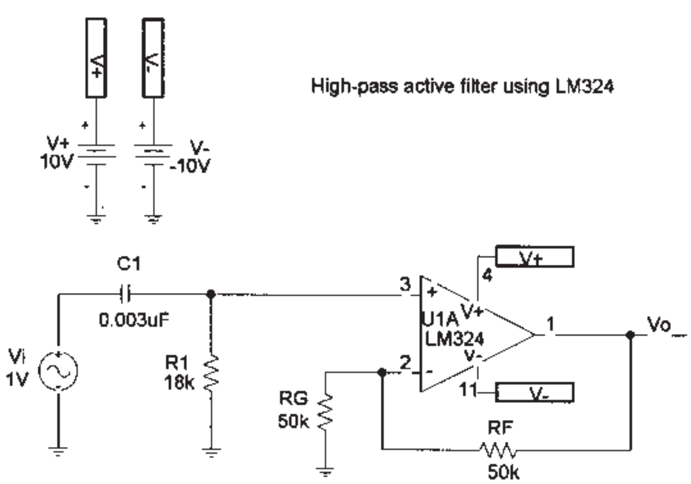


Figure 15.40 High-pass active filter.

For the circuit of Fig. 15.40, this is

$$f_{OH} = 1/(2\pi R_1 C_1) = 1/(2\pi \cdot 18\text{ k}\Omega \cdot 0.003\ \mu\text{F}) = 2.95\text{ kHz}$$

The **Analysis Setup** is set for an ac sweep of 10 points per decade from 10 Hz to 100 kHz. After running the analysis, a **PROBE** output showing the output voltage, V_O, is that shown in Fig. 15.41. The cutoff frequency obtained using probe is seen to be **fL** = 2.9 kHz, very close to that calculated above.

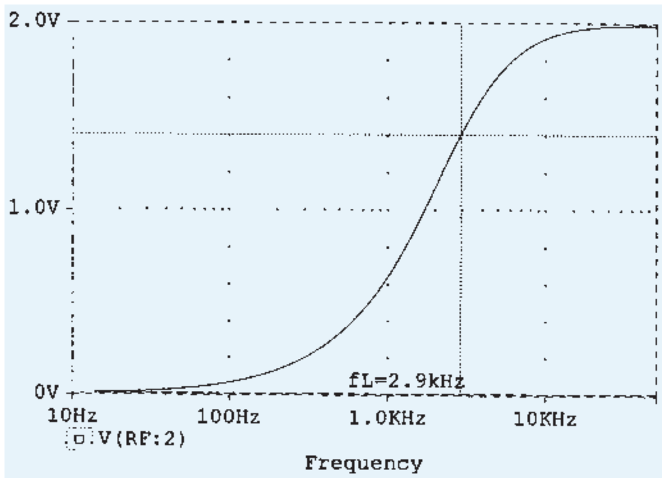


Figure 15.41 Probe output of V_O for the active high-pass filter circuit of Fig. 15.40.

Program 15.5—Second-Order High-Pass Active Filter

Figure 15.42 shows the schematic of a second-order high-pass active filter. This second-order filter circuit passes frequencies above a cutoff frequency determined by resistor R_1 and capacitor C_1 using

$$f_{OL} = 1/(2\pi R_1 C_1)$$

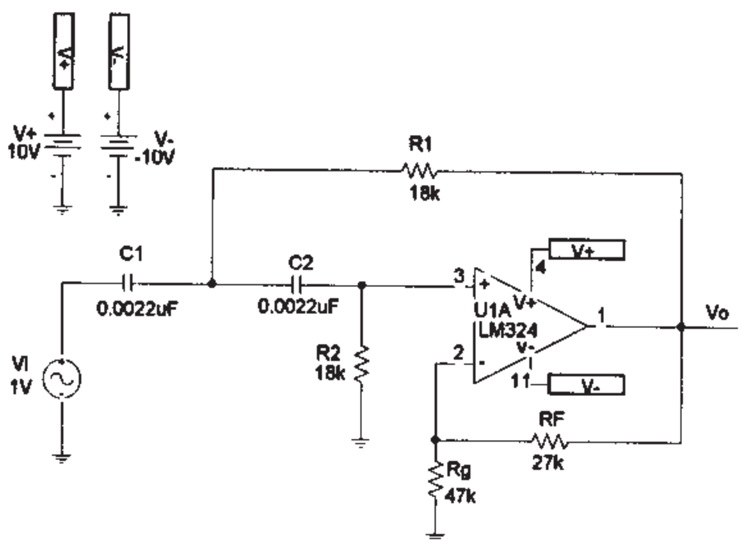


Figure 15.42 Second-order high-pass active filter.

For the circuit of Fig. 15.42, this is

$$f_{OL} = 1/(2\pi R_1 C_1) = 1/(2\ \pi \cdot 18\text{ k}\Omega \cdot 0.0022\ \mu\text{F}) = 4\text{ kHz}$$

The **Analysis Setup** is set for an ac sweep of 20 points per decade from 100 Hz to 100 kHz, as shown in Fig. 15.43. After running the analysis a **PROBE** output showing the output voltage (V_O) is shown in Fig. 15.44. The cutoff frequency obtained using **PROBE** is seen to be **fL** = 4 kHz, the same as that calculated above.

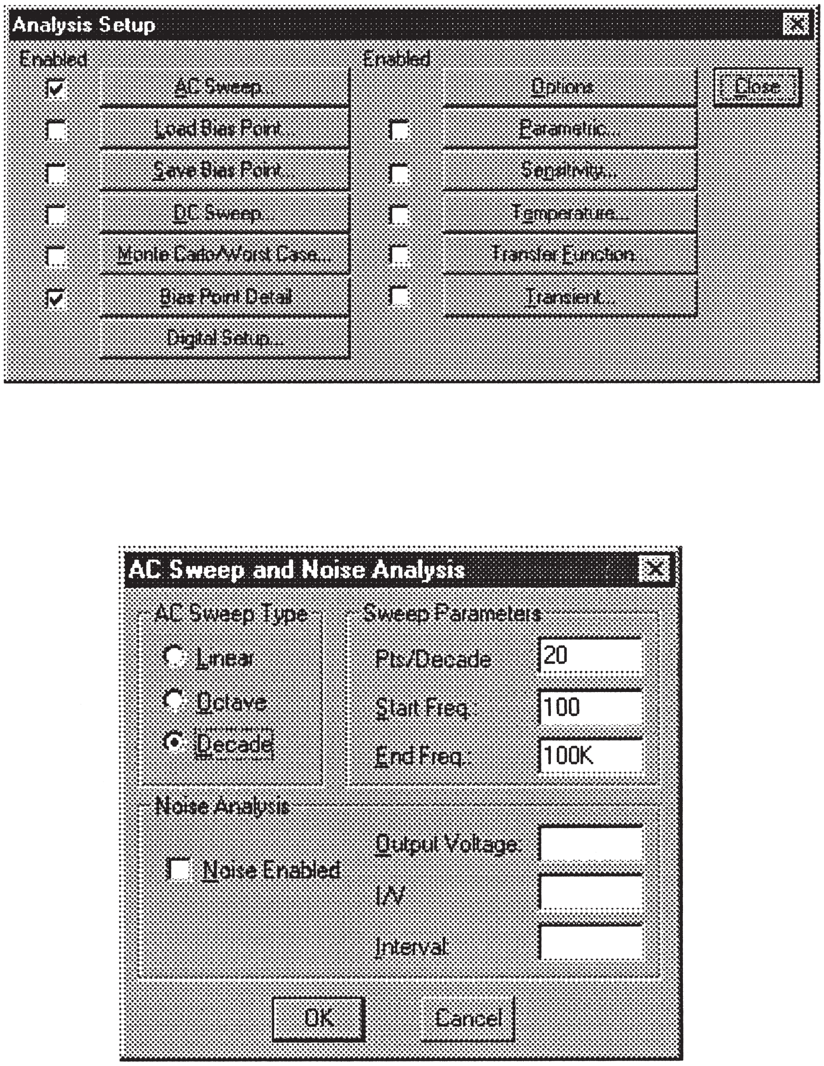


Figure 15.43 Analysis Setup for Fig. 15.42.

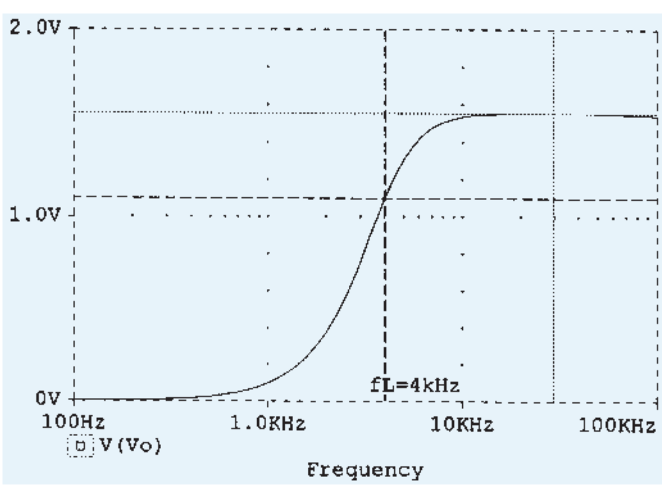


Figure 15.44 Probe plot of V_O for second-order high-pass active filter.

Fig. 15.45 shows the **PROBE** plot of the dB gain versus frequency, showing that over a decade (from about 200 Hz to about 2 kHz) the gain changes by about 40 dB—as expected for a second-order filter.

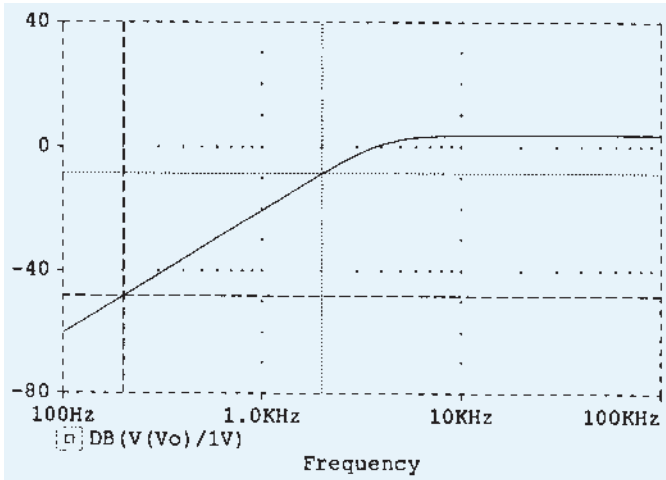


Figure 15.45 Probe plot of dB (V_O/V_i) for second-order high-pass active filter.

Program 15.6—Bandpass Active Filter

Figure 15.46 shows a bandpass active filter circuit. Using the values of Example 15.14, the bandpass frequencies are

$$f_{OL} = 1/(2\pi R_1C_1) = 1/(2\pi \cdot 10\text{ k}\Omega \cdot 0.1\ \mu\text{F}) = 159\text{ Hz}$$

$$f_{OH} = 1/(2\pi R_2C_2) = 1/(2\pi \cdot 10\text{ k}\Omega \cdot 0.002\ \mu\text{F}) = 7.96\text{ kHz}$$

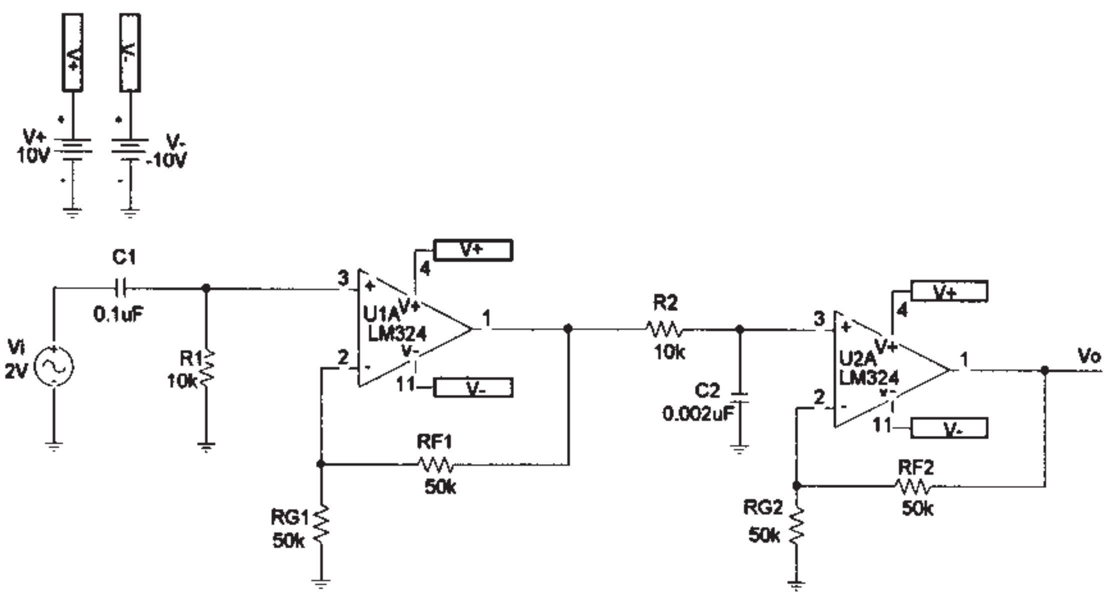


Figure 15.46 Bandpass active filter.

The sweep is set at 10 points per decade from 10 Hz to 1 MHz. The probe plot of V_O in Fig. 15.47 shows the low cutoff frequency at about 153 Hz and the upper cutoff frequency at about 8.2 kHz, these values matching those calculated above quite well.

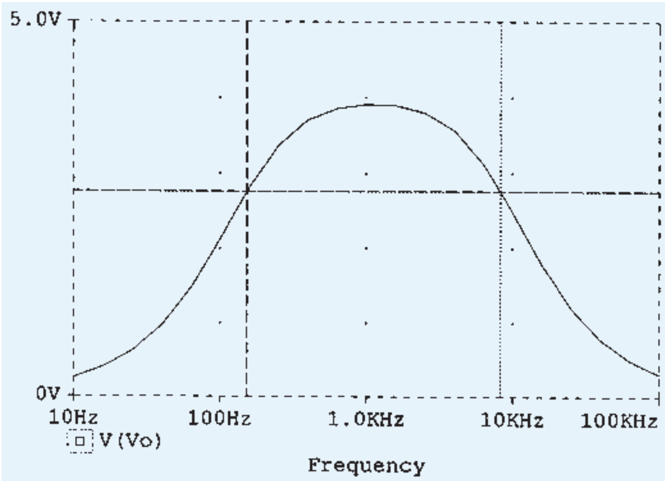


Figure 15.47 Probe plot of bandpass active filter.

PROBLEMS

§ 15.1 Constant-Gain Multiplier

1. Calculate the output voltage for the circuit of Fig. 15.48 for an input of $V_i = 3.5$ mV rms.

2. Calculate the output voltage of the circuit of Fig. 15.49 for input of 150 mV rms.

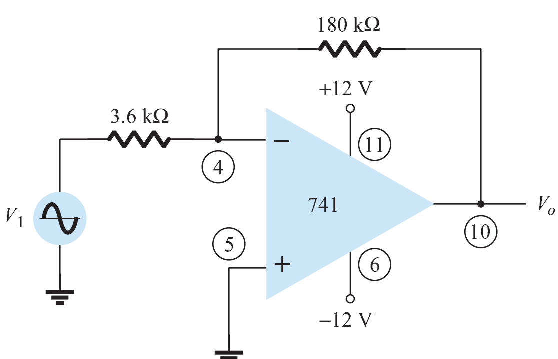


Figure 15.48 Problem 1

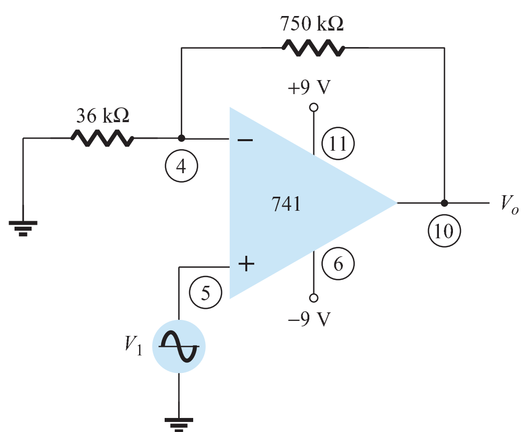


Figure 15.49 Problem 2

*__3.__ Calculate the output voltage in the circuit of Fig. 15.50.

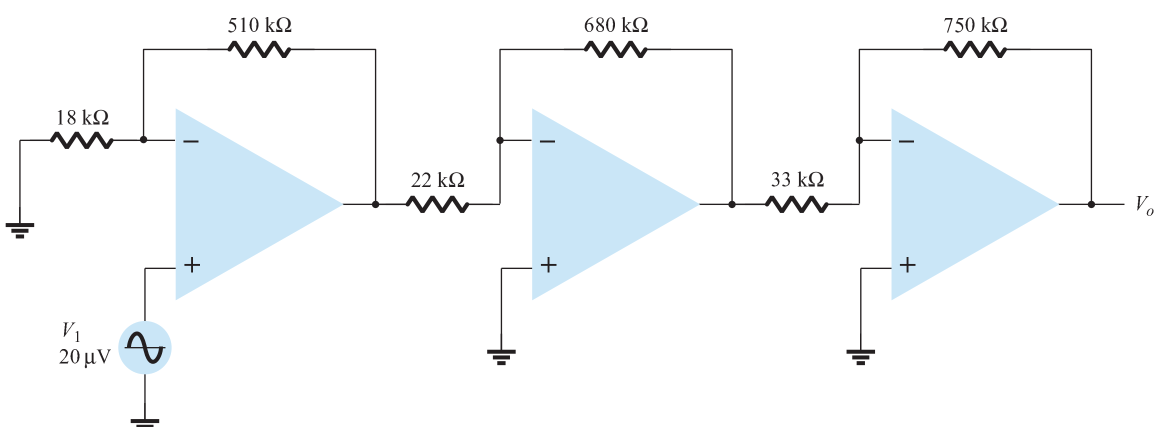


Figure 15.50 Problem 3

*4. Show the connection of an LM124 quad op-amp as a three-stage amplifier with gains of +15, −22, and −30. Use a 420-kΩ feedback resistor for all stages. What output voltage results for an input of $V_1 = 80\ \mu V$?

5. Show the connection of two op-amp stages using an LM358 IC to provide outputs that are 15 and −30 times larger than the input. Use a feedback resistor, $R_F = 150$ kΩ, in all stages.

§ 15.2 Voltage Summing

6. Calculate the output voltage for the circuit of Fig. 15.51 with inputs of $V_1 = 40$ mV rms and $V_2 = 20$ mV rms.

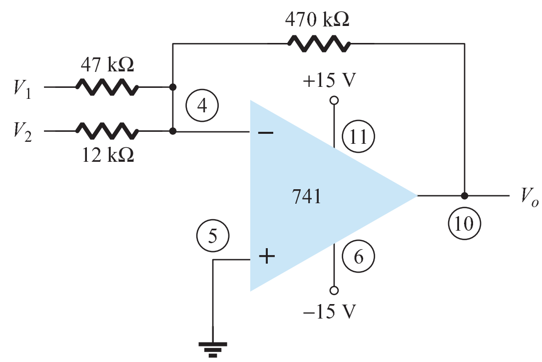


Figure 15.51 Problem 6

7. Determine the output voltage for the circuit of Fig. 15.52.

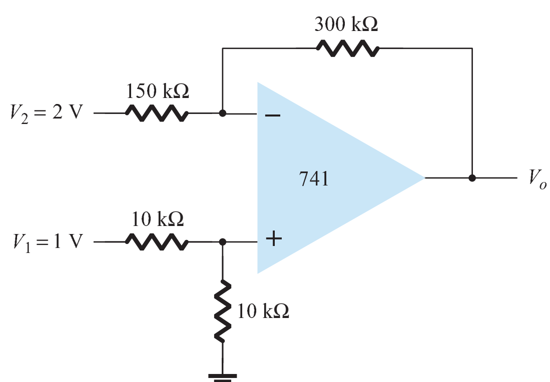


Figure 15.52 Problem 7

8. Determine the output voltage for the circuit of Fig. 15.53.

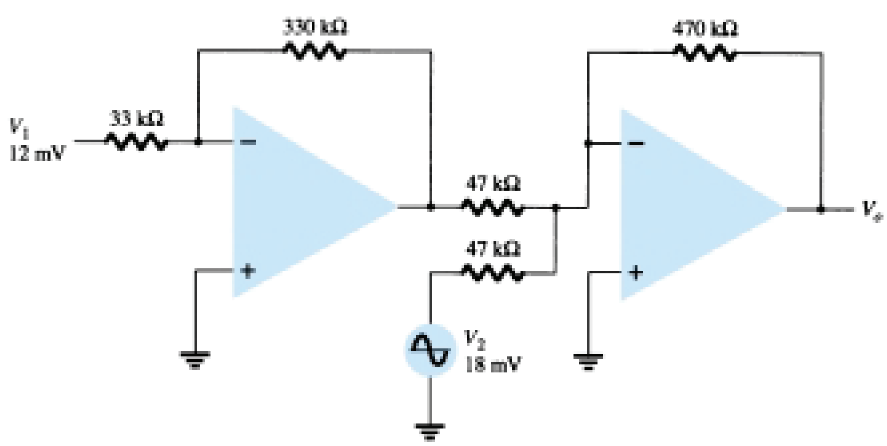


Figure 15.53 Problem 8

§ 15.3 Voltage Buffer

9. Show the connection (including pin information) of an LM124 IC stage connected as a unity-gain amplifier.

10. Show the connection (including pin information) of two LM358 stages connected as unity-gain amplifiers to provide the same output.

§ 15.4 Controlled Sources

11. For the circuit of Fig. 15.54, calculate I_L.

12. Calculate V_o for the circuit of Fig. 15.55.

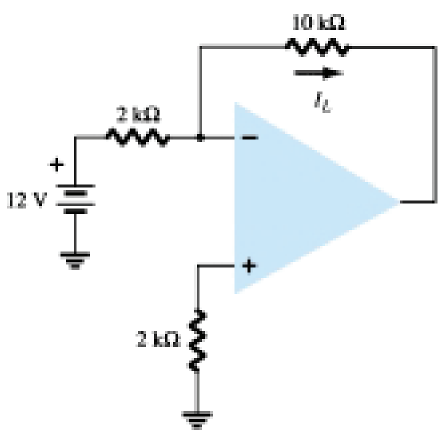


Figure 15.54 Problem 11

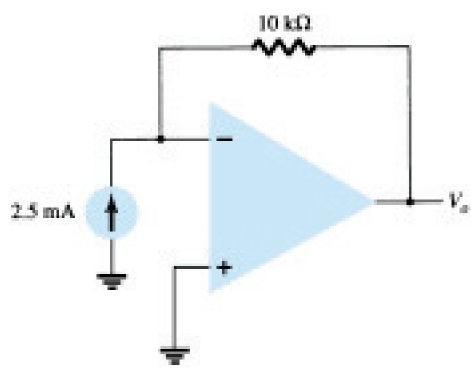


Figure 15.55 Problem 12

§ 15.5 Instrumentation Circuits

13. Calculate the output current I_o in the circuit of Fig. 15.56.

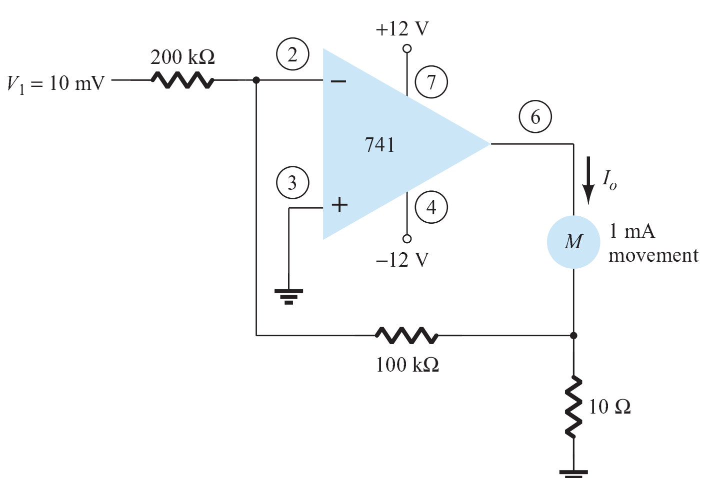


Figure 15.56 Problem 13

*14. **Calculate** V_o in the circuit of Fig. 15.57.

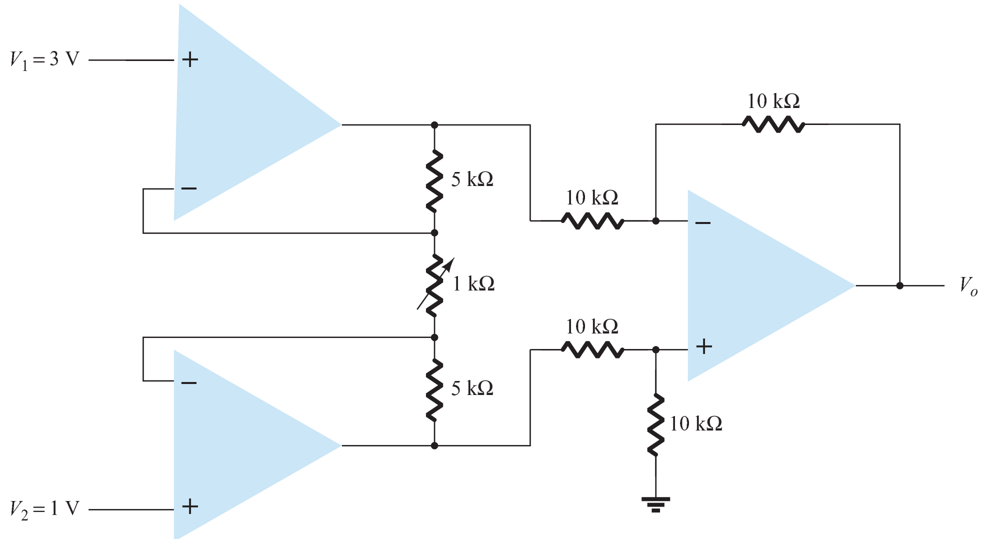


Figure 15.57 Problem 14

§ 15.6 Active Filters

15. Calculate the cutoff frequency of a first-order low-pass filter in the circuit of Fig. 15.58.

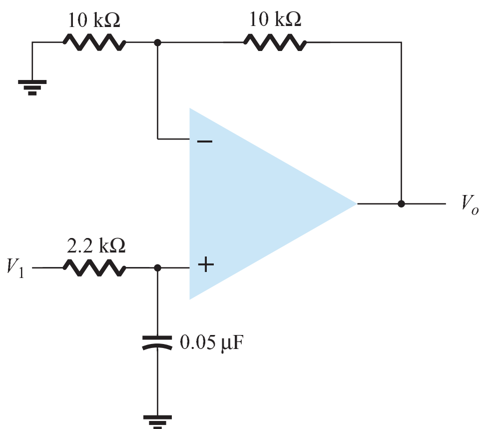


Figure 15.58 Problem 15

16. Calculate the cutoff frequency of the high-pass filter circuit in Fig. 15.59.

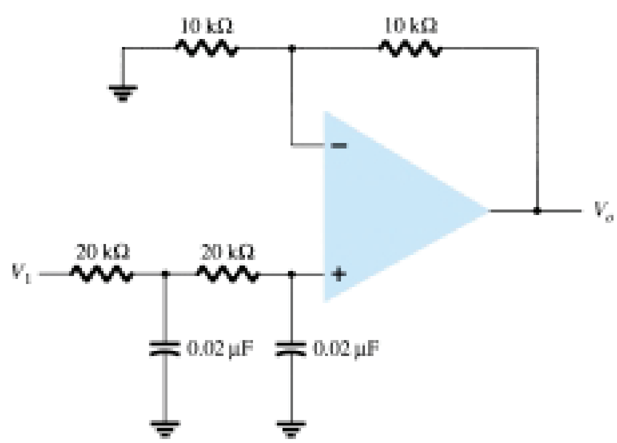


Figure 15.59 Problem 16

17. Calculate the lower and upper cutoff frequencies of the bandpass filter circuit in Fig. 15.60.

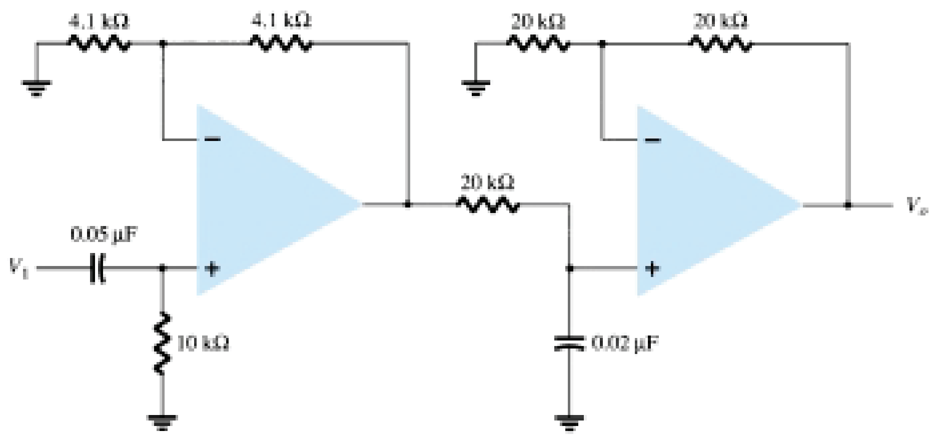


Figure 15.60 Problem 17

§ 15.7 PSpice Windows

*18. Use Design Center to draw the schematic of Fig. 15.61 and determine V_O.

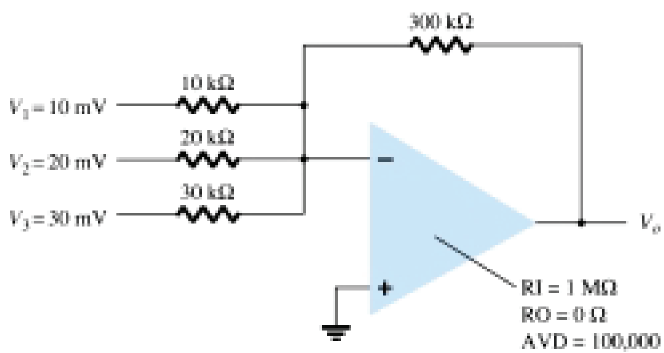


Figure 15.61 Problem 18

*19. Use Design Center to calculate I(VSENSE) in the circuit of Fig. 15.62.

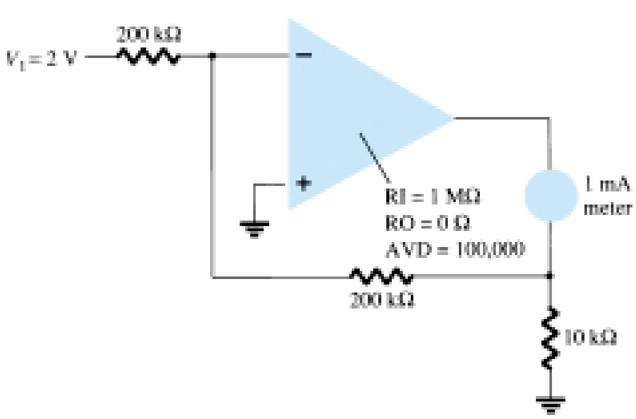


Figure 15.62 Problem 19

*20. Use Design Center to plot the response of the low-pass filter circuit in Fig. 15.63.

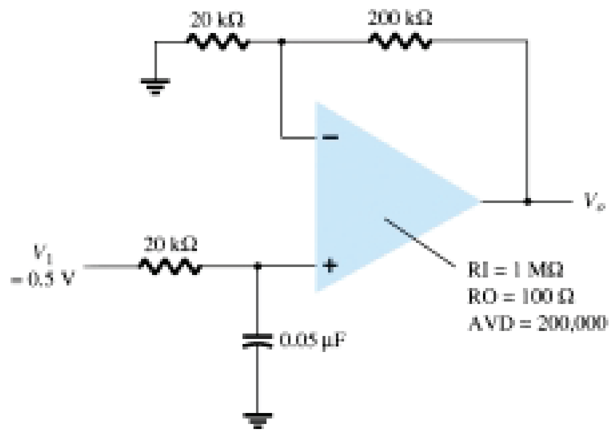


Figure 15.63 Problem 20

*21. Use Design Center to plot the response of the high-pass filter circuit in Fig. 15.64.

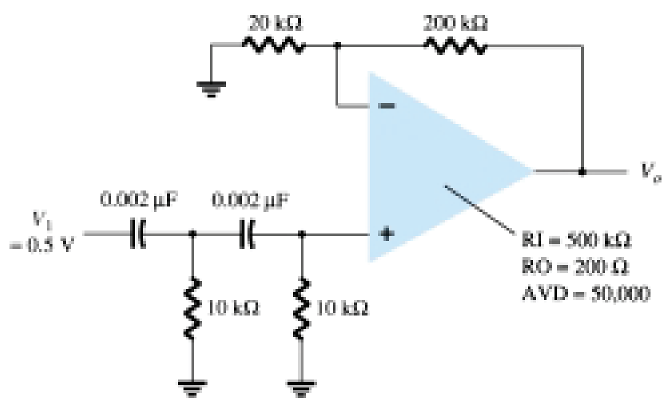


Figure 15.64 Problem 21

*22. Use Design Center to plot the response of the bandpass filter circuit in Fig. 15.65.

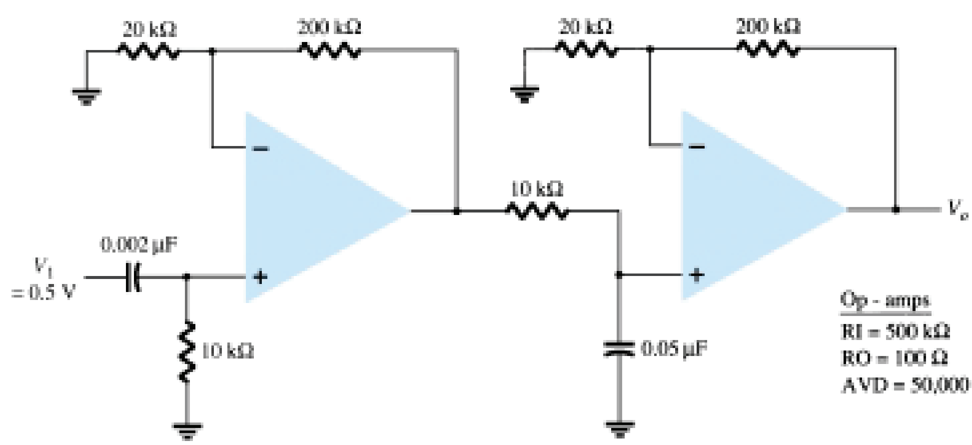


Figure 15.65 Problem 22

*Please Note: Asterisks indicate more difficult problems.

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CHAPTER 16
Power Amplifiers

16.1 INTRODUCTION—DEFINITIONS AND AMPLIFIER TYPES

An amplifier receives a signal from some pickup transducer or other input source and provides a larger version of the signal to some output device or to another amplifier stage. An input transducer signal is generally small (a few millivolts from a cassette or CD input, or a few microvolts from an antenna) and needs to be amplified sufficiently to operate an output device (speaker or other power-handling device). In small-signal amplifiers, the main factors are usually amplification linearity and magnitude of gain. Since signal voltage and current are small in a small-signal amplifier, the amount of power-handling capacity and power efficiency are of little concern. A voltage amplifier provides voltage amplification primarily to increase the voltage of the input signal. Large-signal or power amplifiers, on the other hand, primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts. In the present chapter, we concentrate on those amplifier circuits used to handle large-voltage signals at moderate to high current levels. The main features of a large-signal amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device.

One method used to categorize amplifiers is by class. Basically, amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal. A brief description of amplifier classes is provided next.

Class A: The output signal varies for a full 360° of the cycle. Figure 16.1a shows

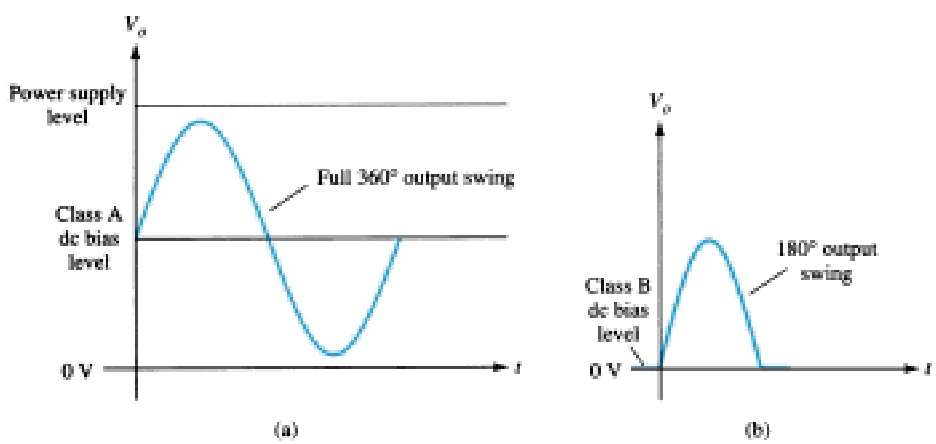

Figure 16.1 Amplifier operating classes.

that this requires the Q-point to be biased at a level so that at least half the signal swing of the output may vary up and down without going to a high-enough voltage to be limited by the supply voltage level or too low to approach the lower supply level, or 0 V in this description.

Class B: A class B circuit provides an output signal varying over one-half the input signal cycle, or for 180° of signal, as shown in Fig. 16.1b. The dc bias point for class B is therefore at 0 V, with the output then varying from this bias point for a half-cycle. Obviously, the output is not a faithful reproduction of the input if only one half-cycle is present. Two class B operations—one to provide output on the positive-output half-cycle and another to provide operation on the negative-output half-cycle are necessary. The combined half-cycles then provide an output for a full 360° of operation. This type of connection is referred to as push-pull operation, which is discussed later in this chapter. Note that class B operation by itself creates a very distorted output signal since reproduction of the input takes place for only 180° of the output signal swing.

Class AB: An amplifier may be biased at a dc level above the zero base current level of class B and above one-half the supply voltage level of class A; this bias condition is class AB. Class AB operation still requires a push-pull connection to achieve a full output cycle, but the dc bias level is usually closer to the zero base current level for better power efficiency, as described shortly. For class AB operation, the output signal swing occurs between 180° and 360° and is neither class A nor class B operation.

Class C: The output of a class C amplifier is biased for operation at less than 180° of the cycle and will operate only with a tuned (resonant) circuit, which provides a full cycle of operation for the tuned or resonant frequency. This operating class is therefore used in special areas of tuned circuits, such as radio or communications.

Class D: This operating class is a form of amplifier operation using pulse (digital) signals, which are on for a short interval and off for a longer interval. Using digital techniques makes it possible to obtain a signal that varies over the full cycle (using sample-and-hold circuitry) to recreate the output from many pieces of input signal. The major advantage of class D operation is that the amplifier is on (using power) only for short intervals and the overall efficiency can practically be very high, as described next.

Amplifier Efficiency

The power efficiency of an amplifier, defined as the ratio of power output to power input, improves (gets higher) going from class A to class D. In general terms, we see that a class A amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency, especially with small input signals, when very little ac power is delivered to the load. In fact, the maximum efficiency of a class A circuit, occurring for the largest output voltage and current swing, is only 25% with a direct or series-fed load connection and 50% with a transformer connection to the load. Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%. Class D operation can achieve power efficiency over 90% and provides the most efficient operation of all the operating classes. Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings—between 25% (or 50%) and 78.5%. Table 16.1 summarizes the operation of the various amplifier classes. This table provides a relative comparison of the output cycle operation and power efficiency for the various class types. In class B operation, a push-pull connection is obtained using either a transformer coupling or by using complementary (or quasi-complementary) operation with *npn* and *pnp* transistors to provide operation on opposite polarity cycles. While transformer oper-

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TABLE 16.1 Comparison of Amplifier Classes

	Class				
	A	*AB*	*B*	*C**	*D*
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

**Class C is usually not used for delivering large amounts of power, thus the efficiency is not given here.*

ation can provide opposite cycle signals, the transformer itself is quite large in many applications. A transformerless circuit using complementary transistors provides the same operation in a much smaller package. Circuits and examples are provided later in this chapter.

16.2 SERIES-FED CLASS A AMPLIFIER

The simple fixed-bias circuit connection shown in Fig. 16.2 can be used to discuss the main features of a class A series-fed amplifier. The only differences between this circuit and the small-signal version considered previously is that the signals handled by the large-signal circuit are in the range of volts and the transistor used is a power transistor that is capable of operating in the range of a few to tens of watts. As will be shown in this section, this circuit is not the best to use as a large-signal amplifier because of its poor power efficiency. The beta of a power transistor is generally less than 100, the overall amplifier circuit using power transistors that are capable of handling large power or current while not providing much voltage gain.

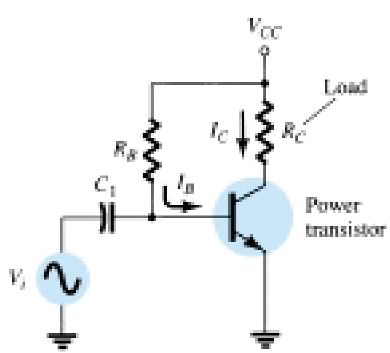

Figure 16.2 Series-fed class A large-signal amplifier.

DC Bias Operation

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7\ \text{V}}{R_B} \tag{16.1}$$

with the collector current then being

$$I_C = \beta I_B \tag{16.2}$$

with the collector–emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C \tag{16.3}$$

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To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig. 16.3. An ac load line is drawn using the values of V_{CC} and R_C. The intersection of the dc bias value of I_B with the dc load line then determines the operating point (Q-point) for the circuit. The quiescent-point values are those calculated using Eqs. (16.1) through (16.3). If the dc bias collector current is set at one-half the possible signal swing (between 0 and V_{CC}/R_C), the largest collector current swing will be possible. Additionally, if the quiescent collector–emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible. With the Q-point set at this optimum bias point, the power considerations for the circuit of Fig. 16.2 are determined as described below.

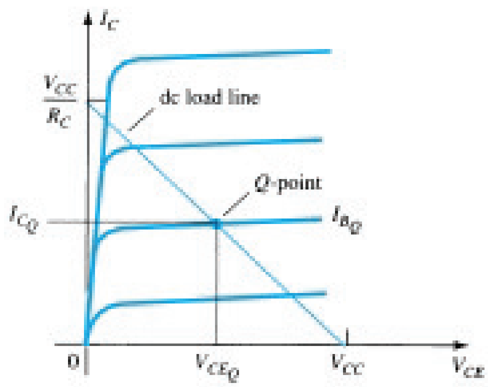

Figure 16.3 Transistor characteristic showing load line and Q-point.

AC Operation

When an input ac signal is applied to the amplifier of Fig. 16.2, the output will vary from its dc bias operating voltage and current. A small input signal, as shown in Fig. 16.4, will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well

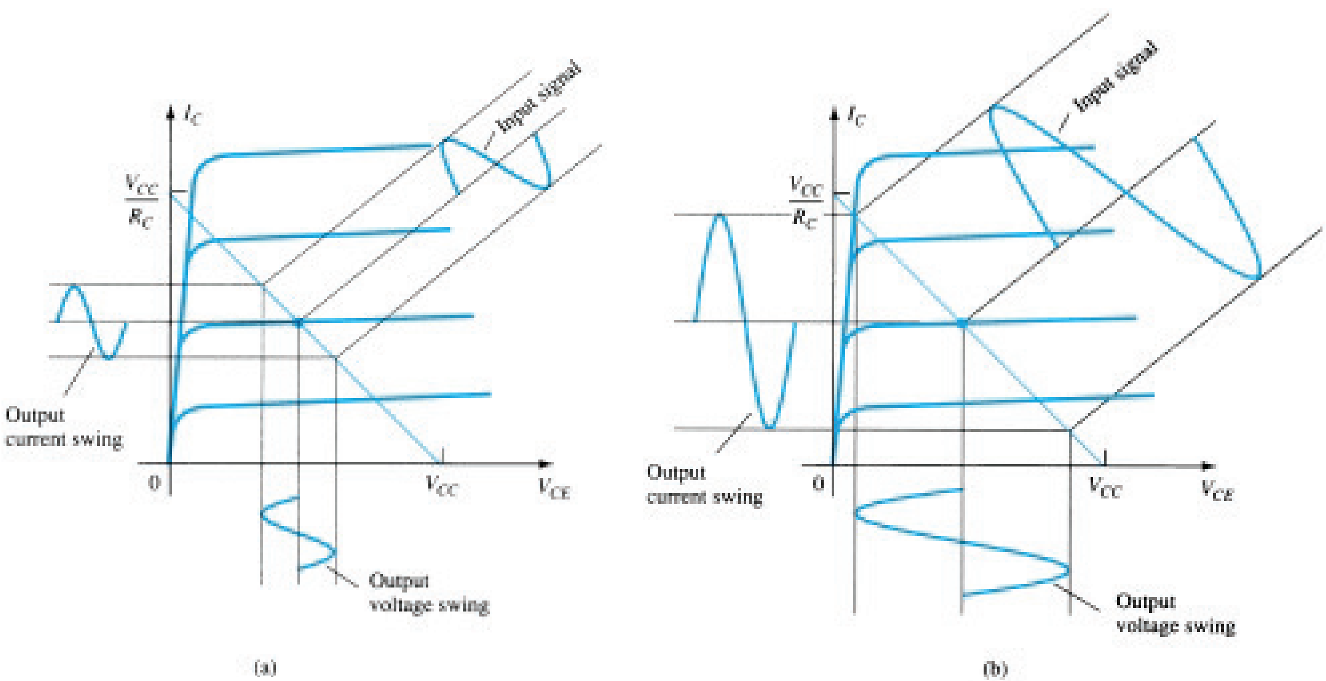

Figure 16.4 Amplifier input and output signal variation.

as the collector–emitter voltage to vary around its dc bias value. As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition. For the current this limiting condition is either zero current at the low end or V_{CC}/R_C at the high end of its swing. For the collector–emitter voltage, the limit is either 0 V or the supply voltage, V_{CC}.

Power Considerations

The power into an amplifier is provided by the supply. With no input signal, the dc current drawn is the collector bias current, I_{C_Q}. The power then drawn from the supply is

$$P_i(\text{dc}) = V_{CC} I_{C_Q} \tag{16.4}$$

Even with an ac signal applied, the average current drawn from the supply remains the same, so that Eq. (16.4) represents the input power supplied to the class A series-fed amplifier.

OUTPUT POWER

The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load, R_C, in the circuit of Fig. 16.2. The ac signal, V_i, causes the base current to vary around the dc bias current and the collector current around its quiescent level, I_{C_Q}. As shown in Fig. 16.4, the ac input signal results in ac current and ac voltage signals. The larger the input signal, the larger the output swing, up to the maximum set by the circuit. The ac power delivered to the load (R_C) can be expressed in a number of ways.

Using rms signals: The ac power delivered to the load (R_C) may be expressed using

$$P_o(\text{ac}) = V_{CE}(\text{rms}) I_C(\text{rms}) \tag{16.5a}$$

$$P_o(\text{ac}) = I_C^2(\text{rms}) R_C \tag{16.5b}$$

$$P_o(\text{ac}) = \frac{V_C^2(\text{rms})}{R_C} \tag{16.5c}$$

Using peak signals: The ac power delivered to the load may be expressed using

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p}) I_C(\text{p})}{2} \tag{16.6a}$$

$$P_o(\text{ac}) = \frac{I_C^2(\text{p})}{2R_C} \tag{16.6b}$$

$$P_o(\text{ac}) = \frac{V_{CE}^2(\text{p})}{2R_C} \tag{16.6c}$$

Using peak-to-peak signals: The ac power delivered to the load may be expressed using

$$P_o(\text{ac}) = \frac{V_{CE}(\text{p-p}) I_C(\text{p-p})}{8} \tag{16.7a}$$

P_L

$$P_o(\text{ac}) = \frac{I_C^2(\text{p-p})}{8} R_C \tag{16.7b}$$

$$P_o(\text{ac}) = \frac{V_{CE}^2(\text{p-p})}{8R_C} \tag{16.7c}$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% \tag{16.8}$$

MAXIMUM EFFICIENCY

For the class A series-fed amplifier, the maximum efficiency can be determined using the maximum voltage and current swings. For the voltage swing it is

$$\text{maximum } V_{CE}(\text{p-p}) = V_{CC}$$

For the current swing it is

$$\text{maximum } I_C(\text{p-p}) = \frac{V_{CC}}{R_C}$$

Using the maximum voltage swing in Eq. (16.7a) yields

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}(V_{CC}/R_C)}{8}$$

$$= \frac{V_{CC}^2}{8R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the maximum value:

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_C) = V_{CC}\frac{V_{CC}/R_C}{2}$$

$$= \frac{V_{CC}^2}{2R_C}$$

We can then use Eq. (16.8) to calculate the maximum efficiency:

$$\text{maximum } \%\ \eta = \frac{\text{maximum } P_o(\text{ac})}{\text{maximum } P_i(\text{dc})} \times 100\%$$

$$= \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\%$$

$$= 25\%$$

The maximum efficiency of a class A series-fed amplifier is thus seen to be 25%. Since this maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most series-fed circuits will provide efficiencies of much less than 25%.

Calculate the input power, output power, and efficiency of the amplifier circuit in

Fig. 16.5 for an input voltage that results in a base current of 10 mA peak.

EXAMPLE 16.1

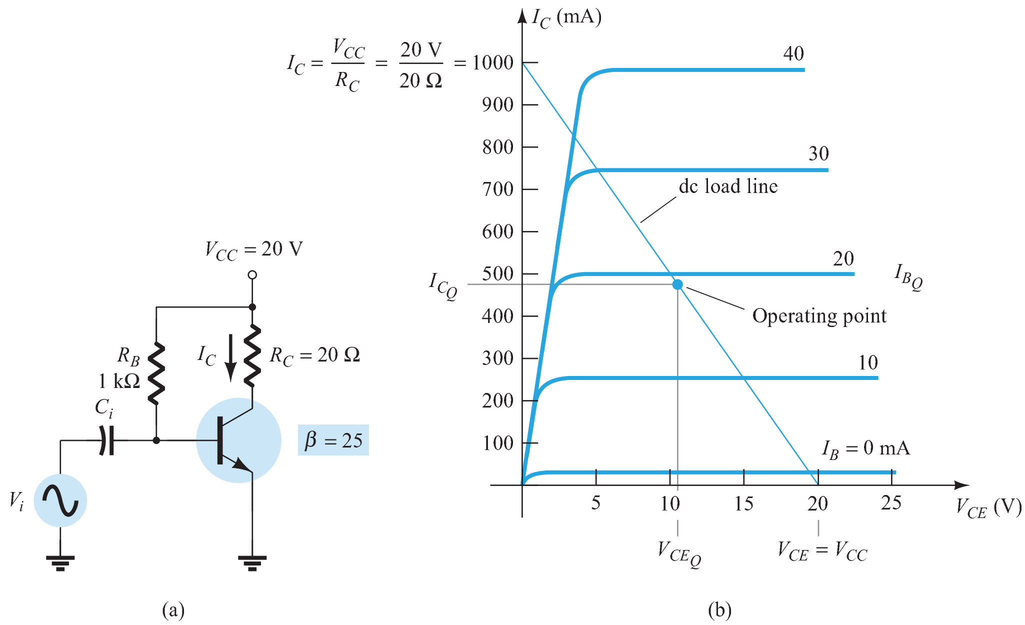

Figure 16.5 Operation of a series-fed circuit for Example 16.1.

Solution

Using Eqs. (16.1) through (16.3), the *Q*-point can be determined to be

$$I_{B_Q} = \frac{V_{CC} - 0.7\text{ V}}{R_B} = \frac{20\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = 19.3\text{ mA}$$

$$I_{C_Q} = \beta I_B = 25(19.3\text{ mA}) = 482.5\text{ mA} \cong 0.48\text{ A}$$

$$V_{CE_Q} = V_{CC} - I_C R_C = 20\text{ V} - (0.48\ \Omega)(20\ \Omega) = 10.4\text{ V}$$

This bias point is marked on the transistor collector characteristic of Fig. 16.5b. The ac variation of the output signal can be obtained graphically using the dc load line drawn on Fig. 16.5b by connecting $V_{CE} = V_{CC} = 20$ V with $I_C = V_{CC}/R_C = 1000$ mA $= 1$ A, as shown. When the input ac base current increases from its dc bias level, the collector current rises by

$$I_C(\text{p}) = \beta I_B(\text{p}) = 25(10\text{ mA peak}) = 250\text{ mA peak}$$

Using Eq. (16.6b) yields

$$P_o(\text{ac}) = \frac{I_C^2(\text{p})}{2} R_C = \frac{(250 \times 10^{-3}\text{ A})^2}{2}(20\ \Omega) = \mathbf{0.625\ W}$$

Using Eq. (16.4) results in

$$P_i(\text{dc}) = V_{CC} I_{C_Q} = (20\text{ V})(0.48\text{ A}) = \mathbf{9.6\ W}$$

The amplifier's power efficiency can then be calculated using Eq. (16.8):

$$\%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.625\text{ W}}{9.6\text{ W}} \times 100\% = \mathbf{6.5\%}$$

P_L

16.3 TRANSFORMER-COUPLED CLASS A AMPLIFIER

A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in Fig. 16.6. This is a simple circuit form to use in presenting a few basic concepts. More practical circuit versions are covered later. Since the circuit uses a transformer to step voltage or current, a review of voltage and current step-up and step-down is presented next.

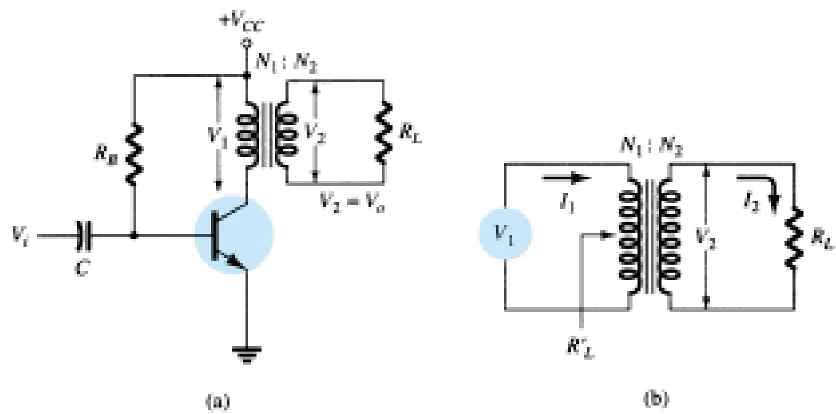

Figure 16.6 Transformer-coupled audio power amplifier.

Transformer Action

A transformer can increase or decrease voltage or current levels according to the turns ratio, as explained below. In addition, the impedance connected to one side of a transformer can be made to appear either larger or smaller (step up or step down) at the other side of the transformer, depending on the square of the transformer winding turns ratio. The following discussion assumes ideal (100%) power transfer from primary to secondary, that is, no power losses are considered.

VOLTAGE TRANSFORMATION

As shown in Fig. 16.7a, the transformer can step up or step down a voltage applied to one side directly as the ratio of the turns (or number of windings) on each side. The voltage transformation is given by

$$\frac{V_2}{V_1} = \frac{N_2}{N_1} \tag{16.9}$$

Equation (16.9) shows that if the number of turns of wire on the secondary side is larger than on the primary, the voltage at the secondary side is larger than the voltage at the primary side.

CURRENT TRANSFORMATION

The current in the secondary winding is inversely proportional to the number of turns in the windings. The current transformation is given by

$$\frac{I_2}{I_1} = \frac{N_1}{N_2} \tag{16.10}$$

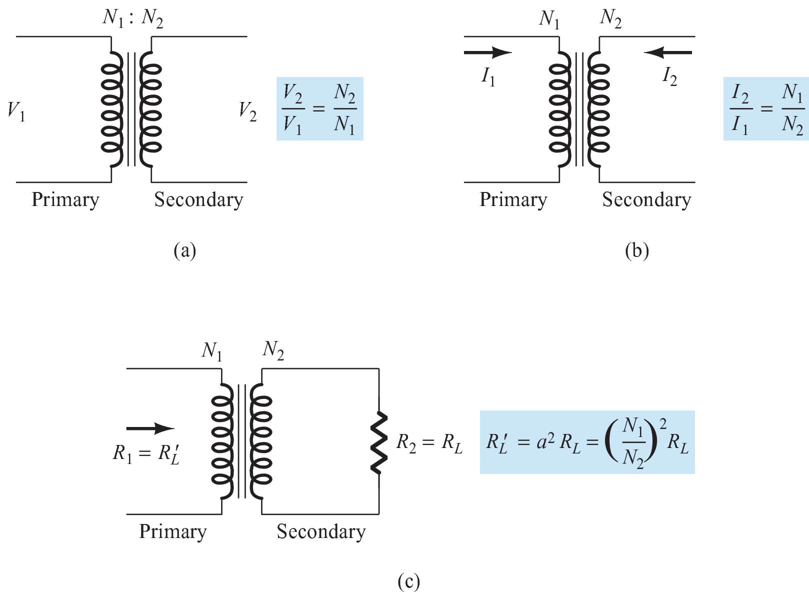

Figure 16.7 Transformer operation: (a) voltage transformation; (b) current transformation; (c) impedance transformation.

This relationship is shown in Fig. 16.7b. If the number of turns of wire on the secondary is greater than that on the primary, the secondary current will be less than the current in the primary.

IMPEDANCE TRANSFORMATION

Since the voltage and current can be changed by a transformer, an impedance "seen" from either side (primary or secondary) can also be changed. As shown in Fig. 16.7c, an impedance R_L is connected across the transformer secondary. This impedance is changed by the transformer when viewed at the primary side (R_L'). This can be shown as follows:

$$\frac{R_L}{R_L'} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2}{I_2}\frac{I_1}{V_1} = \frac{V_2}{V_1}\frac{I_1}{I_2} = \frac{N_2}{N_1}\frac{N_2}{N_1} = \left(\frac{\mathbf{N_2}}{\mathbf{N_1}}\right)^2$$

If we define $a = N_1/N_2$, where a is the turns ratio of the transformer, the above equation becomes

$$\frac{R_L'}{R_L} = \frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2 = a^2 \qquad (16.11)$$

We can express the load resistance reflected to the primary side as:

$$R_1 = a^2R_2 \quad \text{or} \quad R_L' = a^2R_L \qquad (16.12)$$

where R_L' is the reflected impedance. As shown in Eq. (16.12), the reflected impedance is related directly to the square of the turns ratio. If the number of turns of the secondary is smaller than that of the primary, the impedance seen looking into the primary is larger than that of the secondary by the square of the turns ratio.

EXAMPLE 16.2

Calculate the effective resistance seen looking into the primary of a 15:1 transformer connected to an 8-Ω load.

Solution

Eq. (16.12): $R_L' = a^2R_L = (15)^2(8\ \Omega) = 1800\ \Omega = \mathbf{1.8\ k\Omega}$

P_L

EXAMPLE 16.3 What transformer turns ratio is required to match a 16-Ω speaker load so that the effective load resistance seen at the primary is 10 kΩ?

Solution

$$\text{Eq. (16.11):}\quad \left(\frac{N_1}{N_2}\right)^2 = \frac{R'_L}{R_L} = \frac{10\text{ k}\Omega}{16\ \Omega} = 625$$

$$\frac{N_1}{N_2} = \sqrt{625} = \mathbf{25:1}$$

Operation of Amplifier Stage

DC LOAD LINE

The transformer (dc) winding resistance determines the dc load line for the circuit of Fig. 16.6. Typically, this dc resistance is small (ideally 0 Ω) and, as shown in Fig. 16.8, a 0-Ω dc load line is a straight vertical line. A practical transformer winding resistance would be a few ohms, but only the ideal case will be considered in this discussion. There is no dc voltage drop across the 0-Ω dc load resistance, and the load line is drawn straight vertically from the voltage point, $V_{CE_Q} = V_{CC}$.

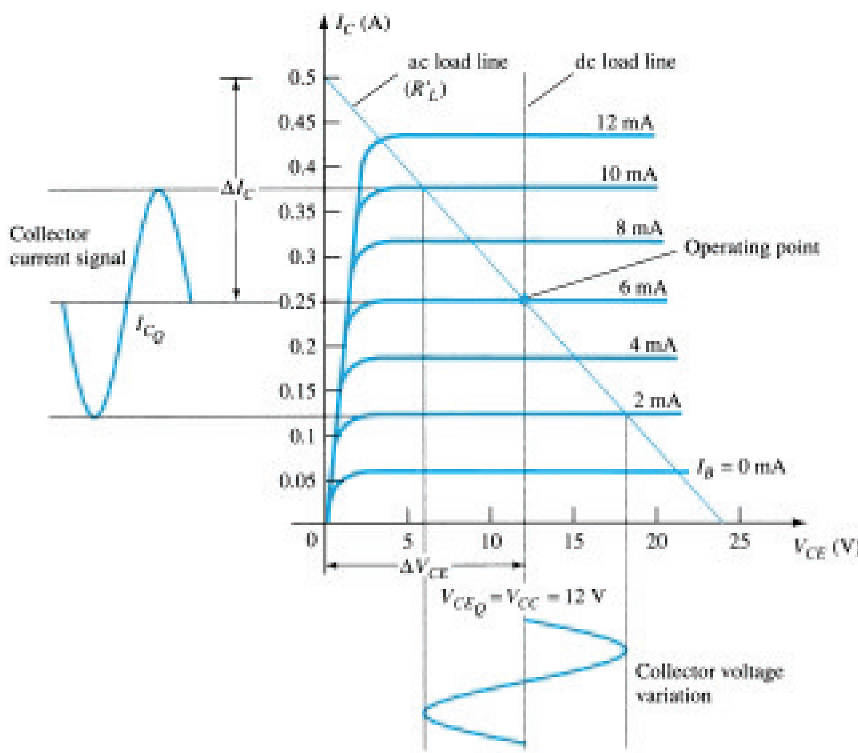

Figure 16.8 Load lines for class A transformer-coupled amplifier.

QUIESCENT OPERATING POINT

The operating point in the characteristic curve of Fig. 16.8 can be obtained graphically at the point of intersection of the dc load line and the base current set by the circuit. The collector quiescent current can then be obtained from the operating point. In class A operation, keep in mind that the dc bias point sets the conditions for the maximum undistorted signal swing for both collector current and collector–emitter voltage. If the input signal produces a voltage swing less than the maximum possible, the efficiency of the circuit at that time will be less than 25%. The dc bias point is therefore important in setting the operation of a class A series-fed amplifier.

AC LOAD LINE

To carry out ac analysis, it is necessary to calculate the ac load resistance "seen" looking into the primary side of the transformer, then draw the ac load line on the collector characteristic. The reflected load resistance (R'_L) is calculated using Eq. (16.12) using the value of the load connected across the secondary (R_L) and the turns ratio of the transformer. The graphical analysis technique then proceeds as follows. Draw the ac load line so that it passes through the operating point and has a slope equal to $-1/R'_L$ (the reflected load resistance), the load line slope being the negative reciprocal of the ac load resistance. Notice that the ac load line shows that the output signal swing can exceed the value of V_{CC}. In fact, the voltage developed across the transformer primary can be quite large. It is therefore necessary after obtaining the ac load line to check that the possible voltage swing does not exceed transistor maximum ratings.

SIGNAL SWING AND OUTPUT AC POWER

Figure 16.9 shows the voltage and current signal swings from the circuit of Fig. 16.6. From the signal variations shown in Fig. 16.9, the values of the peak-to-peak signal swings are

$$V_{CE}(\text{p-p}) = V_{CE_{\max}} - V_{CE_{\min}}$$

$$I_C(\text{p-p}) = I_{C_{\max}} - I_{C_{\min}}$$

The ac power developed across the transformer primary can then be calculated using

$$P_o(\text{ac}) = \frac{(V_{CE_{\max}} - V_{CE_{\min}})(I_{C_{\max}} - I_{C_{\min}})}{8} \qquad (16.13)$$

The ac power calculated is that developed across the primary of the transformer. Assuming an ideal transformer (a highly efficient transformer has an efficiency of well over 90%), the power delivered by the secondary to the load is approximately that calculated using Eq. (16.13). The output ac power can also be determined using the voltage delivered to the load.

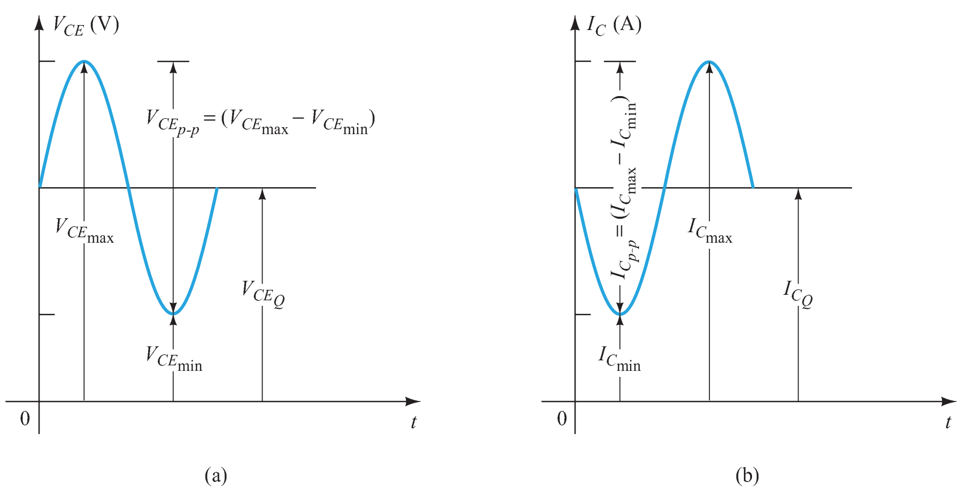

Figure 16.9 Graphical operation of transformer-coupled class A amplifier.

P_L

For the ideal transformer, the voltage delivered to the load can be calculated using Eq. (16.9):

$$V_L = V_2 = \frac{N_2}{N_1}V_1$$

The power across the load can then be expressed as

$$P_L = \frac{V_L^2(\text{rms})}{R_L}$$

and equals the power calculated using Eq. (16.5c).

Using Eq. (16.10) to calculate the load current yields

$$I_L = I_2 = \frac{N_1}{N_2}I_C$$

with the output ac power then calculated using

$$P_L = I_L^2(\text{rms})R_L$$

EXAMPLE 16.4

Calculate the ac power delivered to the 8-Ω speaker for the circuit of Fig. 16.10. The circuit component values result in a dc base current of 6 mA, and the input signal (V_i) results in a peak base current swing of 4 mA.

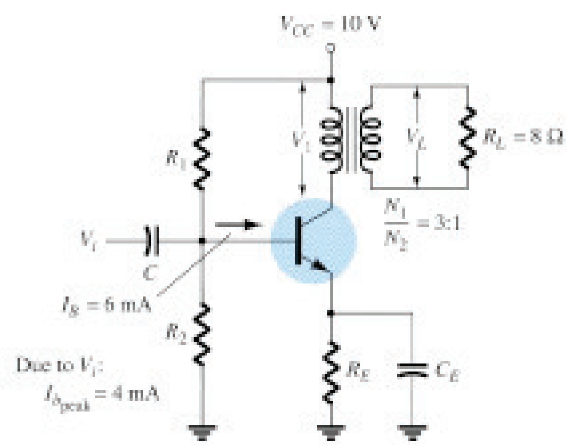

Figure 16.10 Transformer-coupled class A amplifier for Example 16.4.

Solution

The dc load line is drawn vertically (see Fig. 16.11) from the voltage point:

$$V_{CE_Q} = V_{CC} = 10 \text{ V}$$

For $I_B = 6$ mA, the operating point on Fig. 16.11 is

$$V_{CE_Q} = 10 \text{ V} \qquad \text{and} \qquad I_{C_Q} = 140 \text{ mA}$$

The effective ac resistance seen at the primary is

$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = (3)^2(8) = 72\ \Omega$$

The ac load line can then be drawn of slope −1/72 going through the indicated operating point. To help draw the load line, consider the following procedure. For a current swing of

P_L

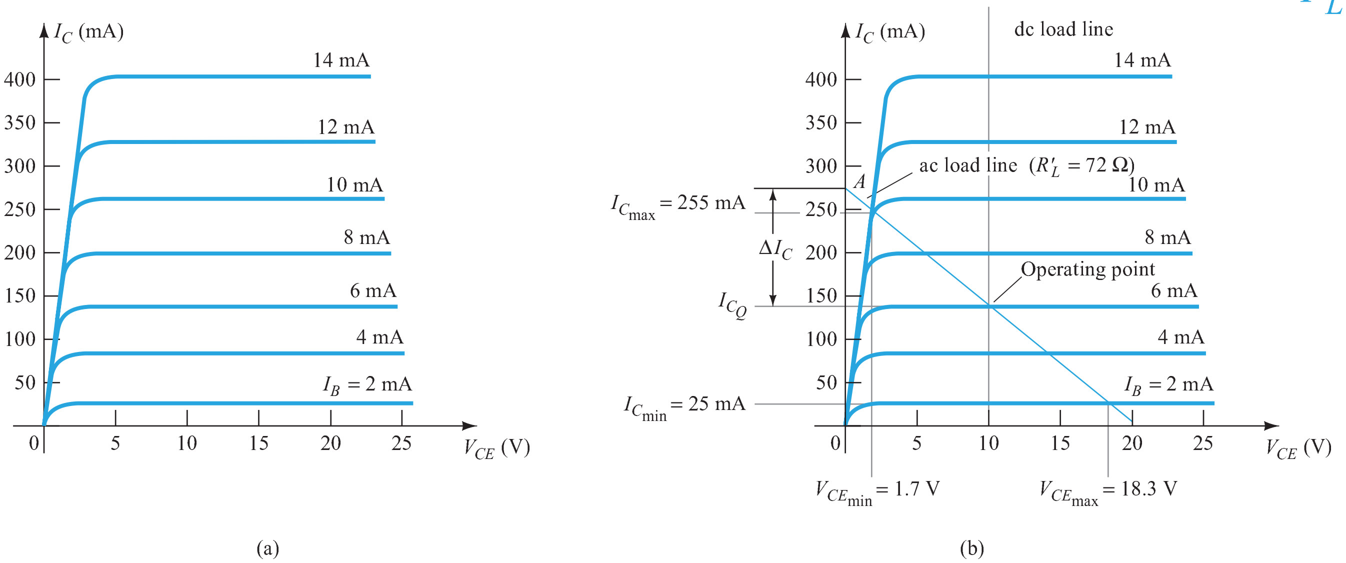

Figure 16.11 Transformer-coupled class A transistor characteristic for Examples 16.4 and 16.5: (a) device characteristic; (b) dc and ac load lines.

$$I_C = \frac{V_{CE}}{R'_L} = \frac{10\text{ V}}{72\ \Omega} = 139\text{ mA}$$

mark a point (A):

$$I_{CE_Q} + I_C = 140\text{ mA} + 139\text{ mA} = 279\text{ mA along the } y\text{-axis}$$

Connect point A through the Q-point to obtain the ac load line. For the given base current swing of 4 mA peak, the maximum and minimum collector current and collector–emitter voltage obtained from Fig. 16.11 are

$$V_{CE_{min}} = 1.7\text{ V} \qquad I_{C_{min}} = 25\text{ mA}$$

$$V_{CE_{max}} = 18.3\text{ V} \qquad I_{C_{max}} = 255\text{ mA}$$

The ac power delivered to the load can then be calculated using Eq. (16.13):

$$P_o\text{ (ac)} = \frac{(V_{CE_{max}} - V_{CE_{min}})(I_{C_{max}} - I_{C_{min}})}{8}$$

$$= \frac{(18.3\text{ V} - 1.7\text{ V})(255\text{ mA} - 25\text{ mA})}{8} = \mathbf{0.477\ W}$$

Efficiency

So far we have considered calculating the ac power delivered to the load. We next consider the input power from the battery, power losses in the amplifier, and the overall power efficiency of the transformer-coupled class A amplifier.

The input (dc) power obtained from the supply is calculated from the supply dc voltage and the average power drawn from the supply:

$$P_i(\text{dc}) = V_{CC} I_{C_Q} \tag{16.14}$$

For the transformer-coupled amplifier, the power dissipated by the transformer is small (due to the small dc resistance of a coil) and will be ignored in the present calculations. Thus the only power loss considered here is that dissipated by the power tran-

P_L

sistor and calculated using

$$P_Q = P_i(\text{dc}) - P_o(\text{ac}) \tag{16.15}$$

where P_Q is the power dissipated as heat. While the equation is simple, it is nevertheless significant when operating a class A amplifier. The amount of power dissipated by the transistor is the difference between that drawn from the dc supply (set by the bias point) and the amount delivered to the ac load. When the input signal is very small, with very little ac power delivered to the load, the maximum power is dissipated by the transistor. When the input signal is larger and power delivered to the load is larger, less power is dissipated by the transistor. In other words, the transistor of a class A amplifier has to work hardest (dissipate the most power) when the load is disconnected from the amplifier, and the transistor dissipates least power when the load is drawing maximum power from the circuit.

EXAMPLE 16.5

For the circuit of Fig. 16.10 and results of Example 16.4, calculate the dc input power, power dissipated by the transistor, and efficiency of the circuit for the input signal of Example 16.4.

Solution

$$\text{Eq. (16.14):}\quad P_i(\text{dc}) = V_{CC}I_{C_Q} = (10\text{ V})(140\text{ mA}) = \mathbf{1.4\ W}$$

$$\text{Eq. (16.15):}\quad P_Q = P_i(\text{dc}) - P_o(\text{ac}) = 1.4\text{ W} - 0.477\text{ W} = \mathbf{0.92\ W}$$

The efficiency of the amplifier is then

$$\%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.477\text{ W}}{1.4\text{ W}} \times 100\% = \mathbf{34.1\%}$$

MAXIMUM THEORETICAL EFFICIENCY

For a class A transformer-coupled amplifier, the maximum theoretical efficiency goes up to 50%. Based on the signals obtained using the amplifier, the efficiency can be expressed as

$$\%\ \eta = 50\left(\frac{V_{CE_{\max}} - V_{CE_{\min}}}{V_{CE_{\max}} + V_{CE_{\min}}}\right)^2 \% \tag{16.16}$$

The larger the value of $V_{CE_{\max}}$ and the smaller the value of $V_{CE_{\min}}$, the closer the efficiency approaches the theoretical limit of 50%.

EXAMPLE 16.6

Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 12 V and outputs of:

(a) $V(\text{p}) = 12$ V.
(b) $V(\text{p}) = 6$ V.
(c) $V(\text{p}) = 2$ V.

Solution

Since $V_{CE_Q} = V_{CC} = 12$ V, the maximum and minimum of the voltage swing are

(a) $V_{CE_{\max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 12\text{ V} = 24\text{ V}$
$V_{CE_{\min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 12\text{ V} = 0\text{ V}$

resulting in

P_L

$$\% \ \eta = 50\left(\frac{24\text{ V} - 0\text{ V}}{24\text{ V} + 0\text{ V}}\right)^2\% = \mathbf{50\%}$$

(b) $V_{CE_{\max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 6\text{ V} = 18\text{ V}$
$V_{CE_{\min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 6\text{ V} = 6\text{ V}$
resulting in

$$\% \ \eta = 50\left(\frac{18\text{ V} - 6\text{ V}}{18\text{ V} + 6\text{ V}}\right)^2\% = \mathbf{12.5\%}$$

(c) $V_{CE_{\max}} = V_{CE_Q} + V(\text{p}) = 12\text{ V} + 2\text{ V} = 14\text{ V}$
$V_{CE_{\min}} = V_{CE_Q} - V(\text{p}) = 12\text{ V} - 2\text{ V} = 10\text{ V}$
resulting in

$$\% \ \eta = 50\left(\frac{14\text{ V} - 10\text{ V}}{14\text{ V} + 10\text{ V}}\right)^2\% = \mathbf{1.39\%}$$

Notice how dramatically the amplifier efficiency drops from a maximum of 50% for $V(\text{p}) = V_{CC}$ to slightly over 1% for $V(\text{p}) = 2$ V.

16.4 CLASS B AMPLIFIER OPERATION

Class B operation is provided when the dc bias leaves the transistor biased just off, the transistor turning on when the ac signal is applied. This is essentially no bias, and the transistor conducts current for only one-half of the signal cycle. To obtain output for the full cycle of signal, it is necessary to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output signal. Since one part of the circuit pushes the signal high during one half-cycle and the other part pulls the signal low during the other half-cycle, the circuit is referred to as a *push-pull circuit.* Figure 16.12 shows a diagram for push-pull operation. An ac input signal is applied to the push-pull circuit, with each half operating on alternate half-cycles, the load then receiving a signal for the full ac cycle. The power transistors used in the push-pull circuit are capable of delivering the desired power to the load, and the class B operation of these transistors provides greater efficiency than was possible using a single transistor in class A operation.

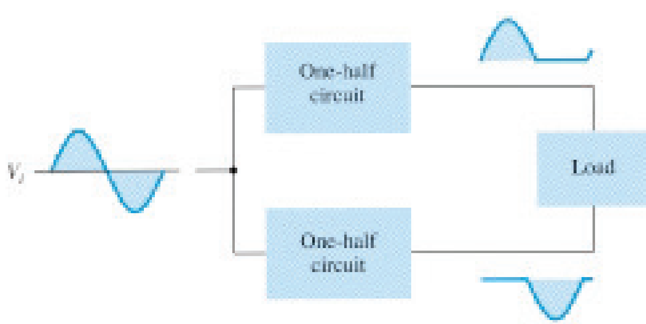

Figure 16.12 Block representation of push-pull operation.

Input (DC) Power

The power supplied to the load by an amplifier is drawn from the power supply (or power supplies; see Fig. 16.13) that provides the input or dc power. The amount of this input power can be calculated using

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} \tag{16.17}$$

P_L

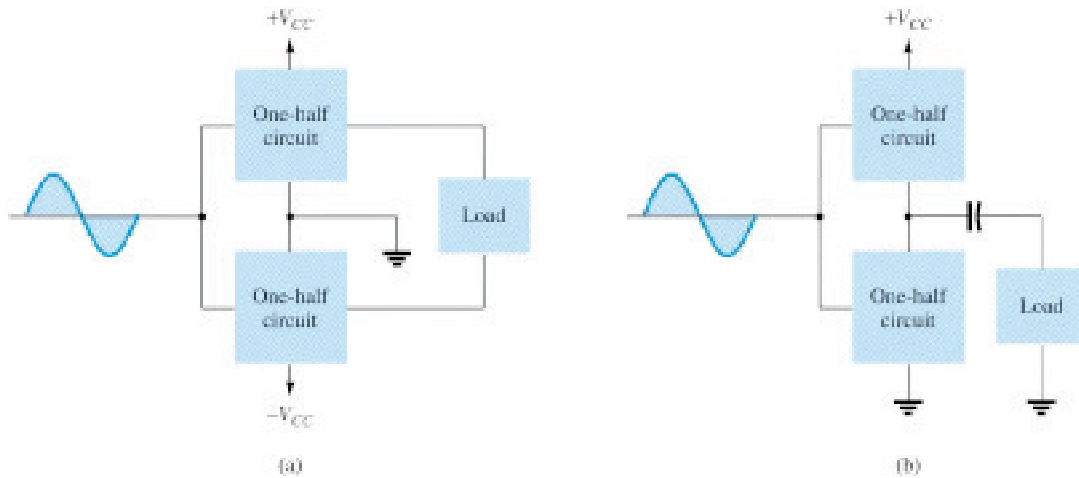

Figure 16.13 Connection of push-pull amplifier to load: (a) using two voltage supplies; (b) using one voltage supply.

where I_{dc} is the average or dc current drawn from the power supplies. In class B operation, the current drawn from a single power supply has the form of a full-wave rectified signal, while that drawn from two power supplies has the form of a half-wave rectified signal from each supply. In either case, the value of the average current drawn can be expressed as

$$I_{dc} = \frac{2}{\pi} I(\text{p}) \tag{16.18}$$

where $I(\text{p})$ is the peak value of the output current waveform. Using Eq. (16.18) in the power input equation (Eq. 16.17) results in

$$P_i(\text{dc}) = V_{CC}\left(\frac{2}{\pi} I(\text{p})\right) \tag{16.19}$$

Output (AC) Power

The power delivered to the load (usually referred to as a resistance, R_L) can be calculated using any one of a number of equations. If one is using an rms meter to measure the voltage across the load, the output power can be calculated as

$$P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L} \tag{16.20}$$

If one is using an oscilloscope, the peak, or peak-to-peak, output voltage measured can be used:

$$P_o(\text{ac}) = \frac{V_L^2(\text{p-p})}{8R_L} = \frac{V_L^2(\text{p})}{2R_L} \tag{16.21}$$

The larger the rms or peak output voltage, the larger the power delivered to the load.

Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation:

$$\%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Using Eqs. (16.19) and (16.21) in the efficiency equation above results in

$$\% \ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)I(\text{p})]} \times 100\% = \frac{\pi}{4}\frac{V_L(\text{p})}{V_{CC}} \times 100\% \qquad (16.22)$$

(using $I(\text{p}) = V_L(\text{p})/R_L$). Equation (16.22) shows that the larger the peak voltage, the higher the circuit efficiency, up to a maximum value when $V_L(\text{p}) = V_{CC}$, this maximum efficiency then being

$$\text{maximum efficiency} = \frac{\pi}{4} \times 100\% = 78.5\%$$

Power Dissipated by Output Transistors

The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load.

$$P_{2Q} = P_i(\text{dc}) - P_o(\text{ac}) \qquad (16.23)$$

where P_{2Q} is the power dissipated by the two output power transistors. The dissipated power handled by each transistor is then

$$P_Q = \frac{P_{2Q}}{2} \qquad (16.24)$$

EXAMPLE 16.7

For a class B amplifier providing a 20-V peak signal to a 16-Ω load (speaker) and a power supply of $V_{CC} = 30$ V, determine the input power, output power, and circuit efficiency.

Solution

A 20-V peak signal across a 16-Ω load provides a peak load current of

$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{20 \text{ V}}{16 \ \Omega} = 1.25 \text{ A}$$

The dc value of the current drawn from the power supply is then

$$I_{\text{dc}} = \frac{2}{\pi}I_L(\text{p}) = \frac{2}{\pi}(1.25 \text{ A}) = 0.796 \text{ A}$$

and the input power delivered by the supply voltage is

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} = (30 \text{ V})(0.796 \text{ A}) = \mathbf{23.9 \ W}$$

The output power delivered to the load is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(20 \text{ V})^2}{2(16 \ \Omega)} = \mathbf{12.5 \ W}$$

for a resulting efficiency of

$$\% \ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{12.5 \text{ W}}{23.9 \text{ W}} \times 100\% = \mathbf{52.3\%}$$

Maximum Power Considerations

For class B operation, the maximum output power is delivered to the load when $V_L(\text{p}) = V_{CC}$:

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} \tag{16.25}$$

The corresponding peak ac current $I(\text{p})$ is then

$$I(\text{p}) = \frac{V_{CC}}{R_L}$$

so that the maximum value of average current from the power supply is

$$\text{maximum } I_{\text{dc}} = \frac{2}{\pi} I(\text{p}) = \frac{2V_{CC}}{\pi R_L}$$

Using this current to calculate the maximum value of input power results in

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_{\text{dc}}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L} \tag{16.26}$$

The maximum circuit efficiency for class B operation is then

$$\text{maximum } \% \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_{CC}^2/2R_L}{V_{CC}[(2/\pi)(V_{CC}/R_L)]} \times 100\%$$

$$= \frac{\pi}{4} \times 100\% = \mathbf{78.54\%} \tag{16.27}$$

When the input signal results in less than the maximum output signal swing, the circuit efficiency is less than 78.5%.

For class B operation, the maximum power dissipated by the output transistors does not occur at the maximum power input or output condition. The maximum power dissipated by the two output transistors occurs when the output voltage across the load is

$$V_L(\text{p}) = 0.636 V_{CC} \qquad \left(= \frac{2}{\pi} V_{CC}\right)$$

for a maximum transistor power dissipation of

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} \tag{16.28}$$

EXAMPLE 16.8 For a class B amplifier using a supply of $V_{CC} = 30$ V and driving a load of 16 Ω, determine the maximum input power, output power, and transistor dissipation.

Solution

The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(30\text{ V})^2}{2(16\ \Omega)} = \mathbf{28.125\ W}$$

The maximum input power drawn from the voltage supply is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi RL} = \frac{2(30\text{ V})^2}{\pi(16\ \Omega)} = \mathbf{35.81\ W}$$

The circuit efficiency is then

$$\text{maximum } \%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{28.125\text{ W}}{35.81\text{ W}} \times 100\% = 78.54\%$$

as expected. The maximum power dissipated by each transistor is

$$\text{maximum } P_Q = \frac{\text{maximum } P_{2Q}}{2} = 0.5\left(\frac{2V_{CC}^2}{\pi^2 R_L}\right) = 0.5\left[\frac{2(30\text{ V})^2}{\pi^2 16\ \Omega}\right] = \mathbf{5.7\ W}$$

Under maximum conditions a pair of transistors, each handling 5.7 W at most, can deliver 28.125 W to a 16-Ω load while drawing 35.81 W from the supply.

The maximum efficiency of a class B amplifier can also be expressed as follows:

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L}$$

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} = V_{CC}\left[\frac{2V_L(\text{p})}{\pi R_L}\right]$$

so that

$$\%\ \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\ \% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)(V_L(\text{p})/R_L)]} \times 100\%$$

$$= 78.54\frac{V_L(\text{p})}{V_{CC}}\% \qquad (16.29)$$

EXAMPLE 16.9

Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 24$ V with peak output voltages of:

(a) $V_L(\text{p}) = 22$ V.

(b) $V_L(\text{p}) = 6$ V.

Solution

Using Eq. (16.29) gives

(a) $\%\ \eta = 78.54\,\frac{V_L(\text{p})}{V_{CC}}\% = 78.54\left(\frac{22\text{ V}}{24\text{ V}}\right) = \mathbf{72\%}$

(b) $\%\ \eta = 78.54\left(\frac{6\text{ V}}{24\text{ V}}\right)\% = \mathbf{19.6\%}$

Notice that a voltage near the maximum [22 V in part (a)] results in an efficiency near the maximum, while a small voltage swing [6 V in part (b)] still provides an efficiency near 20%. Similar power supply and signal swings would have resulted in much poorer efficiency in a class A amplifier.

16.5 CLASS B AMPLIFIER CIRCUITS

A number of circuit arrangements for obtaining class B operation are possible. We will consider the advantages and disadvantages of a number of the more popular circuits in this section. The input signals to the amplifier could be a single signal, the circuit then providing two different output stages, each operating for one-half the cycle. If the input is in the form of two opposite polarity signals, two similar stages could be used, each operating on the alternate cycle because of the input signal. One means of obtaining polarity or phase inversion is using a transformer, the transformer-coupled amplifier having been very popular for a long time. Opposite polarity inputs can easily be obtained using an op-amp having two opposite outputs or using a few op-amp stages to obtain two opposite polarity signals. An opposite polarity operation can also be achieved using a single input and complementary transistors (*npn* and *pnp*, or *n*MOS and *p*MOS).

Figure 16.14 shows different ways to obtain phase-inverted signals from a single input signal. Figure 16.14a shows a center-tapped transformer to provide opposite phase signals. If the transformer is exactly center-tapped, the two signals are exactly

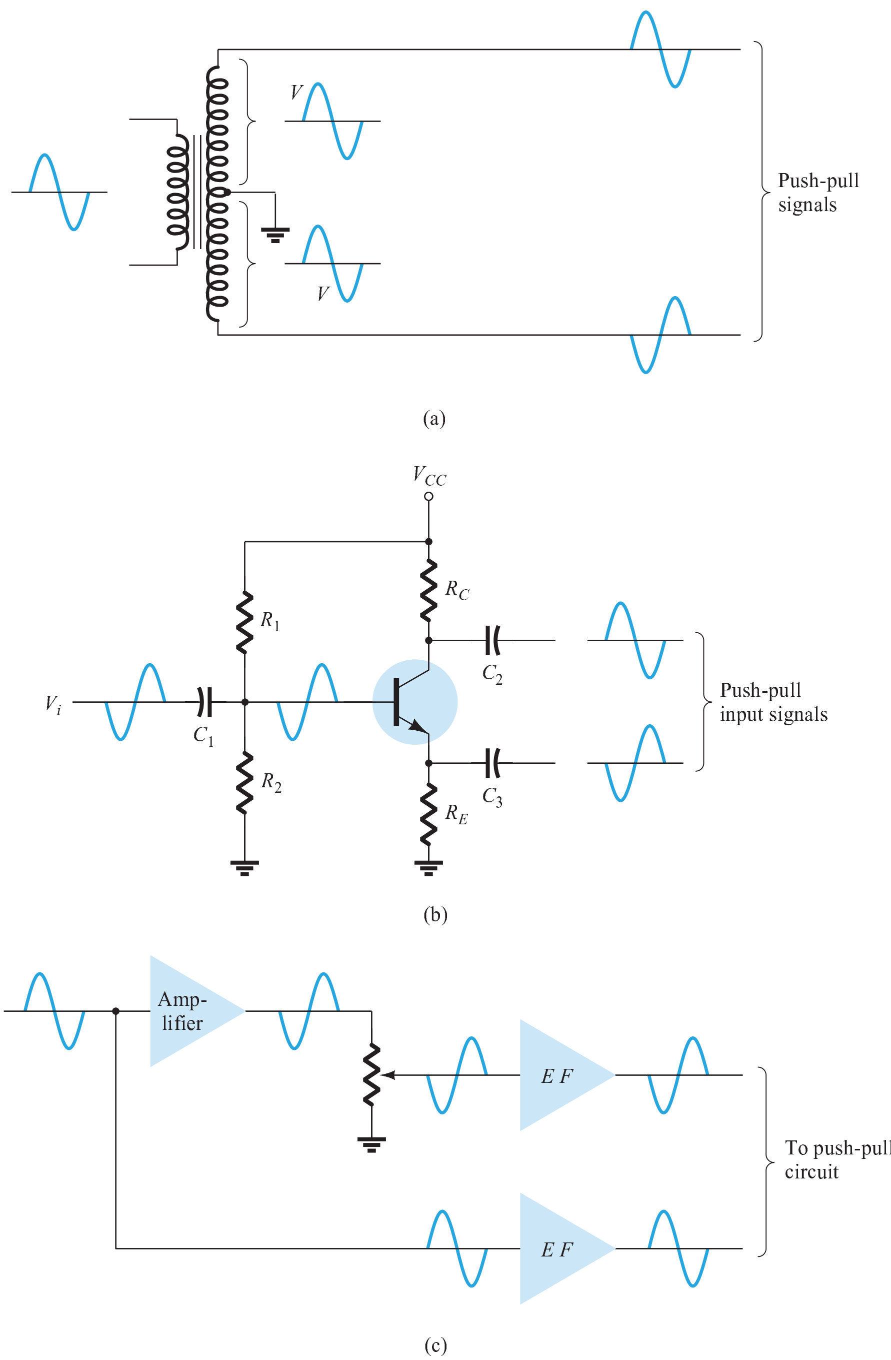

Figure 16.14 Phase-splitter circuits.

P_L

opposite in phase and of the same magnitude. The circuit of Fig. 16.14b uses a BJT stage with in-phase output from the emitter and opposite phase output from the collector. If the gain is made nearly 1 for each output, the same magnitude results. Probably most common would be using op-amp stages, one to provide an inverting gain of unity and the other a noninverting gain of unity, to provide two outputs of the same magnitude but of opposite phase.

Transformer-Coupled Push–Pull Circuits

The circuit of Fig. 16.15 uses a center-tapped input transformer to produce opposite polarity signals to the two transistor inputs and an output transformer to drive the load in a push-pull mode of operation described next.

During the first half-cycle of operation, transistor Q_1 is driven into conduction whereas transistor Q_2 is driven off. The current I_1 through the transformer results in the first half-cycle of signal to the load. During the second half-cycle of the input signal, Q_2 conducts whereas Q_1 stays off, the current I_2 through the transformer resulting in the second half-cycle to the load. The overall signal developed across the load then varies over the full cycle of signal operation.

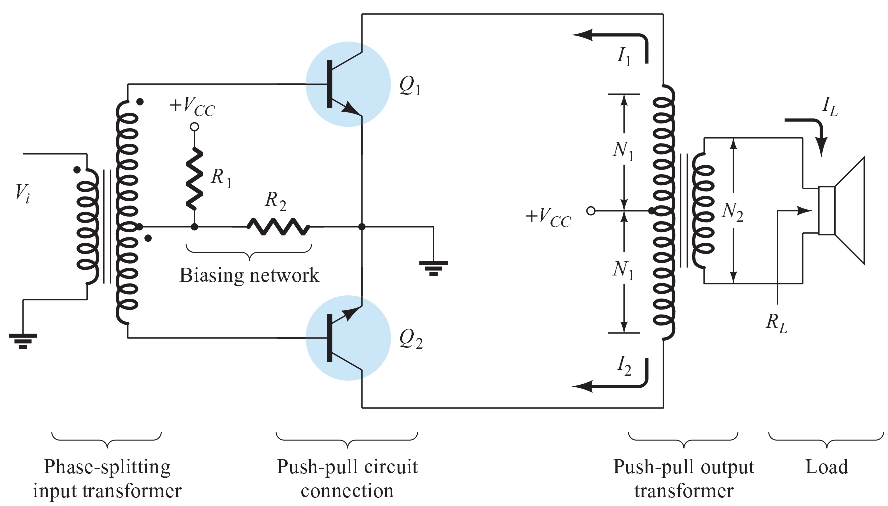

Figure 16.15 Push-pull circuit.

Complementary-Symmetry Circuits

Using complementary transistors (*npn* and *pnp*) it is possible to obtain a full cycle output across a load using half-cycles of operation from each transistor, as shown in Fig. 16.16a. While a single input signal is applied to the base of both transistors, the transistors, being of opposite type, will conduct on opposite half-cycles of the input. The *npn* transistor will be biased into conduction by the positive half-cycle of signal, with a resulting half-cycle of signal across the load as shown in Fig. 16.16b. During the negative half-cycle of signal, the *pnp* transistor is biased into conduction when the input goes negative, as shown in Fig. 16.16c.

During a complete cycle of the input, a complete cycle of output signal is developed across the load. One disadvantage of the circuit is the need for two separate voltage supplies. Another, less obvious disadvantage with the complementary circuit is shown in the resulting crossover distortion in the output signal (see Fig. 16.16d). *Crossover distortion* refers to the fact that during the signal crossover from positive to negative (or vice versa) there is some nonlinearity in the output signal. This results from the fact that the circuit does not provide exact switching of one transistor off and the other on at the zero-voltage condition. Both transistors may be partially off

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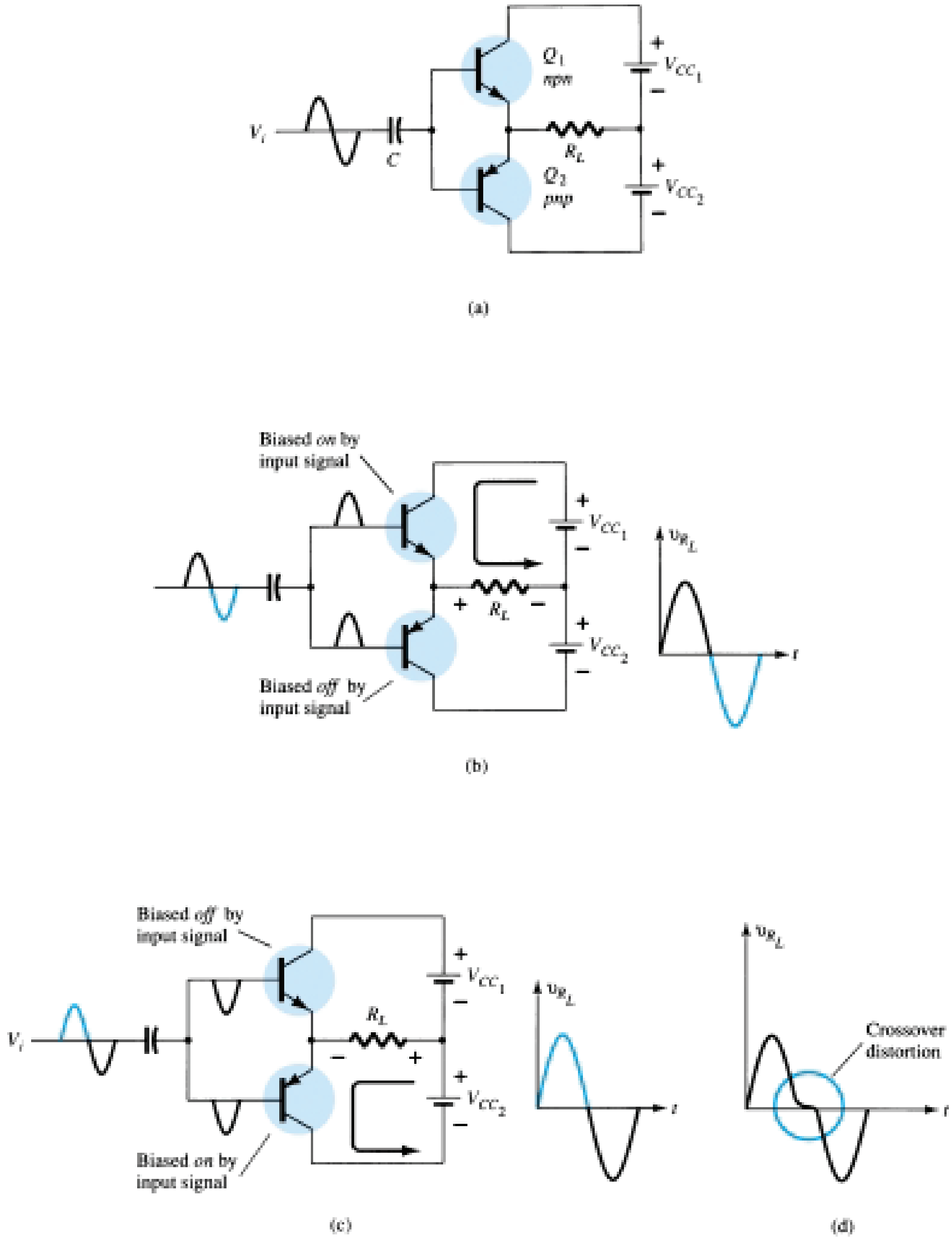

Figure 16.16 Complementary-symmetry push-pull circuit.

so that the output voltage does not follow the input around the zero-voltage condition. Biasing the transistors in class AB improves this operation by biasing both transistors to be on for more than half a cycle.

A more practical version of a push-pull circuit using complementary transistors is shown in Fig. 16.17. Note that the load is driven as the output of an emitter-follower so that the load resistance of the load is matched by the low output resistance of the driving source. The circuit uses complementary Darlington-connected transistors to provide higher output current and lower output resistance.

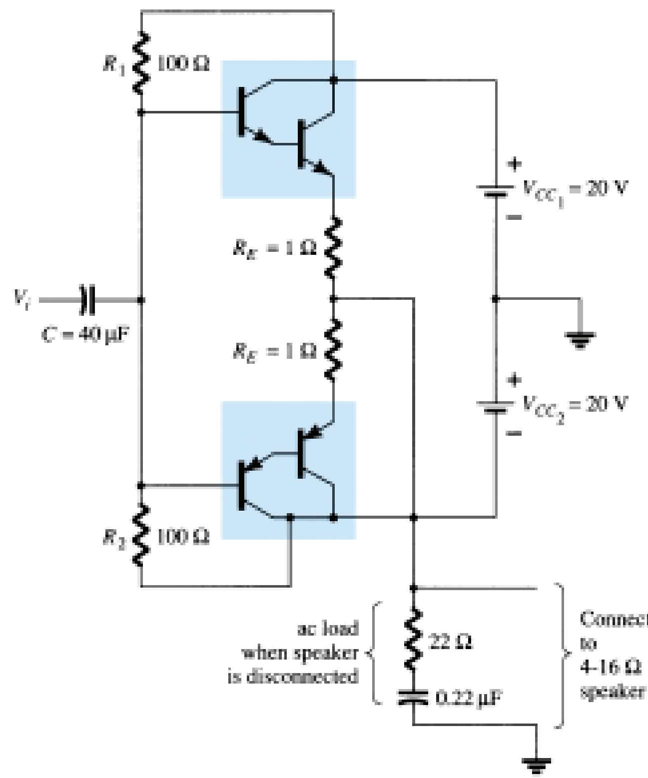

Figure 16.17 Complementary-symmetry push-pull circuit using Darlington transistors.

Quasi-Complementary Push–Pull Amplifier

In practical power amplifier circuits, it is preferable to use *npn* transistors for both high-current-output devices. Since the push-pull connection requires complementary devices, a *pnp* high-power transistor must be used. A practical means of obtaining complementary operation while using the same, matched *npn* transistors for the output is provided by a quasi-complementary circuit, as shown in Fig. 16.18. The push-

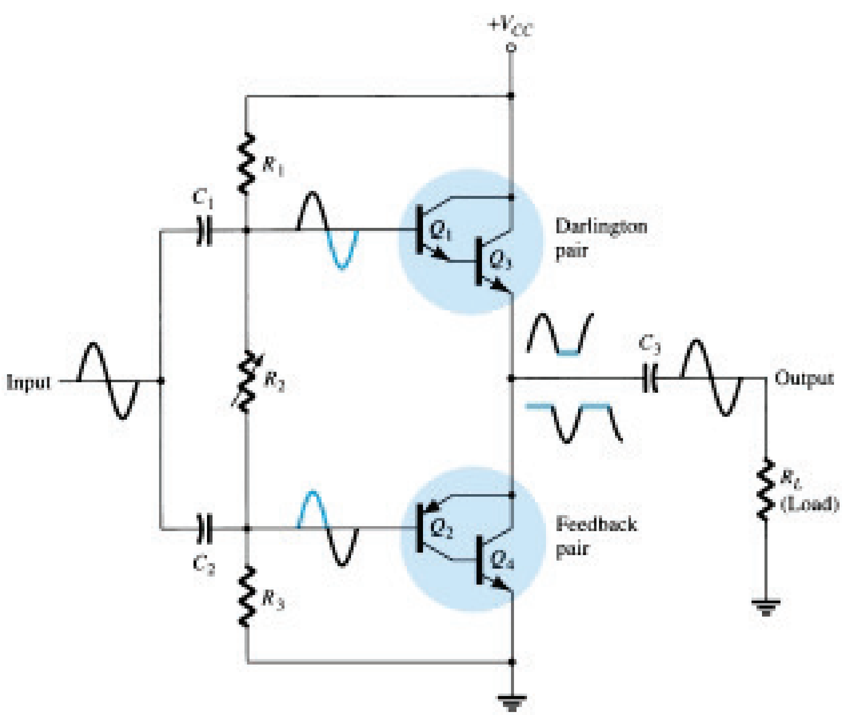

Figure 16.18 Quasi-complementary push-pull transformerless power amplifier.

pull operation is achieved by using complementary transistors (Q_1 and Q_2) before the matched *npn* output transistors (Q_3 and Q_4). Notice that transistors Q_1 and Q_3 form a Darlington connection that provides output from a low-impedance emitter-follower. The connection of transistors Q_2 and Q_4 forms a feedback pair, which similarly provides a low-impedance drive to the load. Resistor R_2 can be adjusted to minimize crossover distortion by adjusting the dc bias condition. The single input signal applied to the push-pull stage then results in a full cycle output to the load. The quasi-complementary push-pull amplifier is presently the most popular form of power amplifier.

EXAMPLE 16.10 For the circuit of Fig. 16.19, calculate the input power, output power, and power handled by each output transistor and the circuit efficiency for an input of 12 V rms.

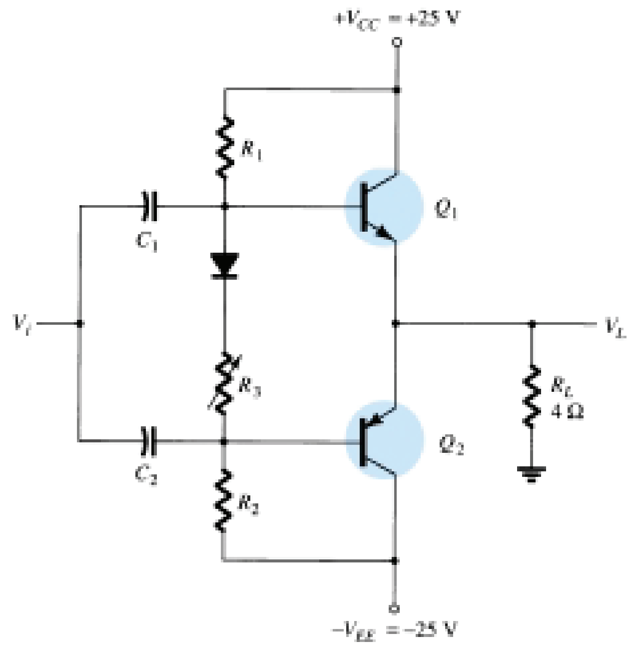

Figure 16.19 Class B power amplifier for Examples 16.10 thru 16.12.

Solution

The peak input voltage is

$$V_i(\text{p}) = \sqrt{2}\, V_i\,(\text{rms}) = \sqrt{2}\,(12\text{ V}) = 16.97\text{ V} \approx 17\text{ V}$$

Since the resulting voltage across the load is ideally the same as the input signal (the amplifier has, ideally, a voltage gain of unity),

$$V_L(\text{p}) = 17\text{ V}$$

and the output power developed across the load is

$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(17\text{ V})^2}{2(4\ \Omega)} = \mathbf{36.125\ W}$$

The peak load current is

$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{17\text{ V}}{4\ \Omega} = 4.25\text{ A}$$

from which the dc current from the supplies is calculated to be

$$I_{\text{dc}} = \frac{2}{\pi} I_L(\text{p}) = \frac{2(4.25\text{ A})}{\pi} = 2.71\text{ A}$$

so that the power supplied to the circuit is

$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} = (25 \text{ V})(2.71 \text{ A}) = \mathbf{67.75 \text{ W}}$$

The power dissipated by each output transistor is

$$P_Q = \frac{P_{2Q}}{2} = \frac{P_i - P_o}{2} = \frac{67.75 \text{ W} - 36.125 \text{ W}}{2} = \mathbf{15.8 \text{ W}}$$

The circuit efficiency (for the input of 12 V, rms) is then

$$\% \eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125 \text{ W}}{67.75 \text{ W}} \times 100\% = \mathbf{53.3\%}$$

EXAMPLE 16.11

For the circuit of Fig. 16.19, calculate the maximum input power, maximum output power, input voltage for maximum power operation, and the power dissipated by the output transistors at this voltage.

Solution

The maximum input power is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi R_L} = \frac{2(25 \text{ V})^2}{\pi 4 \ \Omega} = \mathbf{99.47 \text{ W}}$$

The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(25 \text{ V})^2}{2(4 \ \Omega)} = \mathbf{78.125 \text{ W}}$$

[Note that the maximum efficiency is achieved:]

$$\% \eta = \frac{P_o}{P_i} \times 100\% = \frac{78.125 \text{ W}}{99.47 \text{ W}} 100\% = 78.54\%$$

To achieve maximum power operation the output voltage must be

$$V_L(\text{p}) = V_{CC} = 25 \text{ V}$$

and the power dissipated by the output transistors is then

$$P_{2Q} = P_i - P_o = 99.47 \text{ W} - 78.125 \text{ W} = \mathbf{21.3 \text{ W}}$$

EXAMPLE 16.12

For the circuit of Fig. 16.19, determine the maximum power dissipated by the output transistors and the input voltage at which this occurs.

Solution

The maximum power dissipated by both output transistors is

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} = \frac{2(25 \text{ V})^2}{\pi^2 4 \ \Omega} = \mathbf{31.66 \text{ W}}$$

This maximum dissipation occurs at

$$V_L = 0.636V_L(\text{p}) = 0.636(25 \text{ V}) = \mathbf{15.9 \text{ V}}$$

(Notice that at $V_L = 15.9$ V the circuit required the output transistors to dissipate 31.66 W, while at $V_L = 25$ V they only had to dissipate 21.3 W.)

P_L

16.6 AMPLIFIER DISTORTION

A pure sinusoidal signal has a single frequency at which the voltage varies positive and negative by equal amounts. Any signal varying over less than the full 360° cycle is considered to have distortion. An ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version, the resulting waveform being a pure single-frequency sinusoidal signal. When distortion occurs the output will not be an exact duplicate (except for magnitude) of the input signal.

Distortion can occur because the device characteristic is not linear, in which case nonlinear or amplitude distortion occurs. This can occur with all classes of amplifier operation. Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

One technique for describing distorted but period waveforms uses Fourier analysis, a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples—these components are called *harmonic components* or *harmonics.* For example, a signal that is originally 1000 Hz could result, after distortion, in a frequency component at 1000 Hz (1 kHz) and harmonic components at 2 kHz (2 × 1 kHz), 3 kHz (3 × 1 kHz), 4 kHz (4 × 1 kHz), and so on. The original frequency of 1 kHz is called the *fundamental frequency;* those at integer multiples are the harmonics. The 2-kHz component is therefore called a *second harmonic,* that at 3 kHz is the *third harmonic,* and so on. The fundamental frequency is not considered a harmonic. Fourier analysis does not allow for fractional harmonic frequencies—only integer multiples of the fundamental.

Harmonic Distortion

A signal is considered to have harmonic distortion when there are harmonic frequency components (not just the fundamental component). If the fundamental frequency has an amplitude, A_1, and the nth frequency component has an amplitude, A_n, a harmonic distortion can be defined as

$$\%\ n\text{th harmonic distortion} = \%\ D_n = \frac{|A_n|}{|A_1|} \times 100\% \qquad (16.30)$$

The fundamental component is typically larger than any harmonic component.

EXAMPLE 16.13

Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V, and fourth harmonic amplitude of 0.05 V.

Solution

Using Eq. (16.30) yields

$$\%\ D_2 = \frac{|A_2|}{|A_1|} \times 100\% = \frac{0.25\text{ V}}{2.5\text{ V}} \times 100\% = \mathbf{10\%}$$

$$\%\ D_3 = \frac{|A_3|}{|A_1|} \times 100\% = \frac{0.1\text{ V}}{2.5\text{ V}} \times 100\% = \mathbf{4\%}$$

$$\%\ D_4 = \frac{|A_4|}{|A_1|} \times 100\% = \frac{0.05\text{ V}}{2.5\text{ V}} \times 100\% = \mathbf{2\%}$$

TOTAL HARMONIC DISTORTION

When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based on the individual elements as combined by the relationship of the following equation:

$$\% \text{ THD} = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\% \tag{16.31}$$

where THD is total harmonic distortion.

EXAMPLE 16.14

Calculate the total harmonic distortion for the amplitude components given in Example 16.13.

Solution

Using the computed values of $D_2 = 0.10$, $D_3 = 0.04$, and $D_4 = 0.02$ in Eq. (16.31),

$$\begin{aligned}\% \text{ THD} &= \sqrt{D_2^2 + D_3^2 + D_4^2} \times 100\% \\ &= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100\% = 0.1095 \times 100\% \\ &= \mathbf{10.95\%}\end{aligned}$$

An instrument such as a spectrum analyzer would allow measurement of the harmonics present in the signal by providing a display of the fundamental component of a signal and a number of its harmonics on a display screen. Similarly, a wave analyzer instrument allows more precise measurement of the harmonic components of a distorted signal by filtering out each of these components and providing a reading of these components. In any case, the technique of considering any distorted signal as containing a fundamental component and harmonic components is practical and useful. For a signal occurring in class AB or class B, the distortion may be mainly even harmonics, of which the second harmonic component is the largest. Thus, although the distorted signal theoretically contains all harmonic components from the second harmonic up, the most important in terms of the amount of distortion in the classes presented above is the second harmonic.

SECOND HARMONIC DISTORTION

Figure 16.20 shows a waveform to use for obtaining second harmonic distortion. A collector current waveform is shown with the quiescent, minimum, and maximum signal levels, and the time at which they occur is marked on the waveform. The sig-

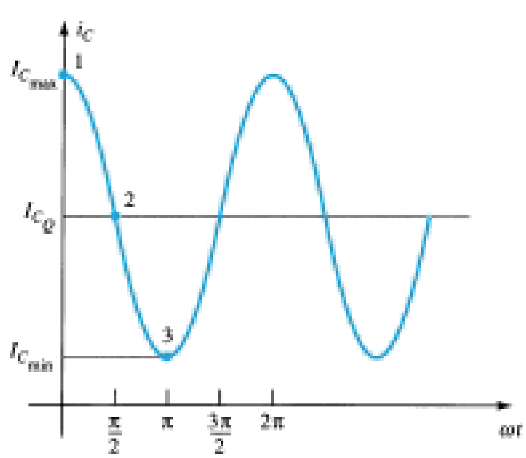

Figure 16.20 Waveform for obtaining second harmonic distortion.

P_L

nal shown indicates that some distortion is present. An equation that approximately describes the distorted signal waveform is

$$i_C \approx I_{C_Q} + I_0 + I_1 \cos \omega t + I_2 \cos \omega t \tag{16.32}$$

The current waveform contains the original quiescent current I_{C_Q}, which occurs with zero input signal; an additional dc current I_0, due to the nonzero average of the distorted signal; the fundamental component of the distorted ac signal, I_1; and a second harmonic component I_2, at twice the fundamental frequency. Although other harmonics are also present, only the second is considered here. Equating the resulting current from Eq. (16.32) at a few points in the cycle to that shown on the current waveform provides the following three relations:

At point 1 ($\omega t = 0$):

$$i_C = I_{C_{\text{max}}} = I_{C_Q} + I_0 + I_1 \cos 0 + I_2 \cos 0$$

$$I_{C_{\text{max}}} = I_{C_Q} + I_0 + I_1 + I_2$$

At point 2 ($\omega t = \pi/2$):

$$i_C = I_{C_Q} = I_{C_Q} + I_0 + I_1 \cos \frac{\pi}{2} + I_2 \cos \frac{2\pi}{2}$$

$$I_{C_Q} = I_{C_Q} + I_0 - I_2$$

At point 3 ($\omega t = \pi$):

$$i_C = I_{C\text{min}} = I_{C_Q} + I_0 + I_1 \cos \pi + I_2 \cos 2\pi$$

$$I_{C\text{min}} = I_{C_Q} + I_0 - I_1 + I_2$$

Solving the preceding three equations simultaneously gives the following results:

$$I_0 = I_2 = \frac{I_{C_{\text{max}}} + I_{C_{\text{min}}} - 2I_{C_Q}}{4}, \qquad I_1 = \frac{I_{C_{\text{max}}} - I_{C_{\text{min}}}}{2}$$

Referring to Eq. (16.30), the definition of second harmonic distortion may be expressed as

$$D_2 = \left|\frac{I_2}{I_1}\right| \times 100\%$$

Inserting the values of I_1 and I_2 determined above gives

$$D_2 = \left|\frac{\frac{1}{2}(I_{C_{\text{max}}} + I_{C_{\text{min}}}) - I_{C_Q}}{I_{C_{\text{max}}} - I_{C_{\text{min}}}}\right| \times 100\% \tag{16.33}$$

In a similar manner, the second harmonic distortion can be expressed in terms of measured collector–emitter voltages:

$$D_2 = \left|\frac{\frac{1}{2}(V_{CE_{\text{max}}} + V_{CE_{\text{min}}}) - V_{CE_Q}}{V_{CE_{\text{max}}} - V_{CE_{\text{min}}}}\right| \times 100\% \tag{16.34}$$

EXAMPLE 16.15

An output waveform displayed on an oscilloscope provides the following measurements:

(a) $V_{CE_{\text{min}}} = 1$ V, $V_{CE_{\text{max}}} = 22$ V, $V_{CE_Q} = 12$ V.
(b) $V_{CE_{\text{min}}} = 4$ V, $V_{CE_{\text{max}}} = 20$ V, $V_{CE_Q} = 12$ V.

Solution

Using Eq. (16.34), we get

(a) $$D_2 = \left|\frac{\frac{1}{2}(22\text{ V} + 1\text{ V}) - 12\text{ V}}{22\text{ V} - 1\text{ V}}\right| \times 100\% = \mathbf{2.38\%}$$

(b) $$D_2 = \left|\frac{\frac{1}{2}(20\text{ V} + 4\text{ V}) - 12\text{ V}}{20\text{ V} - 4\text{ V}}\right| \times 100\% = \mathbf{0\%} \qquad \text{(no distortion)}$$

Power of Signal Having Distortion

When distortion does occur, the output power calculated for the undistorted signal is no longer correct. When distortion is present, the output power delivered to the load resistor R_C due to the fundamental component of the distorted signal is

$$P_1 = \frac{I_1^2 R_C}{2} \tag{16.35}$$

The total power due to all the harmonic components of the distorted signal can then be calculated using

$$P = (I_1^2 + I_2^2 + I_3^2 + \cdots)\,\frac{R_C}{2} \tag{16.36}$$

The total power can also be expressed in terms of the total harmonic distortion,

$$P = (1 + D_2^2 + D_3^2 + \cdots)\, I_1^2 \frac{R_C}{2} = (1 + \text{THD}^2)P_1 \tag{16.37}$$

EXAMPLE 16.16

For harmonic distortion reading of $D_2 = 0.1$, $D_3 = 0.02$, and $D_4 = 0.01$, with $I_1 = 4$ A and $R_C = 8\ \Omega$, calculate the total harmonic distortion, fundamental power component, and total power.

Solution

The total harmonic distortion is

$$\text{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2} = \sqrt{(0.1)^2 + (0.02)^2 + (0.01)^2} \approx \mathbf{0.1}$$

The fundamental power, using Eq. (16.35), is

$$P_1 = \frac{I_1^2 R_C}{2} = \frac{(4\text{ A})^2(8\ \Omega)}{2} = \mathbf{64\ W}$$

The total power calculated using Eq. (16.37) is then

$$P = (1 + \text{THD}^2)P_1 = [1 + (0.1)^2]64 = (1.01)64 = \mathbf{64.64\ W}$$

(Note that the total power is due mainly to the fundamental component even with 10% second harmonic distortion.)

Graphical Description of Harmonic Components of Distorted Signal

A distorted waveform such as that which occurs in class B operation can be represented using Fourier analysis as a fundamental with harmonic components. Figure 16.21a shows a positive half-cycle such as the type that would result in one side of a

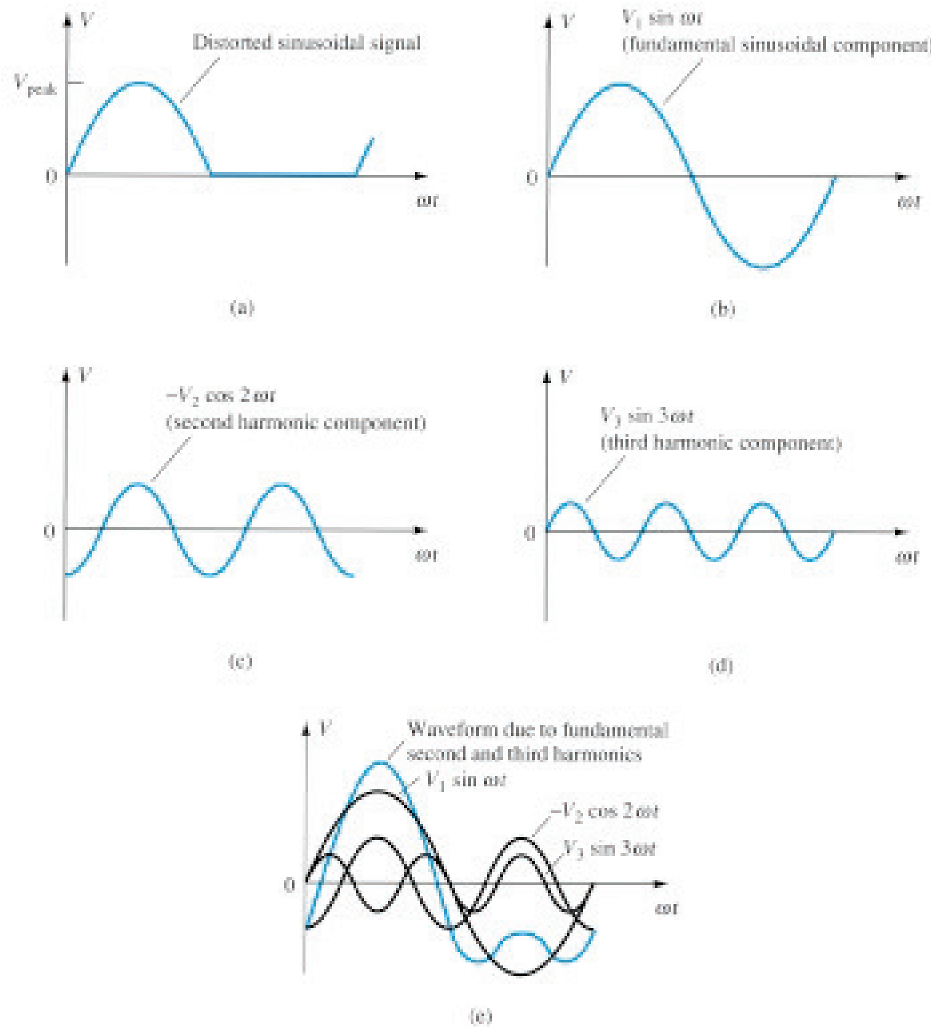

Figure 16.21 Graphical representation of a distorted signal through the use of harmonic components.

class B amplifier. Using Fourier analysis techniques, the fundamental component of the distorted signal can be obtained, as shown in Fig. 16.21b. Similarly, the second and third harmonic components can be obtained and are shown in Fig. 16.21c and d, respectively. Using the Fourier technique, the distorted waveform can be made by adding the fundamental and harmonic components, as shown in Fig. 16.21e. In general, any periodic distorted waveform can be represented by adding a fundamental component and all harmonic components, each of varying amplitude and at various phase angles.

16.7 POWER TRANSISTOR HEAT SINKING

While integrated circuits are used for small-signal and low-power applications, most high-power applications still require individual power transistors. Improvements in production techniques have provided higher power ratings in small-sized packaging cases, have increased the maximum transistor breakdown voltage, and have provided faster-switching power transistors.

The maximum power handled by a particular device and the temperature of the transistor junctions are related since the power dissipated by the device causes an increase in temperature at the junction of the device. Obviously, a 100-W transistor will provide more power capability than a 10-W transistor. On the other hand, proper heat-sinking techniques will allow operation of a device at about one-half its maximum power rating.

We should note that of the two types of bipolar transistors—germanium and silicon—silicon transistors provide greater maximum temperature ratings. Typically, the maximum junction temperature of these types of power transistors is

Silicon: 150–200°C

Germanium: 100–110°C

For many applications the average power dissipated may be approximated by

$$P_D = V_{CE} I_C \tag{16.38}$$

This power dissipation, however, is allowed only up to a maximum temperature. Above this temperature, the device power dissipation capacity must be reduced (or derated) so that at higher case temperatures the power-handling capacity is reduced, down to 0 W at the device maximum case temperature.

The greater the power handled by the transistor, the higher the case temperature. Actually, the limiting factor in power handling by a particular transistor is the temperature of the device's collector junction. Power transistors are mounted in large metal cases to provide a large area from which the heat generated by the device may radiate (be transferred). Even so, operating a transistor directly into air (mounting it on a plastic board, for example) severely limits the device power rating. If, instead (as is usual practice), the device is mounted on some form of heat sink, its power-handling capacity can approach the rated maximum value more closely. A few heat sinks are shown in Fig. 16.22. When the heat sink is used, the heat produced by the transistor dissipating power has a larger area from which to radiate (transfer) the heat into the air, thereby holding the case temperature to a much lower value than would result without the heat sink. Even with an infinite heat sink (which, of course, is not available), for which the case temperature is held at the ambient (air) temperature, the junction will be heated above the case temperature and a maximum power rating must be considered.

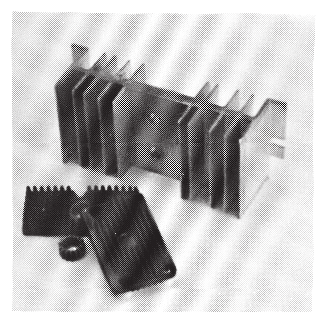

Figure 16.22 Typical power heat sinks.

Since even a good heat sink cannot hold the transistor case temperature at ambient (which, by the way, could be more than 25°C if the transistor circuit is in a confined area where other devices are also radiating a good amount of heat), it is necessary to derate the amount of maximum power allowed for a particular transistor as a function of increased case temperature.

Figure 16.23 shows a typical power derating curve for a silicon transistor. The curve shows that the manufacturer will specify an upper temperature point (not nec-

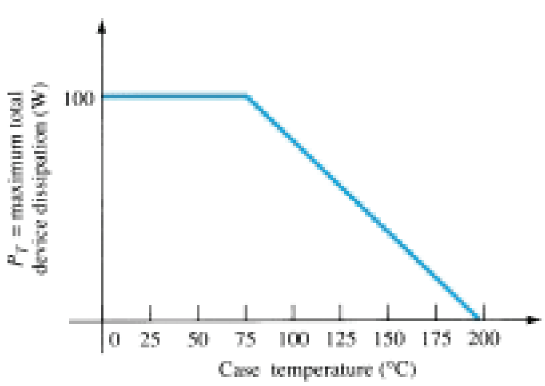

Figure 16.23 Typical power derating curve for silicon transistors.

essarily 25°C), after which a linear derating takes place. For silicon, the maximum power that should be handled by the device does not reduce to 0 W until the case temperature is 200°C.

It is not necessary to provide a derating curve since the same information could be given simply as a listed derating factor on the device specification sheet. Stated mathematically, we have

$$P_D(\text{temp}_1) = P_D(\text{temp}_0) - (\text{Temp}_1 - \text{Temp}_0)(\text{derating factor}) \qquad (16.39)$$

where the value of Temp_0 is the temperature at which derating should begin, the value of Temp_1 is the particular temperature of interest (above the value Temp_0), $P_D(\text{temp}_0)$ and $P_D(\text{temp}_1)$ are the maximum power dissipations at the temperatures specified, and the derating factor is the value given by the manufacturer in units of watts (or milliwatts) per degree of temperature.

EXAMPLE 16.17 Determine what maximum dissipation will be allowed for an 80-W silicon transistor (rated at 25°C) if derating is required above 25°C by a derating factor of 0.5 W/°C at a case temperature of 125°C.

Solution

$$P_D(125°\text{C}) = P_D(25°\text{C}) - (125°\text{C} - 25°\text{C})(0.5\text{ W/°C})$$
$$= 80\text{ W} - 100°\text{C}(0.5\text{ W/°C}) = \mathbf{30\text{ W}}$$

It is interesting to note what power rating results from using a power transistor without a heat sink. For example, a silicon transistor rated at 100 W at (or below) 100°C is rated only 4 W at (or below) 25°C, the free-air temperature. Thus, operated without a heat sink, the device can handle a maximum of only 4 W at the room temperature of 25°C. Using a heat sink large enough to hold the case temperature to 100°C at 100 W allows operating at the maximum power rating.

Thermal Analogy of Power Transistor

Selection of a suitable heat sink requires a considerable amount of detail that is not appropriate to our present basic considerations of the power transistor. However, more detail about the thermal characteristics of the transistor and its relation to the power dissipation of the transistor may help provide a clearer understanding of power as limited by temperature. The following discussion should prove useful.

A picture of how the junction temperature (T_J), case temperature (T_C), and ambient (air) temperature (T_A) are related by the device heat-handling capacity—a temperature coefficient usually called thermal resistance—is presented in the thermal-electric analogy shown in Fig. 16.24.

In providing a thermal-electrical analogy, the term *thermal resistance* is used to describe heat effects by an electrical term. The terms in Fig. 16.24 are defined as follows:

θ_{JA} = total thermal resistance (junction to ambient)

θ_{JC} = transistor thermal resistance (junction to case)

θ_{CS} = insulator thermal resistance (case to heat sink)

θ_{SA} = heat-sink thermal resistance (heat sink to ambient)

Using the electrical analogy for thermal resistances, we can write

$$\boxed{\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}} \qquad (16.40)$$

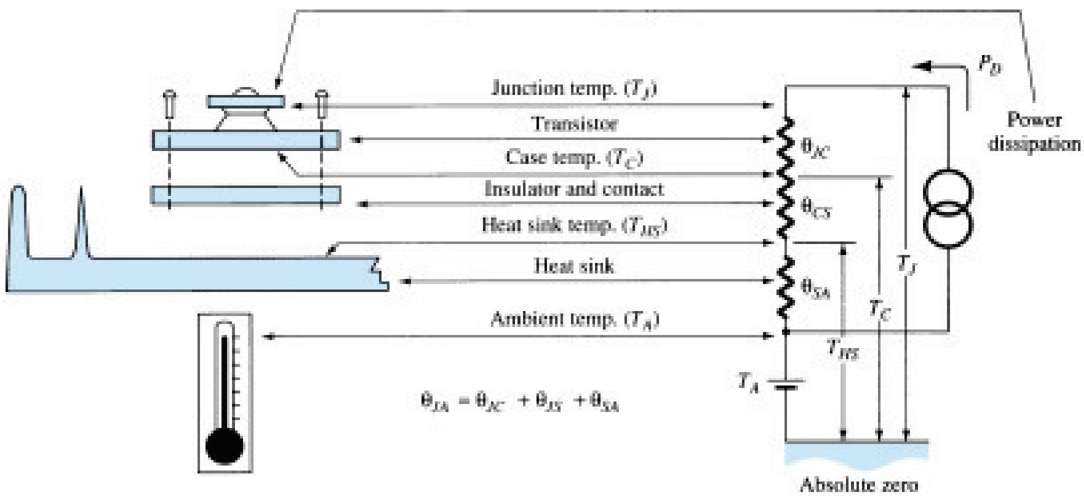

Figure 16.24 Thermal-to-electrical analogy.

The analogy can also be used in applying Kirchhoff's law to obtain

$$T_J = P_D\theta_{JA} + T_A \tag{16.41}$$

The last relation shows that the junction temperature "floats" on the ambient temperature and that the higher the ambient temperature, the lower the allowed value of device power dissipation.

The thermal factor θ provides information about how much temperature drop (or rise) results for a given amount of power dissipation. For example, the value of θ_{JC} is usually about 0.5°C/W. This means that for a power dissipation of 50 W, the difference in temperature between case temperature (as measured by a thermocouple) and the inside junction temperature is only

$$T_J - T_C = \theta_{JC}P_D = (0.5°\text{C/W})(50\text{ W}) = 25°\text{C}$$

Thus, if the heat sink can hold the case at, say, 50°C, the junction is then only at 75°C. This is a relatively small temperature difference, especially at lower power-dissipation levels.

The value of thermal resistance from junction to free air (using no heat sink) is, typically,

$$\theta_{JA} = 40°\text{C/W} \qquad \text{(into free air)}$$

For this thermal resistance, only 1 W of power dissipation results in a junction temperature 40°C greater than the ambient.

A heat sink can now be seen to provide a low thermal resistance between case and air—much less than the 40°C/W value of the transistor case alone. Using a heat sink having

$$\theta_{SA} = 2°\text{C/W}$$

and with an insulating thermal resistance (from case to heat sink) of

$$\theta_{CS} = 0.8°\text{C/W}$$

and finally, for the transistor,

$$\theta_{CJ} = 0.5°\text{C/W}$$

we can obtain

$$\begin{aligned}\theta_{JA} &= \theta_{SA} + \theta_{CS} + \theta_{CJ}\\ &= 2.0°\text{C/W} + 0.8°\text{C/W} + 0.5°\text{C/W} = 3.3°\text{C/W}\end{aligned}$$

P_L

So with a heat sink, the thermal resistance between air and the junction is only 3.3°C/W, compared to 40°C/W for the transistor operating directly into free air. Using the value of θ_{JA} above for a transistor operated at, say, 2 W, we calculate

$$T_J - T_A = \theta_{JA} P_D = (3.3°\text{C/W})(2\ \text{W}) = 6.6°\text{C}$$

In other words, the use of a heat sink in this example provides only a 6.6°C increase in junction temperature as compared to an 80°C rise without a heat sink.

EXAMPLE 16.18

A silicon power transistor is operated with a heat sink ($\theta_{SA} = 1.5°\text{C/W}$). The transistor, rated at 150 W (25°C), has $\theta_{JC} = 0.5°\text{C/W}$, and the mounting insulation has $\theta_{CS} = 0.6°\text{C/W}$. What maximum power can be dissipated if the ambient temperature is 40°C and $T_{J_{\max}} = 200°\text{C}$?

Solution

$$P_D = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} = \frac{200°\text{C} - 40°\text{C}}{0.5°\text{C/W} + 0.6°\text{C/W} + 1.5°\text{C/W}} \approx \mathbf{61.5\ W}$$

16.8 CLASS C AND CLASS D AMPLIFIERS

Although class A, class AB, and class B amplifiers are most used as power amplifiers, class D amplifiers are popular because of their very high efficiency. Class C amplifiers, while not used as audio amplifiers, do find use in tuned circuits as used in communications.

Class C Amplifier

A class C amplifier, as that shown in Fig. 16.25, is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output, however, will provide a full cycle of output signal for the fundamental or resonant frequency of the tuned circuit (*L* and *C* tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency, as occurs in a communications circuit, for example. Operation of a class C circuit is not intended primarily for large-signal or power amplifiers.

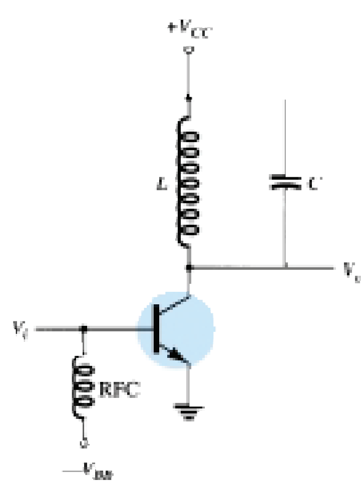

Figure 16.25 Class C amplifier circuit.

Class D Amplifier

A class D amplifier is designed to operate with digital or pulse-type signals. An efficiency of over 90% is achieved using this type of circuit, making it quite desirable in power amplifiers. It is necessary, however, to convert any input signal into a pulse-type waveform before using it to drive a large power load and to convert the signal back to a sinusoidal-type signal to recover the original signal. Figure 16.26 shows how a sinusoidal signal may be converted into a pulse-type signal using some form of sawtooth or chopping waveform to be applied with the input into a comparator-type op-amp circuit so that a representative pulse-type signal is produced. While the letter D is used to describe the next type of bias operation after class C, the D could also be considered to stand for "Digital," since that is the nature of the signals provided to the class D amplifier.

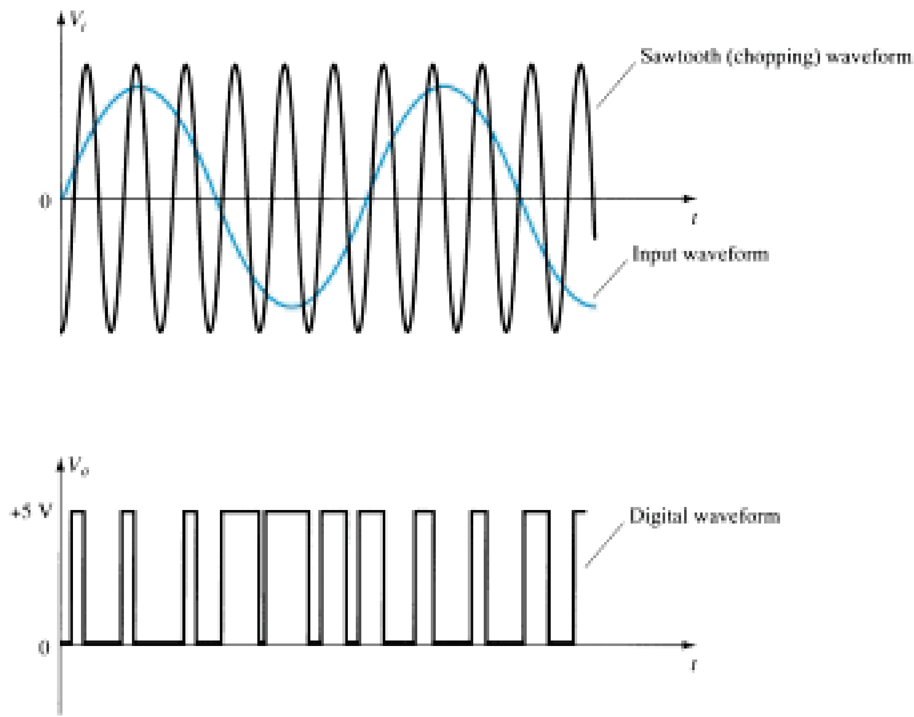

Figure 16.26 Chopping of sinusoidal waveform to produce digital waveform.

Figure 16.27 shows a block diagram of the unit needed to amplify the class D signal and then convert back to the sinusoidal-type signal using a low-pass filter. Since the amplifier's transistor devices used to provide the output are basically either off or on, they provide current only when they are turned on, with little power loss due to

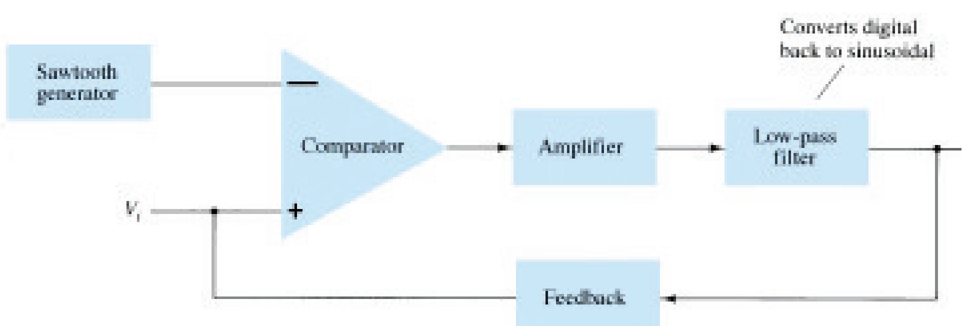

Figure 16.27 Block diagram of class D amplifier.

P_L

their low on-voltage. Since most of the power applied to the amplifier is transferred to the load, the efficiency of the circuit is typically very high. Power MOSFET devices have been quite popular as the driver devices for the class D amplifier.

16.9 PSPICE WINDOWS

Program 16.1—Series-Fed Class A Amplifier

Using Design Center, the circuit of a series-fed class A amplifier is drawn as shown in Fig. 16.28. Figure 16.29 shows some of the analysis output. Edit the transistor model for values of only **BF** = 90 and **IS** = 2E-15. This keeps the transistor model more ideal so that PSpice calculations better match those below.
The dc bias of the collector voltage is shown to be

$$V_c(\text{dc}) = 12.47 \text{ V}$$

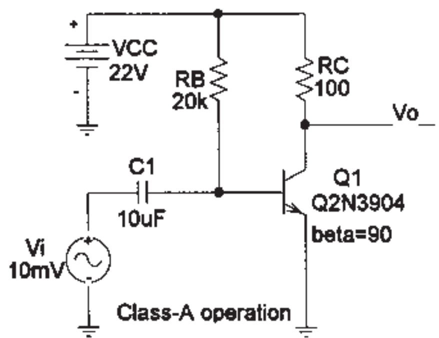

Figure 16.28 Series-fed class A amplifier.

```
Series-fed Class-A Amplifier

****    CIRCUIT DESCRIPTION
**************************************************

****    BJT MODEL PARAMETERS
           Q2N3904-X1
           NPN
        IS   2.000000E-15
        BF   90

****    SMALL SIGNAL BIAS SOLUTION
**************************************************
NODE   VOLTAGE          NODE   VOLTAGE           NODE   VOLTAGE
(  VL)         12.4670  ($N_0001)  22.0000       ($N_0002)   0.0000
($N_0003)       .8146

  VOLTAGE SOURCE CURRENTS
  NAME          CURRENT
  V_Vi          0.000E+00
  V_VCC         -9.639E-02
  TOTAL POWER DISSIPATION  2.12E+00  WATTS

**** BIPOLAR JUNCTION TRANSISTORS
NAME          Q_Q1
MODEL         Q2N3904-X1
IB            1.06E-03
IC            9.53E-02
VBE           8.15E-01
VBC           -1.17E+01
VCE           1.25E+01
BETADC        9.00E+01
GM            3.69E+00
RPI           2.44E+01
RO            1.00E+12
BETAAC        9.00E+01
FT            5.87E+19
```

Figure 16.29 Analysis output for the circuit of Fig. 16.28.

With transistor beta set to 90, the ac gain is calculated as follows:

$$I_E = I_c = 95 \text{ mA (from analysis output of PSpice)}$$

$$R_e = 26 \text{ mV}/95 \text{ mA} = 0.27 \ \Omega$$

For a gain of

$$A_V = -R_c/r_e = -100/0.27 = -370$$

The output voltage is then

$$V_o = A_v V_i = (-370) \cdot 10 \text{ mV} = -3.7 \text{ V(peak)}$$

The output waveform obtained using **probe** is shown in Fig. 16.30.

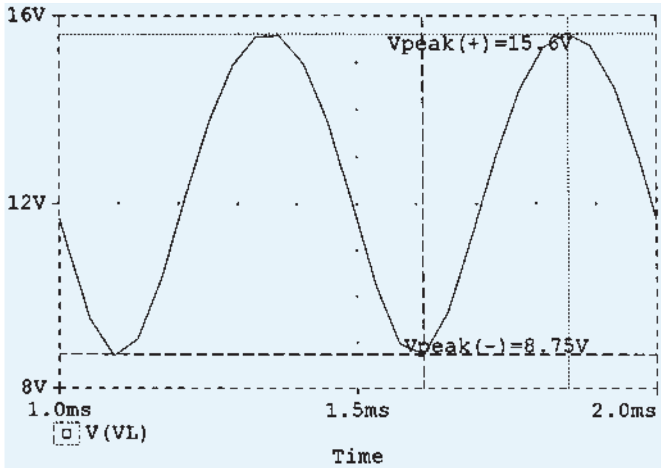

Figure 16.30 Probe output for the circuit of Fig. 16.28.

For a peak-to-peak output of

$$V_o(\text{p-p}) = 15.6\text{ V} - 8.75\text{ V} = 6.85\text{ V}$$

the peak output is

$$V_o(\text{p}) = 6.85\text{ V}/2 = 3.4\text{ V}$$

which compares well with that calculated above.
From the circuit output analysis, the input power is

$$P_i = V_{CC}I_C = (22\text{ V}) \cdot (95\text{ mA}) = 2.09\text{ W}$$

From the probe ac data, the output power is

$$P_o(\text{ac}) = V_o(\text{p-p})^2/[8 \cdot R_L] = (6.85)^2/[8 \cdot 100] = 58\text{ mW}$$

The efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (58\text{ mW}/2.09\text{ W}) \cdot 100\% = 2.8\%$$

A larger input signal would increase the ac power delivered to the load and increase the efficiency (the maximum being 25%).

Program 16.2—Quasi-Complementary Push-Pull Amplifier

Figure 16.31shows a quasi-complementary push-pull class B power amplifier. For the input of $V_i = 20$ V(p), the output waveform obtained using **probe** is shown in Fig. 16.32.

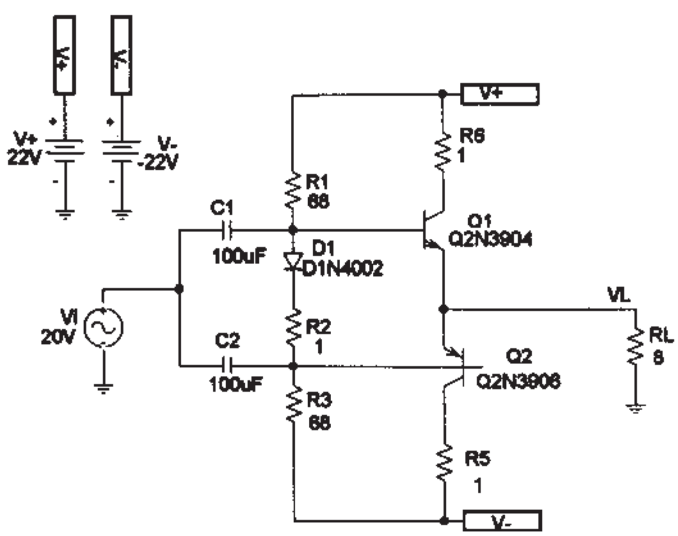

Figure 16.31 Quasi-complementary class B power amplifier.

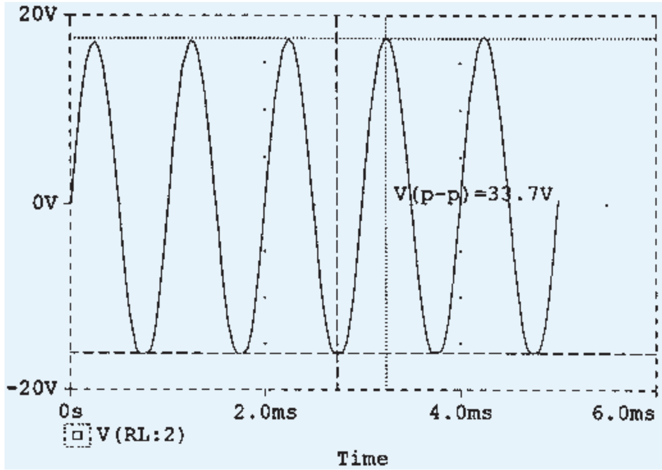

Figure 16.32 Probe output of the circuit in Fig. 16.31.

The resulting ac output voltage is seen to be

$$V_o(\text{p-p}) = 33.7\text{ V}$$

so that

$$P_o = V_o^2(\text{p-p})/(8 \cdot R_L) = (33.7\text{ V})^2/(8 \cdot 8\ \Omega) = 17.7\text{ W}$$

The input power for that amplitude signal is

$$P_i = V_{CC}I_{\text{dc}} = V_{CC}[(2/\pi)(V_o(\text{p-p})/2)R_L)]$$

$$= (22\text{ V}) \cdot [[(2/\pi)(33.7\text{ V}/2)/8] = 29.5\text{ W}$$

The circuit efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (17.7\text{ W}/29.5\text{ W}) \cdot 100\% = 60\%$$

Program 16.3—Op-Amp Push-Pull Amplifier

Figure 16.33 shows an op-amp push-pull amplifier providing ac output to an 8-Ω load.

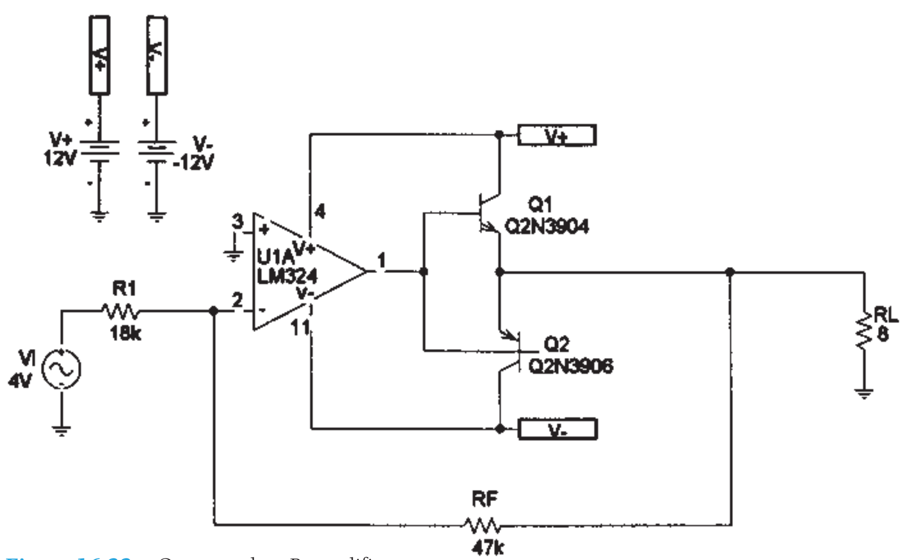

Figure 16.33 Op-amp class B amplifier.

P_L

As shown, the op-amp provides a gain of

$$A_v = -R_F/R_1 = -47\ \text{k}\Omega/18\ \text{k}\Omega = -2.6$$

For the input, V_i 1 V, the output is

$$V_o(\text{p}) = A_v V_i = -2.6 \cdot (1\ \text{V}) = -2.6\ \text{V}$$

Figure 16.34 shows the **PROBE** display of the output voltage.

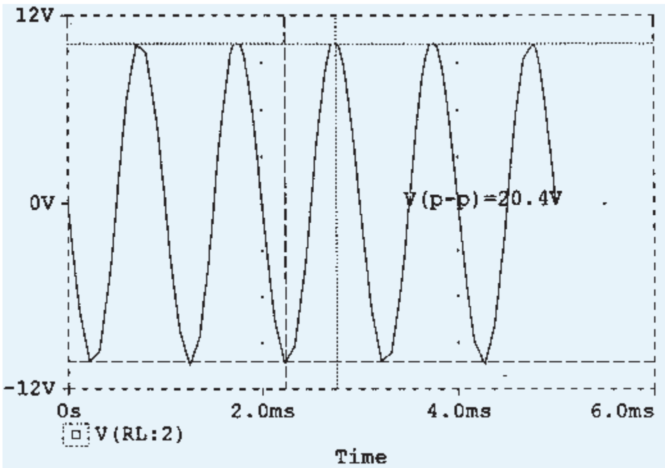

Figure 16.34 Probe output for the circuit of Fig. 16.33.

The output power, input power, and circuit efficiency are then calculated to be

$$P_o = V_o^2(\text{p-p})/(8 \cdot R_L) = (20.4\ \text{V})^2/(8 \cdot 8\ \Omega) = 6.5\ \text{W}$$

The input power for that amplitude signal is

$$P_i = V_{CC}I_{\text{dc}} = V_{CC}[(2/\pi)(V_o(\text{p-p})/2)/R_L]$$

$$= (12\ \text{V}) \cdot [(2/\pi) \cdot (20.4\ \text{V}/2)/8] = 9.7\ \text{W}$$

The circuit efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (6.5\ \text{W}/9.7\ \text{W}) \cdot 100\% = 67\%$$

PROBLEMS

§ 16.2 Series-Fed Class A Amplifier

1. Calculate the input and output power for the circuit of Fig. 16.35. The input signal results in a base current of 5 mA rms.
2. Calculate the input power dissipated by the circuit of Fig. 16.35 if R_B is changed to 1.5 kΩ.
3. What maximum output power can be delivered by the circuit of Fig. 16.35 if R_B is changed to 1.5 kΩ?
4. If the circuit of Fig. 16.35 is biased at its center voltage and center collector operating point, what is the input power for a maximum output power of 1.5 W?

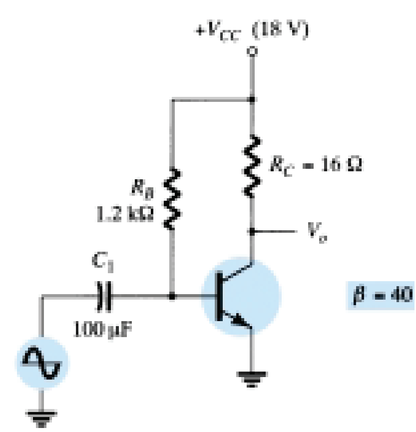

Figure 16.35 Problems 1–4

§ 16.3 Transformer-Coupled Class A Amplifier

5. A class A transformer-coupled amplifier uses a 25:1 transformer to drive a 4-Ω load. Calculate the effective ac load (seen by the transistor connected to the larger turns side of the transformer).
6. What turns ratio transformer is needed to couple to an 8-Ω load so that it appears as an 8-kΩ effective load?
7. Calculate the transformer turns ratio required to connect four parallel 16-Ω speakers so that they appear as an 8-kΩ effective load.

P_L

* **8.** A transformer-coupled class A amplifier drives a 16-Ω speaker through a 3.87:1 transformer. Using a power supply of $V_{CC} = 36$ V, the circuit delivers 2 W to the load. Calculate:
(a) P(ac) across transformer primary.
(b) V_L(ac).
(c) V(ac) at transformer primary.
(d) The rms values of load and primary current.

9. Calculate the efficiency of the circuit of Problem 8 if the bias current is $I_{C_Q} = 150$ mA.

10. Draw the circuit diagram of a class A transformer-coupled amplifier using an *npn* transistor.

§ 16.4 Class B Amplifier Operation

11. Draw the circuit diagram of a class B *npn* push-pull power amplifier using transformer-coupled input.

12. For a class B amplifier providing a 22-V peak signal to an 8-Ω load and a power supply of $V_{CC} = 25$ V, determine:
(a) Input power.
(b) Output power.
(c) Circuit efficiency.

13. For a class B amplifier with $V_{CC} = 25$ V driving an 8-Ω load, determine:
(a) Maximum input power.
(b) Maximum output power.
(c) Maximum circuit efficiency.

* **14.** Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 22$ V driving a 4-Ω load with peak output voltages of:
(a) $V_L(\text{p}) = 20$ V.
(b) $V_L(\text{p}) = 4$ V.

§ 16.5 Class B Amplifier Circuits

15. Sketch the circuit diagram of a quasi-complementary amplifier, showing voltage waveforms in the circuit.

16. For the class B power amplifier of Fig. 16.36, calculate:
(a) Maximum P_o(ac).
(b) Maximum P_i(dc).
(c) Maximum %η.
(d) Maximum power dissipated by both transistors.

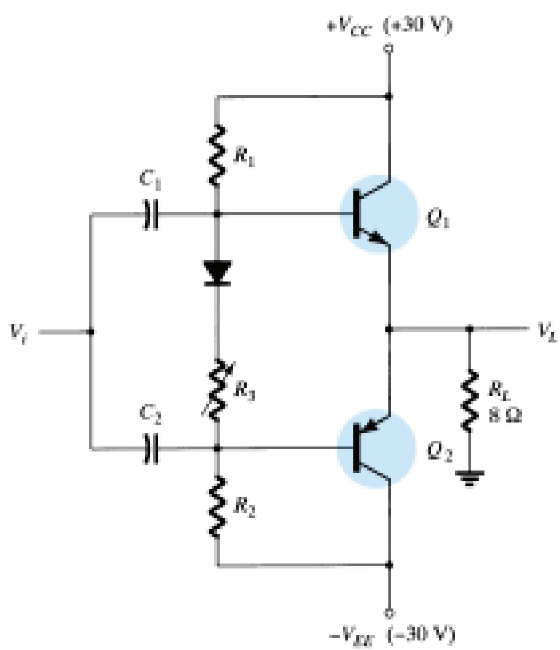

Figure 16.36 Problems 16 and 17

* **17.** If the input voltage to the power amplifier of Fig. 16.36 is 8-V rms, calculate:
(a) P_i(dc).
(b) P_o(ac).
(c) $\%\eta$.
(d) Power dissipated by both power output transistors.

* **18.** For the power amplifier of Fig. 16.37, calculate:
(a) P_o(ac).
(b) P_i(dc).
(c) $\%\eta$.
(d) Power dissipated by both output transistors.

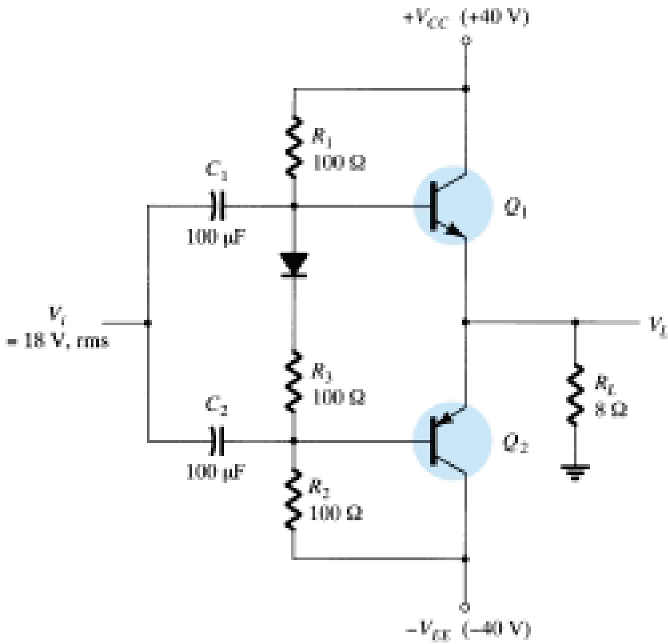

Figure 16.37 Problem 18

§ 16.6 Amplifier Distortion

19. Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.1 V, second harmonic amplitude of 0.3 V, third harmonic component of 0.1 V, and fourth harmonic component of 0.05 V.

20. Calculate the total harmonic distortion for the amplitude components of Problem 19.

21. Calculate the second harmonic distortion for an output waveform having measured values of $V_{CE_{\min}} = 2.4$ V, $V_{CE_Q} = 10$ V, and $V_{CE_{\max}} = 20$ V.

22. For distortion readings of $D_2 = 0.15$, $D_3 = 0.01$, and $D_4 = 0.05$, with $I_1 = 3.3$ A and $R_C = 4\ \Omega$, calculate the total harmonic distortion fundamental power component and total power.

§ 16.7 Power Transistor Heat Sinking

23. Determine the maximum dissipation allowed for a 100-W silicon transistor (rated at 25°C) for a derating factor of 0.6 W/°C at a case temperature of 150°C.

* **24.** A 160-W silicon power transistor operated with a heat sink ($\Theta_{SA} = 1.5$°C/W) has Θ_{JC} 0.5°C/W and a mounting insulation of Θ_{CS}=0.8°C/W. What maximum power can be handled by the transistor at an ambient temperature of 80°C? (The junction temperature should not exceed 200°C.)

25. What maximum power can a silicon transistor ($T_{J_{\max}} = 200$°C) dissipate into free air at an ambient temperature of 80°C?

P_L

§ 16.9 PSpice Windows

* **26.** Use Design Center to draw the schematic of Fig. 16.35 with $V_i = 9.1$ mV.

* **27.** Use Design Center to draw the schematic of Fig. 16.36 with $V_i = 25$ V(p). Determine the circuit efficiency.

* **28.** Use Design Center to draw the schematic of an op-amp class B amplifier as in Fig. 16.33. Use $R_1 = 10$ kΩ, $R_F = 50$ kΩ, and $V_i = 2.5$ V(p). Determine the circuit efficiency.

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*Please Note: Asterisks indicate more difficult problems.

CHAPTER

Linear-Digital ICs 17

17.1 INTRODUCTION

While there are many ICs containing only digital circuits and many that contain only linear circuits, there are a number of units that contain both linear and digital circuits. Among the linear/digital ICs are comparator circuits, digital/analog converters, interface circuits, timer circuits, voltage-controlled oscillator (VCO) circuits, and phase-locked loops (PLLs).

The comparator circuit is one to which a linear input voltage is compared to another reference voltage, the output being a digital condition representing whether the input voltage exceeded the reference voltage.

Circuits that convert digital signals into an analog or linear voltage, and those that convert a linear voltage into a digital value, are popular in aerospace equipment, automotive equipment, and compact disk (CD) players, among many others.

Interface circuits are used to enable connecting signals of different digital voltage levels, from different types of output devices, or from different impedances so that both the driver stage and the receiver stage operate properly.

Timer ICs provide linear and digital circuits to use in various timing operations, as in a car alarm, a home timer to turn lights on or off, and a circuit in electromechanical equipment to provide proper timing to match the intended unit operation. The 555 timer has long been a popular IC unit. A voltage-controlled oscillator provides an output clock signal whose frequency can be varied or adjusted by an input voltage. One popular application of a VCO is in a phase-locked loop unit, as used in various communication transmitters and receivers.

17.2 COMPARATOR UNIT OPERATION

A comparator circuit accepts input of linear voltages and provides a digital output that indicates when one input is less than or greater than the second. A basic comparator circuit can be represented as in Fig. 17.1a. The output is a digital signal that stays at a high voltage level when the noninverting (+) input is greater than the voltage at the inverting (−) input and switches to a lower voltage level when the noninverting input voltage goes below the inverting input voltage.

Figure 17.1b shows a typical connection with one input (the inverting input in this example) connected to a reference voltage, the other connected to the input signal voltage. As long as V_{in} is less than the reference voltage level of +2 V, the output remains at a low voltage level (near −10 V). When the input rises just above +2 V, the

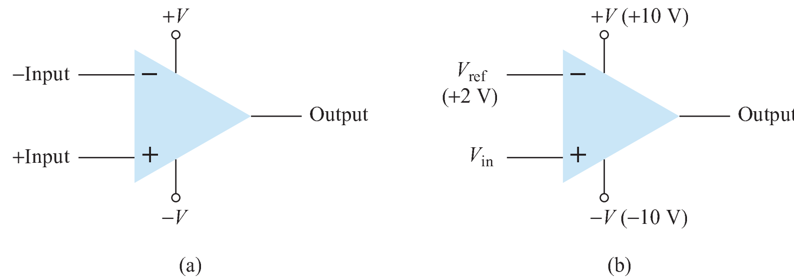

Figure 17.1 Comparator unit: (a) basic unit; (b) typical application.

output quickly switches to a high-voltage level (near +10 V). Thus the high output indicates that the input signal is greater than +2 V.

Since the internal circuit used to build a comparator contains essentially an op-amp circuit with very high voltage gain, we can examine the operation of a comparator using a 741 op-amp, as shown in Fig. 17.2. With reference input (at pin 2) set to 0 V, a sinusoidal signal applied to the noninverting input (pin 3) will cause the output to switch between its two output states, as shown in Fig. 17.2b. The input V_i going even a fraction of a millivolt above the 0-V reference level will be amplified by the very high voltage gain (typically over 100,000) so that the output rises to its positive output saturation level and remains there while the input stays above $V_{ref} = 0$ V. When the input drops just below the 0-V reference level, the output is driven to its lower saturation level and stays there while the input remains below $V_{ref} = 0$ V. Figure 17.2b clearly shows that the input signal is linear while the output is digital.

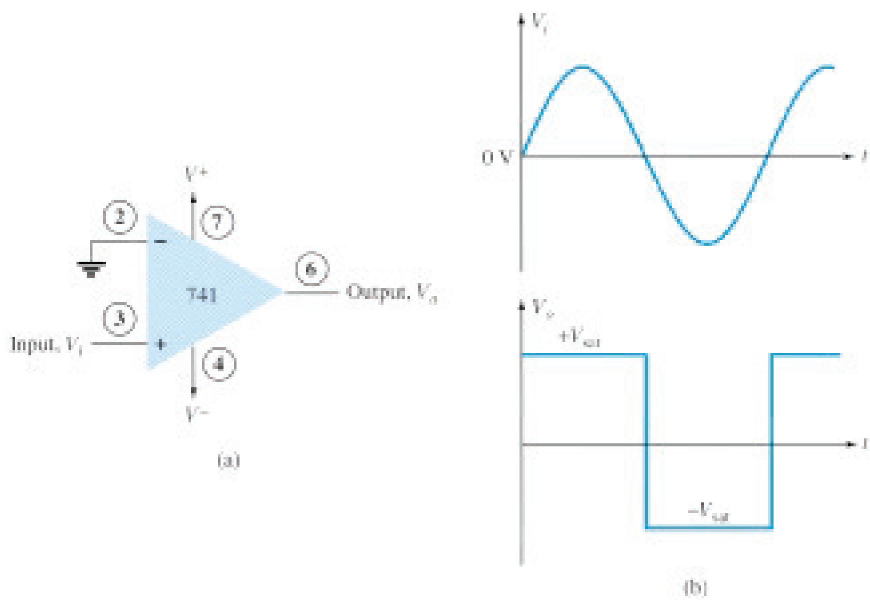

Figure 17.2 Operation of 741 op-amp as comparator.

In general use, the reference level need not be 0 V but can be any desired positive or negative voltage. Also, the reference voltage may be connected to either plus or minus input and the input signal then applied to the other input.

Use of Op-Amp as Comparator

Figure 17.3a shows a circuit operating with a positive reference voltage connected to the minus input and the output connected to an indicator LED. The reference voltage level is set at

$$V_{ref} = \frac{10\text{ k}\Omega}{10\text{ k}\Omega + 10\text{ k}\Omega}(+12\text{ V}) = +6\text{ V}$$

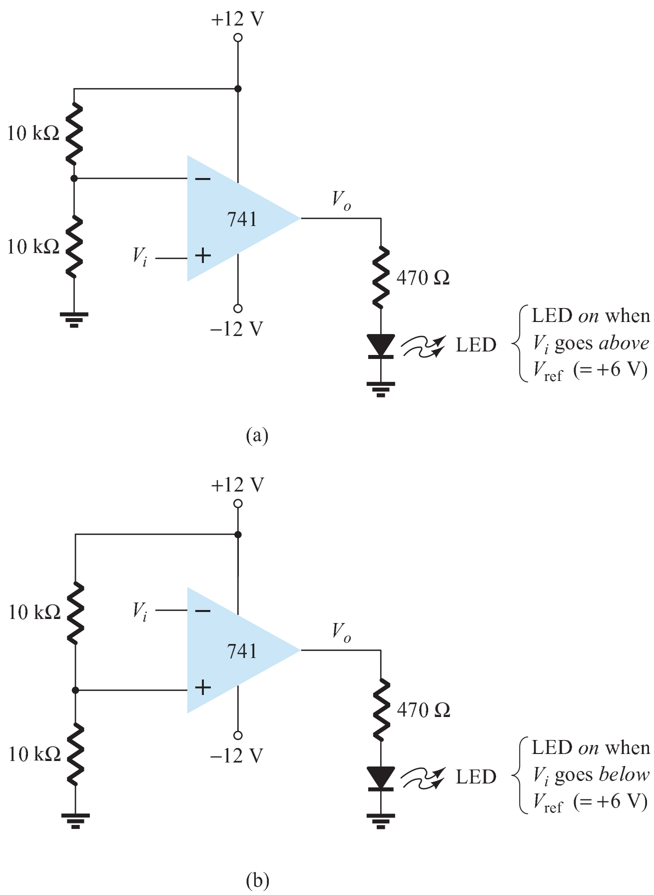

Figure 17.3 A 741 op-amp used as a comparator.

Since the reference voltage is connected to the inverting input, the output will switch to its positive saturation level when the input, V_i, goes more positive than the +6-V reference voltage level. The output, V_o, then drives the LED on as an indication that the input is more positive than the reference level.

As an alternative connection, the reference voltage could be connected to the non-inverting input as shown in Fig. 17.3b. With this connection, the input signal going below the reference level would cause the output to drive the LED on. The LED can thus be made to go on when the input signal goes above or below the reference level, depending on which input is connected as signal input and which as reference input.

Using Comparator IC Units

While op-amps can be used as comparator circuits, separate IC comparator units are more suitable. Some of the improvements built into a comparator IC are faster switching between the two output levels, built-in noise immunity to prevent the output from oscillating when the input passes by the reference level, and outputs capable of directly driving a variety of loads. A few popular IC comparators are covered next, describing their pin connections and how they may be used.

311 COMPARATOR

The 311 voltage comparator shown in Fig. 17.4 contains a comparator circuit that can operate as well from dual power supplies of ±15 V as from a single +5-V supply (as used in digital logic circuits). The output can provide a voltage at one of two distinct levels or can be used to drive a lamp or a relay. Notice that the output is taken

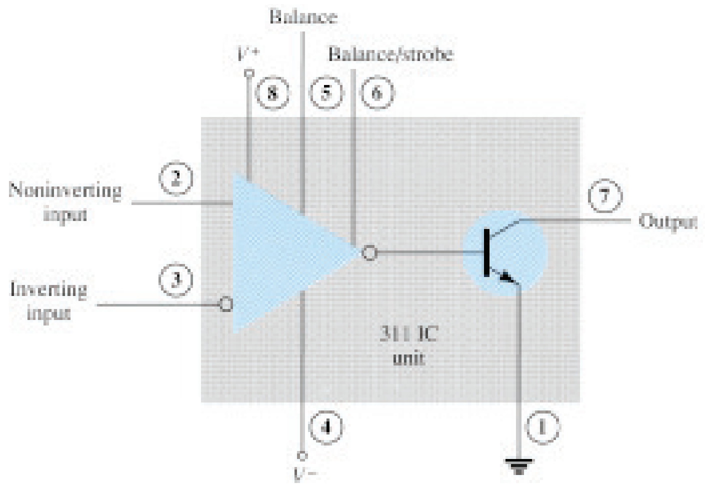

Figure 17.4 A 311 comparator (eight-pin DIP unit).

from a bipolar transistor to allow driving a variety of loads. The unit also has balance and strobe inputs, the strobe input allowing gating of the output. A few examples will show how this comparator unit can be used in some common applications.

A zero-crossing detector that senses (detects) the input voltage crossing through 0 V is shown using the 311 IC in Fig. 17.5. The inverting input is connected to ground (the reference voltage). The input signal going positive drives the output transistor on, with the output then going low (−10 V in this case). The input signal going negative (below 0 V) will drive the output transistor off, the output then going high (to +10 V). The output is thus an indication of whether the input is above or below 0 V. When the input is any positive voltage, the output is low, while any negative voltage will result in the output going to a high voltage level.

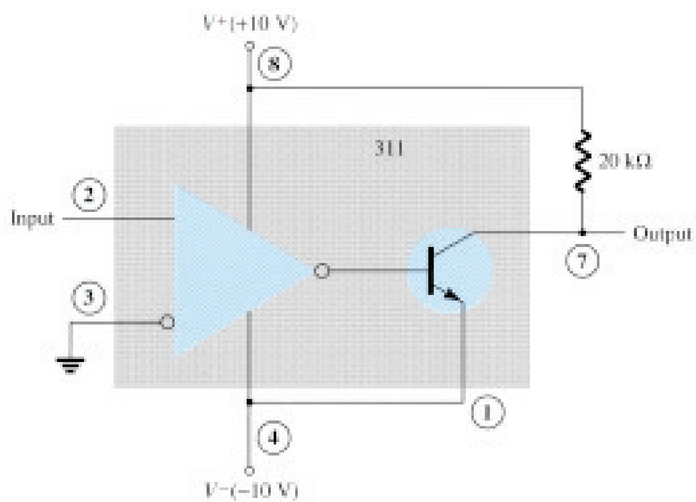

Figure 17.5 Zero-crossing detector using a 311 IC.

Figure 17.6 shows how a 311 comparator can be used with strobing. In this example, the output will go high when the input goes above the reference level—but only if the TTL strobe input is off (or 0 V). If the TTL strobe input goes high, it drives the 311 strobe input at pin 6 low, causing the output to remain in the off state (with output high) regardless of the input signal. In effect, the output remains high

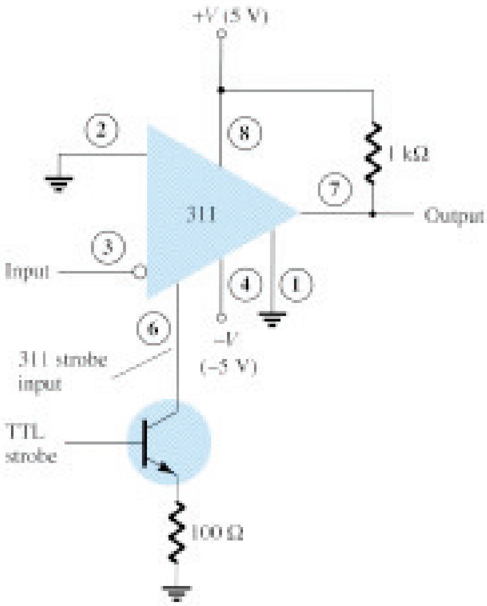

Figure 17.6 Operation of a 311 comparator with strobe input.

unless strobed. If strobed, the output then acts normally, switching from high to low depending on the input signal level. In operation, the comparator output will respond to the input signal only during the time the strobe signal allows such operation.

Figure 17.7 shows the comparator output driving a relay. When the input goes below 0 V, driving the output low, the relay is activated, closing the normally open (N.O.) contacts at that time. These contacts can then be connected to operate a large variety of devices. For example, a buzzer or bell wired to the contacts can be driven on whenever the input voltage drops below 0 V. As long as the voltage is present at the input terminal, the buzzer will remain off.

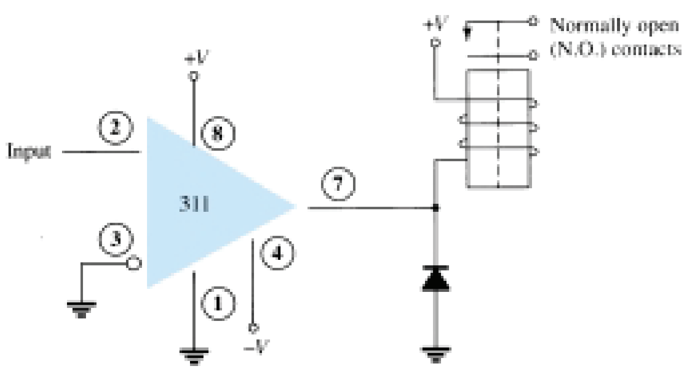

Figure 17.7 Operation of a 311 comparator with relay output.

339 COMPARATOR

The 339 IC is a quad comparator containing four independent voltage comparator circuits connected to external pins as shown in Fig. 17.8. Each comparator has inverting and noninverting inputs and a single output. The supply voltage applied to a pair of pins powers all four comparators. Even if one wishes to use one comparator, all four will be drawing power.