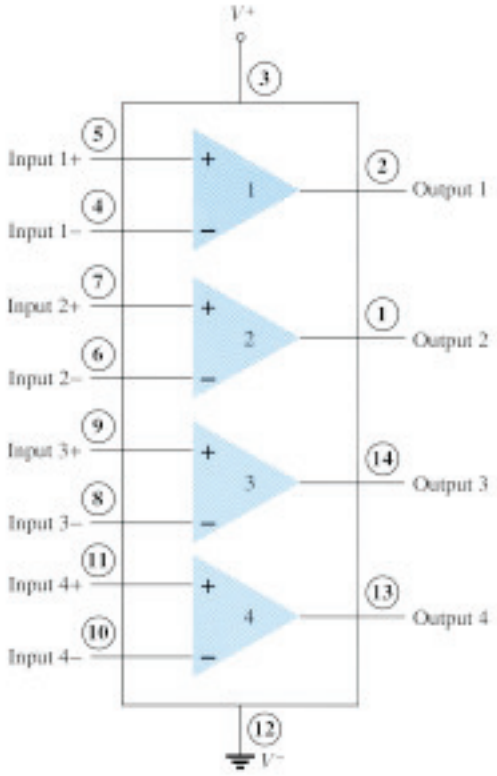


Figure 17.8 Quad comparator IC (339).

To see how these comparator circuits can be used, Fig. 17.9 shows one of the 339 comparator circuits connected as a zero-crossing detector. Whenever the input signal goes above 0 V, the output switches to V^+. The input switches to V^- only when the input goes below 0 V.

A reference level other than 0 V can also be used, and either input terminal could be used as the reference, the other terminal then being connected to the input signal. The operation of one of the comparator circuits is described next.

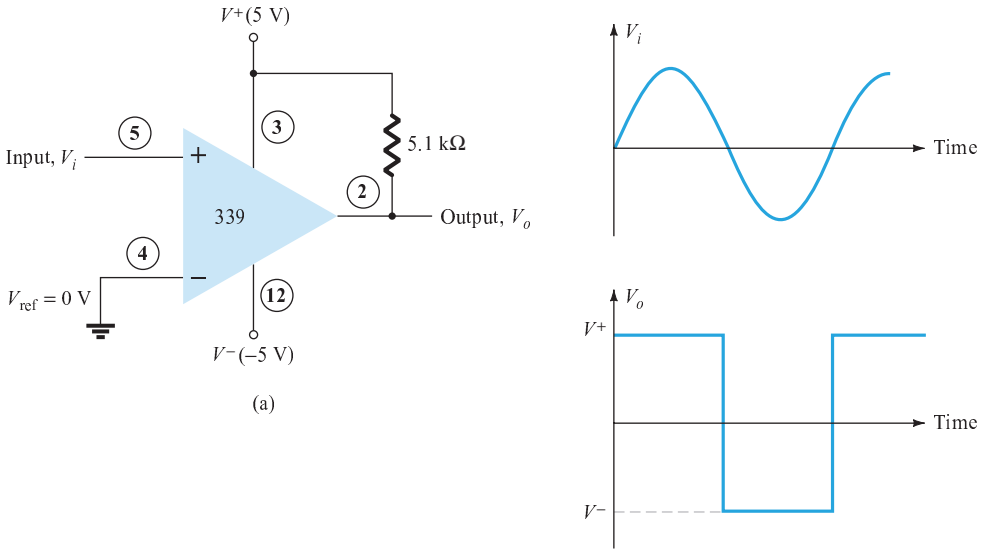


Figure 17.9 Operation of one 339 comparator circuit as a zero-crossing detector.

The differential input voltage (difference voltage across input terminals) going positive drives the output transistor off (open circuit), while a negative differential input voltage drives the output transistor on—the output then at the supply low level.

If the negative input is set at a reference level V_{ref}, the positive input goes above V_{ref} and results in a positive differential input with output driven to the open-circuit state. When the noninverting input goes below V_{ref}, resulting in a negative differential input, the output will be driven to V^-.

If the positive input is set at the reference level, the inverting input going below V_{ref} results in the output open circuit while the inverting input going above V_{ref} results in the output at V^-. This operation is summarized in Fig. 17.10.

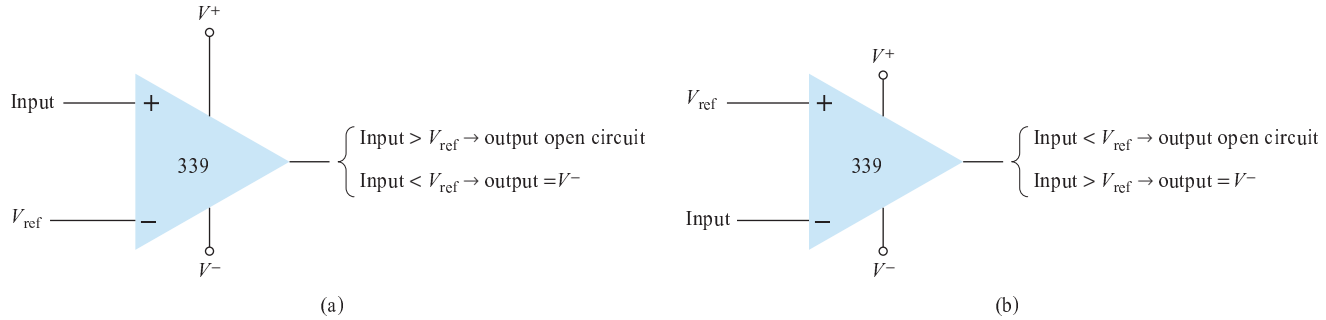


Figure 17.10 Operation of a 339 comparator circuit with reference input: (a) minus input; (b) plus input.

Since the output of one of these comparator circuits is from an open-circuit collector, applications in which the outputs from more than one circuit can be wire-ORed are possible. Figure 17.11 shows two comparator circuits connected with common output and also with common input. Comparator 1 has a +5-V reference voltage in-

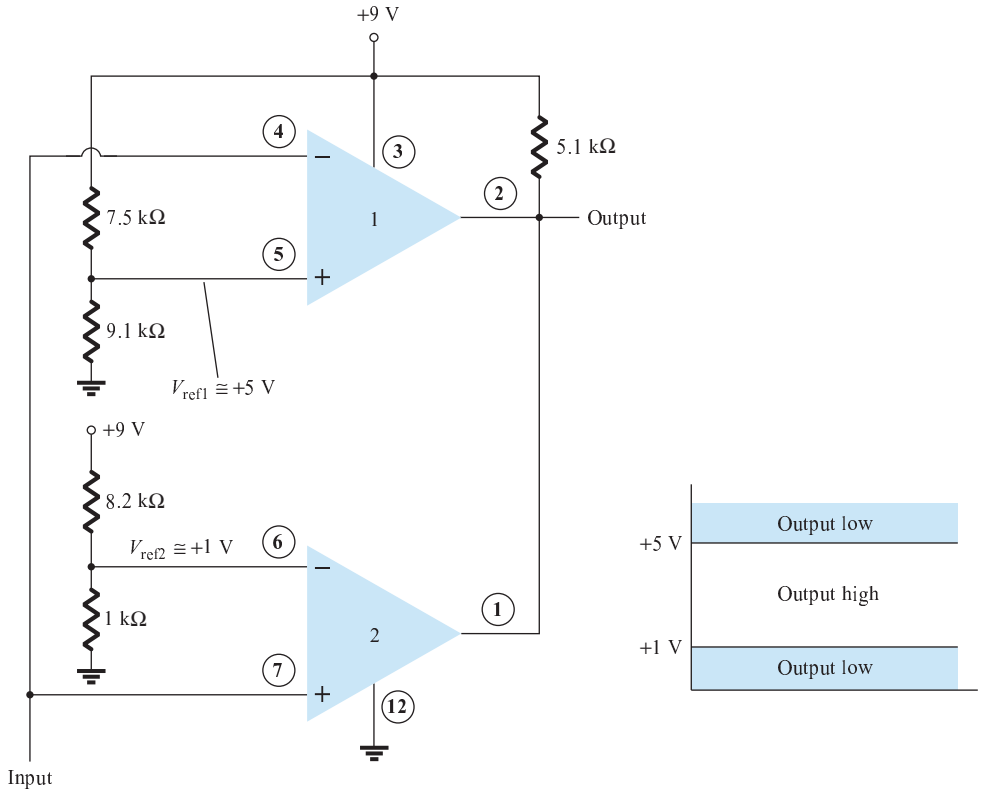


Figure 17.11 Operation of two 339 comparator circuits as a window detector.

put connected to the noninverting input. The output will be driven low by comparator 1 when the input signal goes above +5 V. Comparator 2 has a reference voltage of +1 V connected to the inverting input. The output of comparator 2 will be driven low when the input signal goes below +1 V. In total, the output will go low whenever the input is below +1 V or above +5 V, as shown in Fig. 17.11, the overall operation being that of a voltage window detector. The high output indicates that the input is within a voltage window of +1 to +5 V (these values being set by the reference voltage levels used).

17.3 DIGITAL–ANALOG CONVERTERS

Many voltages and currents in electronics vary continuously over some range of values. In digital circuitry the signals are at either one of two levels, representing the binary values of 1 or zero. An analog–digital converter (ADC) obtains a digital value representing an input analog voltage, while a digital–analog converter (DAC) changes a digital value back into an analog voltage.

Digital-to-Analog Conversion

LADDER NETWORK CONVERSION

Digital-to-analog conversion can be achieved using a number of different methods. One popular scheme uses a network of resistors, called a *ladder network*. A ladder network accepts inputs of binary values at, typically, 0 V or V_{ref} and provides an output voltage proportional to the binary input value. Figure 17.12a shows a ladder network with four input voltages, representing 4 bits of digital data and a dc voltage output. The output voltage is proportional to the digital input value as given by the relation

$$V_o = \frac{D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + D_3 \times 2^3}{2^4} V_{\text{ref}} \tag{17.1}$$

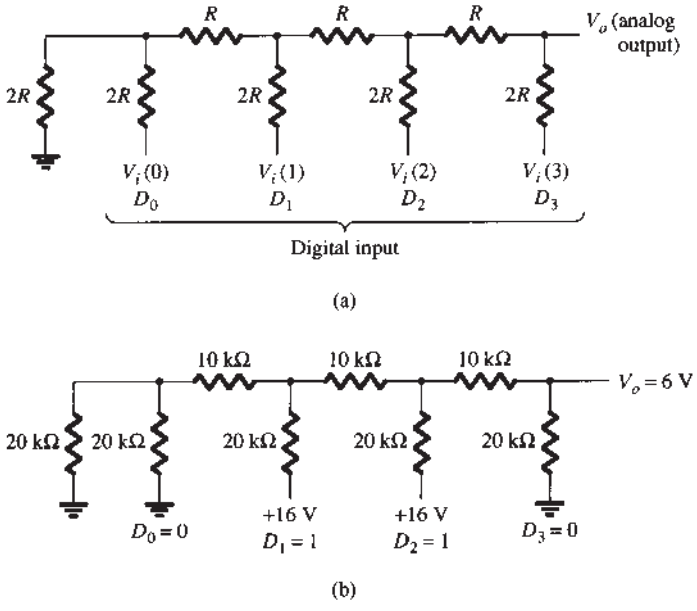


Figure 17.12 Four-stage ladder network used as a DAC: (a) basic circuit; (b) circuit example with 0110 input.

In the example shown in Fig. 17.12b, the output voltage resulting should be

$$V_o = \frac{0 \times 1 + 1 \times 2 + 1 \times 4 + 0 \times 8}{16} (16 \text{ V}) = 6 \text{ V}$$

Therefore, 0110_2, digital, converts to 6 V, analog.

The function of the ladder network is to convert the 16 possible binary values from 0000 to 1111 into one of 16 voltage levels in steps of $V_{\text{ref}}/16$. Using more sections of ladder allows having more binary inputs and greater quantization for each step. For example, a 10-stage ladder network could extend the number of voltage steps or the voltage resolution to $V_{\text{ref}}/2^{10}$ or $V_{\text{ref}}/1024$. A reference voltage of $V_{\text{ref}} = 10$ V would then provide output voltage steps of 10 V/1024 or approximately 10 mV. More ladder stages provide greater voltage resolution. In general, the voltage resolution for n ladder stages is

$$\boxed{\frac{V_{\text{ref}}}{2^n}} \tag{17.2}$$

Figure 17.13 shows a block diagram of a typical DAC using a ladder network. The ladder network, referred in the diagram as an *R-2R ladder,* is sandwiched between the reference current supply and current switches connected to each binary input, the resulting output current proportional to the input binary value. The binary input turns on selected legs of the ladder, the output current being a weighted summing of the reference current. Connecting the output current through a resistor will produce an analog voltage, if desired.

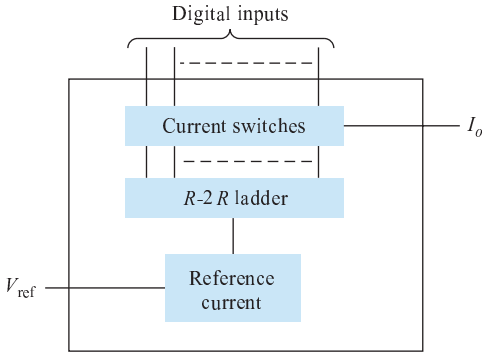


Figure 17.13 DAC IC using R-2R ladder network.

Analog-to-Digital Conversion

DUAL-SLOPE CONVERSION

A popular method for converting an analog voltage into a digital value is the dual-slope method. Figure 17.14a shows a block diagram of the basic dual-slope converter. The analog voltage to be converted is applied through an electronic switch to an integrator or ramp-generator circuit (essentially a constant current charging a capacitor to produce a linear ramp voltage). The digital output is obtained from a counter operated during both positive and negative slope intervals of the integrator.

The method of conversion proceeds as follows. For a fixed time interval (usually the full count range of the counter), the analog voltage connected to the integrator raises the voltage at the comparator input to some positive level. Figure 17.14b shows that at the end of the fixed time interval the voltage from the integrator is greater for the larger input voltage. At the end of the fixed count interval, the count is set to zero and the electronic switch connects the integrator to a reference or fixed input voltage.

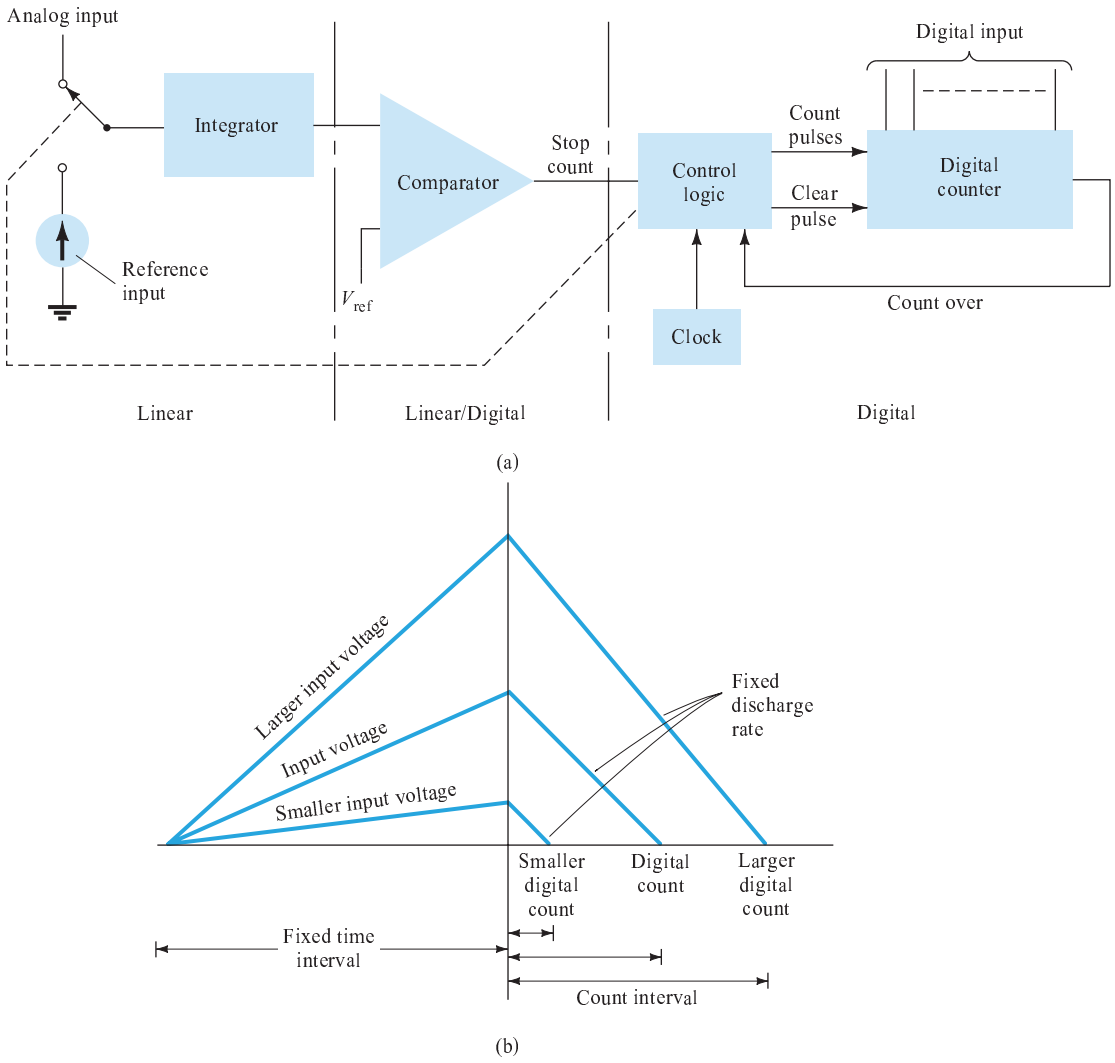


Figure 17.14 Analog-to-digital conversion using dual-slope method: (a) logic diagram; (b) waveform.

The integrator output (or capacitor input) then decreases at a fixed rate. The counter advances during this time, while the integrator's output decreases at a fixed rate until it drops below the comparator reference voltage, at which time the control logic receives a signal (the comparator output) to stop the count. The digital value stored in the counter is then the digital output of the converter.

Using the same clock and integrator to perform the conversion during positive and negative slope intervals tends to compensate for clock frequency drift and integrator accuracy limitations. Setting the reference input value and clock rate can scale the counter output as desired. The counter can be a binary, BCD, or other form of digital counter, if desired.

LADDER-NETWORK CONVERSION

Another popular method of analog-to-digital conversion uses a ladder network along with counter and comparator circuits (see Fig. 17.15). A digital counter advances from a zero count while a ladder network driven by the counter outputs a staircase voltage, as shown in Fig. 17.15b, which increases one voltage increment for each count step. A comparator circuit, receiving both staircase voltage and analog input

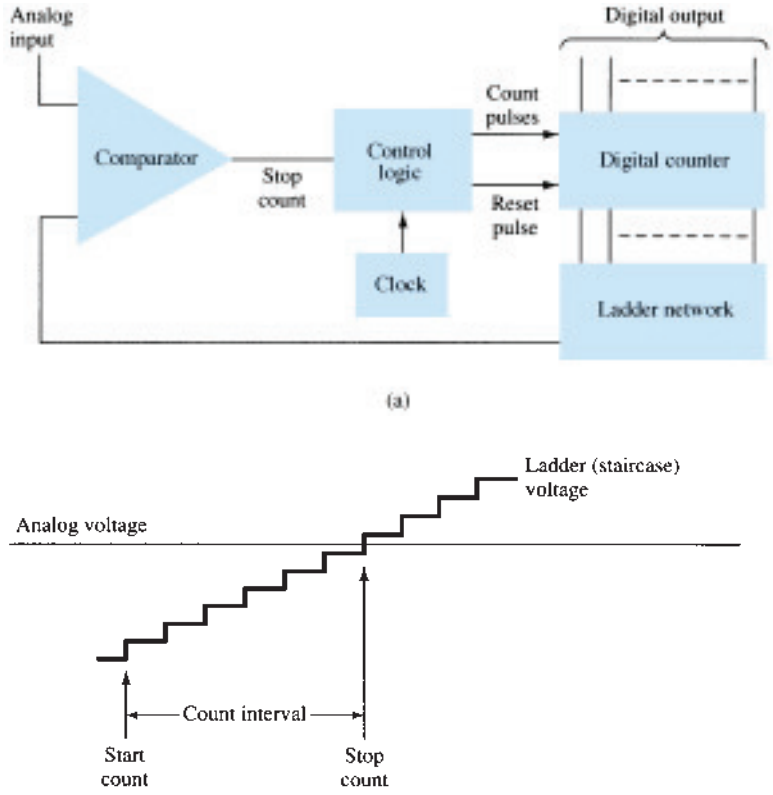


Figure 17.15 Analog-to-digital conversion using ladder network: (a) logic diagram; (b) waveform.

voltage, provides a signal to stop the count when the staircase voltage rises above the input voltage. The counter value at that time is the digital output.

The amount of voltage change stepped by the staircase signal depends on the number of count bits used. A 12-stage counter operating a 12-stage ladder network using a reference voltage of 10 V would step each count by a voltage of

$$\frac{V_{\text{ref}}}{2^{12}} = \frac{10\text{ V}}{4096} = 2.4\text{ mV}$$

This would result in a conversion resolution of 2.4 mV. The clock rate of the counter would affect the time required to carry out a conversion. A clock rate of 1 MHz operating a 12-stage counter would need a maximum conversion time of

$$4096 \times 1\ \mu\text{s} = 4096\ \mu\text{s} \approx 4.1\text{ ms}$$

The minimum number of conversions that could be carried out each second would then be

$$\text{number of conversions} = 1/4.1\text{ ms} \approx 244\text{ conversions/second}$$

Since on the average, with some conversions requiring little count time and others near maximum count time, a conversion time of 4.1 ms/2 = 2.05 ms would be needed, and the average number of conversions would be 2 × 244 = 488 conversions/second. A slower clock rate would result in fewer conversions per second. A converter using fewer count stages (and less conversion resolution) would carry out more conversions per second. The conversion accuracy depends on the accuracy of the comparator.

17.4 TIMER IC UNIT OPERATION

Another popular analog–digital integrated circuit is the versatile 555 timer. The IC is made of a combination of linear comparators and digital flip-flops as described in Fig. 17.16. The entire circuit is usually housed in an 8-pin package as specified in Fig. 17.16. A series connection of three resistors sets the reference voltage levels to the two comparators at $2V_{CC}/3$ and $V_{CC}/3$, the output of these comparators setting or resetting the flip-flop unit. The output of the flip-flop circuit is then brought out through an output amplifier stage. The flip-flop circuit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor.

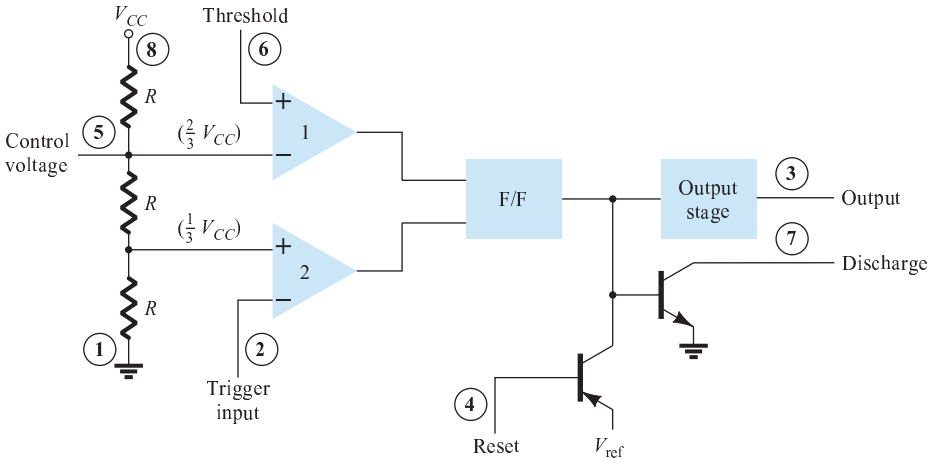


Figure 17.16 Details of 555 timer IC.

Astable Operation

One popular application of the 555 timer IC is as an astable multivibrator or clock circuit. The following analysis of the operation of the 555 as an astable circuit includes details of the different parts of the unit and how the various inputs and outputs are utilized. Figure 17.17 shows an astable circuit built using an external resistor and capacitor to set the timing interval of the output signal.

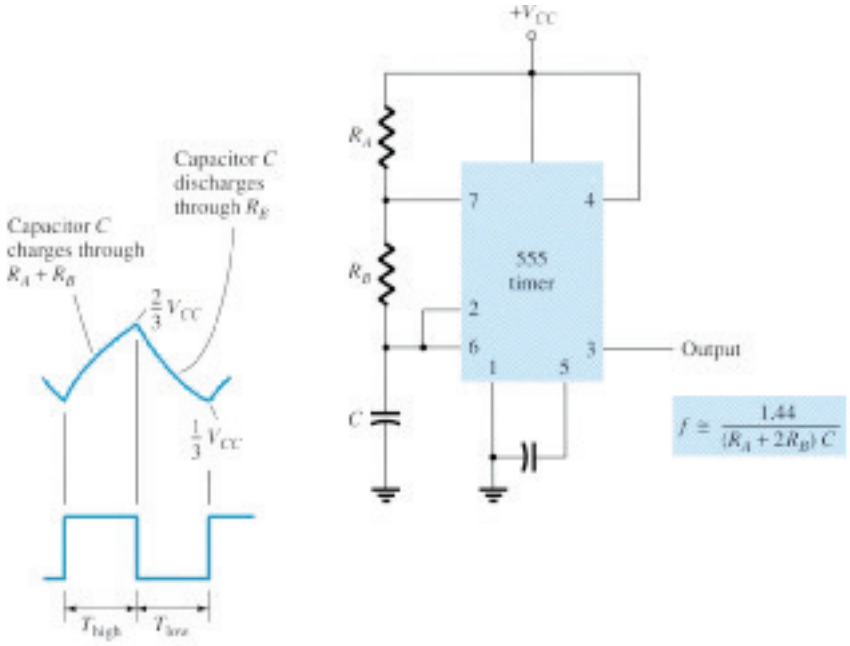


Figure 17.17 Astable multivibrator using 555 IC.

Capacitor C charges toward V_{CC} through external resistors R_A and R_B. Referring to Fig. 17.17, the capacitor voltage rises until it goes above $2V_{CC}/3$. This voltage is the threshold voltage at pin 6, which drives comparator 1 to trigger the flip-flop so that the output at pin 3 goes low. In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor R_B. The capacitor voltage then decreases until it drops below the trigger level ($V_{CC}/3$). The flip-flop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors R_A and R_B toward V_{CC}.

Figure 17.18a shows the capacitor and output waveforms resulting from the astable circuit. Calculation of the time intervals during which the output is high and low can be made using the relations

$$T_{\text{high}} \approx 0.7(R_A + R_B)C \tag{17.3}$$

$$T_{\text{low}} \approx 0.7R_BC \tag{17.4}$$

The total period is

$$T = \text{period} = T_{\text{high}} + T_{\text{low}} \tag{17.5}$$

The frequency of the astable circuit is then calculated using*

$$f = \frac{1}{T} \approx \frac{1.44}{(R_A + 2R_B)C} \tag{17.6}$$

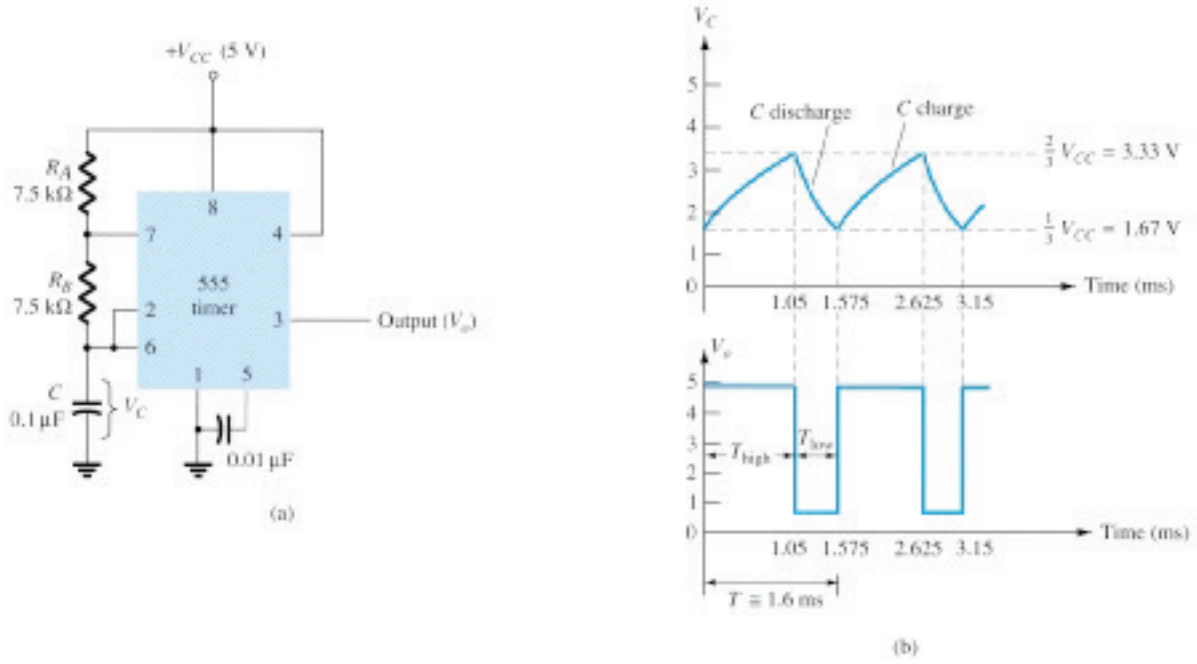


Figure 17.18 Astable multivibrator for Example 17.1: (a) circuit; (b) waveforms.

*The period can be directly calculated from

$$T = 0.693(R_A + 2R_B)C \approx 0.7(R_A + 2R_B)C$$

and the frequency from

$$f \approx \frac{1.44}{(R_A + 2R_B)C}$$

EXAMPLE 17.1 Determine the frequency and draw the output waveform for the circuit of Fig. 17.18a.

Solution

Using Eqs. (17.3) through (17.6) yields

$$T_{\text{high}} = 0.7(R_A + R_B)C = 0.7(7.5 \times 10^3 + 7.5 \times 10^3)(0.1 \times 10^{-6})$$

$$= 1.05 \text{ ms}$$

$$T_{\text{low}} = 0.7R_BC = 0.7(7.5 \times 10^3)(0.1 \times 10^{-6}) = 0.525 \text{ ms}$$

$$T = T_{\text{high}} + T_{\text{low}} = 1.05 \text{ ms} + 0.525 \text{ ms} = 1.575 \text{ ms}$$

$$f = \frac{1}{T} = \frac{1}{1.575 \times 10^{-3}} \approx \mathbf{635 \text{ Hz}}$$

The waveforms are drawn in Fig. 17.18b.

Monostable Operation

The 555 timer can also be used as a one-shot or monostable multivibrator circuit, as shown in Fig. 17.19. When the trigger input signal goes negative, it triggers the one-shot, with output at pin 3 then going high for a time period

$$T_{\text{high}} = 1.1R_AC \tag{17.7}$$

Referring back to Fig. 17.16, the negative edge of the trigger input causes comparator 2 to trigger the flip-flop, with the output at pin 3 going high. Capacitor C charges toward V_{CC} through resistor R_A. During the charge interval, the output remains high. When the voltage across the capacitor reaches the threshold level of $2V_{CC}/3$, comparator 1 triggers the flip-flop, with output going low. The discharge transistor also goes low, causing the capacitor to remain at near 0 V until triggered again.

Figure 17.19b shows the input trigger signal and the resulting output waveform for the 555 timer operated as a one-shot. Time periods for this circuit can range from microseconds to many seconds, making this IC useful for a range of applications.

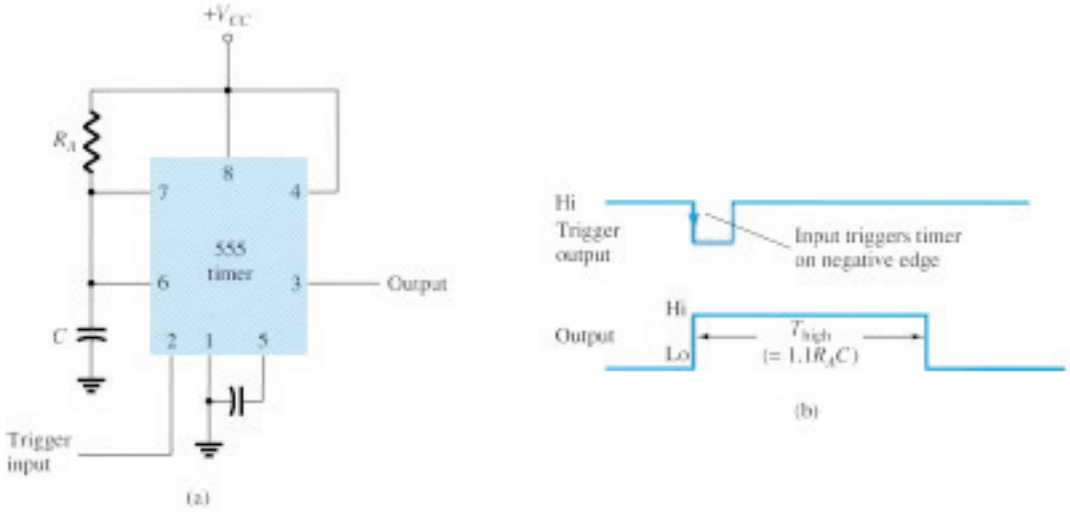


Figure 17.19 Operation of 555 timer as one-shot: (a) circuit; (b) waveforms.

Determine the period of the output waveform for the circuit of Fig. 17.20 when triggered by a negative pulse.

EXAMPLE 17.2

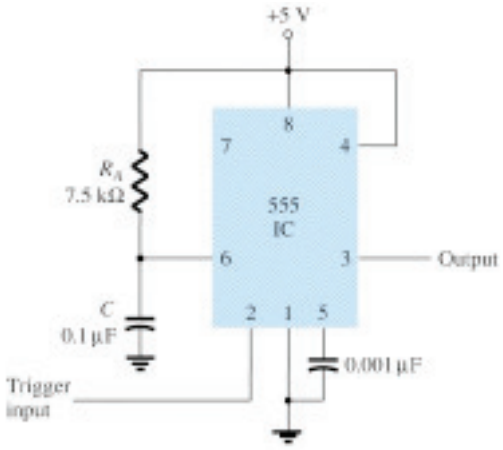


Figure 17.20 Monostable circuit for Example 17.2.

Solution

Using Eq. (17.7), we obtain

$$T_{\text{high}} = 1.1R_AC = 1.1(7.5 \times 10^3)(0.1 \times 10^{-6}) = \mathbf{0.825\ ms}$$

17.5 VOLTAGE-CONTROLLED OSCILLATOR

A voltage-controlled oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by a dc voltage. An example of a VCO is the 566 IC unit, which contains circuitry to generate both square-wave and triangular-wave signals whose frequency is set by an external resistor and capacitor and then varied by an applied dc voltage. Figure 17.21a shows that the 566 contains current sources to charge and discharge an external capacitor C_1 at a rate set by external resistor R_1 and the modulating dc input voltage. A Schmitt trigger circuit is used to switch the current sources between charging and discharging the capacitor, and the triangular voltage developed across the capacitor and square wave from the Schmitt trigger are provided as outputs through buffer amplifiers.

Figure 17.21b shows the pin connection of the 566 unit and a summary of formula and value limitations. The oscillator can be programmed over a 10-to-1 frequency range by proper selection of an external resistor and capacitor, and then modulated over a 10-to-1 frequency range by a control voltage, V_C.

A free-running or center-operating frequency, f_o, can be calculated from

$$f_o = \frac{2}{R_1C_1}\left(\frac{V^+ - V_C}{V^+}\right) \tag{17.8}$$

with the following practical circuit value restrictions:

1. R_1 should be within the range $2\ \text{k}\Omega \leq R_1 \leq 20\ \text{k}\Omega$.
2. V_C should be within range $\frac{3}{4}V^+ \leq V_C \leq V^+$.

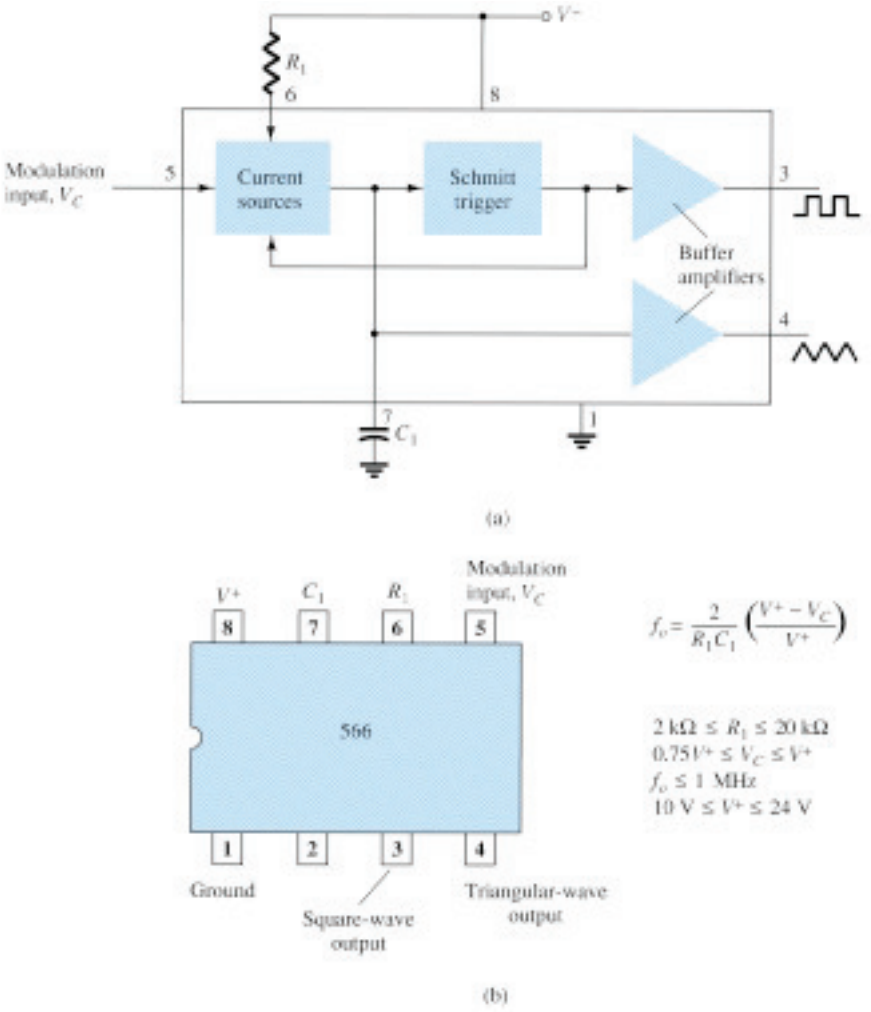


Figure 17.21 A 566 function generator: (a) block diagram; (b) pin configuration and summary of operating data.

3. f_o should be below 1 MHz.
4. V^+ should range between 10 V and 24 V.

Figure 17.22 shows an example in which the 566 function generator is used to provide both square-wave and triangular-wave signals at a fixed frequency set by R_1, C_1, and V_C. A resistor divider R_2 and R_3 sets the dc modulating voltage at a fixed value

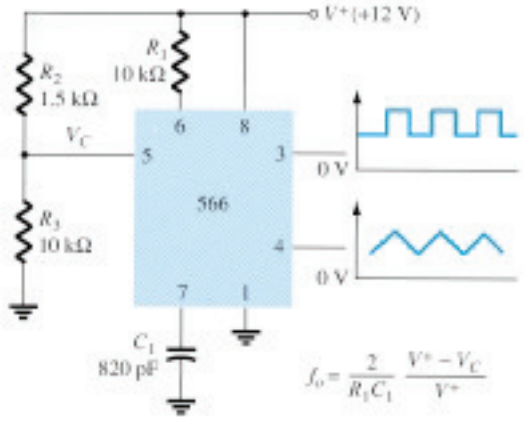


Figure 17.22 Connection of 566 VCO unit.

$$V_C = \frac{R_3}{R_2 + R_3} V^+ = \frac{10\ \text{k}\Omega}{1.5\ \text{k}\Omega + 10\ \text{k}\Omega}(12\ \text{V}) = 10.4\ \text{V}$$

(which falls properly in the voltage range $0.75V^+ = 9$ V and $V^+ = 12$ V). Using Eq. (17.8) yields

$$f_o = \frac{2}{(10 \times 10^3)(820 \times 10^{-12})}\left(\frac{12 - 10.4}{12}\right) \approx 32.5\ \text{kHz}$$

The circuit of Fig. 17.23 shows how the output square-wave frequency can be adjusted using the input voltage, V_C, to vary the signal frequency. Potentiometer R_3 allows varying V_C from about 9 V to near 12 V, over the full 10-to-1 frequency range. With the potentiometer wiper set at the top, the control voltage is

$$V_C = \frac{R_3 + R_4}{R_2 + R_3 + R_4}(V^+) = \frac{5\ \text{k}\Omega + 18\ \text{k}\Omega}{510\ \Omega + 5\ \text{k}\Omega + 18\ \text{k}\Omega}(+12\ \text{V}) = 11.74\ \text{V}$$

resulting in a lower output frequency of

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 11.74}{12}\right) \approx 19.7\ \text{kHz}$$

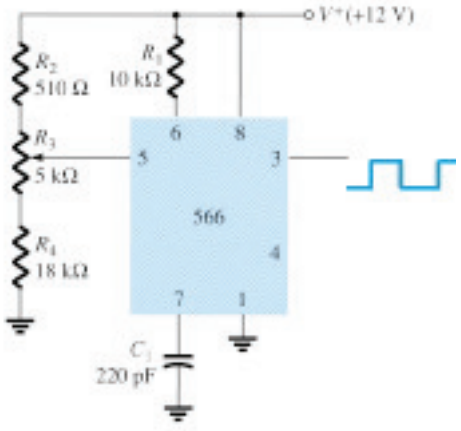


Figure 17.23 Connection of 566 as a VCO unit.

With the wiper arm of R_3 set at the bottom, the control voltage is

$$V_C = \frac{R_4}{R_2 + R_3 + R_4}(V^+) = \frac{18\ \text{k}\Omega}{510\ \Omega + 5\ \text{k}\Omega + 18\ \text{k}\Omega}(+12\ \text{V}) = 9.19\ \text{V}$$

resulting in an upper frequency of

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 9.19}{12}\right) \approx 212.9\ \text{kHz}$$

The frequency of the output square wave can then be varied using potentiometer R_3 over a frequency range of at least 10 to 1.

Rather than varying a potentiometer setting to change the value of V_C, an input modulating voltage, V_{in}, can be applied as shown in Fig. 17.24. The voltage divider sets V_C at about 10.4 V. An input ac voltage of about 1.4 V peak can drive V_C around the bias point between voltages of 9 and 11.8 V, causing the output frequency to vary over about a 10-to-1 range. The input signal V_{in} thus frequency-modulates the output voltage around the center frequency set by the bias value of $V_C = 10.4$ V ($f_o = 121.2$ kHz).

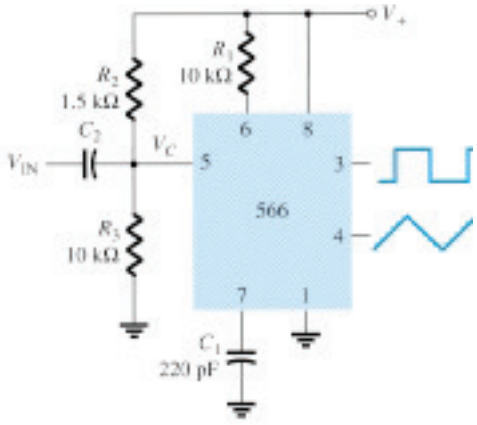


Figure 17.24 Operation of VCO with frequency-modulating input.

17.6 PHASE-LOCKED LOOP

A phase-locked loop (PLL) is an electronic circuit that consists of a phase detector, a low-pass filter, and a voltage-controlled oscillator connected as shown in Fig. 17.25. Common applications of a PLL include: (1) frequency synthesizers that provide multiples of a reference signal frequency [e.g., the carrier frequency for the multiple channels of a citizens' band (CB) unit or marine-radio-band unit can be generated using a single-crystal-controlled frequency and its multiples generated using a PLL]; (2) FM demodulation networks for FM operation with excellent linearity between the input signal frequency and the PLL output voltage; (3) demodulation of the two data transmission or carrier frequencies in digital-data transmission used in frequency-shift keying (FSK) operation; and (4) a wide variety of areas including modems, telemetry receivers and transmitters, tone decoders, AM detectors, and tracking filters.

An input signal, V_i, and that from a VCO, V_o, are compared by a phase comparator (refer to Fig. 17.25) providing an output voltage, V_e, that represents the phase difference between the two signals. This voltage is then fed to a low-pass filter that pro-

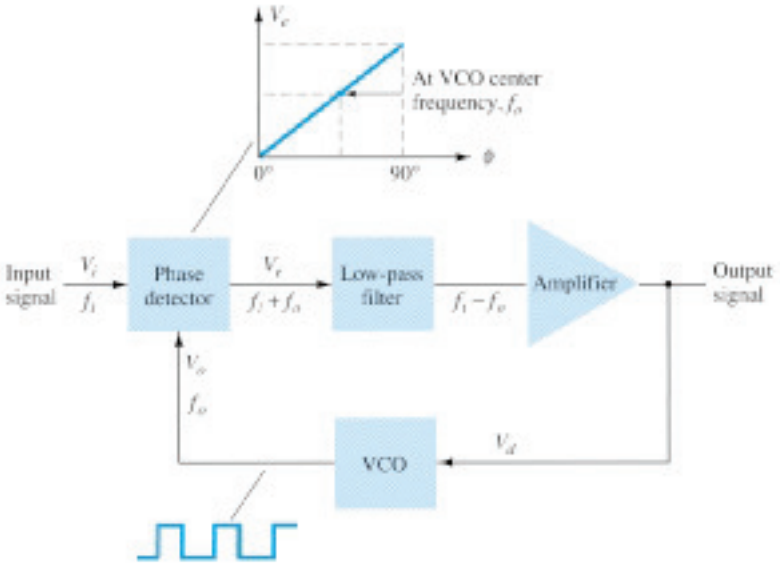


Figure 17.25 Block diagram of basic phase-locked loop (PLL).

vides an output voltage (amplified if necessary) that can be taken as the output voltage from the PLL and is used internally as the voltage to modulate the VCO's frequency. The closed-loop operation of the circuit is to maintain the VCO frequency locked to that of the input signal frequency.

Basic PLL Operation

The basic operation of a PLL circuit can be explained using the circuit of Fig. 17.25 as reference. We will first consider the operation of the various circuits in the phase-locked loop when the loop is operating in lock (the input signal frequency and the VCO frequency are the same). When the input signal frequency is the same as that from the VCO to the comparator, the voltage, V_d, taken as output is the value needed to hold the VCO in lock with the input signal. The VCO then provides output of a fixed-amplitude square-wave signal at the frequency of the input. Best operation is obtained if the VCO center frequency, f_o, is set with the dc bias voltage midway in its linear operating range. The amplifier allows this adjustment in dc voltage from that obtained as output of the filter circuit. When the loop is in lock, the two signals to the comparator are of the same frequency, although not necessarily in phase. A fixed phase difference between the two signals to the comparator results in a fixed dc voltage to the VCO. Changes in the input signal frequency then result in change in the dc voltage to the VCO. Within a capture-and-lock frequency range, the dc voltage will drive the VCO frequency to match that of the input.

While the loop is trying to achieve lock, the output of the phase comparator contains frequency components at the sum and difference of the signals compared. A low-pass filter passes only the lower-frequency component of the signal so that the loop can obtain lock between input and VCO signals.

Owing to the limited operating range of the VCO and the feedback connection of the PLL circuit, there are two important frequency bands specified for a PLL. The capture range of a PLL is the frequency range centered about the VCO free-running frequency, f_o, over which the loop can acquire lock with the input signal. Once the PLL has achieved capture, it can maintain lock with the input signal over a somewhat wider frequency range called the *lock range.*

Applications

The PLL can be used in a wide variety of applications, including (1) frequency demodulation, (2) frequency synthesis, and (3) FSK decoders. Examples of each of these follow.

FREQUENCY DEMODULATION

FM demodulation or detection can be directly achieved using the PLL circuit. If the PLL center frequency is selected or designed at the FM carrier frequency, the filtered or output voltage of the circuit of Fig. 17.25 is the desired demodulated voltage, varying in value proportional to the variation of the signal frequency. The PLL circuit thus operates as a complete intermediate-frequency (IF) strip, limiter, and demodulator as used in FM receivers.

One popular PLL unit is the 565, shown in Fig. 17.26a. The 565 contains a phase detector, amplifier, and voltage-controlled oscillator, which are only partially connected internally. An external resistor and capacitor, R_1 and C_1, are used to set the free-running or center frequency of the VCO. Another external capacitor, C_2, is used to set the low-pass filter passband, and the VCO output must be connected back as input to the phase detector to close the PLL loop. The 565 typically uses two power supplies, V^+ and V^-.

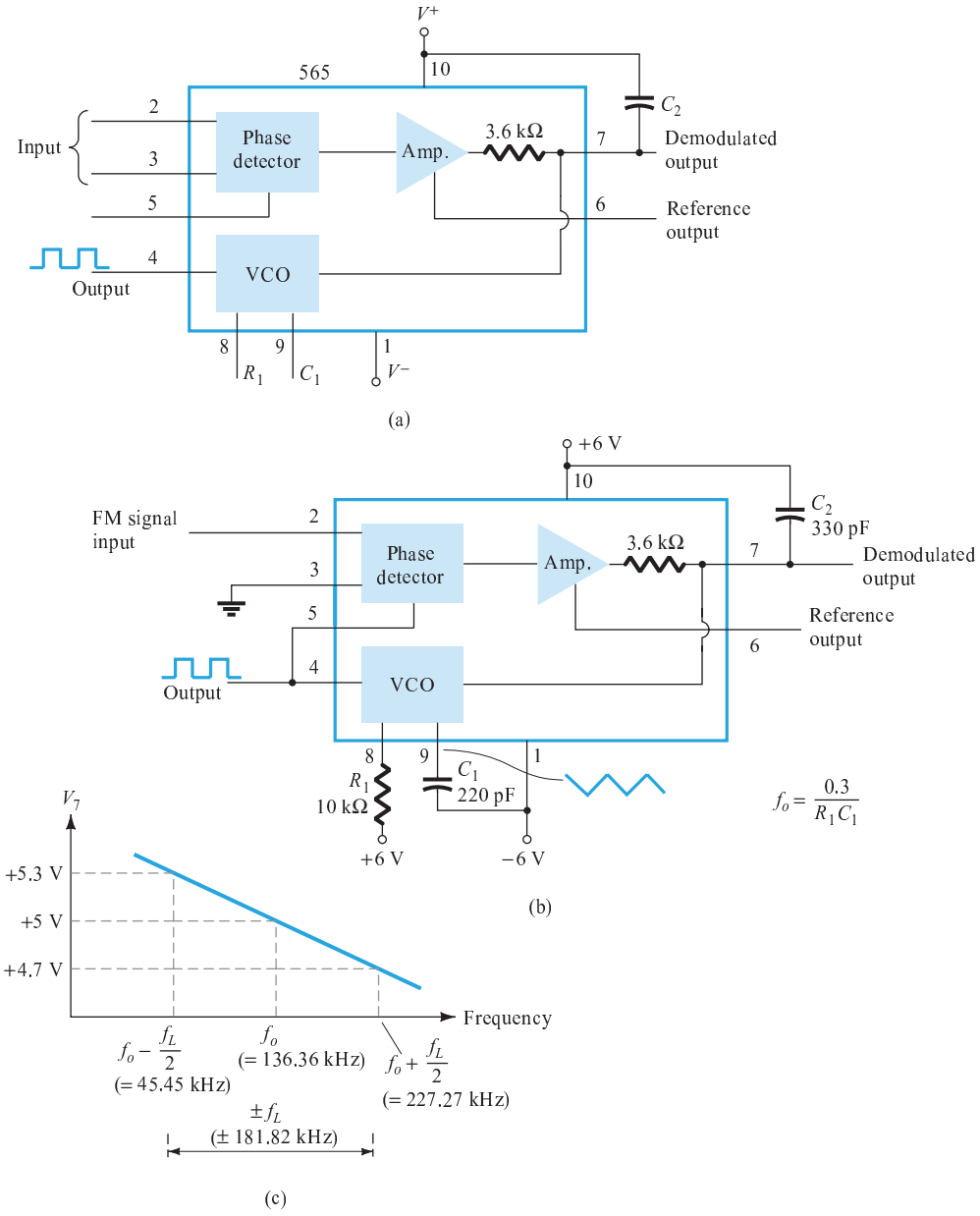


Figure 17.26 Phase-locked loop (PLL): (a) basic block diagram: (b) PLL connected as a frequency demodulator: (c) output voltage vs. frequency plot.

Figure 17.26b shows the PLL connected to work as an FM demodulator. Resistor R_1 and capacitor C_1 set the free-running frequency, f_o,

$$f_o = \frac{0.3}{R_1 C_1} \tag{17.9}$$

$$= \frac{0.3}{(10 \times 10^3)(220 \times 10^{-12})} = 136.36 \text{ kHz}$$

with limitation 2 kΩ ≤ R_1 ≤ 20 kΩ. The lock range is

$$f_L = \pm \frac{8 f_o}{V}$$

$$= \pm \frac{8(136.36 \times 10^3)}{6} = \pm 181.8 \text{ kHz}$$

for supply voltages $V = \pm 6$ V. The capture range is

$$f_C = \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{R_2 C_2}}$$

$$= \pm \frac{1}{2\pi}\sqrt{\frac{2\pi(181.8 \times 10^3)}{(3.6 \times 10^3)(330 \times 10^{-12})}} = 156.1 \text{ kHz}$$

The signal at pin 4 is a 136.36-kHz square wave. An input within the lock range of 181.8 kHz will result in the output at pin 7 varying around its dc voltage level set with input signal at f_o. Figure 17.26c shows the output at pin 7 as a function of the input signal frequency. The dc voltage at pin 7 is linearly related to the input signal frequency within the frequency range $f_L = 181.8$ kHz around the center frequency 136.36 kHz. The output voltage is the demodulated signal that varies with frequency within the operating range specified.

FREQUENCY SYNTHESIS

A frequency synthesizer can be built around a PLL as shown in Fig. 17.27. A frequency divider is inserted between the VCO output and the phase comparator so that the loop signal to the comparator is at frequency f_o while the VCO output is Nf_o. This output is a multiple of the input frequency as long as the loop is in lock. The input signal can be stabilized at f_1 with the resulting VCO output at Nf_1 if the loop is set

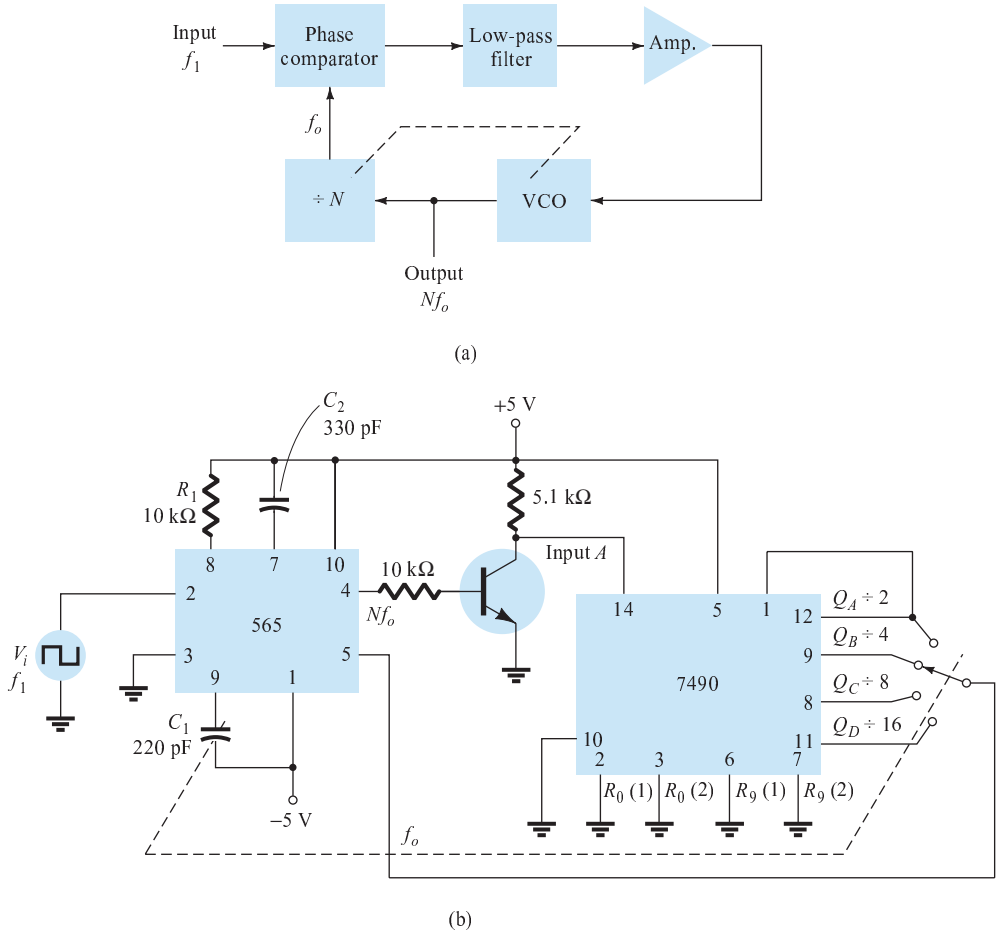


Figure 17.27 Frequency synthesizer: (a) block diagram; (b) implementation using 565 PLL unit.

up to lock at the fundamental frequency (when $f_o = f_1$). Figure 17.27b shows an example using a 565 PLL as frequency multiplier and a 7490 as divider. The input V_i at frequency f_1 is compared to the input (frequency f_o) at pin 5. An output at Nf_o ($4f_o$ in the present example) is connected through an inverter circuit to provide an input at pin 14 of the 7490, which varies between 0 and +5 V. Using the output at pin 9, which is divided by 4 from that at the input to the 7490, the signal at pin 4 of the PLL is four times the input frequency as long as the loop remains in lock. Since the VCO can vary over only a limited range from its center frequency, it may be necessary to change the VCO frequency whenever the divider value is changed. As long as the PLL circuit is in lock, the VCO output frequency will be exactly N times the input frequency. It is only necessary to readjust f_o to be within the capture-and-lock range, the closed loop then resulting in the VCO output becoming exactly Nf_1 at lock.

FSK DECODERS

An FSK (frequency-shift keyed) signal decoder can be built as shown in Fig. 17.28. The decoder receives a signal at one of two distinct carrier frequencies, 1270 Hz or 1070 Hz, representing the RS-232C logic levels or mark (−5 V) or space (+14 V), respectively. As the signal appears at the input, the loop locks to the input frequency and tracks it between two possible frequencies with a corresponding dc shift at the output.

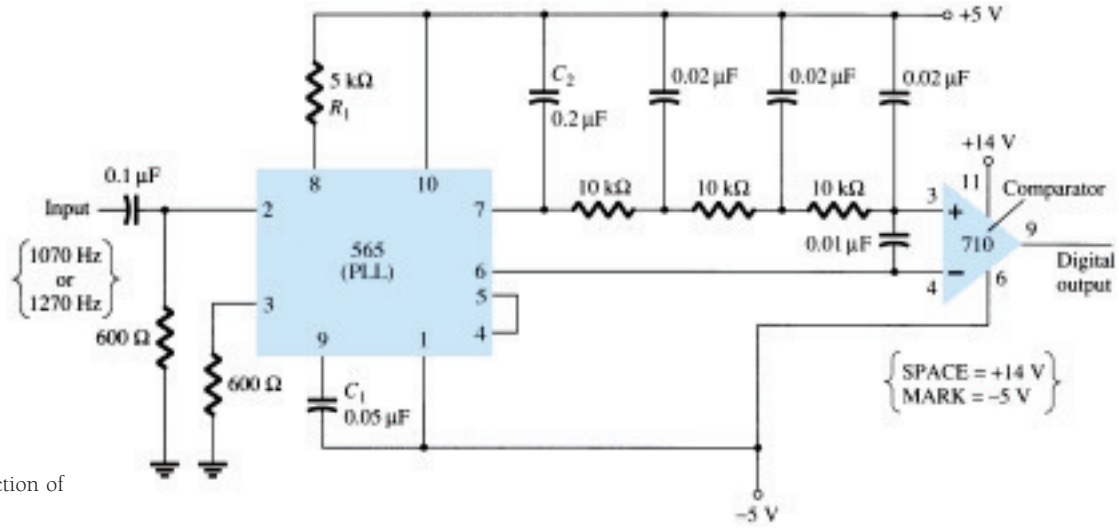


Figure 17.28 Connection of 565 as FSK decoder.

The RC ladder filter (three sections of $C = 0.02$ μF and $R = 10$ kΩ) is used to remove the sum frequency component. The free-running frequency is adjusted with R_1 so that the dc voltage level at the output (pin 7) is the same as that at pin 6. Then an input at frequency 1070 Hz will drive the decoder output voltage to a more positive voltage level, driving the digital output to the high level (space or +14 V). An input at 1270 Hz will correspondingly drive the 565 dc output less positive with the digital output, which then drops to the low level (mark or −5 V).

17.7 INTERFACING CIRCUITRY

Connecting different types of circuits, either in digital or analog circuits, may require some sort of interfacing circuit. An interface circuit may be used to drive a load or to obtain a signal as a receiver circuit. A driver circuit provides the output signal at a

voltage or current level suitable to operate a number of loads, or to operate such devices as relays, displays, or power units. A receiver circuit essentially accepts an input signal, providing high input impedance to minimize loading of the input signal. Furthermore, the interface circuits may include strobing, which provides connecting the interface signals during specific time intervals established by the strobe.

Figure 17.29a shows a dual-line driver, each driver accepting input of TTL signals, providing output capable of driving TTL or MOS device circuits. This type of interface circuit comes in various forms, some as inverting and others as noninverting units. The circuit of Fig. 17.29b shows a dual-line receiver having both inverting and noninverting inputs so that either operating condition can be selected. As an example, connection of an input signal to the inverting input would result in an inverted output from the receiver unit. Connecting the input to the noninverting input would provide the same interfacing except that the output obtained would have the same polarity as the received signal. The driver-receiver unit of Fig. 17.29 provides an output when the strobe signal is present (high in this case).

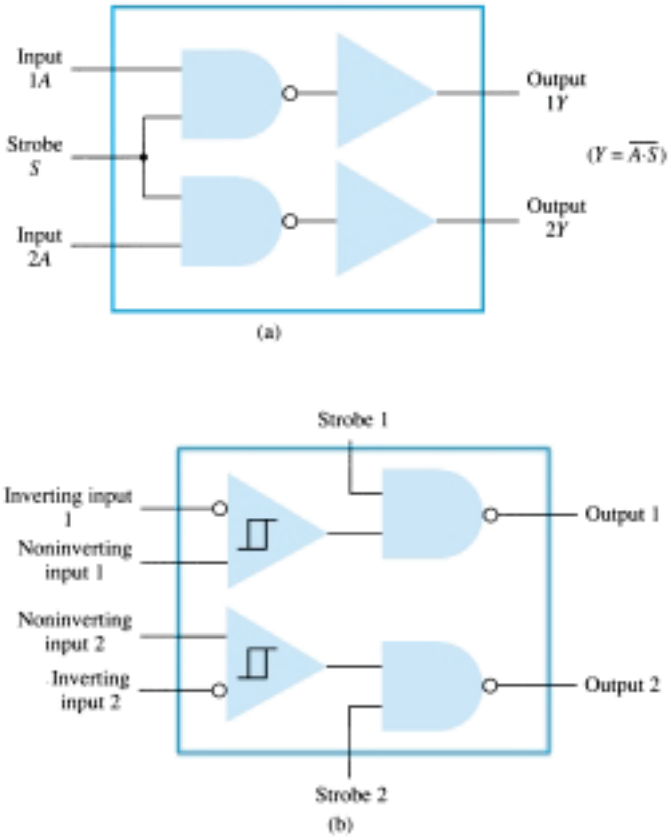


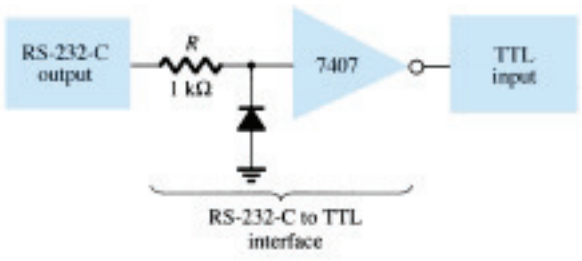
Figure 17.29 Interface units: (a) dual-line drivers (SN75150); (b) dual-line receivers (SN75152).

Another type of interface circuit is that used to connect various digital input and output units, signals with devices such as keyboards, video terminals, and printers. One of the EIA electronic industry standards is referred to as RS-232C. This standard states that a digital signal represents a mark (logic-1) and a space (logic-0). The definitions of mark and space vary with the type of circuit used (although a full reading of the standard will spell out the acceptable limits of mark and space signals).

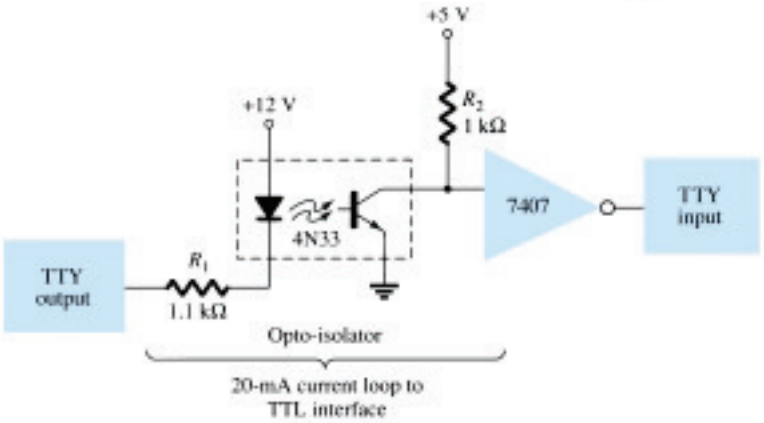
RS-232C-to-TTL Converter

For TTL circuits, +5 V is a mark and 0 V is a space. For RS-232C, a mark could be −12 V and a space +12 V. Figure 17.30a provides a tabulation of some mark and space definitions. For a unit having outputs defined by RS-232C that is to operate into another unit operating with a TTL signal level, an interface circuit as shown in Fig. 17.30b could be used. A mark output from the driver (at −12 V) would be clipped by the diode so that the input to the inverter circuit is near 0 V, resulting in an output of +5 V (TTL mark). A space output at +12 V would drive the inverter output low for a 0-V output (a space).

	Current Loop	RS-232-C	TTL
MARK	20 mA	−12 V	+5 V
SPACE	0 mA	+12 V	0 V



(b)

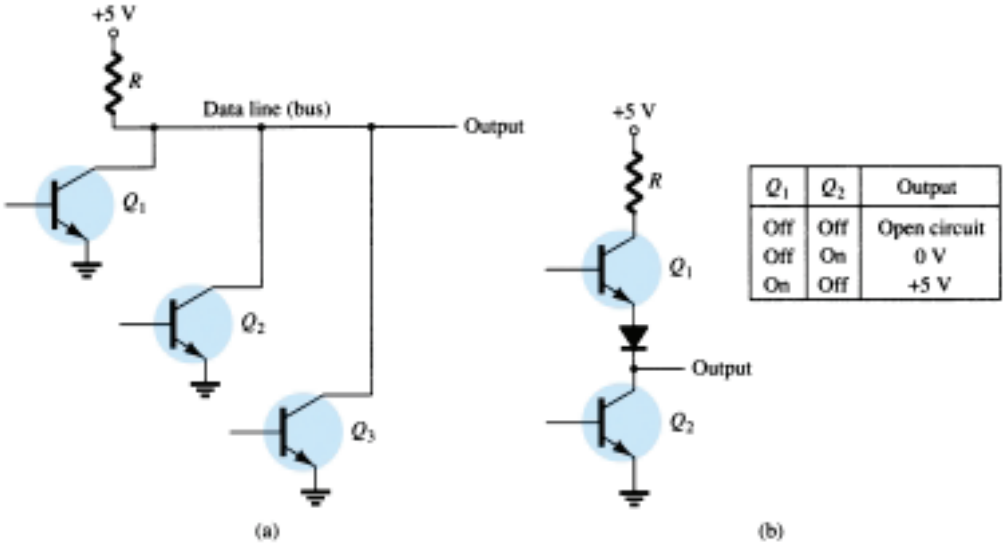


(c)

Figure 17.30 Interfacing signal standards and converter circuits.

Another example of an interface circuit converts the signals from a TTY current loop into TTL levels as shown in Fig. 17.30c. An input mark results when 20 mA of current is drawn from the source through the output line of the teletype (TTY). This current then goes through the diode element of an opto-isolator, driving the output transistor on. The input to the inverter going low results in a +5-V signal from the 7407 inverter output so that a mark from the teletype results in a mark to the TTL input. A space from the teletype current loop provides no current, with the opto-isolator transistor remaining off and the inverter output then 0 V, which is a TTL space signal.

Another means of interfacing digital signals is made using open-collector output or tri-state output. When a signal is output from a transistor collector (see Fig. 17.31) that is not connected to any other electronic component, the output is open-collector. This permits connecting a number of signals to the same wire or bus. Any transistor going on then provides a low output voltage, while all transistors remaining off provide a high output voltage.



Q_1	Q_2	Output
Off	Off	Open circuit
Off	On	0 V
On	Off	+5 V

Figure 17.31 Connections to data lines: (a) open-collector output; (b) tri-state output.

17.8 PSPICE WINDOWS

Many of the practical op-amp applications covered in this chapter can be analyzed using PSpice. Analysis of various problems can display the resulting dc bias, or one can use **PROBE** to display resulting waveforms.

Program 17.1—Comparator Circuit Used to Drive an LED

Using Design Center, draw the circuit of a comparator circuit with output driving an LED indicator as shown in Fig. 17.32. To be able to view the magnitude of the dc output voltage, place a **VPRINT1** component at V_o with **DC** and **MAG** selected. To view the dc current through the LED, place an **IPRINT** component in series with the LED current meter as shown in Fig. 17.32. The **Analysis Setup** provides for a dc sweep as shown in Fig. 17.33. The **DC Sweep** is set, as shown, for V_i from 4 to 8 V in 1-V steps. After running the simultation, some of the resulting analysis output obtained is shown in Fig. 17.34.

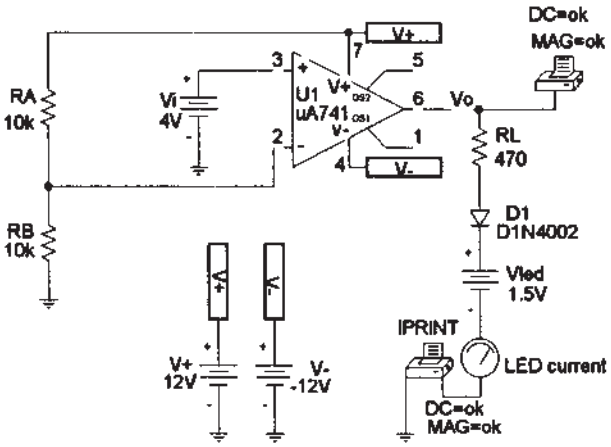


Figure 17.32 Comparator circuit used to drive an LED.

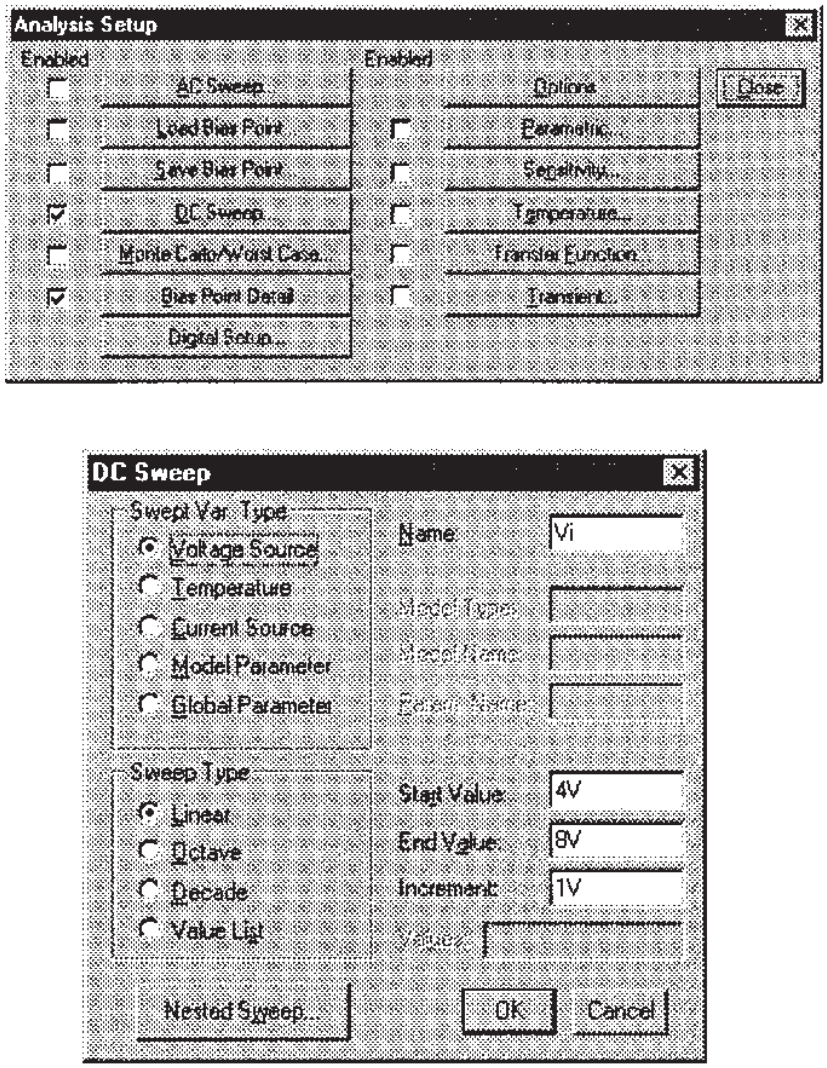


Figure 17.33 Analysis Setup for a dc sweep of the circuit of Fig. 17.32.

The circuit of Fig. 17.32 shows a voltage divider which provides 6 V to the minus input so that any input (V_i) below 6 V will result in the output at the minus saturation voltage (near −10 V). Any input above +6 V results in the output going to the positive saturation level (near +10 V). The LED will therefore be driven *on* by any input above the reference level of +6 V and left *off* by any input below +6 V. The listing of Fig. 17.34 shows a table of the output voltage and a table of the LED current for inputs from 4 to 8 V. The table shows that the LED current is nearly 0 for inputs up to +6 V and that a current of about 20 mA lights the LED for inputs at +6 V or above.

```
Comparator Circuit Driving LED

****     DC TRANSFER CURVES
 V_Vi          V(Vo)
 4.000E+00     -1.161E+01
 5.000E+00     -1.161E+01
 6.000E+00     1.145E+01
 7.000E+00     1.161E+01
 8.000E+00     1.161E+01

****     DC TRANSFER CURVES
 V_Vi          I(V_PRINT3)
 4.000E+00     1.312E-11
 5.000E+00     1.312E-11
 6.000E+00     -1.953E-02
 7.000E+00     -1.987E-02
 8.000E+00     -1.987E-02
```

Figure 17.34 Analysis output (edited) for circuit of Fig. 17.32.

Program 17.2—Comparator Operation

The operation of a comparator IC can be demonstrated using a 741 op-amp as shown in Fig. 17.35. The input is a 5 V, peak sinusoidal signa. The **Analysis Setup** provides for **Transient** analysis with **Print Step** of **20 ns** and **Final Time** of **3 ms.** Since the input signal is applied to the noninverting input, the output is in-phase with the input. When the input goes above 0 V, the output goes to the positive saturation level,

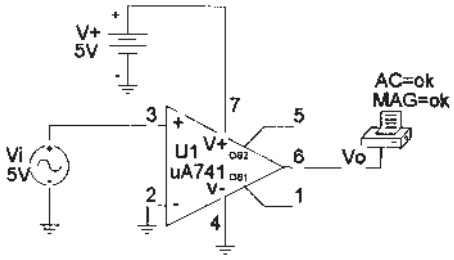


Figure 17.35 Schematic for a comparator.

near +5 V. When the input goes below 0 V, the output goes to the negative saturation level—this being 0 V since the minus voltage input is set to that value. Figure 17.36 shows a **PROBE** output of input and output voltages.

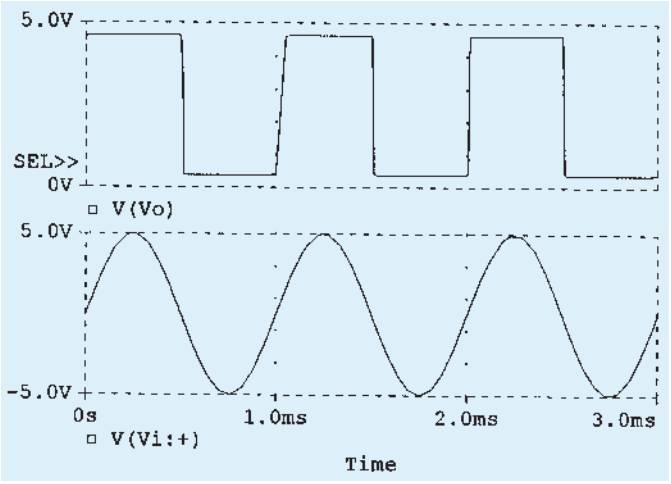


Figure 17.36 Probe output for the comparator of Fig. 17.35.

Program 17.3—Operation of 555 Timer as Oscillator

Figure 17.37 shows a 555 timer connected as an oscillator. Equations (17.3) and (17.4) can be used to calculate the charge and discharge times as follows:

$$T_{\text{high}} = 0.7(R_A + R_B)C = 0.7(7.5\ \text{k}\Omega + 7.15\ \text{k}\Omega)(0.1\ \mu\text{F}) = 1.05\ \text{ms}$$

$$T_{\text{low}} = 0.7R_BC = 0.7(7.5\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.525\ \text{ms}$$

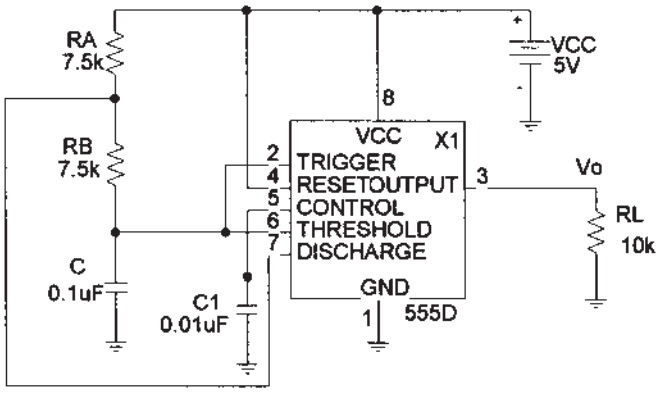


Figure 17.37 Schematic of a 555 timer oscillator.

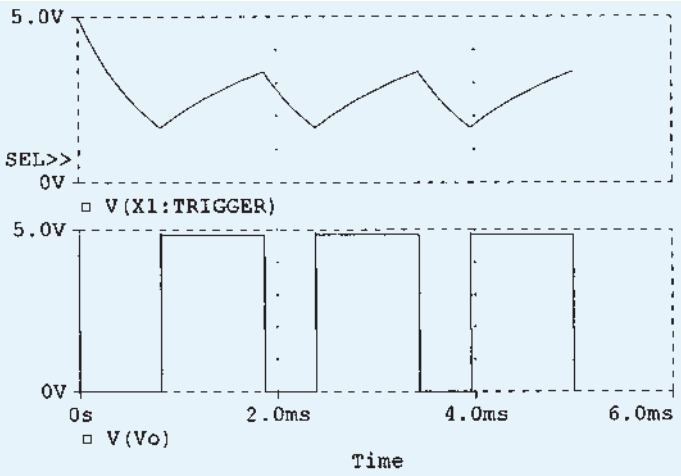


Figure 17.38 Probe output for the 555 oscillator of Fig. 17.37.

The resulting trigger and output waveforms are shown in Fig. 17.38. When the trigger charges to the upper trigger level, the output goes to the low output level of 0 V. The output stays low until the trigger input discharges to the low trigger level, at which time the output goes to the high level of +5 V.

PROBLEMS

§ 17.2 Comparator Unit Operation

1. Draw the diagram of a 741 op-amp operated from ±15-V supplies with $V_i(-) = 0$ V and $V_i(+) = +5$ V. Include terminal pin connections.
2. Sketch the output waveform for the circuit of Fig. 17.39.
3. Draw a circuit diagram of a 311 op-amp showing an input of 10 V rms applied to the inverting input and the plus input to ground. Identify all pin numbers.
4. Draw the resulting output waveform for the circuit of Fig. 17.40.

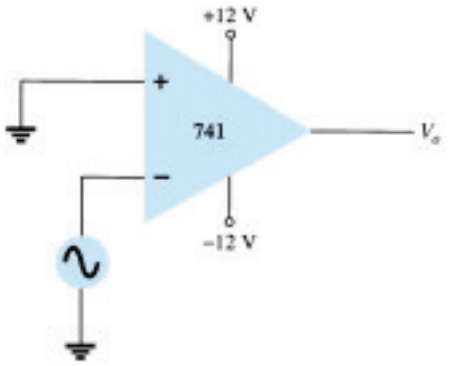


Figure 17.39 Problem 2

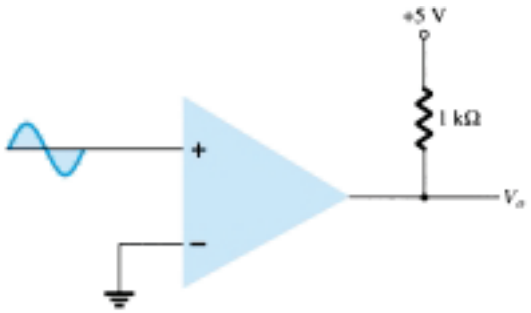


Figure 17.40 Problem 4

5. Draw the circuit diagram of a zero-crossing detector using a 339 comparator stage with ±12-V supplies.

6. Sketch the output waveform for the circuit of Fig. 17.41.

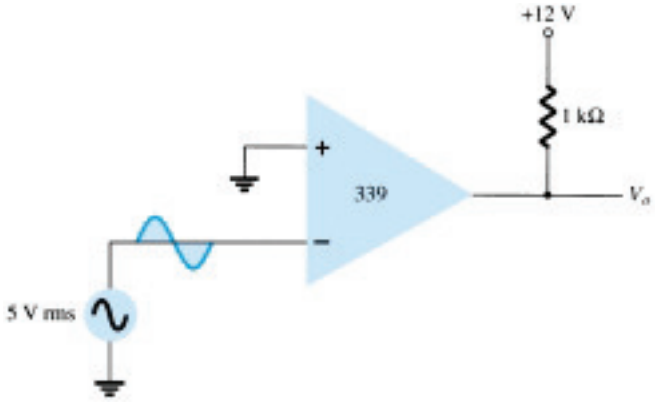


Figure 17.41 Problem 6

* 7. Describe the operation of the circuit in Fig. 17.42.

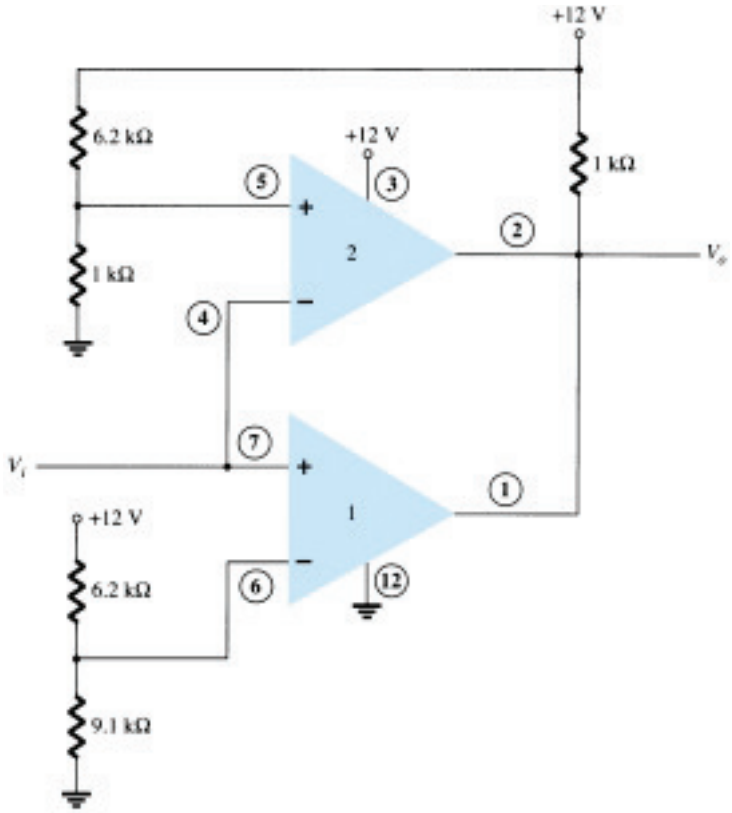


Figure 17.42 Problem 7

§ 17.3 Digital–Analog Converters

8. Sketch a five-stage ladder network using 15-kΩ and 30-kΩ resistors.
9. For a reference voltage of 16 V, calculate the output voltage for an input of 11010 to the circuit of Problem 8.
10. What voltage resolution is possible using a 12-stage ladder network with a 10-V reference voltage?

11. For a dual-slope converter, describe what occurs during the fixed time interval and the count interval.

12. How many count steps occur using a 12-stage digital counter at the output of an ADC?

13. What is the maximum count interval using a 12-stage counter operated at a clock rate of 20 MHz?

§ 17.4 Timer IC Unit Operation

14. Sketch the circuit of a 555 timer connected as an astable multivibrator for operation at 350 kHz. Determine the value of capacitor, C, needed using $R_A = R_B = 7.5\ \text{k}\Omega$.

15. Draw the circuit of a one-shot using a 555 timer to provide one time period of 20 μs. If $R_A = 7.5\ \text{k}\Omega$, what value of C is needed?

16. Sketch the input and output waveforms for a one-shot using a 555 timer triggered by a 10-kHz clock for $R_A = 5.1\ \text{k}\Omega$ and $C = 5$ nF.

§ 17.5 Voltage-Controlled Oscillator

17. Calculate the center frequency of a VCO using a 566 IC as in Fig. 17.22 for $R_1 = 4.7\ \text{k}\Omega$, $R_2 = 1.8\ \text{k}\Omega$, $R_3 = 11\ \text{k}\Omega$, and $C_1 = 0.001\ \mu\text{F}$.

* 18. What frequency range results in the circuit of Fig. 17.23 for $C_1 = 0.001\ \mu\text{F}$?

19. Determine the capacitor needed in the circuit of Fig. 17.22 to obtain a 200-kHz output.

§ 17.6 Phase-Locked Loop

20. Calculate the VCO free-running frequency for the circuit of Fig. 17.26b with $R_1 = 4.7\ \text{k}\Omega$ and $C_1 = 0.001\ \mu\text{F}$.

21. What value of capacitor, C_1, is required in the circuit of Fig. 17.26b to obtain a center frequency of 100 kHz?

22. What is the lock range of the PLL circuit in Fig. 17.26b for $R_1 = 4.7\ \text{k}\Omega$ and $C_1 = 0.001\ \mu\text{F}$?

§ 17.7 Interfacing Circuitry

23. Describe the signal conditions for current-loop and RS-232C interfaces.

24. What is a data bus?

25. What is the difference between open-collector and tri-state output?

§ 17.8 PSpice Windows

* 26. Use Design Center to draw a schematic circuit as in Fig. 17.32, using an LM111 with $V_i = 5$ V rms applied to minus (−) input and +5 V rms applied to plus (+) input. Use Probe to view the output waveform.

* 27. Use Design Center to draw a schematic circuit as in Fig. 17.35. Examine the output listing for the results.

* 28. Use Design Center to draw a 555 oscillator with resulting output with $t_{\text{low}} = 2$ ms, $t_{\text{high}} = 5$ ms.

*Please note: Asterisks indicate more difficult problems.

A_f

CHAPTER

18 Feedback and Oscillator Circuits

18.1 FEEDBACK CONCEPTS

Feedback has been mentioned previously. In particular, feedback was used in op-amp circuits as described in Chapters 14 and 15. Depending on the relative polarity of the signal being fed back into a circuit, one may have negative or positive feedback. Negative feedback results in decreased voltage gain, for which a number of circuit features are improved as summarized below. Positive feedback drives a circuit into oscillation as in various types of oscillator circuits.

A typical feedback connection is shown in Fig. 18.1. The input signal, V_s, is applied to a mixer network, where it is combined with a feedback signal, V_f. The difference of these signals, V_i, is then the input voltage to the amplifier. A portion of the amplifier output, V_o, is connected to the feedback network (β), which provides a reduced portion of the output as feedback signal to the input mixer network.

If the feedback signal is of opposite polarity to the input signal, as shown in Fig. 18.1, negative feedback results. While negative feedback results in reduced overall voltage gain, a number of improvements are obtained, among them being:

1. Higher input impedance.
2. Better stabilized voltage gain.
3. Improved frequency response.
4. Lower output impedance.
5. Reduced noise.
6. More linear operation.

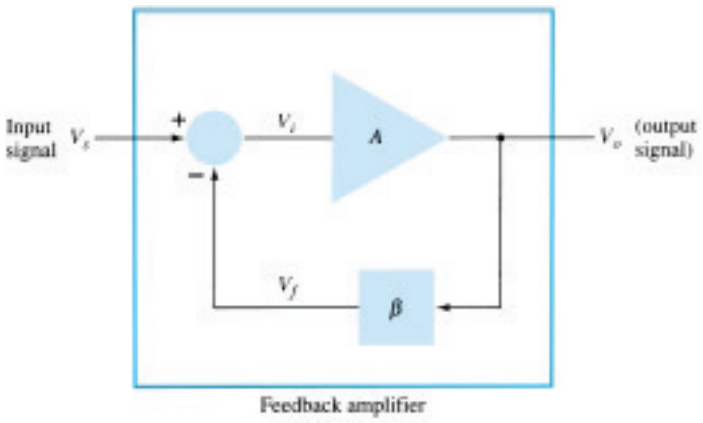


Figure 18.1 Simple block diagram of feedback amplifier.

A_f

18.2 FEEDBACK CONNECTION TYPES

There are four basic ways of connecting the feedback signal. Both *voltage* and *current* can be fed back to the input either in *series* or *parallel*. Specifically, there can be:

1. Voltage-series feedback (Fig. 18.2a).
2. Voltage-shunt feedback (Fig. 18.2b).
3. Current-series feedback (Fig. 18.2c).
4. Current-shunt feedback (Fig. 18.2d).

In the list above, *voltage* refers to connecting the output voltage as input to the feedback network; *current* refers to tapping off some output current through the feedback network. *Series* refers to connecting the feedback signal in series with the input signal voltage; *shunt* refers to connecting the feedback signal in shunt (parallel) with an input current source.

Series feedback connections tend to *increase* the input resistance, while shunt feedback connections tend to *decrease* the input resistance. Voltage feedback tends to *decrease* the output impedance, while current feedback tends to *increase* the output impedance. Typically, higher input and lower output impedances are desired for most

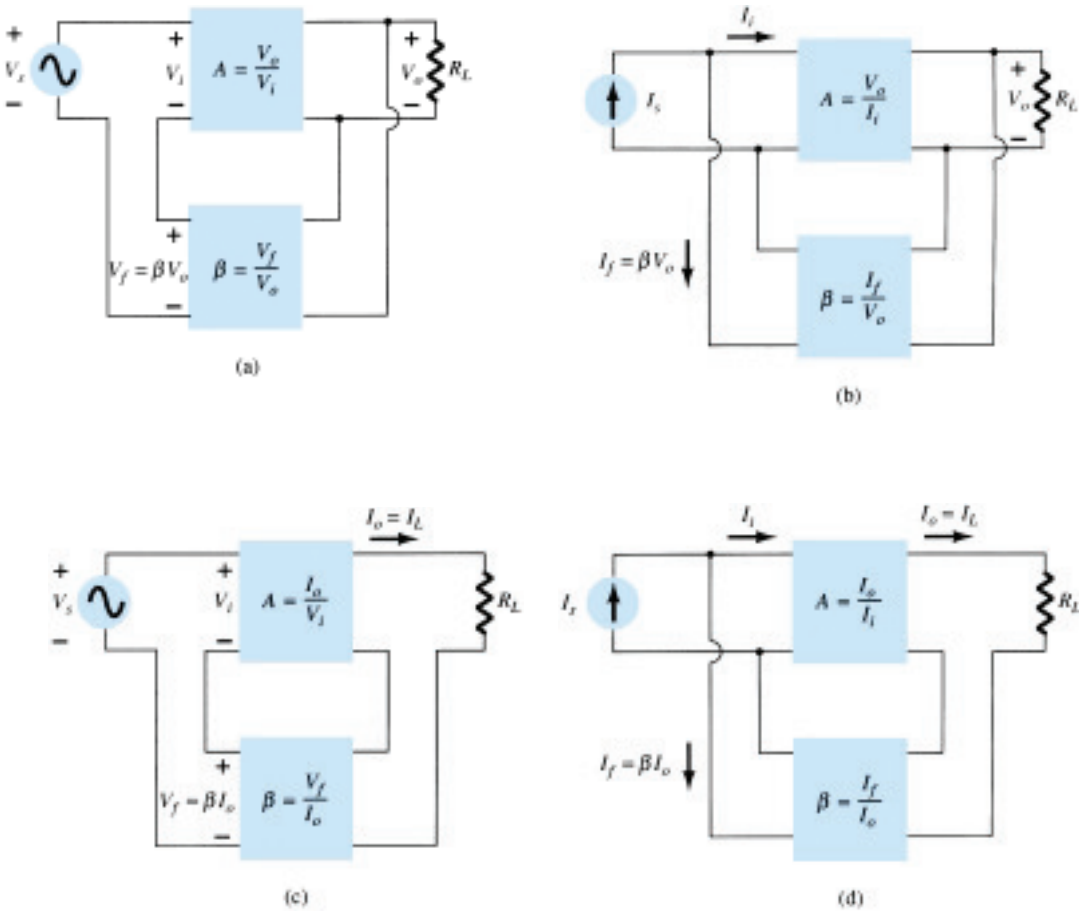


Figure 18.2 Feedback amplifier types: (a) voltage-series feedback, $A_f = V_o/V_s$; (b) voltage-shunt feedback, $A_f = V_o/I_s$; (c) current-series feedback, $A_f = I_o/V_s$; (d) current-shunt feedback, $A_f = I_o/I_s$.

cascade amplifiers. Both of these are provided using the voltage-series feedback connection. We shall therefore concentrate first on this amplifier connection.

Gain with Feedback

In this section we examine the gain of each of the feedback circuit connections of Fig. 18.2. The gain without feedback, A, is that of the amplifier stage. With feedback, β, the overall gain of the circuit is reduced by a factor $(1 + \beta A)$, as detailed below. A summary of the gain, feedback factor, and gain with feedback of Fig. 18.2 is provided for reference in Table 18.1.

TABLE 18.1 Summary of Gain, Feedback, and Gain with Feedback from Fig. 18.2

		Voltage-Series	*Voltage-Shunt*	*Current-Series*	*Current-Shunt*
Gain without feedback	A	$\frac{V_o}{V_i}$	$\frac{V_o}{I_i}$	$\frac{I_o}{V_i}$	$\frac{I_o}{I_i}$
Feedback	β	$\frac{V_f}{V_o}$	$\frac{I_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$
Gain with feedback	A_f	$\frac{V_o}{V_s}$	$\frac{V_o}{I_s}$	$\frac{I_o}{V_s}$	$\frac{I_o}{I_s}$

VOLTAGE-SERIES FEEDBACK

Figure 18.2a shows the voltage-series feedback connection with a part of the output voltage fed back in series with the input signal, resulting in an overall gain reduction. If there is no feedback ($V_f = 0$), the voltage gain of the amplifier stage is

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i} \tag{18.1}$$

If a feedback signal, V_f, is connected in series with the input, then

$$V_i = V_s - V_f$$

Since $$V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$$

then $$(1 + \beta A)V_o = AV_s$$

so that the overall voltage gain *with* feedback is

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}} \tag{18.2}$$

Equation (18.2) shows that the gain *with* feedback is the amplifier gain reduced by the factor $(1 + \beta A)$. This factor will be seen also to affect input and output impedance among other circuit features.

VOLTAGE-SHUNT FEEDBACK

The gain with feedback for the network of Fig. 18.2b is

$$A_f = \frac{V_o}{I_s} = \frac{A\,I_i}{I_i + I_f} = \frac{A\,I_i}{I_i + \beta V_o} = \frac{A\,I_i}{I_i + \beta A\,I_i}$$

$$\boxed{A_f = \frac{A}{1 + \beta A}} \tag{18.3}$$

A_f

Input Impedance with Feedback

VOLTAGE-SERIES FEEDBACK

A more detailed voltage-series feedback connection is shown in Fig. 18.3. The input impedance can be determined as follows:

$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta V_o}{Z_i} = \frac{V_s - \beta A V_i}{Z_i}$$

$$I_i Z_i = V_s - \beta A V_i$$

$$V_s = I_i Z_i + \beta A V_i = I_i Z_i + \beta A I_i Z_i$$

$$\boxed{Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A) Z_i = Z_i(1 + \beta A)} \tag{18.4}$$

The input impedance with series feedback is seen to be the value of the input impedance without feedback multiplied by the factor $(1 + \beta A)$ and applies to both voltage-series (Fig. 18.2a) and current-series (Fig. 18.2c) configurations.

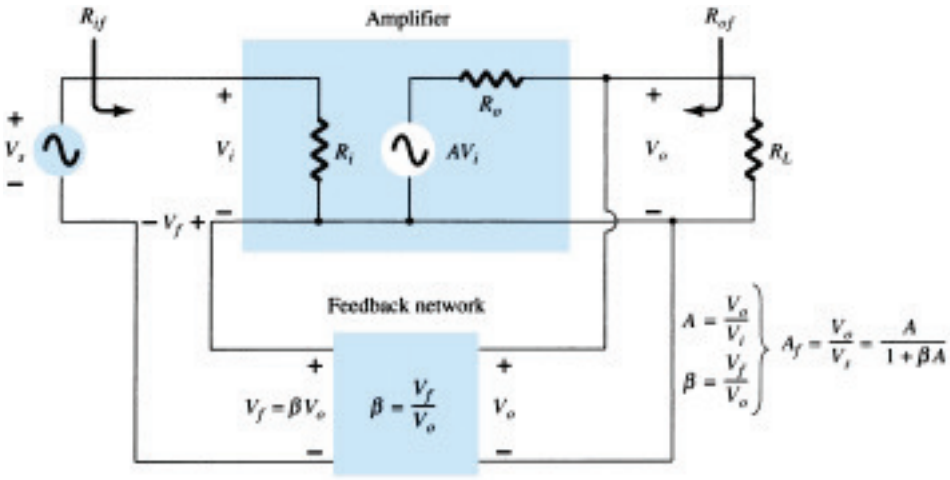


Figure 18.3 Voltage-series feedback connection.

VOLTAGE-SHUNT FEEDBACK

A more detailed voltage-shunt feedback connection is shown in Fig. 18.4. The input impedance can be determined to be

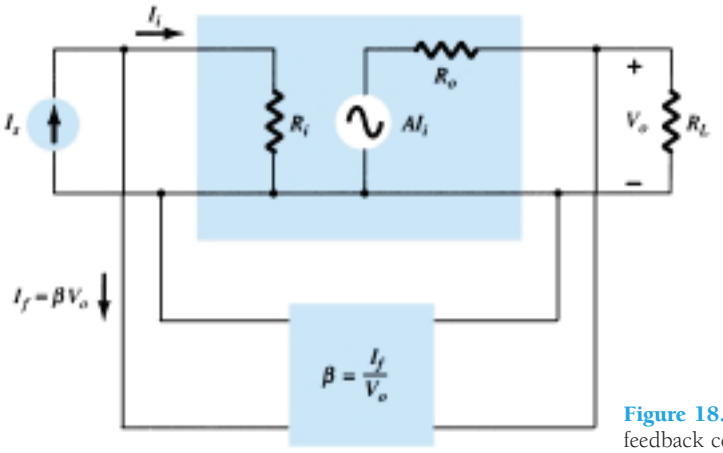


Figure 18.4 Voltage-shunt feedback connection.

$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} = \frac{V_i}{I_i + \beta V_o}$$
$$= \frac{V_i/I_i}{I_i/I_i + \beta V_o/I_i}$$

$$\boxed{Z_{if} = \frac{Z_i}{1 + \beta A}} \tag{18.5}$$

This reduced input impedance applies to the voltage-series connection of Fig. 18.2a and the voltage-shunt connection of Fig. 18.2b.

Output Impedance with Feedback

The output impedance for the connections of Fig. 18.2 are dependent on whether voltage or current feedback is used. For voltage feedback, the output impedance is decreased, while current feedback increases the output impedance.

VOLTAGE-SERIES FEEDBACK

The voltage-series feedback circuit of Fig. 18.3 provides sufficient circuit detail to determine the output impedance with feedback. The output impedance is determined by applying a voltage, V, resulting in a current, I, with V_s shorted out ($V_s = 0$). The voltage V is then

$$V = IZ_o + AV_i$$

For $V_s = 0$, $V_i = -V_f$

so that $V = IZ_o - AV_f = IZ_o - A(\beta V)$

Rewriting the equation as

$$V + \beta AV = IZ_o$$

allows solving for the output resistance with feedback:

$$\boxed{Z_{of} = \frac{V}{I} = \frac{Z_o}{1 + \beta A}} \tag{18.6}$$

Equation (18.6) shows that with voltage-series feedback the output impedance is reduced from that without feedback by the factor $(1 + \beta A)$.

CURRENT-SERIES FEEDBACK

The output impedance with current-series feedback can be determined by applying a signal V to the output with V_s shorted out, resulting in a current I, the ratio of V to I being the output impedance. Figure 18.5 shows a more detailed connection with current-series feedback. For the output part of a current-series feedback connection shown in Fig. 18.5, the resulting output impedance is determined as follows. With $V_s = 0$,

$$V_i = V_f$$
$$I = \frac{V}{Z_o} - AV_i = \frac{V}{Z_o} - AV_f = \frac{V}{Z_o} - A\beta I$$
$$Z_o(1 + \beta A)I = V$$

$$\boxed{Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)} \tag{18.7}$$

A_f

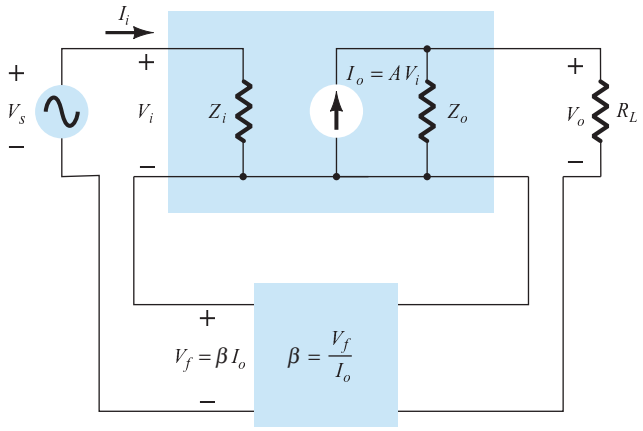


Figure 18.5 Current-series feedback connection.

A summary of the effect of feedback on input and output impedance is provided in Table 18.2.

TABLE 18.2 Effect of Feedback Connection on Input and Output Impedance

	Voltage-Series	*Current-Series*	*Voltage-Shunt*	*Current-Shunt*
Z_{if}	$Z_i(1 + \beta A)$ (increased)	$Z_i(1 + \beta A)$ (increased)	$\frac{Z_i}{1 + \beta A}$ (decreased)	$\frac{Z_i}{1 + \beta A}$ (decreased)
Z_{of}	$\frac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)	$\frac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)

EXAMPLE 18.1

Determine the voltage gain, input, and output impedance with feedback for voltage series feedback having $A = -100$, $R_i = 10\ \text{k}\Omega$, $R_o = 20\ \text{k}\Omega$ for feedback of (a) $\beta = -0.1$ and (b) $\beta = -0.5$.

Solution

Using Eqs. (18.2), (18.4), and (18.6), we obtain

(a) $$A_f = \frac{A}{1 + \beta A} = \frac{-100}{1 + (-0.1)(-100)} = \frac{-100}{11} = \mathbf{-9.09}$$

$$Z_{if} = Z_i\,(1 + \beta A) = 10\ \text{k}\Omega\ (11) = \mathbf{110\ k\Omega}$$

$$Z_{of} = \frac{Z_o}{1 + \beta A} = \frac{20 \times 10^3}{11} = \mathbf{1.82\ k\Omega}$$

(b) $$A_f = \frac{A}{1 + \beta A} = \frac{-100}{1 + (0.5)(100)} = \frac{-100}{51} = \mathbf{-1.96}$$

$$Z_{if} = Z_i\,(1 + \beta A) = 10\ \text{k}\Omega\ (51) = \mathbf{510\ k\Omega}$$

$$Z_{of} = \frac{Z_o}{1 + \beta A} = \frac{20 \times 10^3}{51} = \mathbf{392.16\ \Omega}$$

Example 18.1 demonstrates the trade-off of gain for improved input and output resistance. Reducing the gain by a factor of 11 (from 100 to 9.09) is complemented by a reduced output resistance and increased input resistance by the same factor of 11. Reducing the gain by a factor of 51 provides a gain of only 2 but with input resistance

increased by the factor of 51 (to over 500 kΩ) and output resistance reduced from 20 kΩ to under 400 Ω. Feedback offers the designer the choice of trading away some of the available amplifier gain for other improved circuit features.

Reduction in Frequency Distortion

For a negative-feedback amplifier having $\beta A \gg 1$, the gain with feedback is $A_f \cong 1/\beta$. It follows from this that if the feedback network is purely resistive, the gain with feedback is not dependent on frequency even though the basic amplifier gain is frequency dependent. Practically, the frequency distortion arising because of varying amplifier gain with frequency is considerably reduced in a negative-voltage feedback amplifier circuit.

Reduction in Noise and Nonlinear Distortion

Signal feedback tends to hold down the amount of noise signal (such as power-supply hum) and nonlinear distortion. The factor $(1 + \beta A)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. However, it should be noted that there is a reduction in overall gain (the price required for the improvement in circuit performance). If additional stages are used to bring the overall gain up to the level without feedback, it should be noted that the extra stage(s) might introduce as much noise back into the system as that reduced by the feedback amplifier. This problem can be somewhat alleviated by readjusting the gain of the feedback-amplifier circuit to obtain higher gain while also providing reduced noise signal.

Effect of Negative Feedback on Gain and Bandwidth

In Eq. (18.2), the overall gain with negative feedback is shown to be

$$A_f = \frac{A}{1 + \beta A} \cong \frac{A}{\beta A} = \frac{1}{\beta} \qquad \text{for } \beta A \gg 1$$

As long as $\beta A \gg 1$, the overall gain is approximately $1/\beta$. We should realize that for a practical amplifier (for single low- and high-frequency breakpoints) the open-loop gain drops off at high frequencies due to the active device and circuit capacitances. Gain may also drop off at low frequencies for capacitively coupled amplifier stages. Once the open-loop gain A drops low enough and the factor βA is no longer much larger than 1, the conclusion of Eq. (18.2) that $A_f \cong 1/\beta$ no longer holds true.

Figure 18.6 shows that the amplifier with negative feedback has more bandwidth (B_f) than the amplifier without feedback (B). The feedback amplifier has a higher upper 3-dB frequency and smaller lower 3-dB frequency.

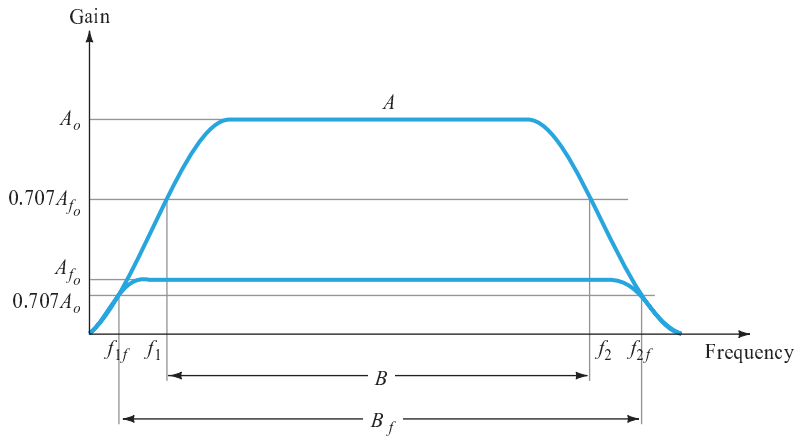


Figure 18.6 Effect of negative feedback on gain and bandwidth.

A_f

It is interesting to note that the use of feedback, while resulting in a lowering of voltage gain, has provided an increase in B and in the upper 3-dB frequency particularly. In fact, the product of gain and frequency remains the same so that the gain–bandwidth product of the basic amplifier is the same value for the feedback amplifier. However, since the feedback amplifier has lower gain, the net operation was to *trade* gain for bandwidth (we use bandwidth for the upper 3-dB frequency since typically $f_2 \gg f_1$).

Gain Stability with Feedback

In addition to the β factor setting a precise gain value, we are also interested in how stable the feedback amplifier is compared to an amplifier without feedback. Differentiating Eq. (18.2) leads to

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1 + \beta A|}\left|\frac{dA}{A}\right| \tag{18.8}$$

$$\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \qquad \text{for } \beta A \gg 1 \tag{18.9}$$

This shows that magnitude of the relative change in gain $\left|\frac{dA_f}{A_f}\right|$ is reduced by the factor $|\beta A|$ compared to that without feedback $\left(\left|\frac{dA}{A}\right|\right)$.

EXAMPLE 18.2

If an amplifier with gain of -1000 and feedback of $\beta = -0.1$ has a gain change of 20% due to temperature, calculate the change in gain of the feedback amplifier.

Solution

Using Eq. (18.9), we get

$$\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| = \left|\frac{1}{-0.1(-1000)}(20\%)\right| = \mathbf{0.2\%}$$

The improvement is 100 times. Thus, while the amplifier gain changes from $|A| = 1000$ by 20%, the gain with feedback changes from $|A_f| = 100$ by only 0.2%.

18.3 PRACTICAL FEEDBACK CIRCUITS

Examples of practical feedback circuits will provide a means of demonstrating the effect feedback has on the various connection types. This section provides only a basic introduction to this topic.

Voltage-Series Feedback

Figure 18.7 shows an FET amplifier stage with voltage-series feedback. A part of the output signal (V_o) is obtained using a feedback network of resistors R_1 and R_2. The feedback voltage V_f is connected in series with the source signal V_s, their difference being the input signal V_i.

Without feedback the amplifier gain is

$$A = \frac{V_o}{V_i} = -g_m R_L \tag{18.10}$$

where R_L is the parallel combination of resistors:

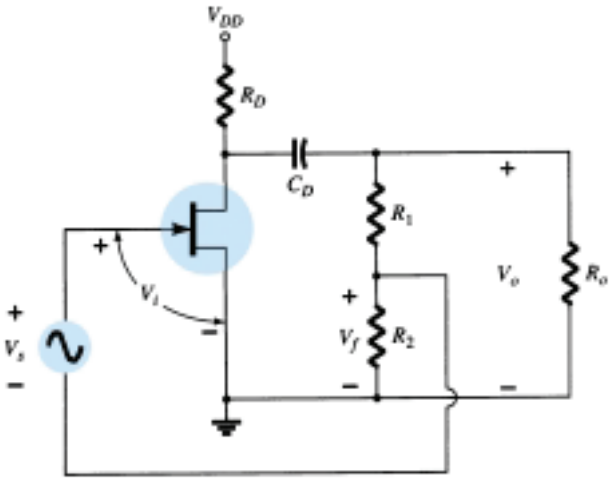


Figure 18.7 FET amplifier stage with voltage-series feedback.

$$R_L = R_D \| R_o \| (R_1 + R_2) \tag{18.11}$$

The feedback network provides a feedback factor of

$$\beta = \frac{V_f}{V_o} = \frac{-R_2}{R_1 + R_2} \tag{18.12}$$

Using the values of A and β above in Eq. (18.2), we find the gain with negative feedback to be

$$A_f = \frac{A}{1 + \beta A} = \frac{-g_m R_L}{1 + [R_2 R_L/(R_1 + R_2)]g_m} \tag{18.13}$$

If $\beta A \gg 1$, we have

$$\boxed{A_f \cong \frac{1}{\beta} = -\frac{R_1 + R_2}{R_2}} \tag{18.14}$$

EXAMPLE 18.3

Calculate the gain without and with feedback for the FET amplifier circuit of Fig. 18.7 and the following circuit values: $R_1 = 80\ \text{k}\Omega$, $R_2 = 20\ \text{k}\Omega$, $R_o = 10\ \text{k}\Omega$, $R_D = 10\ \text{k}\Omega$, and $g_m = 4000\ \mu\text{S}$.

Solution

$$R_L \cong \frac{R_o R_D}{R_o + R_D} = \frac{10\ \text{k}\Omega\ (10\ \text{k}\Omega)}{10\ \text{k}\Omega + 10\ \text{k}\Omega} = 5\ \text{k}\Omega$$

Neglecting 100 kΩ resistance of R_1 and R_2 in series

$$A = -g_m R_L = -(4000 \times 10^{-6}\ \mu\text{S})(5\ \text{k}\Omega) = \mathbf{-20}$$

The feedback factor is

$$\beta = \frac{-R_2}{R_1 + R_2} = \frac{-20\ \text{k}\Omega}{80\ \text{k}\Omega + 20\ \text{k}\Omega} = -0.2$$

The gain with feedback is

$$A_f = \frac{A}{1 + \beta A} = \frac{-20}{1 + (-0.2)(-20)} = \frac{-20}{5} = \mathbf{-4}$$

A_f

Figure 18.8 shows a voltage-series feedback connection using an op-amp. The gain of the op-amp, A, without feedback, is reduced by the feedback factor

$$\beta = \frac{R_2}{R_1 + R_2} \tag{18.15}$$

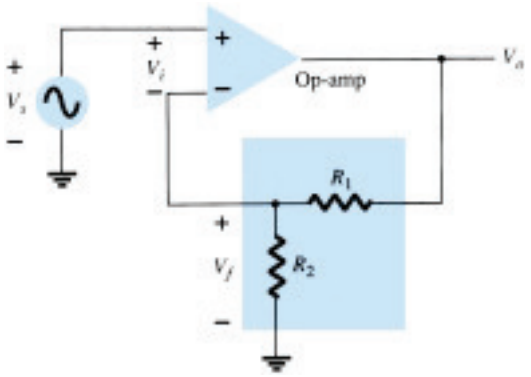


Figure 18.8 Voltage-series feedback in an op-amp connection.

EXAMPLE 18.4

Calculate the amplifier gain of the circuit of Fig. 18.8 for op-amp gain $A = 100{,}000$ and resistances $R_1 = 1.8\ \text{k}\Omega$ and $R_2 = 200\ \Omega$.

Solution

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{200\ \Omega}{200\ \Omega + 1.8\ \text{k}\Omega} = 0.1$$

$$A_f = \frac{A}{1 + \beta A} = \frac{100{,}000}{1 + (0.1)(100{,}000)}$$

$$= \frac{100{,}000}{10{,}001} = 9.999$$

Note that since $\beta A \gg 1$,

$$A_f \cong \frac{1}{\beta} = \frac{1}{0.1} = \mathbf{10}$$

The emitter-follower circuit of Fig. 18.9 provides voltage-series feedback. The signal voltage, V_s, is the input voltage, V_i. The output voltage, V_o, is also the feed-

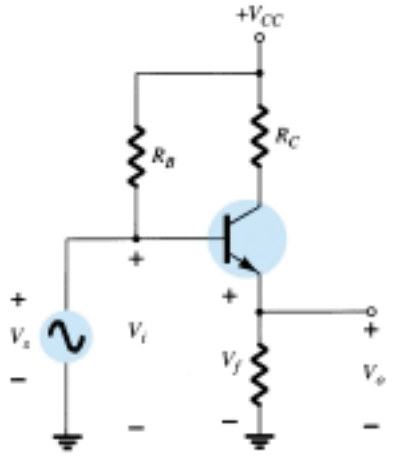


Figure 18.9 Voltage-series feedback circuit (emitter-follower).

back voltage in series with the input voltage. The amplifier, as shown in Fig. 18.9, provides the operation *with* feedback. The operation of the circuit without feedback provides $V_f = 0$, so that

$$A = \frac{V_o}{V_s} = \frac{h_{fe}I_bR_E}{V_s} = \frac{h_{fe}R_E(V_s/h_{ie})}{V_s} = \frac{h_{fe}R_E}{h_{ie}}$$

and

$$\beta = \frac{V_f}{V_o} = 1$$

The operation with feedback then provides that

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A} = \frac{h_{fe}R_E/h_{ie}}{1 + (1)(h_{fe}R_E/h_{ie})}$$

$$= \frac{h_{fe}R_E}{h_{ie} + h_{fe}R_E}$$

For $h_{fe}R_E \gg h_{ie}$,

$$A_f \cong 1$$

Current-Series Feedback

Another feedback technique is to sample the output current (I_o) and return a proportional voltage in series with the input. While stabilizing the amplifier gain, the current-series feedback connection increases input resistance.

Figure 18.10 shows a single transistor amplifier stage. Since the emitter of this stage has an unbypassed emitter, it effectively has current-series feedback. The current through resistor R_E results in a feedback voltage that opposes the source signal applied so that the output voltage V_o is reduced. To remove the current-series feedback, the emitter resistor must be either removed or bypassed by a capacitor (as is usually done).

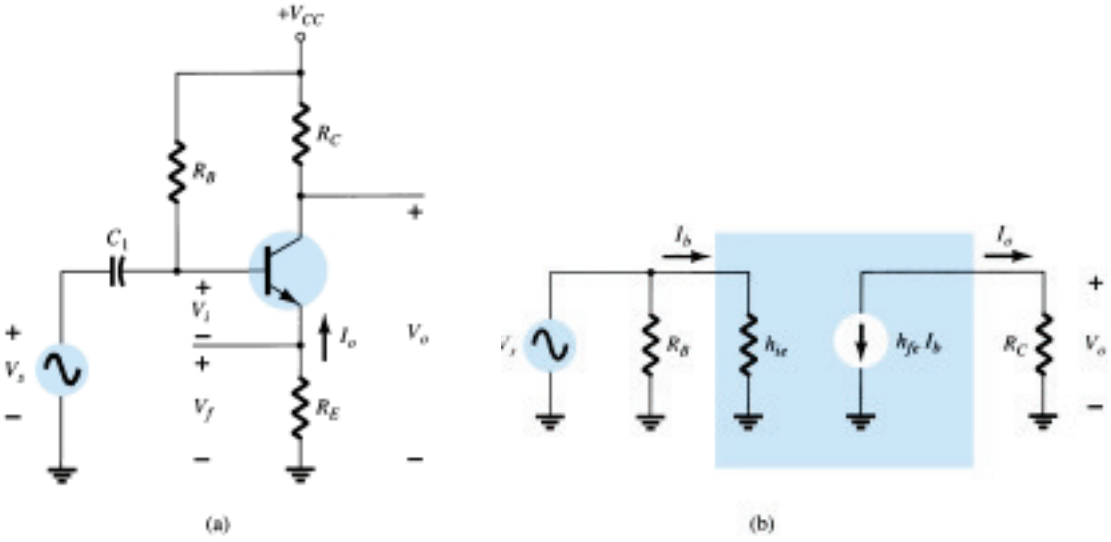


Figure 18.10 Transistor amplifier with unbypassed emitter resistor (R_E) for current-series feedback: (a) amplifier circuit; (b) ac equivalent circuit without feedback.

A_f

WITHOUT FEEDBACK

Referring to the basic format of Fig. 18.2a and summarized in Table 18.1, we have

$$A = \frac{I_o}{V_i} = \frac{-I_b h_{fe}}{I_b h_{ie} + R_E} = \frac{-h_{fe}}{h_{ie} + R_E} \tag{18.16}$$

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_E}{I_o} = -R_E \tag{18.17}$$

The input and output impedances are

$$Z_i = R_B \| (h_{ie} + R_E) \cong h_{ie} + R_E \tag{18.18}$$

$$Z_o = R_C \tag{18.19}$$

WITH FEEDBACK

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} = \frac{-h_{fe}/h_{ie}}{1 + (-R_E)\left(\dfrac{-h_{fe}}{h_{ie} + R_E}\right)} \cong \frac{-h_{fe}}{h_{ie} + h_{fe} R_E} \tag{18.20}$$

The input and output impedance is calculated as specified in Table 18.2.

$$Z_{if} = Z_i\,(1 + \beta A) \cong h_{ie}\left(1 + \frac{h_{fe} R_E}{h_{ie}}\right) = h_{ie} + h_{fe} R_E \tag{18.21}$$

$$Z_{of} = Z_o(1 + \beta A) = R_C\left(1 + \frac{h_{fe} R_E}{h_{ie}}\right) \tag{18.22}$$

The voltage gain (A) with feedback is

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_C}{V_s} = \left(\frac{I_o}{V_s}\right) R_C = A_f R_C \cong \frac{-h_{fe} R_C}{h_{ie} + h_{fe} R_E} \tag{18.23}$$

EXAMPLE 18.5 Calculate the voltage gain of the circuit of Fig. 18.11.

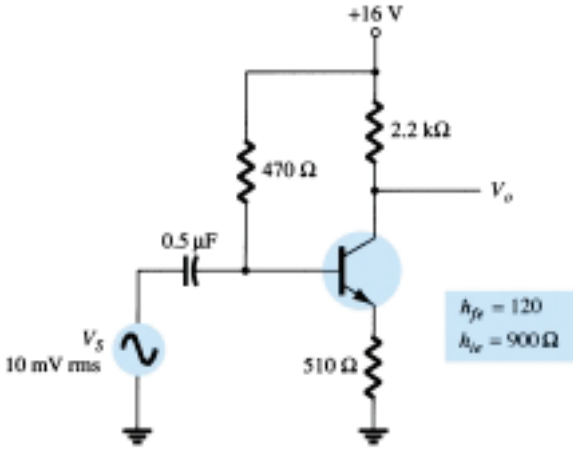


Figure 18.11 BJT amplifier with current-series feedback for Example 18.5.

Solution

Without feedback,

$$A = \frac{I_o}{V_i} = \frac{-h_{fe}}{h_{ie} + R_E} = \frac{-120}{900 + 510} = -0.085$$

$$\beta = \frac{V_f}{I_o} = -R_E = -510$$

The factor $(1 + \beta A)$ is then

$$1 + \beta A = 1 + (-0.085)(-510) = 44.35$$

The gain with feedback is then

$$A_f = \frac{I_o}{V_s} = \frac{A}{1 + \beta A} = \frac{-0.085}{44.35} = -1.92 \times 10^{-3}$$

and the voltage gain with feedback A_{vf} is

$$A_{vf} = \frac{V_o}{V_s} = A_f R_C = (-1.92 \times 10^{-3})(2.2 \times 10^3) = \mathbf{-4.2}$$

Without feedback ($R_E = 0$), the voltage gain is

$$A_v = \frac{-R_C}{r_e} = \frac{-2.2 \times 10^3}{7.5} = \mathbf{-293.3}$$

Voltage-Shunt Feedback

The constant-gain op-amp circuit of Fig. 18.12a provides voltage-shunt feedback. Referring to Fig. 18.2b and Table 18.1 and the op-amp ideal characteristics $I_i = 0$, $V_i = 0$, and voltage gain of infinity, we have

$$A = \frac{V_o}{I_i} = \infty \tag{18.24}$$

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_o} \tag{18.25}$$

The gain with feedback is then

$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i} = \frac{A}{1 + \beta A} = \frac{1}{\beta} = -R_o \tag{18.26}$$

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback,

$$A_{vf} = \frac{V_o}{I_s}\frac{I_s}{V_1} = (-R_o)\frac{1}{R_1} = \frac{-R_o}{R_1} \tag{18.27}$$

The circuit of Fig. 18.13 is a voltage-shunt feedback amplifier using an FET with

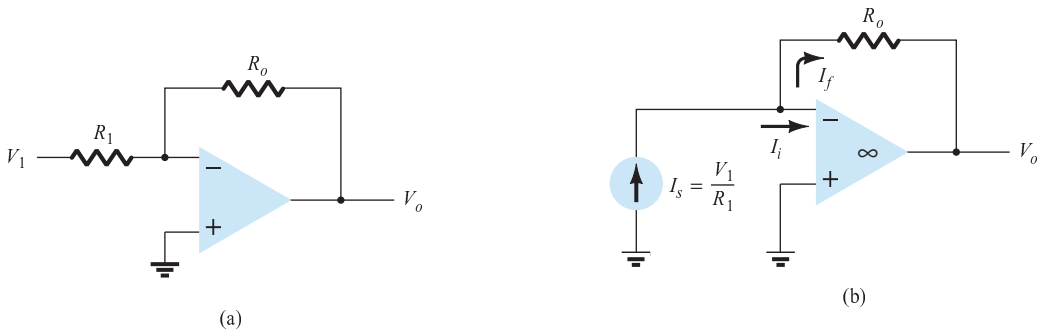


Figure 18.12 Voltage-shunt negative feedback amplifier: (a) constant-gain circuit; (b) equivalent circuit.

A_f

no feedback, $V_f = 0$.

$$A = \frac{V_o}{I_i} \cong -g_m R_D R_S \tag{18.28}$$

The feedback is

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_F} \tag{18.29}$$

With feedback, the gain of the circuit is

$$A_f = \frac{V_o}{I_s} = \frac{A}{1 + \beta A} = \frac{-g_m R_D R_S}{1 + (-1/R_F)(-g_m R_D R_S)}$$

$$= \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S} \tag{18.30}$$

The voltage gain of the circuit with feedback is then

$$A_{vf} = \frac{V_o}{I_s}\frac{I_s}{V_s} = \frac{-g_m R_D R_S R_F}{R_F + g_m R_D R_S}\left(\frac{1}{R_S}\right)$$

$$= \frac{-g_m R_D R_F}{R_F + g_m R_D R_S} = (-g_m R_D)\frac{R_F}{R_F + g_m R_D R_S} \tag{18.31}$$

Calculate the voltage gain with and without feedback for the circuit of Fig. 18.13a

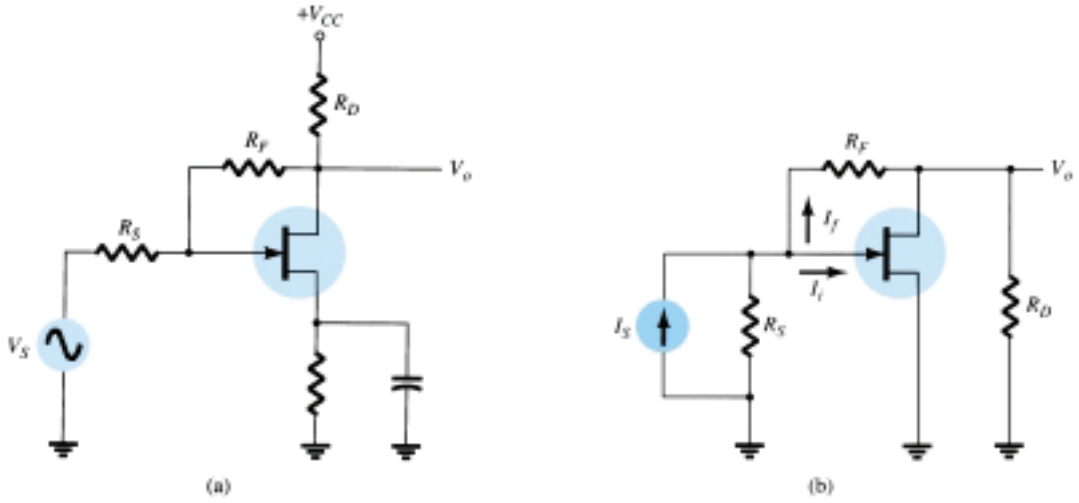


Figure 18.13 Voltage-shunt feedback amplifier using an FET: (a) circuit; (b) equivalent circuit.

EXAMPLE 18.6

with values of $g_m = 5$ mS, $R_D = 5.1$ kΩ, $R_S = 1$ kΩ, and $R_F = 20$ kΩ.

Solution

Without feedback, the voltage gain is

$$A_v = -g_m R_D = -(5 \times 10^{-3})(5.1 \times 10^3) = \mathbf{-25.5}$$

With feedback the gain is reduced to

$$A_{vf} = (-g_m R_D)\frac{R_F}{R_F + g_m R_D R_S}$$

$$= (-25.5)\frac{20 \times 10^3}{(20 \times 10^3) + (5 \times 10^{-3})(5.1 \times 10^3)(1 \times 10^3)}$$

$$= -25.5(0.44) = \mathbf{-11.2}$$

18.4 FEEDBACK AMPLIFIER—PHASE AND FREQUENCY CONSIDERATIONS

So far we have considered the operation of a feedback amplifier in which the feedback signal was *opposite* to the input signal—negative feedback. In any practical circuit this condition occurs only for some mid-frequency range of operation. We know that an amplifier gain will change with frequency, dropping off at high frequencies from the mid-frequency value. In addition, the phase shift of an amplifier will also change with frequency.

If, as the frequency increases, the phase shift changes then some of the feedback signal will *add* to the input signal. It is then possible for the amplifier to break into oscillations due to positive feedback. If the amplifier oscillates at some low or high frequency, it is no longer useful as an amplifier. Proper feedback-amplifier design requires that the circuit be stable at *all* frequencies, not merely those in the range of interest. Otherwise, a transient disturbance could cause a seemingly stable amplifier to suddenly start oscillating.

Nyquist Criterion

In judging the stability of a feedback amplifier, as a function of frequency, the βA product and the phase shift between input and output are the determining factors. One of the most popular techniques used to investigate stability is the Nyquist method. A Nyquist diagram is used to plot gain and phase shift as a function of frequency on a complex plane. The Nyquist plot, in effect, combines the two Bode plots of gain versus frequency and phase shift versus frequency on a single plot. A Nyquist plot is used to quickly show whether an amplifier is stable for all frequencies and how stable the amplifier is relative to some gain or phase-shift criteria.

As a start, consider the *complex plane* shown in Fig. 18.14. A few points of various gain (βA) values are shown at a few different phase-shift angles. By using the positive real axis as reference (0°), a magnitude of $\beta A = 2$ is shown at a phase shift of 0° at point 1. Additionally, a magnitude of $\beta A = 3$ at a phase shift of −135° is

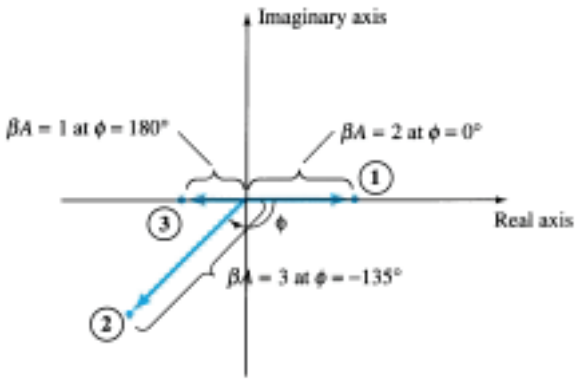


Figure 18.14 Complex plane showing typical gain-phase points.

shown at point 2 and a magnitude/phase of $\beta A = 1$ at 180° is shown at point 3. Thus points on this plot can represent *both* gain magnitude of βA and phase shift. If the points representing gain and phase shift for an amplifier circuit are plotted at increasing frequency, then a Nyquist plot is obtained as shown by the plot in Fig. 18.15. At the origin, the gain is 0 at a frequency of 0 (for *RC*-type coupling). At increasing frequency, points f_1, f_2, and f_3 and the phase shift increased, as did the magnitude of βA. At a representative frequency f_4, the value of A is the vector length from the origin to point f_4 and the phase shift is the angle ϕ. At a frequency f_5, the phase shift is 180°. At higher frequencies, the gain is shown to decrease back to 0.

The Nyquist criterion for stability can be stated as follows:

The amplifier is unstable if the Nyquist curve plotted encloses (encircles) the −1 point, and it is stable otherwise.

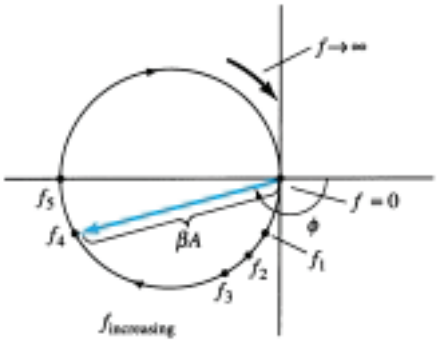


Figure 18.15 Nyquist plot.

An example of the Nyquist criterion is demonstrated by the curves in Fig. 18.16. The Nyquist plot in Fig. 18.16a is stable since it does not encircle the −1 point, whereas that shown in Fig. 18.16b is unstable since the curve does encircle the −1 point. Keep in mind that encircling the −1 point means that at a phase shift of 180° the loop gain (βA) is greater than 1; therefore, the feedback signal is in phase with the input and large enough to result in a larger input signal than that applied, with the result that oscillation occurs.

Gain and Phase Margins

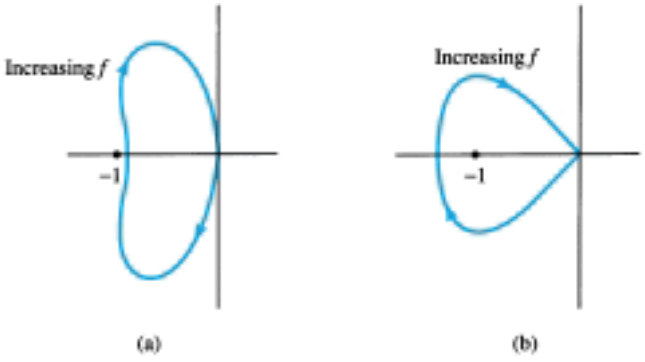


Figure 18.16 Nyquist plots showing stability conditions; (a) stable; (b) unstable.

From the Nyquist criterion, we know that a feedback amplifier is stable if the loop gain (βA) is less than unity (0 dB) when its phase angle is 180°. We can additionally determine some margins of stability to indicate how close to instability the amplifier is. That is, if the gain (βA) is less than unity but, say, 0.95 in value, this would not be as relatively stable as another amplifier having, say, (βA) = 0.7 (both measured at 180°). Of course, amplifiers with loop gains 0.95 and 0.7 are both stable, but one is

closer to instability, if the loop gain increases, than the other. We can define the following terms:

Gain margin (GM) is defined as the negative of the value of $|\beta A|$ in decibels at the frequency at which the phase angle is 180°. Thus, 0 dB, equal to a value of $\beta A = 1$, is on the border of stability and any negative decibel value is stable. The GM may be evaluated in decibels from the curve of Fig. 18.17.

Phase margin (PM) is defined as the angle of 180° minus the magnitude of the angle at which the value $|\beta A|$ is unity (0 dB). The PM may also be evaluated directly from the curve of Fig. 18.17.

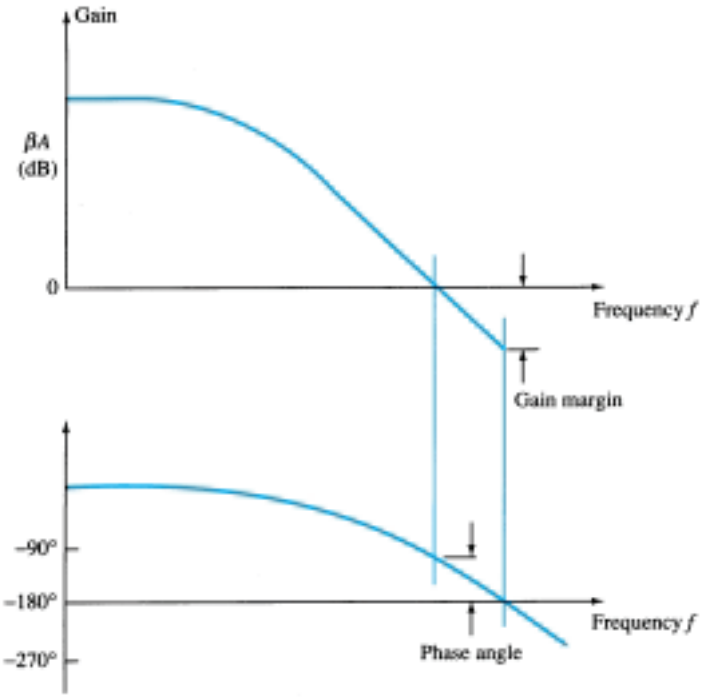


Figure 18.17 Bode plots showing gain and phase margins.

18.5 OSCILLATOR OPERATION

The use of positive feedback that results in a feedback amplifier having closed-loop gain $|A_f|$ greater than 1 and satisfies the phase conditions will result in operation as an oscillator circuit. An oscillator circuit then provides a varying output signal. If the output signal varies sinusoidally, the circuit is referred to as a *sinusoidal oscillator.* If the output voltage rises quickly to one voltage level and later drops quickly to another voltage level, the circuit is generally referred to as a *pulse* or *square-wave oscillator*.

To understand how a feedback circuit performs as an oscillator, consider the feedback circuit of Fig. 18.18. When the switch at the amplifier input is open, no oscillation occurs. Consider that we have a *fictitious* voltage at the amplifier input (V_i). This results in an output voltage $V_o = AV_i$ after the amplifier stage and in a voltage $V_f = \beta(AV_i)$ after the feedback stage. Thus, we have a feedback voltage $V_f = \beta AV_i$, where βA is referred to as the *loop gain.* If the circuits of the base amplifier and feedback network provide βA of a correct magnitude and phase, V_f can be made equal to

A_f

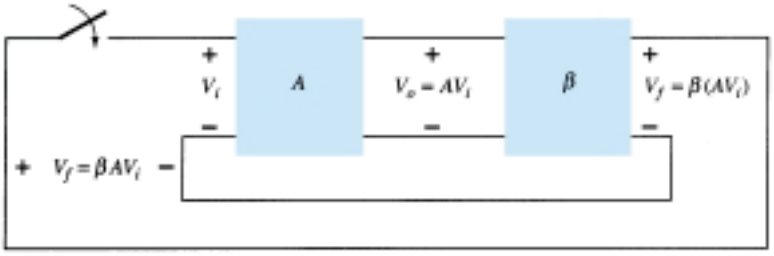


Figure 18.18 Feedback circuit used as an oscillator.

V_i. Then, when the switch is closed and fictitious voltage V_i is removed, the circuit will continue operating since the feedback voltage is sufficient to drive the amplifier and feedback circuits resulting in a proper input voltage to sustain the loop operation. The output waveform will still exist after the switch is closed if the condition

$$\beta A = 1 \tag{18.32}$$

is met. This is known as the *Barkhausen criterion* for oscillation.

In reality, no input signal is needed to start the oscillator going. Only the condition $\beta A = 1$ must be satisfied for self-sustained oscillations to result. In practice, βA is made greater than 1 and the system is started oscillating by amplifying noise voltage, which is always present. Saturation factors in the practical circuit provide an "average" value of βA of 1. The resulting waveforms are never exactly sinusoidal. However, the closer the value βA is to exactly 1, the more nearly sinusoidal is the waveform. Figure 18.19 shows how the noise signal results in a buildup of a steady-state oscillation condition.

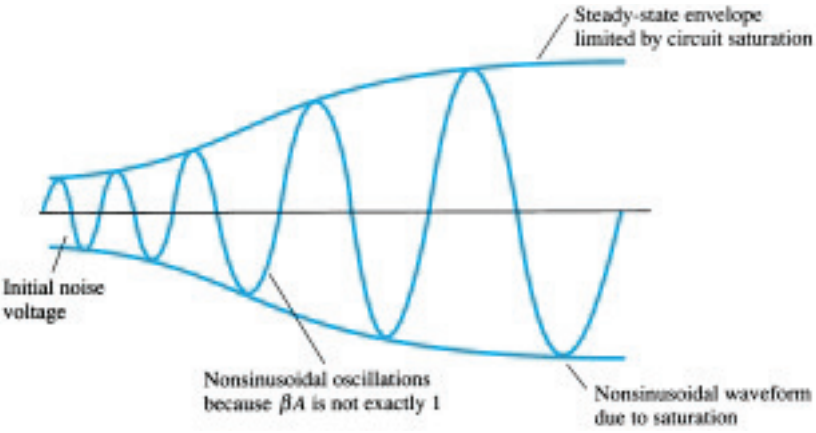


Figure 18.19 Buildup of steady-state oscillations.

Another way of seeing how the feedback circuit provides operation as an oscillator is obtained by noting the denominator in the basic feedback equation (18.2), $A_f = A/(1 + \beta A)$. When $\beta A = -1$ or magnitude 1 at a phase angle of 180°, the denominator becomes 0 and the gain with feedback, A_f, becomes infinite. Thus, an infinitesimal signal (noise voltage) can provide a measurable output voltage, and the circuit acts as an oscillator even without an input signal.

The remainder of this chapter is devoted to various oscillator circuits that use a variety of components. Practical considerations are included so that workable circuits in each of the various cases are discussed.

18.6 PHASE-SHIFT OSCILLATOR

An example of an oscillator circuit that follows the basic development of a feedback circuit is the *phase-shift oscillator*. An idealized version of this circuit is shown in Fig. 18.20. Recall that the requirements for oscillation are that the loop gain, βA, is greater than unity *and* that the phase shift around the feedback network is 180° (providing positive feedback). In the present idealization, we are considering the feedback network to be driven by a perfect source (zero source impedance) and the output of the feedback network to be connected into a perfect load (infinite load impedance). The idealized case will allow development of the theory behind the operation of the phase-shift oscillator. Practical circuit versions will then be considered.

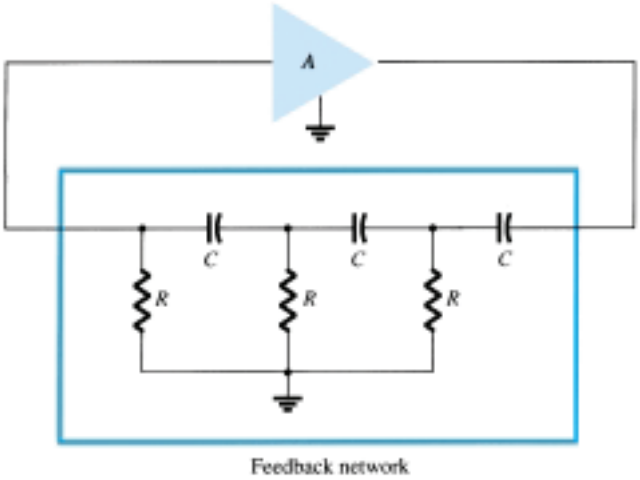


Figure 18.20 Idealized phase-shift oscillator.

Concentrating our attention on the phase-shift network, we are interested in the attenuation of the network at the frequency at which the phase shift is exactly 180°. Using classical network analysis, we find that

$$f = \frac{1}{2\pi RC\sqrt{6}} \tag{18.33}$$

$$\beta = \frac{1}{29} \tag{18.34}$$

and the phase shift is 180°.

For the loop gain βA to be greater than unity, the gain of the amplifier stage must be greater than $1/\beta$ or 29:

$$A > 29 \tag{18.35}$$

When considering the operation of the feedback network, one might naively select the values of R and C to provide (at a specific frequency) 60°-phase shift per section for three sections, resulting in a 180° phase shift, as desired. This, however, is not the case, since each section of the RC in the feedback network loads down the previous one. The net result that the *total* phase shift be 180° is all that is important. The frequency given by Eq. (18.33) is that at which the *total* phase shift is 180°. If one measured the phase shift per RC section, each section would not provide the same phase shift (although the overall phase shift is 180°). If it were desired to obtain exactly a 60° phase shift for each of three stages, then emitter-follower stages would be needed for each RC section to prevent each from being loaded from the following circuit.

A_f

FET Phase-Shift Oscillator

A practical version of a phase-shift oscillator circuit is shown in Fig. 18.21a. The circuit is drawn to show clearly the amplifier and feedback network. The amplifier stage is self-biased with a capacitor bypassed source resistor R_S and a drain bias resistor R_D. The FET device parameters of interest are g_m and r_d. From FET amplifier theory, the amplifier gain magnitude is calculated from

$$|A| = g_m R_L \tag{18.36}$$

where R_L in this case is the parallel resistance of R_D and r_d

$$R_L = \frac{R_D r_d}{R_D + r_d} \tag{18.37}$$

We shall assume as a very good approximation that the input impedance of the FET amplifier stage is infinite. This assumption is valid as long as the oscillator operating frequency is low enough so that FET capacitive impedances can be neglected. The output impedance of the amplifier stage given by R_L should also be small compared to the impedance seen looking into the feedback network so that no attenuation due to loading occurs. In practice, these considerations are not always negligible, and the amplifier stage gain is then selected somewhat larger than the needed factor of 29 to assure oscillator action.

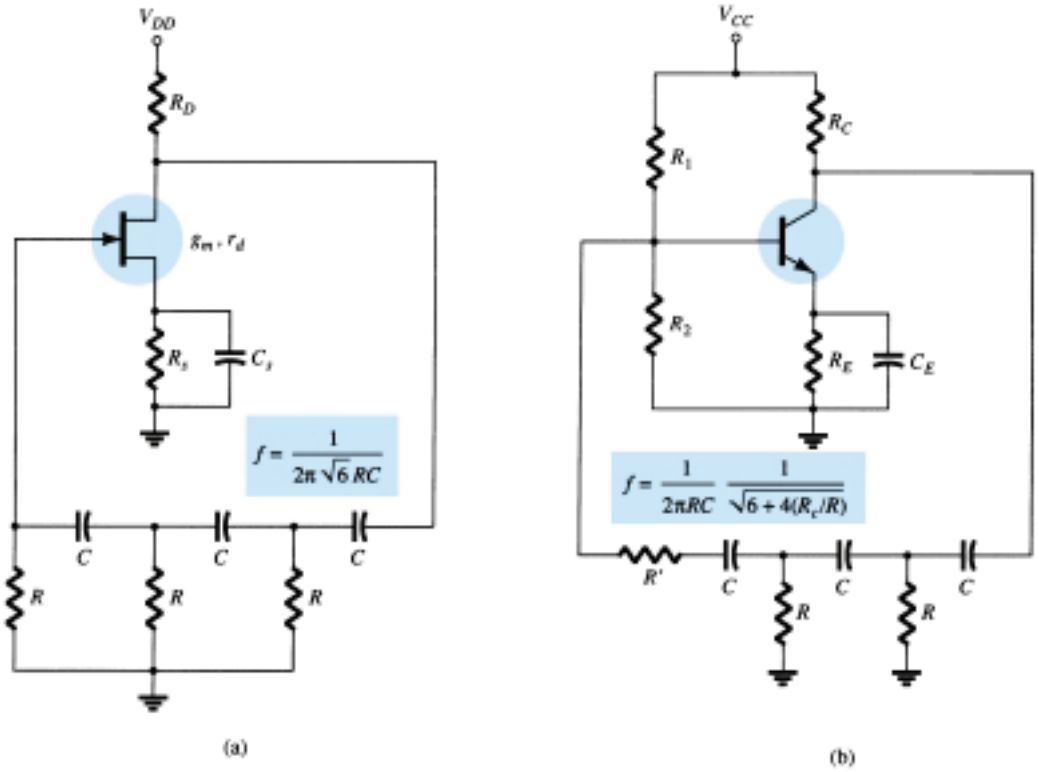


Figure 18.21 Practical phase-shift oscillator circuits: (a) FET version; (b) BJT version.

EXAMPLE 18.7

It is desired to design a phase-shift oscillator (as in Fig. 18.21a) using an FET having $g_m = 5000\ \mu S$, $r_d = 40\ k\Omega$, and feedback circuit value of $R = 10\ k\Omega$. Select the value of C for oscillator operation at 1 kHz and R_D for $A > 29$ to ensure oscillator action.

Solution

Equation (18.33) is used to solve for the capacitor value. Since $f = 1/2\pi RC\sqrt{6}$, we can solve for C:

$$C = \frac{1}{2\pi Rf\sqrt{6}} = \frac{1}{(6.28)(10 \times 10^3)(1 \times 10^3)(2.45)} = \mathbf{6.5\ nF}$$

Using Eq. (18.36), we solve for R_L to provide a gain of, say, $A = 40$ (this allows for some loading between R_L and the feedback network input impedance):

$$|A| = g_m R_L$$

$$R_L = \frac{|A|}{g_m} = \frac{40}{5000 \times 10^{-6}} = 8\ \text{k}\Omega$$

Using Eq. (18.37), we solve for $R_D = \mathbf{10\ k\Omega}$.

Transistor Phase-Shift Oscillator

If a transistor is used as the active element of the amplifier stage, the output of the feedback network is loaded appreciably by the relatively low input resistance (h_{ie}) of the transistor. Of course, an emitter-follower input stage followed by a common-emitter amplifier stage could be used. If a single transistor stage is desired, however, the use of voltage-shunt feedback (as shown in Fig. 18.21b) is more suitable. In this connection, the feedback signal is coupled through the feedback resistor R' in *series* with the amplifier stage input resistance (R_i).

Analysis of the ac circuit provides the following equation for the resulting oscillator frequency:

$$f = \frac{1}{2\pi RC}\frac{1}{\sqrt{6 + 4(R_C/R)}} \tag{18.38}$$

For the loop gain to be greater than unity, the requirement on the current gain of the transistor is found to be

$$h_{fe} > 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R} \tag{18.39}$$

IC Phase-Shift Oscillator

As IC circuits have become more popular, they have been adapted to operate in oscillator circuits. One need buy only an op-amp to obtain an amplifier circuit of stabilized gain setting and incorporate some means of signal feedback to produce an oscillator circuit. For example, a phase-shift oscillator is shown in Fig. 18.22. The output

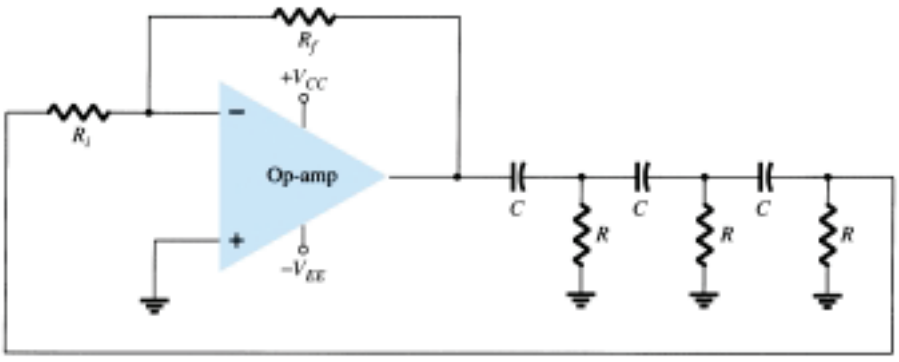


Figure 18.22 Phase-shift oscillator using op-amp.

of the op-amp is fed to a three-stage *RC* network, which provides the needed 180° of phase shift (at an attenuation factor of 1/29). If the op-amp provides gain (set by resistors R_i and R_f) of greater than 29, a loop gain greater than unity results and the circuit acts as an oscillator [oscillator frequency is given by Eq. (18.33)].

18.7 WIEN BRIDGE OSCILLATOR

A practical oscillator circuit uses an op-amp and *RC* bridge circuit, with the oscillator frequency set by the *R* and *C* components. Figure 18.23 shows a basic version of a Wien bridge oscillator circuit. Note the basic bridge connection. Resistors R_1 and R_2 and capacitors C_1 and C_2 form the frequency-adjustment elements, while resistors R_3 and R_4 form part of the feedback path. The op-amp output is connected as the bridge input at points *a* and *c*. The bridge circuit output at points *b* and *d* is the input to the op-amp.

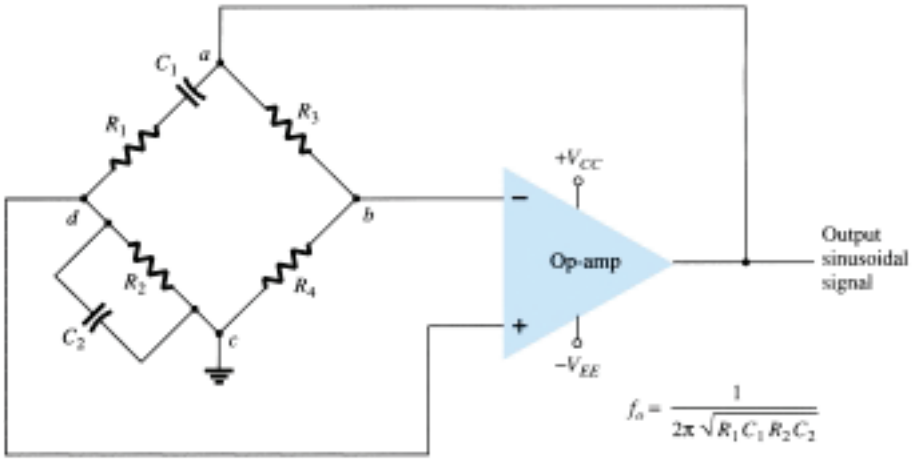


Figure 18.23 Wien bridge oscillator circuit using op-amp amplifier.

Neglecting loading effects of the op-amp input and output impedances, the analysis of the bridge circuit results in

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \tag{18.40}$$

and

$$\boxed{f_o = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}} \tag{18.41}$$

If, in particular, the values are $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the resulting oscillator frequency is

$$f_o = \frac{1}{2\pi RC} \tag{18.42}$$

and

$$\frac{R_3}{R_4} = 2 \tag{18.43}$$

Thus a ratio of R_3 to R_4 greater than 2 will provide sufficient loop gain for the circuit to oscillate at the frequency calculated using Eq. (18.42).

EXAMPLE 18.8

Calculate the resonant frequency of the Wien bridge oscillator of Fig. 18.24.

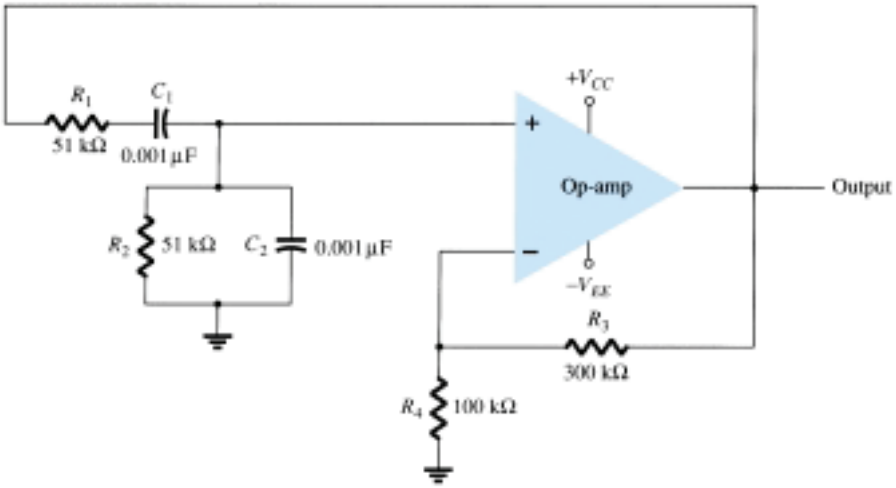


Figure 18.24 Wien bridge oscillator circuit for Example 18.8.

Solution

Using Eq. (18.42) yields

$$f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi\,(51 \times 10^3)(0.001 \times 10^{-6})} = \mathbf{3120.7\ Hz}$$

EXAMPLE 18.9

Design the RC elements of a Wien bridge oscillator as in Fig. 18.24 for operation at $f_o = 10$ kHz.

Solution

Using equal values of R and C we can select $R = 100\ \text{k}\Omega$ and calculate the required value of C using Eq. (18.42):

$$C = \frac{1}{2\pi f_o R} = \frac{1}{6.28(10 \times 10^3)(100 \times 10^3)} = \frac{10^{-9}}{6.28} = \mathbf{159\ pF}$$

We can use $R_3 = 300\ \text{k}\Omega$ and $R_4 = 100\ \text{k}\Omega$ to provide a ratio R_3/R_4 greater than 2 for oscillation to take place.

18.8 TUNED OSCILLATOR CIRCUIT

Tuned-Input, Tuned-Output Oscillator Circuits

A variety of circuits can be built using that shown in Fig. 18.25 by providing tuning in both the input and output sections of the circuit. Analysis of the circuit of Fig. 18.25 reveals that the following types of oscillators are obtained when the reactance elements are as designated:

A_f

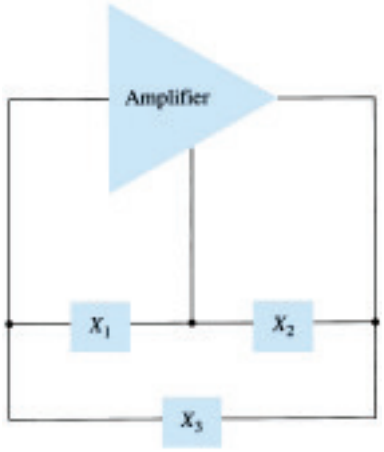


Figure 18.25 Basic configuration of resonant circuit oscillator.

	Reactance Element		
Oscillator Type	X_1	X_2	X_3
Colpitts oscillator	C	C	L
Hartley oscillator	L	L	C
Tuned input, tuned output	LC	LC	—

Colpitts Oscillator

FET COLPITTS OSCILLATOR

A practical version of an FET Colpitts oscillator is shown in Fig. 18.26. The circuit is basically the same form as shown in Fig. 18.25 with the addition of the components needed for dc bias of the FET amplifier. The oscillator frequency can be found to be

$$f_o = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}} \tag{18.44}$$

where

$$C_{\text{eq}} = \frac{C_1 C_2}{C_1 + C_2} \tag{18.45}$$

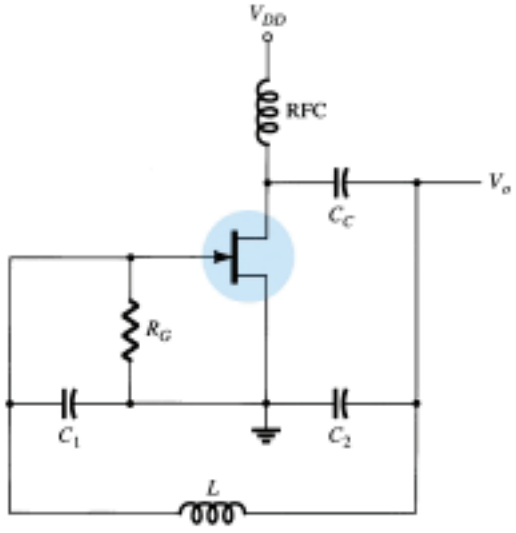


Figure 18.26 FET Colpitts oscillator.

TRANSISTOR COLPITTS OSCILLATOR

A transistor Colpitts oscillator circuit can be made as shown in Fig. 18.27. The circuit frequency of oscillation is given by Eq. (18.44).

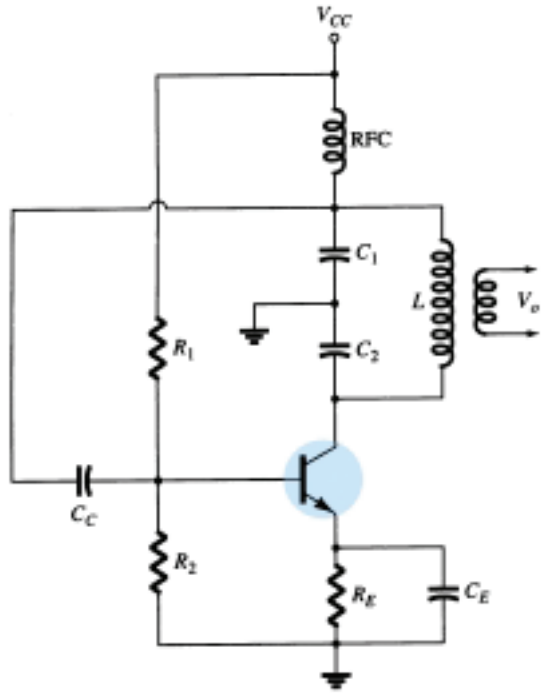


Figure 18.27 Transistor Colpitts oscillator.

IC COLPITTS OSCILLATOR

An op-amp Colpitts oscillator circuit is shown in Fig. 18.28. Again, the op-amp provides the basic amplification needed while the oscillator frequency is set by an LC feedback network of a Colpitts configuration. The oscillator frequency is given by Eq. (18.44).

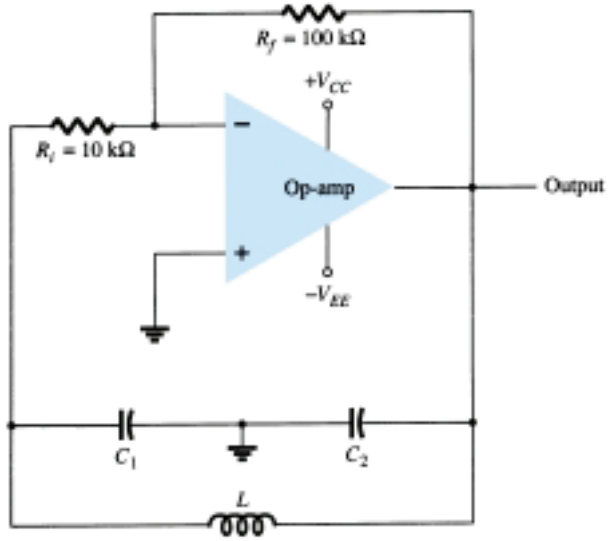


Figure 18.28 Op-amp Colpitts oscillator.

Hartley Oscillator

If the elements in the basic resonant circuit of Fig. 18.25 are X_1 and X_2 (inductors) and X_3 (capacitor), the circuit is a Hartley oscillator.

A_f

FET HARTLEY OSCILLATOR

An FET Hartley oscillator circuit is shown in Fig. 18.29. The circuit is drawn so that the feedback network conforms to the form shown in the basic resonant circuit (Fig. 18.25). Note, however, that inductors L_1 and L_2 have a mutual coupling, M, which must be taken into account in determining the equivalent inductance for the resonant tank circuit. The circuit frequency of oscillation is then given approximately by

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C}} \tag{18.46}$$

with

$$L_{eq} = L_1 + L_2 + 2M \tag{18.47}$$

TRANSISTOR HARTLEY OSCILLATOR

Figure 18.30 shows a transistor Hartley oscillator circuit. The circuit operates at a frequency given by Eq. (18.46).

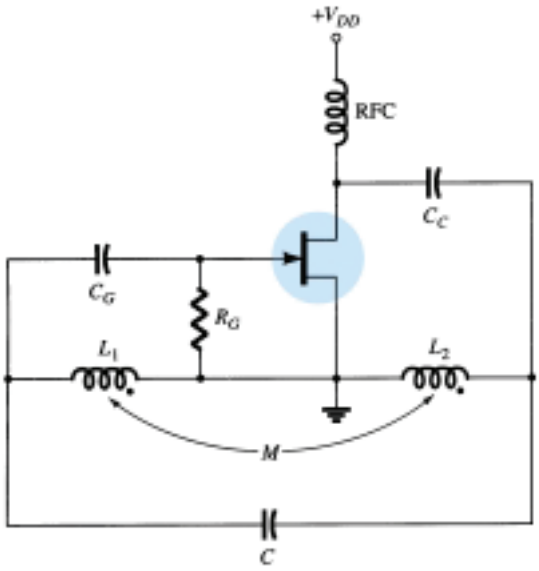


Figure 18.29 FET Hartley oscillator.

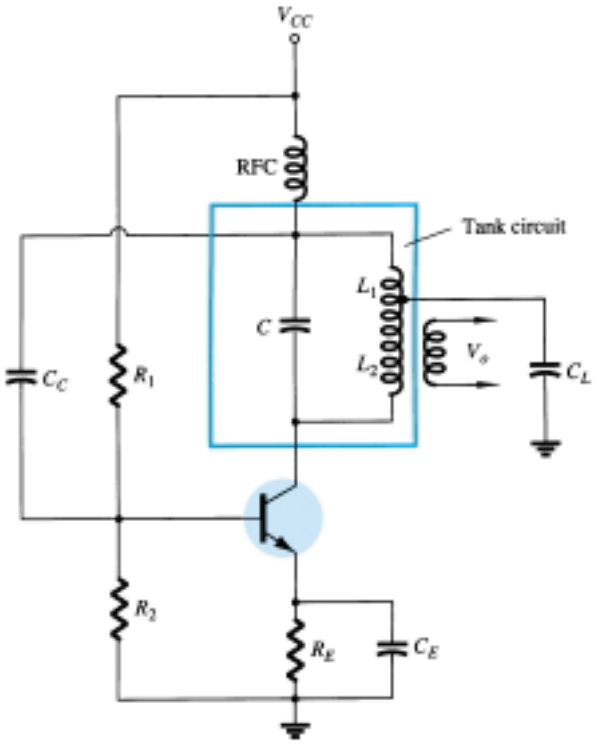


Figure 18.30 Transistor Hartley oscillator circuit.

18.9 CRYSTAL OSCILLATOR

A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as a resonant tank circuit. The crystal (usually quartz) has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used whenever great stability is required, such as in communication transmitters and receivers.

Characteristics of a Quartz Crystal

A quartz crystal (one of a number of crystal types) exhibits the property that when mechanical stress is applied across the faces of the crystal, a difference of potential develops across opposite faces of the crystal. This property of a crystal is called the *piezoelectric effect.* Similarly, a voltage applied across one set of faces of the crystal causes mechanical distortion in the crystal shape.

When alternating voltage is applied to a crystal, mechanical vibrations are set up—these vibrations having a natural resonant frequency dependent on the crystal. Although the crystal has electromechanical resonance, we can represent the crystal action by an equivalent electrical resonant circuit as shown in Fig. 18.31. The inductor L and capacitor C represent electrical equivalents of crystal mass and compliance, while resistance R is an electrical equivalent of the crystal structure's internal friction. The shunt capacitance C_M represents the capacitance due to mechanical mounting of the crystal. Because the crystal losses, represented by R, are small, the equivalent crystal Q (quality factor) is high—typically 20,000. Values of Q up to almost 10^6 can be achieved by using crystals.

The crystal as represented by the equivalent electrical circuit of Fig. 18.31 can have two resonant frequencies. One resonant condition occurs when the reactances of the series RLC leg are equal (and opposite). For this condition, the *series-resonant* impedance is very low (equal to R). The other resonant condition occurs at a higher frequency when the reactance of the series-resonant leg equals the reactance of capacitor C_M. This is a parallel resonance or antiresonance condition of the crystal. At this frequency, the crystal offers a very high impedance to the external circuit. The impedance versus frequency of the crystal is shown in Fig. 18.32. In order to use the crystal properly, it must be connected in a circuit so that its low impedance in the series-resonant operating mode or high impedance in the antiresonant operating mode is selected.

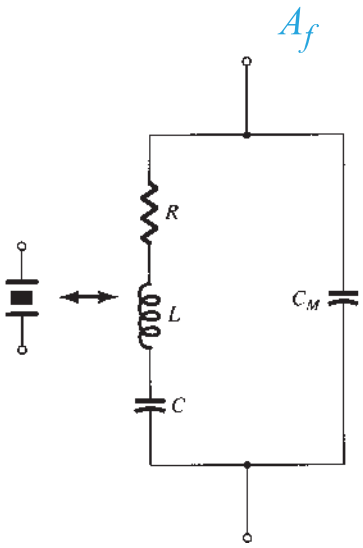


Figure 18.31 Electrical equivalent circuit of a crystal.

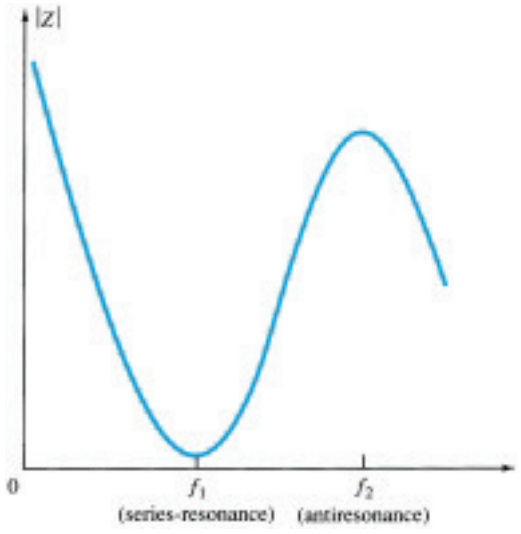


Figure 18.32 Crystal impedance versus frequency.

Series-Resonant Circuits

To excite a crystal for operation in the series-resonant mode, it may be connected as a series element in a feedback path. At the series-resonant frequency of the crystal, its impedance is smallest and the amount of (positive) feedback is largest. A typical transistor circuit is shown in Fig. 18.33. Resistors R_1, R_2, and R_E provide a voltage-divider stabilized dc bias circuit. Capacitor C_E provides ac bypass of the emitter re-

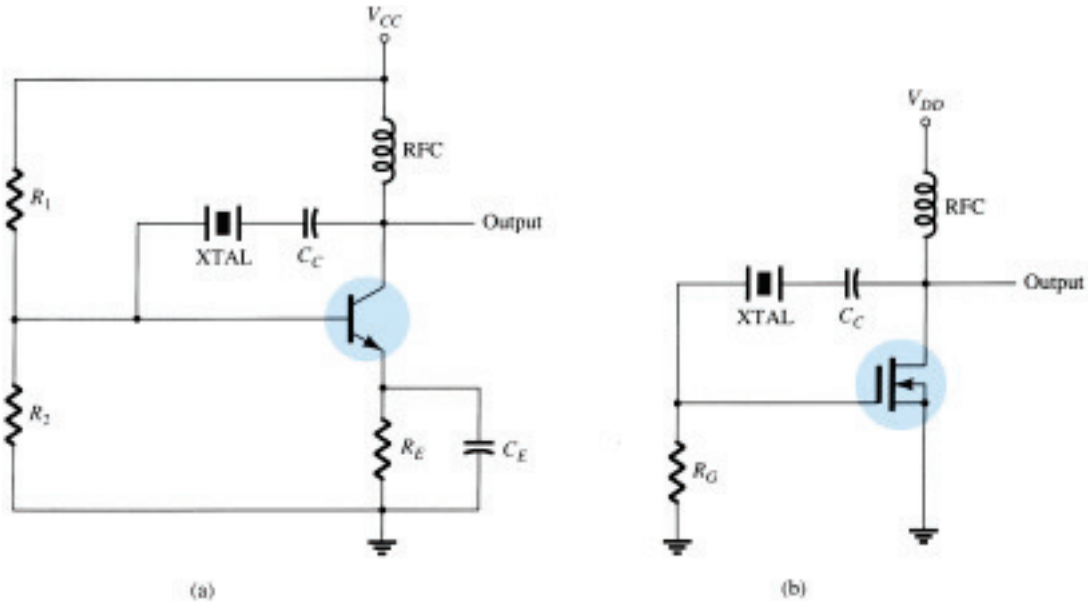


Figure 18.33 Crystal-controlled oscillator using crystal in series-feedback path: (a) BJT circuit; (b) FET circuit.

sistor, and the RFC coil provides for dc bias while decoupling any ac signal on the power lines from affecting the output signal. The voltage feedback from collector to base is a maximum when the crystal impedance is minimum (in series-resonant mode). The coupling capacitor C_C has negligible impedance at the circuit operating frequency but blocks any dc between collector and base.

The resulting circuit frequency of oscillation is set, then, by the series-resonant frequency of the crystal. Changes in supply voltage, transistor device parameters, and so on have no effect on the circuit operating frequency, which is held stabilized by the crystal. The circuit frequency stability is set by the crystal frequency stability, which is good.

Parallel-Resonant Circuits

Since the parallel-resonant impedance of a crystal is a maximum value, it is connected in shunt. At the parallel-resonant operating frequency, a crystal appears as an inductive reactance of largest value. Figure 18.34 shows a crystal connected as the induc-

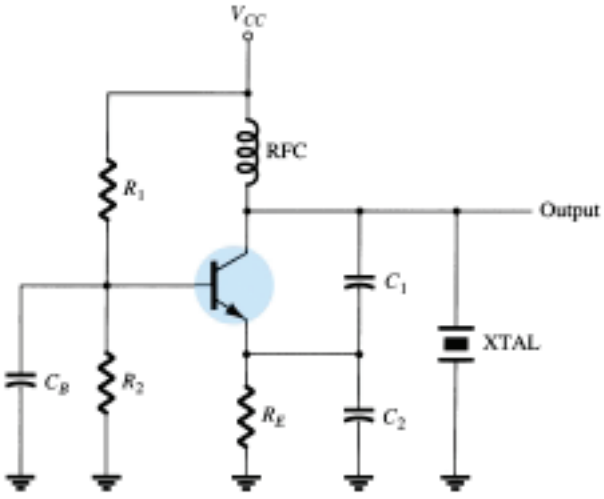


Figure 18.34 Crystal-controlled oscillator operating in parallel-resonant mode.

tor element in a modified Colpitts circuit. The basic dc bias circuit should be evident. Maximum voltage is developed across the crystal at its parallel-resonant frequency. The voltage is coupled to the emitter by a capacitor voltage divider—capacitors C_1 and C_2.

A *Miller crystal-controlled oscillator* circuit is shown in Fig. 18.35. A tuned LC circuit in the drain section is adjusted near the crystal parallel-resonant frequency. The maximum gate–source signal occurs at the crystal antiresonant frequency controlling the circuit operating frequency.

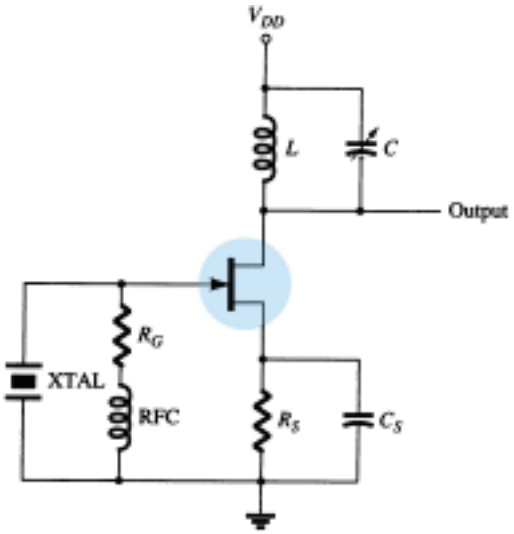


Figure 18.35 Miller crystal-controlled oscillator.

Crystal Oscillator

An op-amp can be used in a crystal oscillator as shown in Fig. 18.36. The crystal is connected in the series-resonant path and operates at the crystal series-resonant frequency. The present circuit has a high gain so that an output square-wave signal results as shown in the figure. A pair of Zener diodes is shown at the output to provide output amplitude at exactly the Zener voltage (V_Z).

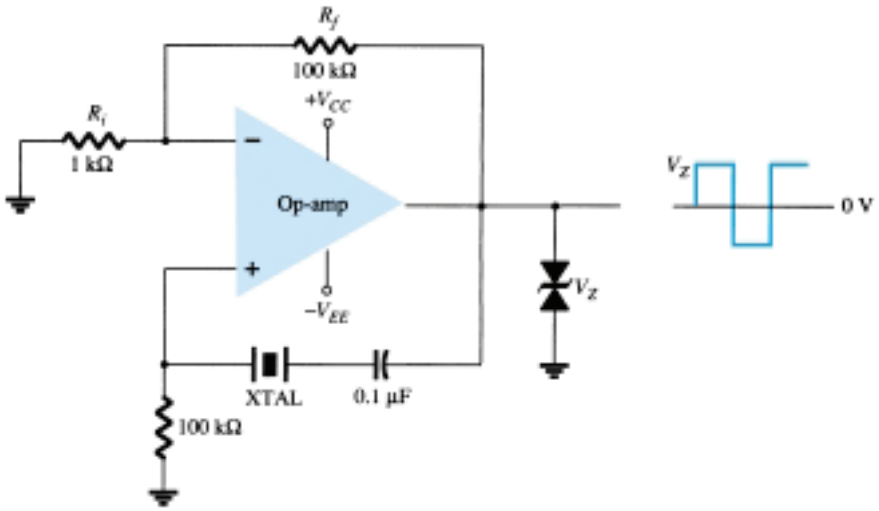


Figure 18.36 Crystal oscillator using op-amp.

A_f

18.10 UNIJUNCTION OSCILLATOR

A particular device, the unijunction transistor can be used in a single-stage oscillator circuit to provide a pulse signal suitable for digital-circuit applications. The unijunction transistor can be used in what is called a *relaxation oscillator* as shown by the basic circuit of Fig. 18.37. Resistor R_T and capacitor C_T are the timing components that set the circuit oscillating rate. The oscillating frequency may be calculated using Eq. (18.48), which includes the unijunction transistor *intrinsic stand-off ratio* η as a factor (in addition to R_T and C_T) in the oscillator operating frequency.

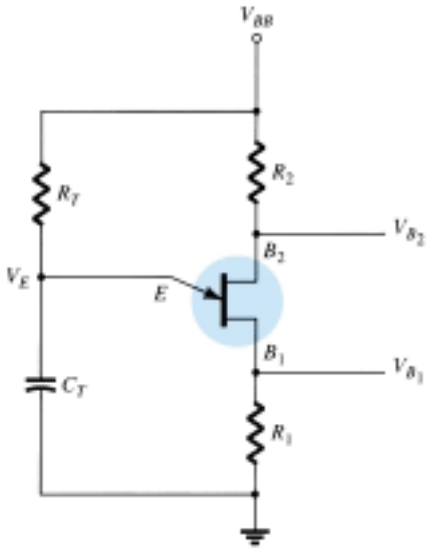


Figure 18.37 Basic unijunction oscillator circuit.

$$f_o \cong \frac{1}{R_T C_T \ln[1/(1-\eta)]} \tag{18.48}$$

Typically, a unijunction transistor has a stand-off ratio from 0.4 to 0.6. Using a value of $\eta = 0.5$, we get

$$f_o \cong \frac{1}{R_T C_T \ln[1/(1-0.5)]} = \frac{1.44}{R_T C_T \ln 2} = \frac{1.44}{R_T C_T}$$

$$\cong \frac{1.5}{R_T C_T} \tag{18.49}$$

Capacitor C_T is charged through resistor R_T toward supply voltage V_{BB}. As long as the capacitor voltage V_E is below a stand-off voltage (V_P) set by the voltage across $B_1 - B_2$ and the transistor stand-off ratio η

$$V_P = \eta V_{B_1} V_{B_2} - V_D \tag{18.50}$$

the unijunction emitter lead appears as an open circuit. When the emitter voltage across capacitor C_T exceeds this value (V_P), the unijunction circuit fires, discharging the capacitor, after which a new charge cycle begins. When the unijunction fires, a voltage rise is developed across R_1 and a voltage drop is developed across R_2 as shown in Fig. 18.38. The signal at the emitter is a sawtooth voltage waveform that at base 1 is a positive-going pulse and at base 2 is a negative-going pulse. A few circuit variations of the unijunction oscillator are provided in Fig. 18.39.

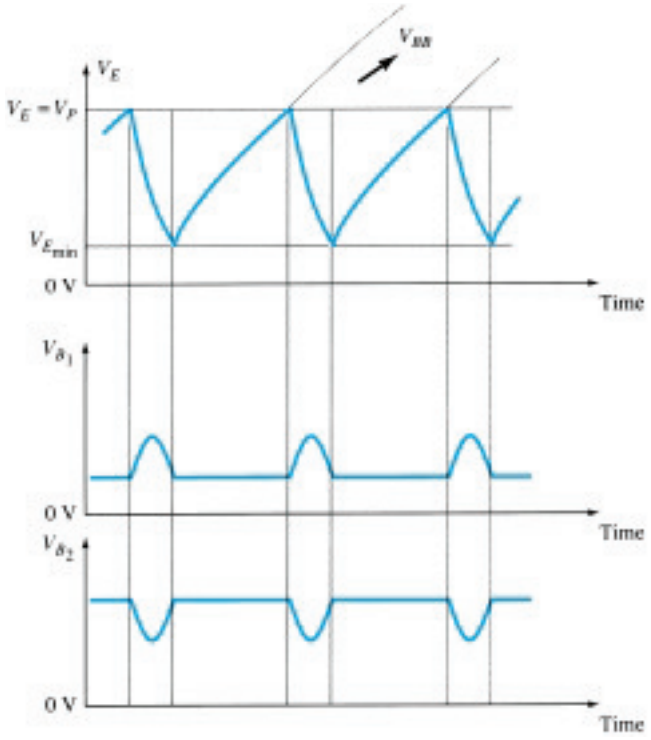


Figure 18.38 Unijunction oscillator waveforms.

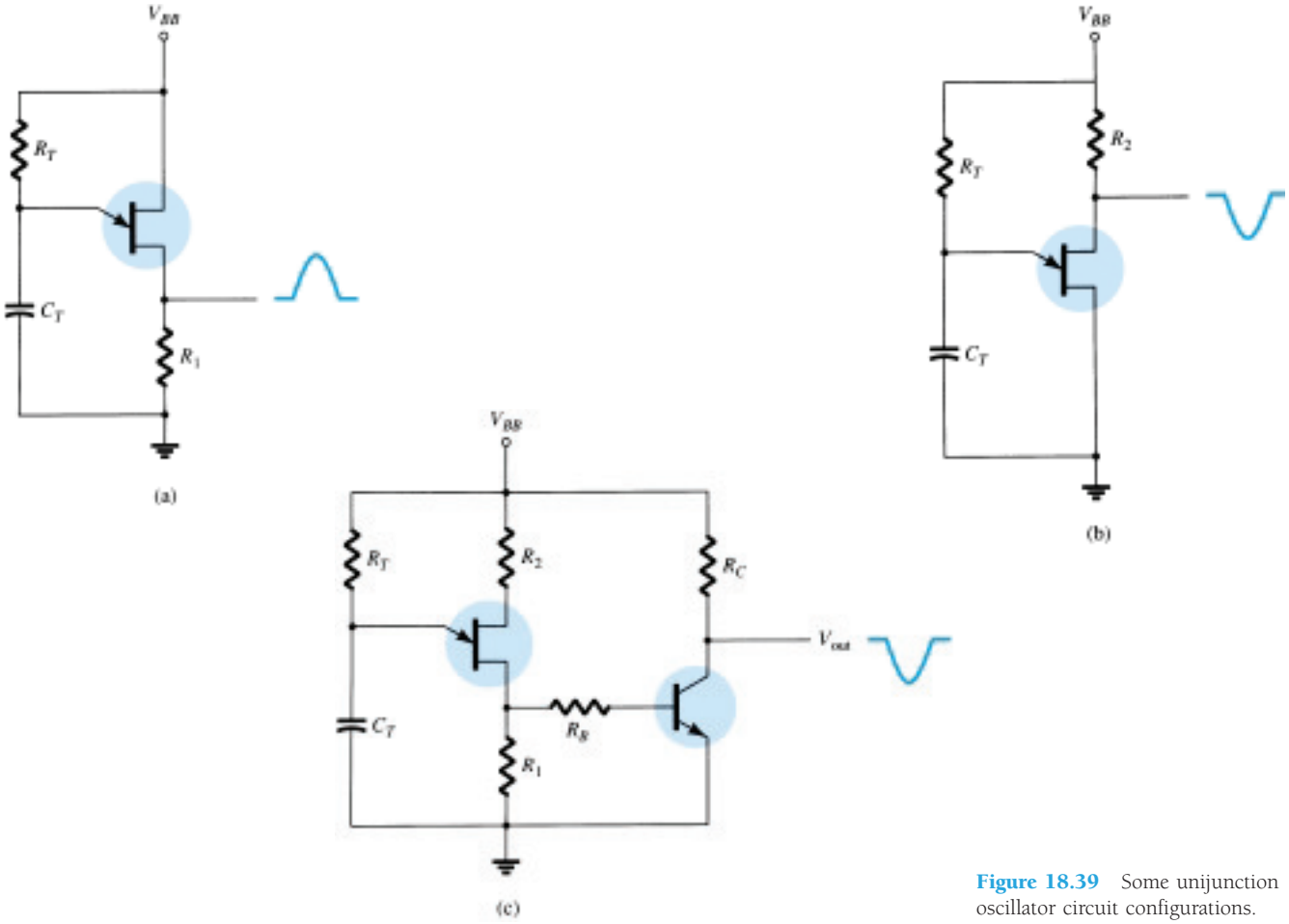


Figure 18.39 Some unijunction oscillator circuit configurations.

PROBLEMS

§ 18.2 Feedback Connection Types

1. Calculate the gain of a negative-feedback amplifier having $A = -2000$ and $\beta = -1/10$.

2. If the gain of an amplifier changes from a value of -1000 by 10%, calculate the gain change if the amplifier is used in a feedback circuit having $\beta = -1/20$.

3. Calculate the gain, input, and output impedances of a voltage-series feedback amplifier having $A = -300$, $R_i = 1.5\ \text{k}\Omega$, $R_o = 50\ \text{k}\Omega$, and $\beta = -1/15$.

§ 18.3 Practical Feedback Circuits

* **4.** Calculate the gain with and without feedback for an FET amplifier as in Fig. 18.7 for circuit values $R_1 = 800\ \text{k}\Omega$, $R_2 = 200\ \Omega$, $R_o = 40\ \text{k}\Omega$, $R_D = 8\ \text{k}\Omega$, and $g_m = 5000\ \mu\text{S}$.

5. For a circuit as in Fig. 18.11 and the following circuit values, calculate the circuit gain and the input and output impedances with and without feedback: $R_B = 600\ \text{k}\Omega$, $R_E = 1.2\ \text{k}\Omega$, $R_C = 4.7\ \text{k}\Omega$, and $\beta = 75$. Use $V_{CC} = 16$ V.

§ 18.6 Phase-Shift Oscillator

6. An FET phase-shift oscillator having $g_m = 6000\ \mu\text{S}$, $r_d = 36\ \text{k}\Omega$, and feedback resistor $R = 12\ \text{k}\Omega$ is to operate at 2.5 kHz. Select C for specified oscillator operation.

7. Calculate the operating frequency of a BJT phase-shift oscillator as in Fig. 18.21b for $R = 6\ \text{k}\Omega$, $C = 1500$ pF, and $R_C = 18\ \text{k}\Omega$.

§ 18.7 Wien Bridge Oscillator

8. Calculate the frequency of a Wien bridge oscillator circuit (as in Fig. 18.23) when $R = 10\ \text{k}\Omega$ and $C = 2400$ pF.

§ 18.8 Tuned Oscillator Circuit

9. For an FET Colpitts oscillator as in Fig. 18.26 and the following circuit values determine the circuit oscillation frequency: $C_1 = 750$ pF, $C_2 = 2500$ pF, and $L = 40\ \mu\text{H}$.

10. For the transistor Colpitts oscillator of Fig. 18.27 and the following circuit values, calculate the oscillation frequency: $L = 100\ \mu\text{H}$, $L_{RFC} = 0.5$ mH, $C_1 = 0.005\ \mu\text{F}$, $C_2 = 0.01\ \mu\text{F}$, and $C_C = 10\ \mu\text{F}$.

11. Calculate the oscillator frequency for an FET Hartley oscillator as in Fig. 18.29 for the following circuit values: $C = 250$ pF, $L_1 = 1.5$ mH, $L_2 = 1.5$ mH, and $M = 0.5$ mH.

12. Calculate the oscillation frequency for the transistor Hartley circuit of Fig. 18.30 and the following circuit values: $L_{RFC} = 0.5$ mH, $L_1 = 750\ \mu\text{H}$, $L_2 = 750\ \mu\text{H}$, $M = 150\ \mu\text{H}$, and $C = 150$ pF.

§ 18.9 Crystal Oscillator

13. Draw circuit diagrams of (a) a series-operated crystal oscillator and (b) a shunt-excited crystal oscillator.

§ 18.10 Unijunction Oscillator

14. Design a unijunction oscillator circuit for operation at (a) 1 kHz and (b) 150 kHz.

*Please Note: Asterisks indicate more difficult problems.

CHAPTER

19 Power Supplies (Voltage Regulators)

19.1 INTRODUCTION

The present chapter introduces the operation of power supply circuits built using filters, rectifiers, and then voltage regulators. (Refer to Chapter 2 for the initial description of diode rectifier circuits.) Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level and, finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in Fig. 19.1. The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

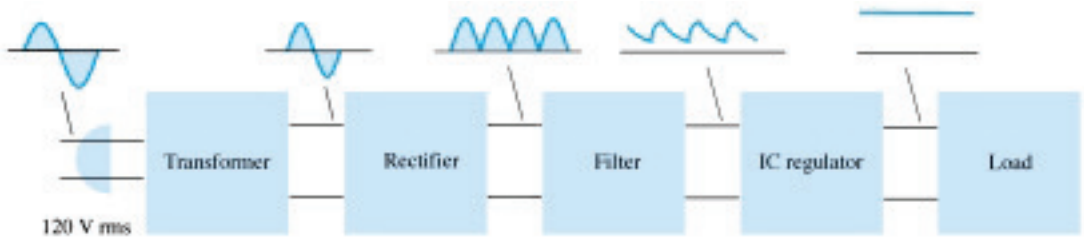


Figure 19.1 Block diagram showing parts of a power supply.

19.2 GENERAL FILTER CONSIDERATIONS

A rectifier circuit is necessary to convert a signal having zero average value into one that has a nonzero average. The output resulting from a rectifier is a pulsating dc voltage and not yet suitable as a battery replacement. Such a voltage could be used in,

say, a battery charger, where the average dc voltage is large enough to provide a charging current for the battery. For dc supply voltages, as those used in a radio, stereo system, computer, and so on, the pulsating dc voltage from a rectifier is not good enough. A filter circuit is necessary to provide a steadier dc voltage.

Filter Voltage Regulation and Ripple Voltage

Before going into the details of a filter circuit, it would be appropriate to consider the usual methods of rating filter circuits so that we can compare a circuit's effectiveness as a filter. Figure 19.2 shows a typical filter output voltage, which will be used to define some of the signal factors. The filtered output of Fig. 19.2 has a dc value and some ac variation (ripple). Although a battery has essentially a constant or dc output voltage, the dc voltage derived from an ac source signal by rectifying and filtering will have some ac variation (ripple). The smaller the ac variation with respect to the dc level, the better the filter circuit's operation.

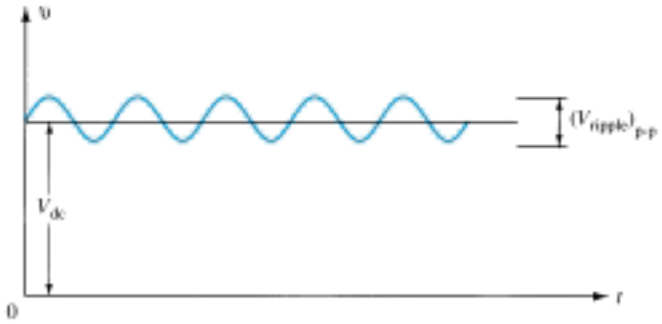


Figure 19.2 Filter voltage waveform showing dc and ripple voltages.

Consider measuring the output voltage of a filter circuit using a dc voltmeter and an ac (rms) voltmeter. The dc voltmeter will read only the average or dc level of the output voltage. The ac (rms) meter will read only the rms value of the ac component of the output voltage (assuming the ac signal is coupled through a capacitor to block out the dc level).

Definition: Ripple

$$r = \frac{\text{ripple voltage (rms)}}{\text{dc voltage}} = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% \tag{19.1}$$

EXAMPLE 19.1

Using a dc and ac voltmeter to measure the output signal from a filter circuit, we obtain readings of 25 V dc and 1.5 V rms. Calculate the ripple of the filter output voltage.

Solution

$$r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{1.5\text{ V}}{25\text{ V}} \times 100\% = \mathbf{6\%}$$

VOLTAGE REGULATION

Another factor of importance in a power supply is the amount the dc output voltage changes over a range of circuit operation. The voltage provided at the output under no-load condition (no current drawn from the supply) is reduced when load current is drawn from the supply (under load). The amount the dc voltage changes

between the no-load and load conditions is described by a factor called voltage regulation.

Definition: Voltage regulation

$$\text{Voltage regulation} = \frac{\text{no-load voltage} - \text{full-load voltage}}{\text{full-load voltage}}$$

$$\boxed{\%\text{V.R.} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%} \tag{19.2}$$

EXAMPLE 19.2

A dc voltage supply provides 60 V when the output is unloaded. When connected to a load, the output drops to 56 V. Calculate the value of voltage regulation.

Solution

$$\text{Eq. (19.2): } \%\text{V.R.} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\% = \frac{60\text{ V} - 56\text{ V}}{56\text{ V}} \times 100\% = \mathbf{7.1\%}$$

If the value of full-load voltage is the same as the no-load voltage, the voltage regulation calculated is 0%, which is the best expected. This means that the supply is a perfect voltage source for which the output voltage is independent of the current drawn from the supply. The smaller the voltage regulation, the better the operation of the voltage supply circuit.

RIPPLE FACTOR OF RECTIFIED SIGNAL

Although the rectified voltage is not a filtered voltage, it nevertheless contains a dc component and a ripple component. We will see that the full-wave rectified signal has a larger dc component and less ripple than the half-wave rectified voltage.

For a half-wave rectified signal, the output dc voltage is

$$V_{dc} = 0.318V_m \tag{19.3}$$

The rms value of the ac component of the output signal can be calculated (see Appendix B) to be

$$V_r(\text{rms}) = 0.385V_m \tag{19.4}$$

The percent ripple of a half-wave rectified signal can then be calculated as

$$r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{0.385V_m}{0.318V_m} \times 100\% = 121\% \tag{19.5}$$

For a full-wave rectified voltage the dc value is

$$V_{dc} = 0.636V_m \tag{19.6}$$

The rms value of the ac component of the output signal can be calculated (see Appendix B) to be

$$V_r(\text{rms}) = 0.308V_m \tag{19.7}$$

The percent ripple of a full-wave rectified signal can then be calculated as

$$r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{0.308V_m}{0.636V_m} \times 100\% = 48\% \tag{19.8}$$

In summary, a full-wave rectified signal has less ripple than a half-wave rectified signal and is thus better to apply to a filter.

19.3 CAPACITOR FILTER

A very popular filter circuit is the capacitor-filter circuit shown in Fig. 19.3. A capacitor is connected at the rectifier output, and a dc voltage is obtained across the capacitor. Figure 19.4a shows the output voltage of a full-wave rectifier before the signal is filtered, while Fig. 19.4b shows the resulting waveform after the filter capacitor is connected at the rectifier output. Notice that the filtered waveform is essentially a dc voltage with some ripple (or ac variation).

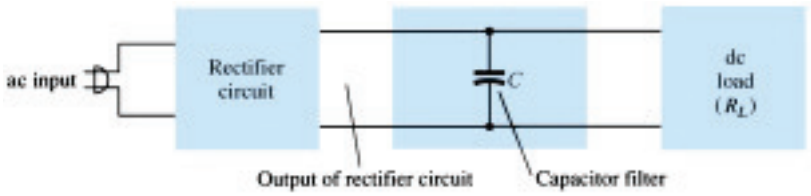


Figure 19.3 Simple capacitor filter.

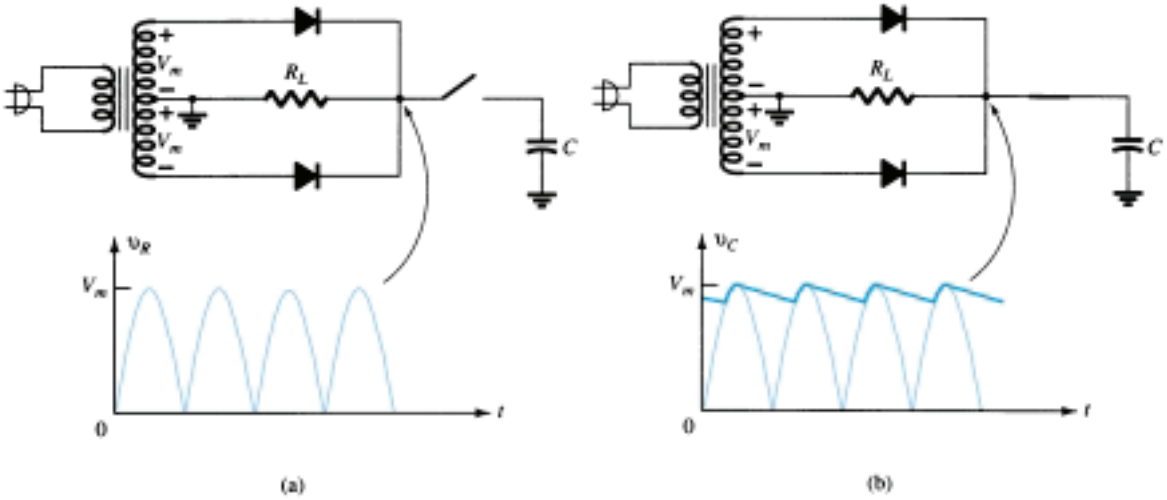


Figure 19.4 Capacitor filter operation: (a) full-wave rectifier voltage; (b) filtered output voltage.

Figure 19.5a shows a full-wave bridge rectifier and the output waveform obtained from the circuit when connected to a load (R_L). If no load were connected across the capacitor, the output waveform would ideally be a constant dc level equal in value to the peak voltage (V_m) from the rectifier circuit. However, the purpose of obtaining a

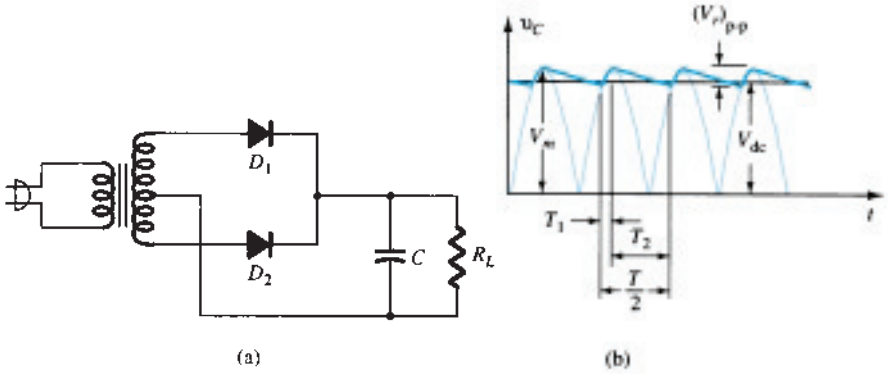


Figure 19.5 Capacitor filter: (a) capacitor filter circuit; (b) output voltage waveform.

dc voltage is to provide this voltage for use by various electronic circuits, which then constitute a load on the voltage supply. Since there will always be a load on the filter output, we must consider this practical case in our discussion.

Output Waveform Times

Figure 19.5b shows the waveform across a capacitor filter. Time T_1 is the time during which diodes of the full-wave rectifier conduct, charging the capacitor up to the peak rectifier voltage, V_m. Time T_2 is the time interval during which the rectifier voltage drops below the peak voltage, and the capacitor discharges through the load. Since the charge–discharge cycle occurs for each half-cycle for a full-wave rectifier, the period of the rectified waveform is $T/2$, one-half the input signal frequency. The filtered voltage, as shown in Fig. 19.6, shows the output waveform to have a dc level V_{dc} and a ripple voltage V_r (rms) as the capacitor charges and discharges. Some details of these waveforms and the circuit elements are considered next.

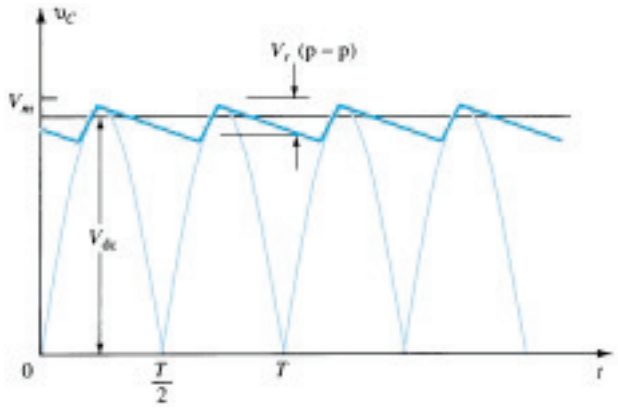


Figure 19.6 Approximate output voltage of capacitor filter circuit.

RIPPLE VOLTAGE, V_r (RMS)

Appendix B provides the details for determining the value of the ripple voltage in terms of the other circuit parameters. The ripple voltage can be calculated from

$$V_r \text{ (rms)} = \frac{I_{dc}}{4\sqrt{3}\,fC} = \frac{2.4\ I_{dc}}{C} = \frac{2.4V_{dc}}{R_L C} \tag{19.9}$$

where I_{dc} is in milliamperes, C is in microfarads, and R_L is in kilohms.

EXAMPLE 19.3

Calculate the ripple voltage of a full-wave rectifier with a 100-μF filter capacitor connected to a load drawing 50 mA.

Solution

$$\text{Eq. (19.9): } V_r(\text{rms}) = \frac{2.4(50)}{100} = \mathbf{1.2\ V}$$

DC VOLTAGE, V_{dc}

From Appendix B, we can express the dc value of the waveform across the filter capacitor as

$$V_{dc} = V_m - \frac{I_{dc}}{4fC} = V_m - \frac{4.17I_{dc}}{C} \tag{19.10}$$

where V_m is the peak rectifier voltage, I_{dc} is the load current in milliamperes, and C is the filter capacitor in microfarads.

EXAMPLE 19.4

If the peak rectified voltage for the filter circuit of Example 19.3 is 30 V, calculate the filter dc voltage.

Solution

$$\text{Eq. (19.10): } V_{dc} = V_m - \frac{4.17I_{dc}}{C} = 30 - \frac{4.17(50)}{100} = \mathbf{27.9\ V}$$

Filter Capacitor Ripple

Using the definition of ripple [Eq. (19.1)], Eq. (19.9), and Eq. (19.10), with $V_{dc} \approx V_m$, we can obtain the expression for the output waveform ripple of a full-wave rectifier and filter-capacitor circuit.

$$r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{2.4\ I_{dc}}{CV_{dc}} \times 100\% = \frac{2.4}{R_L C} \times 100\% \tag{19.11}$$

where I_{dc} is in milliamperes, C is in microfarads, V_{dc} is in volts, and R_L is in kilohms.

EXAMPLE 19.5

Calculate the ripple of a capacitor filter for a peak rectified voltage of 30 V, capacitor $C = 50\ \mu$F, and a load current of 50 mA.

Solution

$$\text{Eq. (19.11): } r = \frac{2.4\ I_{dc}}{CV_{dc}} \times 100\% = \frac{2.4(50)}{100(27.9)} \times 100\% = \mathbf{4.3\%}$$

We could also calculate the ripple using the basic definition

$$r = \frac{V_r(\text{rms})}{V_{dc}} \times 100\% = \frac{1.2\ \text{V}}{27.9\ \text{V}} \times 100\% = \mathbf{4.3\%}$$

Diode Conduction Period and Peak Diode Current

From the previous discussion, it should be clear that larger values of capacitance provide less ripple and higher average voltage, thereby providing better filter action. From this one might conclude that to improve the performance of a capacitor filter it is only necessary to increase the size of the filter capacitor. The capacitor, however, also affects the peak current drawn through the rectifying diodes, and as will be shown next, the larger the value of the capacitor, the larger the peak current drawn through the rectifying diodes.

Recall that the diodes conduct during period T_1 (see Fig. 19.5), during which time the diode must provide the necessary average current to charge the capacitor. The shorter this time interval, the larger the amount of the charging current. Figure 19.7 shows this relation for a half-wave rectified signal (it would be the same basic oper-

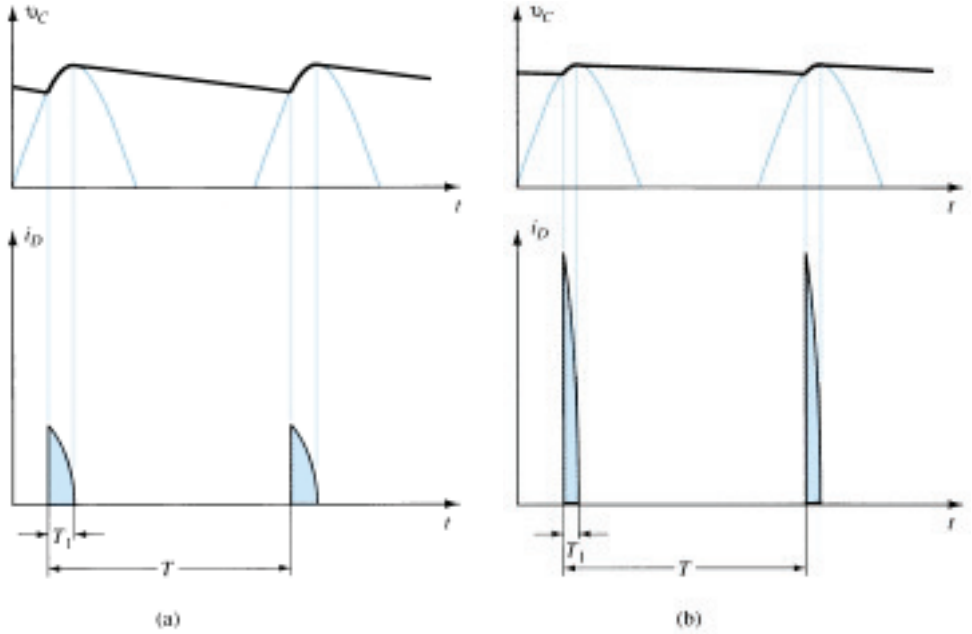


Figure 19.7 Output voltage and diode current waveforms: (a) small C; (b) large C.

ation for full-wave). Notice that for smaller values of capacitor, with T_1 larger, the peak diode current is less than for larger values of filter capacitor.

Since the average current drawn from the supply must equal the average diode current during the charging period, the following relation can be used (assuming constant diode current during charge time):

$$I_{dc} = \frac{T_1}{T} I_{peak}$$

from which we obtain

$$\boxed{I_{peak} = \frac{T}{T_1} I_{dc}} \qquad (19.12)$$

where T_1 = diode conduction time
$T = 1/f$ ($f = 2 \times 60$ for full-wave)
I_{dc} = average current drawn from filter
I_{peak} = peak current through conducting diodes

19.4 RC FILTER

It is possible to further reduce the amount of ripple across a filter capacitor by using an additional RC filter section as shown in Fig. 19.8. The purpose of the added RC section is to pass most of the dc component while attenuating (reducing) as much of

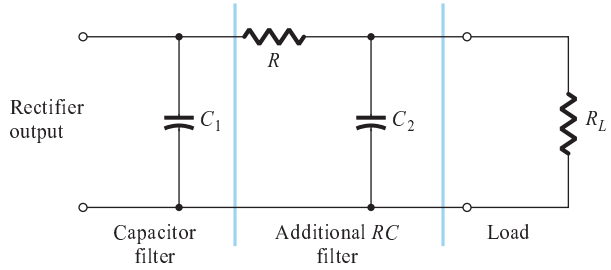


Figure 19.8 RC filter stage.

the ac component as possible. Figure 19.9 shows a full-wave rectifier with capacitor filter followed by an *RC* filter section. The operation of the filter circuit can be analyzed using superposition for the dc and ac components of signal.

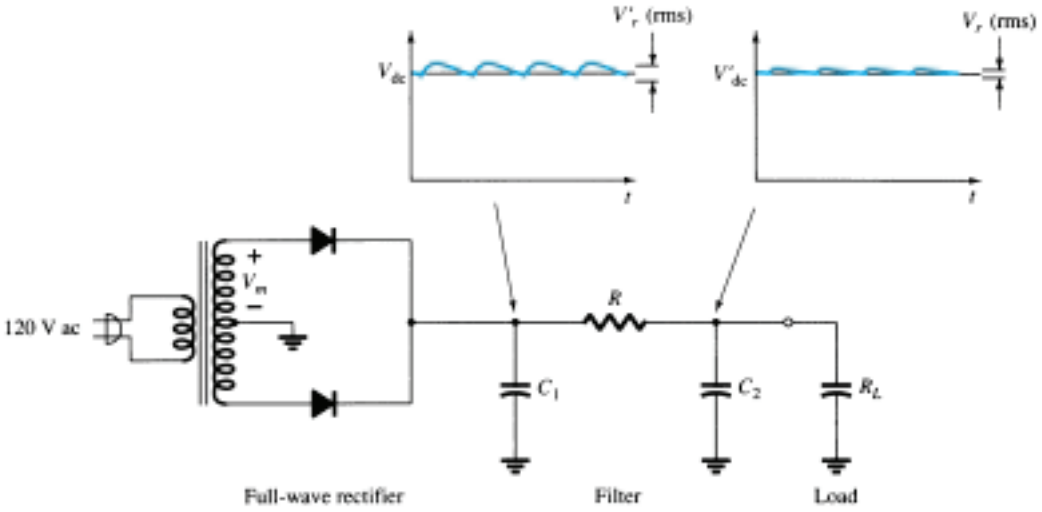


Figure 19.9 Full-wave rectifier and *RC* filter circuit.

DC Operation of *RC* Filter Section

Figure 19.10a shows the dc equivalent circuit to use in analyzing the *RC* filter circuit of Fig. 19.9. Since both capacitors are open-circuit for dc operation, the resulting output dc voltage is

$$V'_{dc} = \frac{R_L}{R + R_L} V_{dc} \tag{19.13}$$

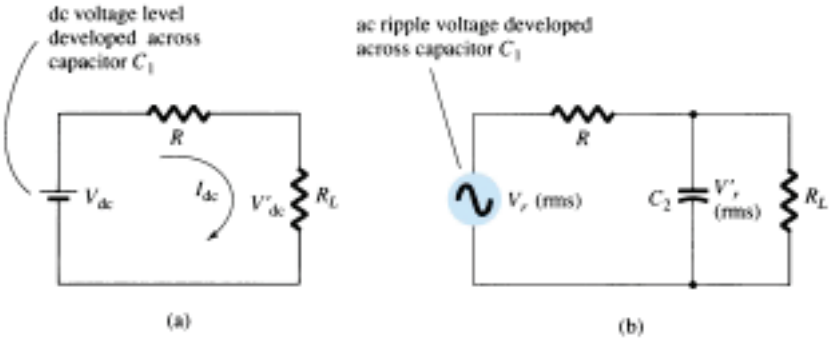


Figure 19.10 (a) Dc and (b) ac equivalent circuits of *RC* filter.

EXAMPLE 19.6

Calculate the dc voltage across a 1-kΩ load for an *RC* filter section ($R = 120\ \Omega$, $C = 10\ \mu$F). The dc voltage across the initial filter capacitor is $V_{dc} = 60$ V.

Solution

$$\text{Eq. (19.13): } V'_{dc} = \frac{R_L}{R + R_L} V_{dc} = \frac{1000}{120 + 1000}(60\text{ V}) = \mathbf{53.6\ V}$$

AC Operation of *RC* Filter Section

Figure 19.10b shows the ac equivalent circuit of the *RC* filter section. Due to the voltage-divider action of the capacitor ac impedance and the load resistor, the ac component of voltage resulting across the load is

$$V'_r(\text{rms}) \approx \frac{X_C}{R} V_r(\text{rms}) \tag{19.14}$$

For a full-wave rectifier with ac ripple at 120 Hz, the impedance of a capacitor can be calculated using

$$X_C = \frac{1.3}{C} \tag{19.15}$$

where C is in microfarads and X_C is in kilohms.

EXAMPLE 19.7

Calculate the dc and ac components of the output signal across load R_L in the circuit of Fig. 19.11. Calculate the ripple of the output waveform.

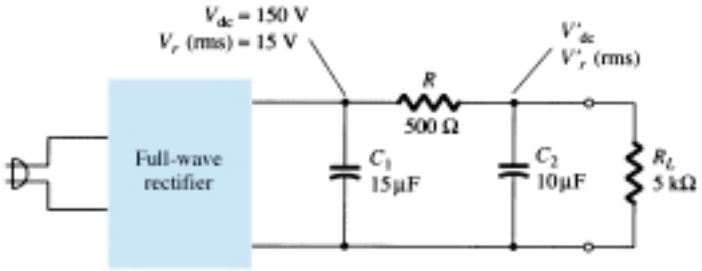


Figure 19.11 *RC* filter circuit for Example 19.7.

Solution

DC Calculation:

$$\text{Eq. (19.13): } V'_{\text{dc}} = \frac{R_L}{R + R_L} V_{\text{dc}} = \frac{5\ \text{k}\Omega}{500 + 5\ \text{k}\Omega}(150\ \text{V}) = \mathbf{136.4\ V}$$

AC Calculation:
The *RC* section capacitive impedance is

$$\text{Eq. (19.15): } X_C = \frac{1.3}{C} = \frac{1.3}{10} = 0.13\ \text{k}\Omega = 130\ \Omega$$

The ac component of the output voltage, calculated using Eq. (19.14), is

$$V'_r(\text{rms}) = \frac{X_C}{R} V_r(\text{rms}) = \frac{130}{500}(15\ \text{V}) = \mathbf{3.9\ V}$$

The ripple of the output waveform is then

$$r = \frac{V'_r(\text{rms})}{V'_{\text{dc}}} \times 100\% = \frac{3.9\ \text{V}}{136.4\ \text{V}} \times 100\% = \mathbf{2.86\%}$$

19.5 DISCRETE TRANSISTOR VOLTAGE REGULATION

Two types of transistor voltage regulators are the series voltage regulator and the shunt voltage regulator. Each type of circuit can provide an output dc voltage that is regulated or maintained at a set value even if the input voltage varies or if the load connected to the output changes.

Series Voltage Regulation

The basic connection of a series regulator circuit is shown in the block diagram of Fig. 19.12. The series element controls the amount of the input voltage that gets to the output. The output voltage is sampled by a circuit that provides a feedback voltage to be compared to a reference voltage.

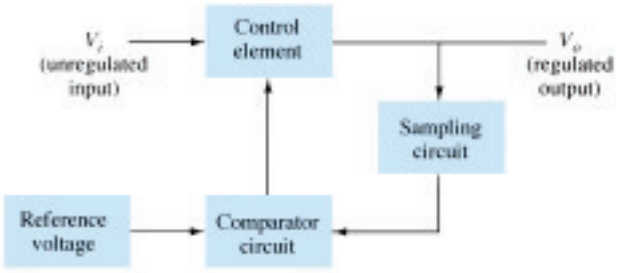


Figure 19.12 Series regulator block diagram.

1. If the output voltage increases, the comparator circuit provides a control signal to cause the series control element to decrease the amount of the output voltage—thereby maintaining the output voltage.
2. If the output voltage decreases, the comparator circuit provides a control signal to cause the series control element to increase the amount of the output voltage.

SERIES REGULATOR CIRCUIT

A simple series regulator circuit is shown in Fig. 19.13. Transistor Q_1 is the series control element, and Zener diode D_Z provides the reference voltage. The regulating operation can be described as follows:

1. If the output voltage decreases, the increased base-emitter voltage causes transistor Q_1 to conduct more, thereby raising the output voltage—maintaining the output constant.
2. If the output voltage increases, the decreased base-emitter voltage causes transistor Q_1 to conduct less, thereby reducing the output voltage—maintaining the output constant.

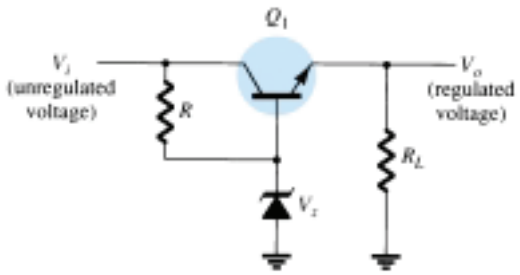


Figure 19.13 Series regulator circuit.

EXAMPLE 19.8

Calculate the output voltage and Zener current in the regulator circuit of Fig. 19.14 for $R_L = 1\ \text{k}\Omega$.

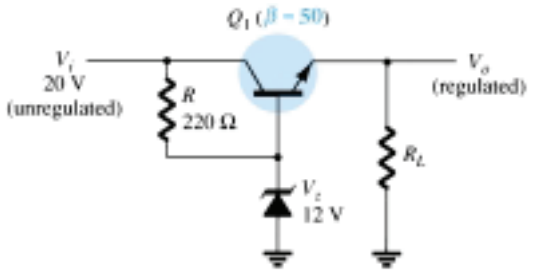


Figure 19.14 Circuit for Example 19.8.

Solution

$$V_o = V_Z - V_{BE} = 12\ \text{V} - 0.7\ \text{V} = \mathbf{11.3\ V}$$

$$V_{CE} = V_i - V_o = 20\ \text{V} - 11.3\ \text{V} = 8.7\ \text{V}$$

$$I_R = \frac{20\ \text{V} - 12\ \text{V}}{220\ \Omega} = \frac{8\ \text{V}}{220\ \Omega} = 36.4\ \text{mA}$$

For $R_L = 1\ \text{k}\Omega$,

$$I_L = \frac{V_o}{R_L} = \frac{11.3\ \text{V}}{1\ \text{k}\Omega} = 11.3\ \text{mA}$$

$$I_B = \frac{I_C}{\beta} = \frac{11.3\ \text{mA}}{50} = 226\ \mu\text{A}$$

$$I_Z = I_R - I_B = 36.4\ \text{mA} - 226\ \mu\text{A} \approx \mathbf{36\ mA}$$

IMPROVED SERIES REGULATOR

An improved series regulator circuit is that of Fig. 19.15. Resistors R_1 and R_2 act as a sampling circuit, Zener diode D_Z providing a reference voltage, and transistor Q_2 then controls the base current to transistor Q_1 to vary the current passed by transistor Q_1 to maintain the output voltage constant.

If the output voltage tries to increase, the increased voltage sampled by R_1 and R_2, increased voltage V_2, causes the base-emitter voltage of transistor Q_2 to go up

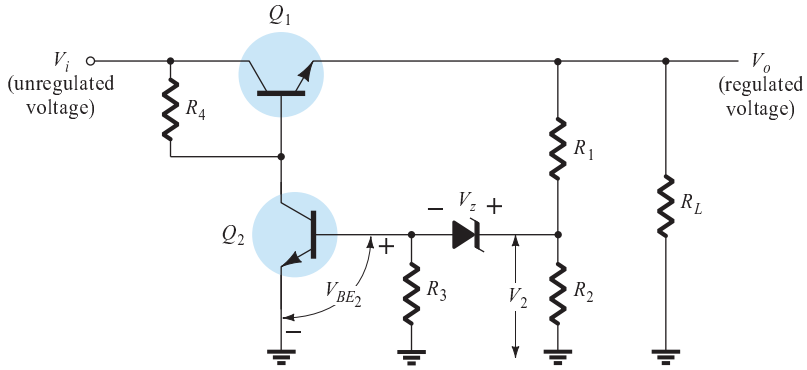


Figure 19.15 Improved series regulator circuit.

(since V_Z remains fixed). If Q_2 conducts more current, less goes to the base of transistor Q_1, which then passes less current to the load, reducing the output voltage—thereby maintaining the output voltage constant. The opposite takes place if the output voltage tries to decrease, causing less current to be supplied to the load, to keep the voltage from decreasing.

The voltage V_2 provided by sensing resistors R_1 and R_2 must equal the sum of the base-emitter voltage of Q_2 and the Zener diode, that is,

$$V_{BE_2} + V_Z = V_2 = \frac{R_2}{R_1 + R_2} V_o \tag{19.16}$$

Solving Eq. (19.16) for the regulated output voltage, V_o,

$$\boxed{V_o = \frac{R_1 + R_2}{R_2}(V_Z + V_{BE_2})} \tag{19.17}$$

EXAMPLE 19.9

What regulated output voltage is provided by the circuit of Fig. 19.15 for the following circuit elements: $R_1 = 20\ \text{k}\Omega$, $R_2 = 30\ \text{k}\Omega$, and $V_Z = 8.3$ V?

Solution

From Eq. (19.17), the regulated output voltage will be

$$V_o = \frac{20\ \text{k}\Omega + 30\ \text{k}\Omega}{30\ \text{k}\Omega}(8.3\ \text{V} + 0.7\ \text{V}) = \mathbf{15\ V}$$

OP-AMP SERIES REGULATOR

Another version of series regulator is that shown in Fig. 19.16. The op-amp compares the Zener diode reference voltage with the feedback voltage from sensing resistors R_1 and R_2. If the output voltage varies, the conduction of transistor Q_1 is controlled to maintain the output voltage constant. The output voltage will be maintained at a value of

$$\boxed{V_o = \left(1 + \frac{R_1}{R_2}\right)V_Z} \tag{19.18}$$

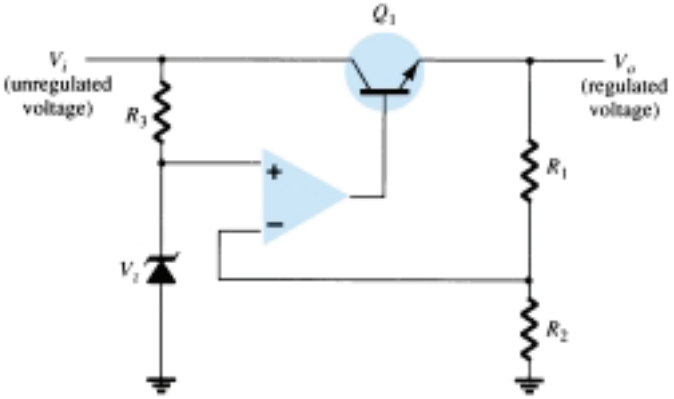


Figure 19.16 Op-amp series regulator circuit.

EXAMPLE 19.10

Calculate the regulated output voltage in the circuit of Fig. 19.17.

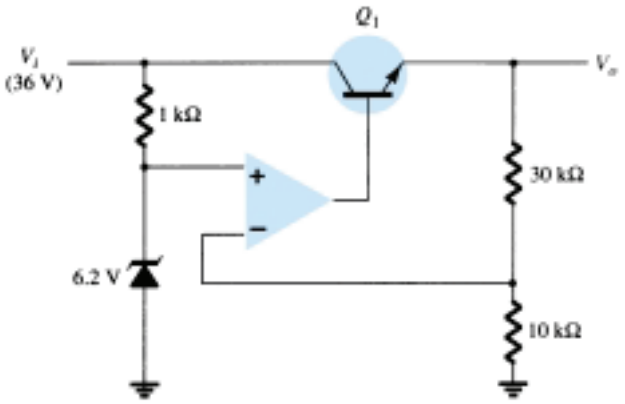


Figure 19.17 Circuit for Example 19.10.

Solution

$$\text{Eq. (19.18): } V_o = \left(1 + \frac{30\ \text{k}\Omega}{10\ \text{k}\Omega}\right)6.2\ \text{V} = \mathbf{24.8\ V}$$

CURRENT-LIMITING CIRCUIT

One form of short-circuit or overload protection is current limiting, as shown in Fig. 19.18. As load current I_L increases, the voltage drop across the short-circuit sensing resistor R_{SC} increases. When the voltage drop across R_{SC} becomes large enough, it will drive Q_2 on, diverting current from the base of transistor Q_1, thereby reducing the load current through transistor Q_1, preventing any additional current to load R_L. The action of components R_{SC} and Q_2 provides limiting of the maximum load current.

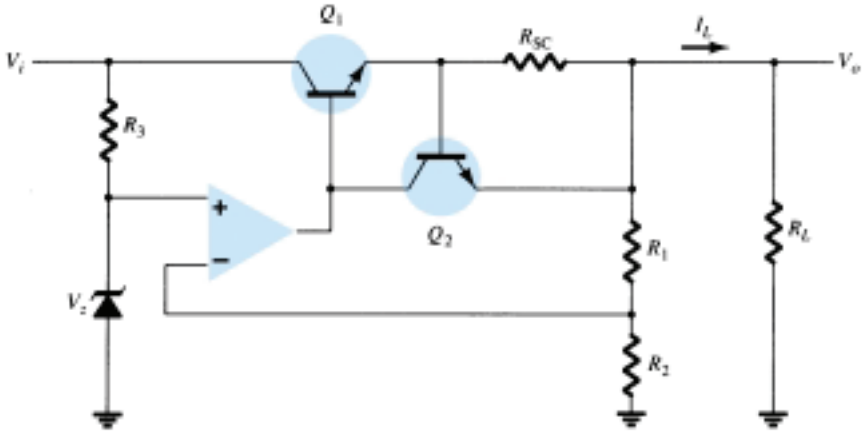


Figure 19.18 Current-limiting voltage regulator.

FOLDBACK LIMITING

Current limiting reduces the load voltage when the current becomes larger than the limiting value. The circuit of Fig. 19.19 provides foldback limiting, which reduces both the output voltage and output current protecting the load from overcurrent, as well as protecting the regulator.

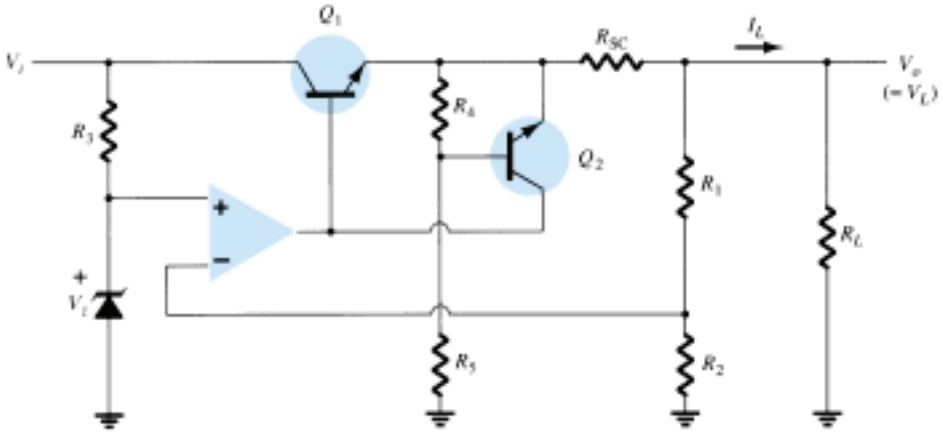


Figure 19.19 Foldback-limiting series regulator circuit.

Foldback limiting is provided by the additional voltage-divider network of R_4 and R_5 in the circuit of Fig. 19.19 (over that of Fig. 19.17). The divider circuit senses the voltage at the output (emitter) of Q_1. When I_L increases to its maximum value, the voltage across R_{SC} becomes large enough to drive Q_2 on, thereby providing current limiting. If the load resistance is made smaller, the voltage driving Q_2 on becomes less, so that I_L drops when V_L also drops in value—this action being foldback limiting. When the load resistance is returned to its rated value, the circuit resumes its voltage regulation action.

Shunt Voltage Regulation

A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. Figure 19.20 shows the block diagram of such a voltage regulator. The input unregulated voltage provides current to the load. Some of the current is pulled away by the control element to maintain the regulated output voltage across the load. If the load voltage tries to change due to a change in the load, the sampling circuit provides a feedback signal to a comparator, which then provides a control signal to vary the amount of the current shunted away from the load. As the output voltage tries to get larger, for example, the sampling circuit provides a feedback signal to the comparator circuit, which then provides a control signal to draw increased shunt current, providing less load current, thereby keeping the regulated voltage from rising.

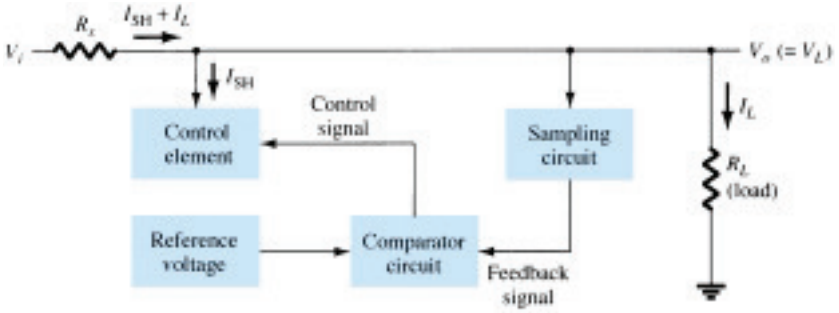


Figure 19.20 Block diagram of shunt voltage regulator.

BASIC TRANSISTOR SHUNT REGULATOR

A simple shunt regulator circuit is shown in Fig. 19.21. Resistor R_S drops the unregulated voltage by an amount that depends on the current supplied to the load, R_L. The voltage across the load is set by the Zener diode and transistor base-emitter volt-

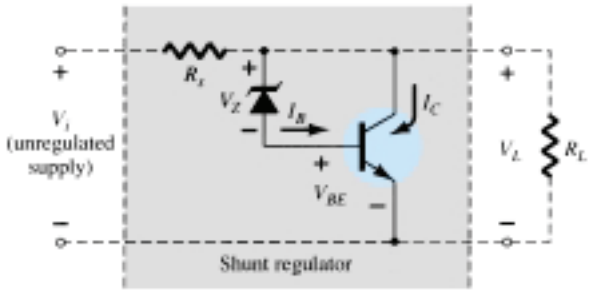


Figure 19.21 Transistor shunt voltage regulator.

age. If the load resistance decreases, a reduced drive current to the base of Q_1 results, shunting less collector current. The load current is thus larger, thereby maintaining the regulated voltage across the load. The output voltage to the load is

$$V_L = V_Z + V_{BE} \tag{19.19}$$

EXAMPLE 19.11

Determine the regulated voltage and circuit currents for the shunt regulator of Fig. 19.22.

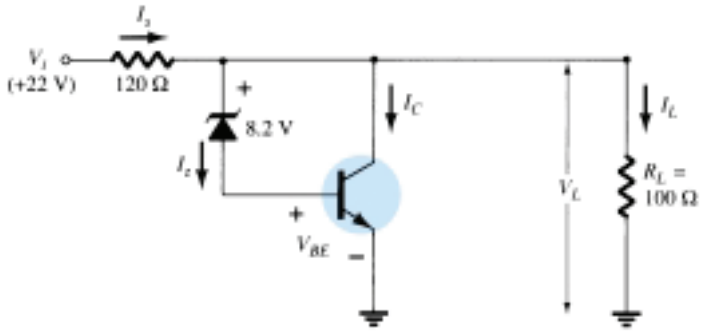


Figure 19.22 Circuit for Example 19.11.

Solution

The load voltage is

$$\text{Eq. (19.19): } V_L = 8.2\text{ V} + 0.7\text{ V} = \mathbf{8.9\text{ V}}$$

For the given load,

$$I_L = \frac{V_L}{R_L} = \frac{8.9\text{ V}}{100\ \Omega} = \mathbf{89\text{ mA}}$$

With the unregulated input voltage at 22 V, the current through R_S is

$$I_S = \frac{V_i - V_L}{R_S} = \frac{22\text{ V} - 8.9\text{ V}}{120} = \mathbf{109\text{ mA}}$$

so that the collector current is

$$I_C = I_S - I_L = 109\text{ mA} - 89\text{ mA} = \mathbf{20\text{ mA}}$$

(The current through the Zener and transistor base–emitter is smaller than I_C by the transistor beta.)

IMPROVED SHUNT REGULATOR

The circuit of Fig. 19.23 shows an improved shunt voltage regulator circuit. The Zener diode provides a reference voltage so that the voltage across R_1 senses the output voltage. As the output voltage tries to change, the current shunted by transistor Q_1 is varied to maintain the output voltage constant. Transistor Q_2 provides a larger base current to transistor Q_1 than the circuit of Fig. 19.21, so that the regulator handles a larger load current. The output voltage is set by the Zener voltage and that across the two transistor base–emitters,

$$V_o = V_L = V_Z + V_{BE_2} + V_{BE_1} \tag{19.20}$$

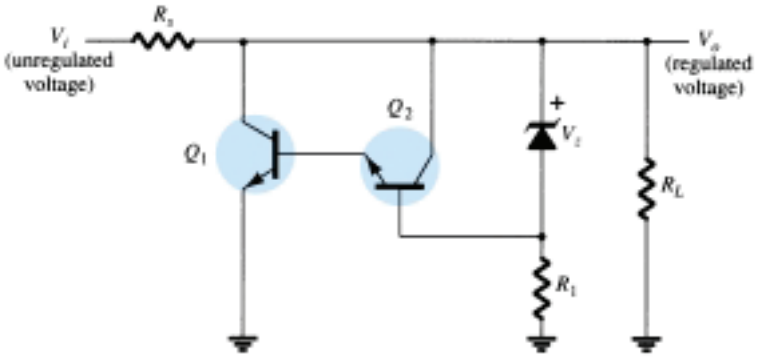


Figure 19.23 Improved shunt voltage regulator circuit.

SHUNT VOLTAGE REGULATOR USING OP-AMP

Figure 19.24 shows another version of a shunt voltage regulator using an op-amp as voltage comparator. The Zener voltage is compared to the feedback voltage obtained from voltage divider R_1 and R_2 to provide the control drive current to shunt element Q_1. The current through resistor R_S is thus controlled to drop a voltage across R_S so that the output voltage is maintained.

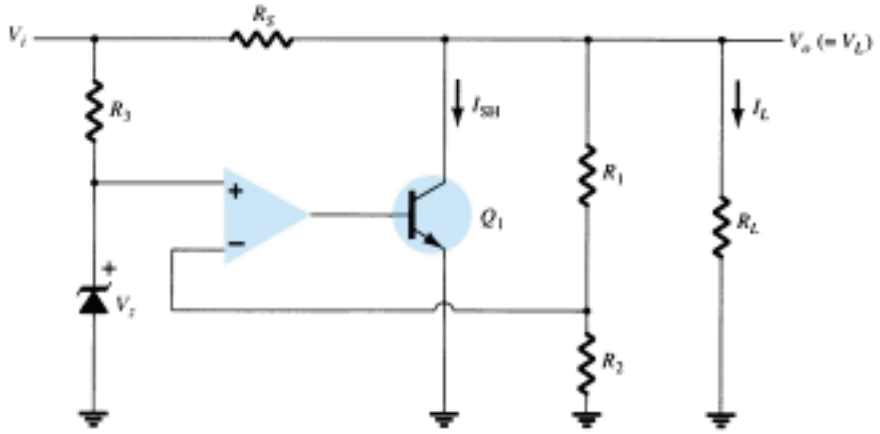


Figure 19.24 Shunt voltage regulator using op-amp.

Switching Regulation

A type of regulator circuit that is quite popular for its efficient transfer of power to the load is the switching regulator. Basically, a switching regulator passes voltage to

the load in pulses, which are then filtered to provide a smooth dc voltage. Figure 19.25 shows the basic components of such a voltage regulator. The added circuit complexity is well worth the improved operating efficiency obtained.

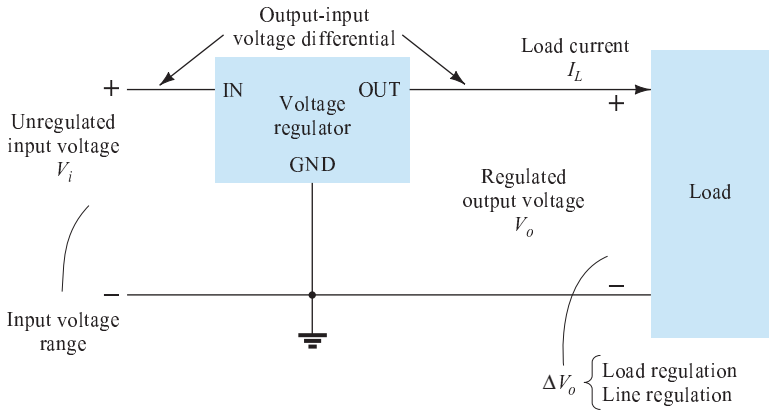


Figure 19.25 Block representation of three-terminal voltage regulator.

19.6 IC VOLTAGE REGULATORS

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering with a capacitor and *RC* filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milliamperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

Three-Terminal Voltage Regulators

Figure 19.25 shows the basic connection of a three-terminal voltage regulator IC to a load. The fixed voltage regulator has an unregulated dc input voltage, V_i, applied to one input terminal, a regulated output dc voltage, V_o, from a second terminal, with the third terminal connected to ground. For a selected regulator, IC device specifications list a voltage range over which the input voltage can vary to maintain a regulated output voltage over a range of load current. The specifications also list the amount of output voltage change resulting from a change in load current (load regulation) or in input voltage (line regulation).

Fixed Positive Voltage Regulators

The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure 19.26 shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12 V dc. An unregulated input voltage V_i is filtered by capacitor C_1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated +12 V, which is filtered by capacitor C_2 (mostly for any high-frequency noise).

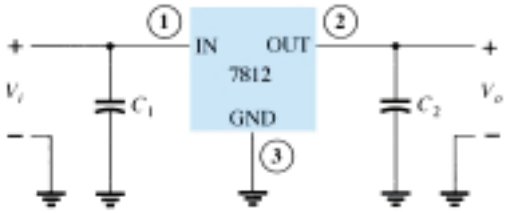


Figure 19.26 Connection of 7812 voltage regulator.

The third IC terminal is connected to ground (GND). While the input voltage may vary over some permissible voltage range and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets. A table of positive voltage regulator ICs is provided in Table 19.1.

TABLE 19.1 Positive Voltage Regulators in 7800 Series

IC Part	*Output Voltage (V)*	*Minimum V_i (V)*
7805	+5	7.3
7806	+6	8.3
7808	+8	10.5
7810	+10	12.5
7812	+12	14.6
7815	+15	17.7
7818	+18	21.0
7824	+24	27.1

The connection of a 7812 in a complete voltage supply is shown in the connection of Fig. 19.27. The ac line voltage (120 V rms) is stepped down to 18 V rms across each half of the center-tapped transformer. A full-wave rectifier and capacitor filter then provides an unregulated dc voltage, shown as a dc voltage of about 22 V, with ac ripple of a few volts as input to the voltage regulator. The 7812 IC then provides an output that is a regulated +12 V dc.

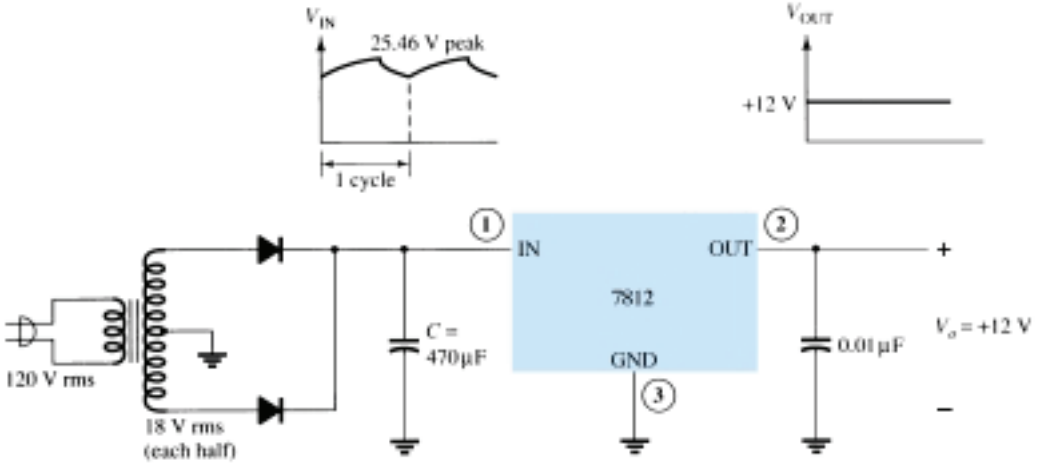
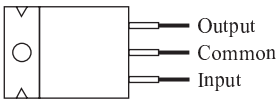


Figure 19.27 +12 V power supply.

POSITIVE VOLTAGE REGULATOR SPECIFICATIONS

The specifications sheet of voltage regulators is typified by that shown in Fig. 19.28 for the group of series 7800 positive voltage regulators. Some consideration of a few of the more important parameters should be made.



Nominal output voltage	Regulator
5 V	7805
6 V	7806
8 V	7808
10 V	7810
12 V	7812
15 V	7815
18 V	7818
24 V	7824

Absolute maximum ratings:

Input voltage	40 V
Continuous total dissipation	2 W
Operating free-air temperature range	−65 to 150°C

μA 7812C electrical characteristics:

Parameter	Min.	Typ.	Max.	Units
Output voltage	11.5	12	12.5	V
Input regulation		3	120	mV
Ripple rejection	55	71		dB
Output regulation		4	100	mV
Output resistance		0.018		Ω
Dropout voltage		2.0		V
Short-circuit output current		350		mA
Peak output current		2.2		A

Figure 19.28 Specification sheet data for voltage regulator ICs.

Output voltage: The specification for the 7812 shows that the output voltage is typically +12 V but could be as low as 11.5 V or as high as 12.5 V.

Output regulation: The output voltage regulation is seen to be typically 4 mV, to a maximum of 100 mV (at output currents from 0.25 to 0.75 A). This information specifies that the output voltage can typically vary only 4 mV from the rated 12 V dc.

Short-circuit output current: The amount of current is limited to typically 0.35 A if the output were to be short-circuited (presumably by accident or by another faulty component).

Peak output current: While the rated maximum current is 1.5 A for this series of IC, the typical peak output current that might be drawn by a load is 2.2 A. This shows that although the manufacturer rates the IC as capable of providing 1.5 A, one could draw somewhat more current (possibly for a short period of time).

Dropout voltage: The dropout voltage, typically 2 V, is the minimum amount of voltage across the input–output terminals that must be maintained if the IC is to operate as a regulator. If the input voltage drops too low or the output rises so that at least 2 V is not maintained across the IC input–output, the IC will no longer provide voltage regulation. One therefore maintains an input voltage large enough to assure that the dropout voltage is provided.

Fixed Negative Voltage Regulators

The series 7900 ICs provide negative voltage regulators, similar to those providing positive voltages. A list of negative voltage regulator ICs is provided in Table 19.2. As shown, IC regulators are available for a range of fixed negative voltages, the selected IC providing the rated output voltage as long as the input voltage is maintained greater than the minimum input value. For example, the 7912 provides an output of −12 V as long as the input to the regulator IC is more negative than −14.6 V.

TABLE 19.2 Negative Voltage Regulators in 7900 Series

IC Part	*Output Voltage (V)*	*Minimum V_i (V)*
7905	−5	−7.3
7906	−6	−8.4
7908	−8	−10.5
7909	−9	−11.5
7912	−12	−14.6
7915	−15	−17.7
7918	−18	−20.8
7924	−24	−27.1

EXAMPLE 19.12

Draw a voltage supply using a full-wave bridge rectifier, capacitor filter, and IC regulator to provide an output of +5 V.

Solution

The resulting circuit is shown in Fig. 19.29.

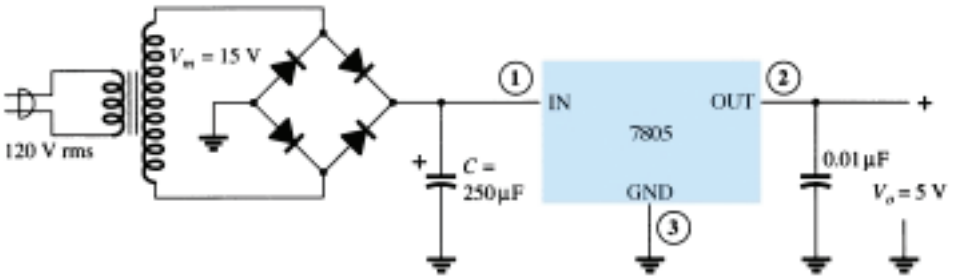


Figure 19.29 + 5-V power supply.

EXAMPLE 19.13

For a transformer output of 15 V and a filter capacitor of 250 μF, calculate the minimum input voltage when connected to a load drawing 400 mA.

Solution

The voltages across the filter capacitor are

$$V_r(\text{peak}) = \sqrt{3}\,V_r(\text{rms}) = \sqrt{3}\frac{2.4I_{dc}}{C} = \sqrt{3}\frac{2.4(400)}{250} = 6.65\text{ V}$$

$$V_{dc} = V_m - V_r(\text{peak}) = 15\text{ V} - 6.65\text{ V} = 8.35\text{ V}$$

Since the input swings around this dc level, the minimum input voltage can drop to as low as

$$V_i(\text{low}) = V_{\text{dc}} - V_r(\text{peak}) = 15\text{ V} - 6.65\text{ V} = \mathbf{8.35\text{ V}}$$

Since this voltage is greater than the minimum required for the IC regulator (from Table 19.1, $V_i = 7.3$ V), the IC can provide a regulated voltage to the given load.

EXAMPLE 19.14

Determine the maximum value of load current at which regulation is maintained for the circuit of Fig. 19.29.

Solution

To maintain $V_i(\text{min}) \geq 7.3$ V,

$$V_r(\text{peak}) \leq V_m - V_i(\text{min}) = 15\text{ V} - 7.3\text{ V} = 7.7\text{ V}$$

so that

$$V_r(\text{rms}) = \frac{V_r(\text{peak})}{\sqrt{3}} = \frac{7.7\text{ V}}{1.73} = 4.4\text{ V}$$

The value of load current is then

$$I_{\text{dc}} = \frac{V_r(\text{rms})C}{2.4} = \frac{(4.4\text{ V})(250)}{2.4} = \mathbf{458\text{ mA}}$$

Any current above this value is too large for the circuit to maintain the regulator output at +5 V.

Adjustable Voltage Regulators

Voltage regulators are also available in circuit configurations that allow the user to set the output voltage to a desired regulated value. The LM317, for example, can be operated with the output voltage regulated at any setting over the range of voltage from 1.2 to 37 V. Figure 19.30 shows how the regulated output voltage of an LM317 can be set.

Resistors R_1 and R_2 set the output to any desired voltage over the adjustment range (1.2 to 37 V). The output voltage desired can be calculated using

$$V_o = V_{\text{ref}}\left(1 + \frac{R_2}{R_1}\right) + I_{\text{adj}}R_2 \tag{19.21}$$

with typical IC values of

$$V_{\text{ref}} = 1.25\text{ V} \qquad \text{and} \qquad I_{\text{adj}} = 100\ \mu\text{A}$$

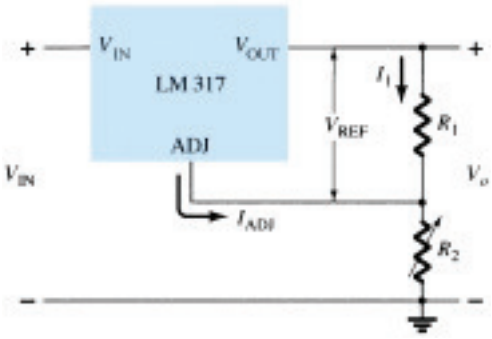


Figure 19.30 Connection of LM317 adjustable-voltage regulator.

EXAMPLE 19.15 Determine the regulated voltage in the circuit of Fig. 19.30 with $R_1 = 240\ \Omega$ and $R_2 = 2.4\ \text{k}\Omega$.

Solution

$$\text{Eq. (19.21): } V_o = 1.25\ \text{V}\left(1 + \frac{2.4\ \text{k}\Omega}{240\ \Omega}\right) + (100\ \mu\text{A})(2.4\ \text{k}\Omega)$$

$$= 13.75\ \text{V} + 0.24\ \text{V} = \mathbf{13.99\ V}$$

EXAMPLE 19.16 Determine the regulated output voltage of the circuit in Fig. 19.31.

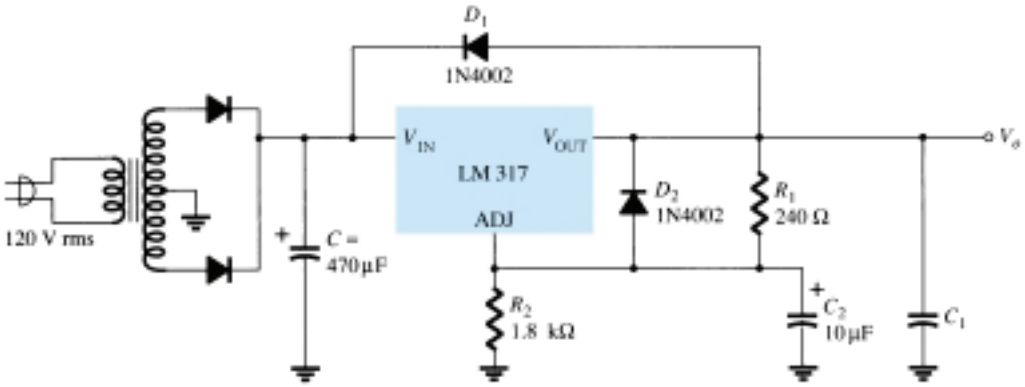


Figure 19.31 Positive adjustable-voltage regulator for Example 19.16.

Solution

The output voltage calculated using Eq. (19.21) is

$$V_o = 1.25\ \text{V}\left(1 + \frac{1.8\ \text{k}\Omega}{240\ \Omega}\right) + (100\ \mu\text{A})(1.8\ \text{k}\Omega) \approx \mathbf{10.8\ V}$$

A check of the filter capacitor voltage shows that an input–output difference of 2 V can be maintained up to at least 200 mA load current.

19.7 PSPICE WINDOWS

Program 19.1—Op-Amp Series Regulator

The op-amp series regulator circuit of Fig. 19.16 can be analyzed using PSpice Windows Design Center, with the resulting schematic drawn as shown in Fig. 19.32. The **Analysis Setup** was used to provide a dc voltage sweep from 8 to 15 V in 0.5-V increments. Diode D_1 provides a Zener voltage of 4.7 V ($V_Z = 4.7$), and transistor Q_1 is set to beta = 100. Using Eq. (19.18),

$$V_O = \left(1 + \frac{R_1}{R_2}\right)V_Z = \left(1 + \frac{1\ \text{k}\Omega}{1\ \text{k}\Omega}\right)4.7\ \text{V} = 9.4\ \text{V}$$

Notice in Fig. 19.32 that the regulated output voltage is 9.25 V when the input is 10 V. Figure 19.33 shows the **PROBE** output for the dc voltage sweep. Notice also that after the input goes above about 9 V, the output is held regulated at about 9.3 V.

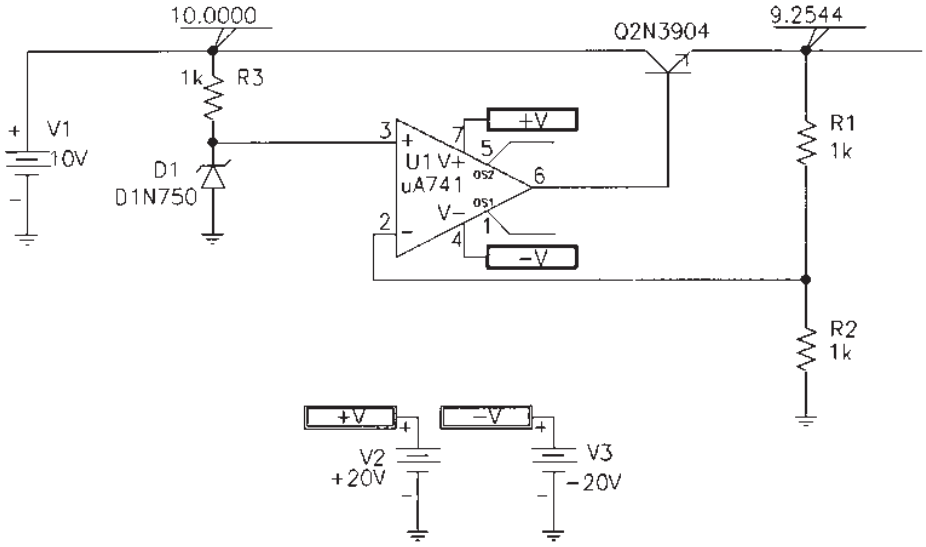


Figure 19.32 Op-amp series regulator drawn using PSpice Design Center.

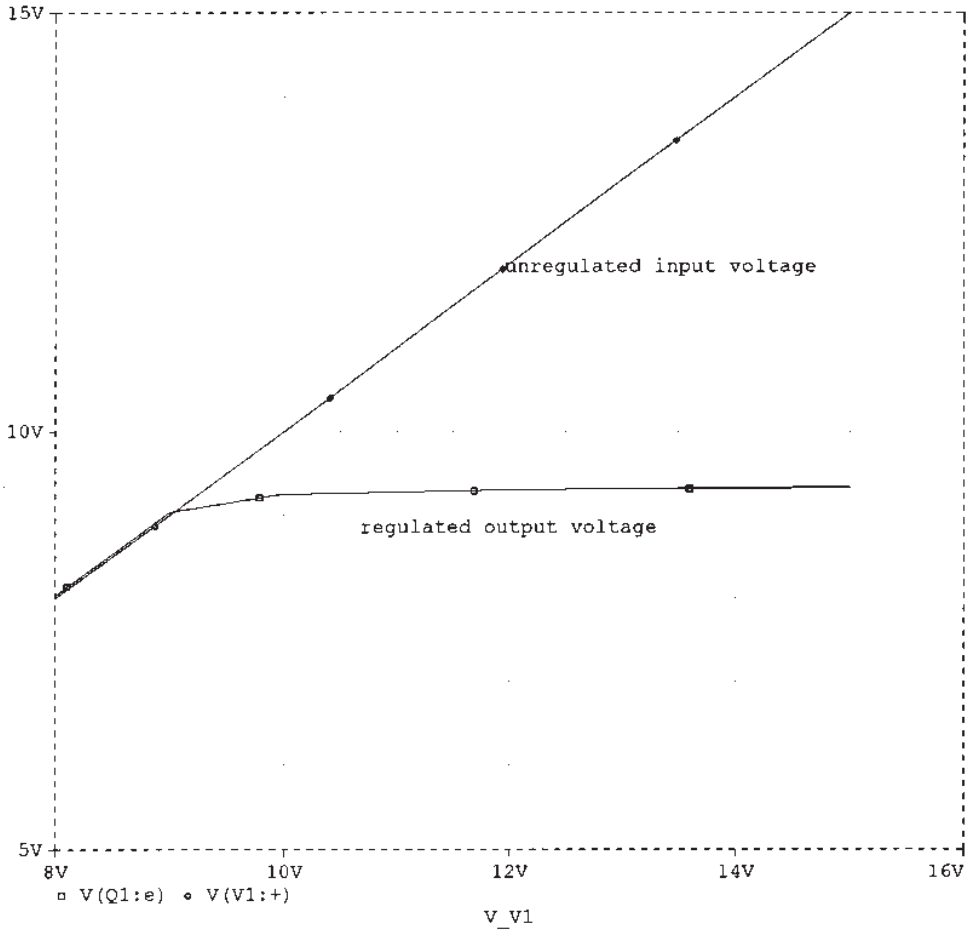


Figure 19.33 Probe output showing voltage regulation of Fig. 19.32.

Program 19.2—Shunt Voltage Regulator Using Op-Amp

The shunt voltage regulator circuit of Fig. 19.34 was drawn using PSpice Windows Design Center. With the Zener voltage set at 4.7 V and transistor beta set at 100, the output is 9.255 V when the input is 10 V. A dc sweep from 8 V to 15 V is shown in the **PROBE** output in Fig. 19.35. The circuit provides good voltage regulation for inputs from about 9.5 to over 14 V, the output being held at the regulated value of about 9.3 V.

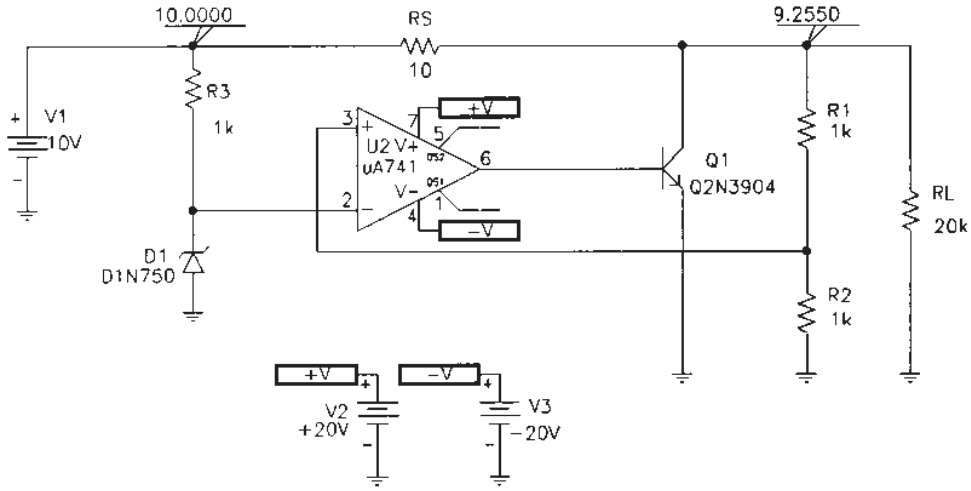


Figure 19.34 Shunt voltage regulator using op-amp (drawn using PSpice Design Center).

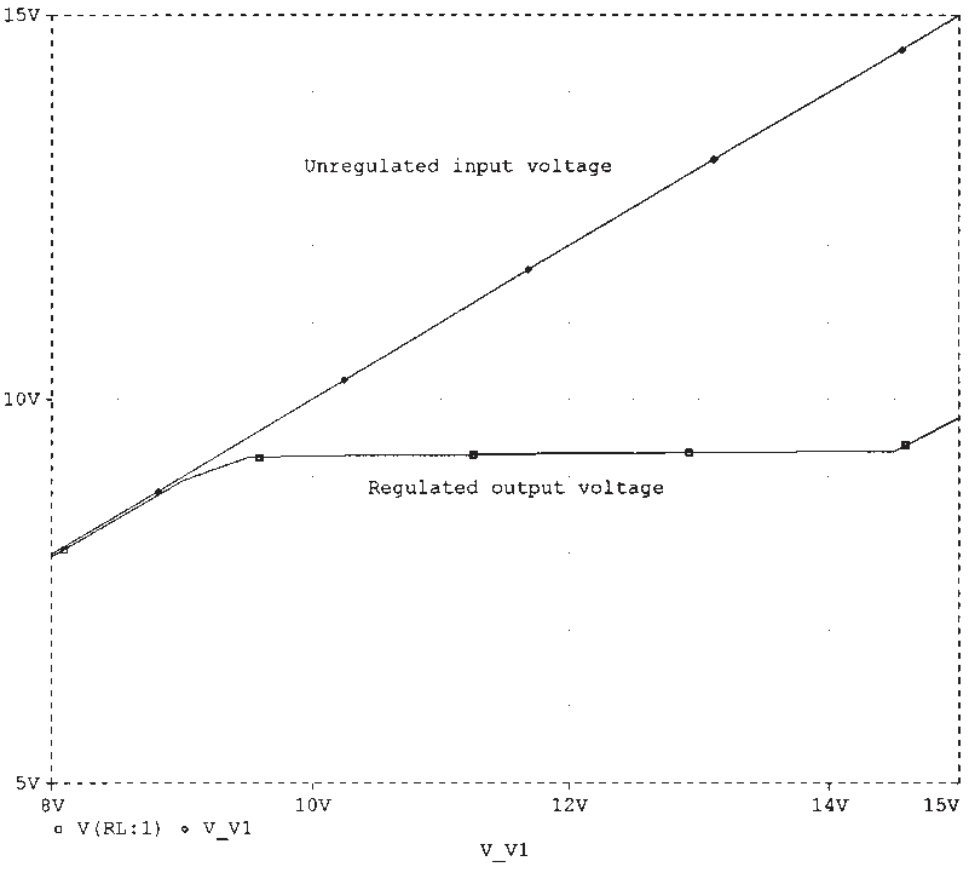


Figure 19.35 Probe output for dc voltage sweep of Fig. 19.34.

§ 19.2 General Filter Considerations

1. What is the ripple factor of a sinusoidal signal having peak ripple of 2 V on an average of 50 V?
2. A filter circuit provides an output of 28 V unloaded and 25 V under full-load operation. Calculate the percent voltage regulation.
3. A half-wave rectifier develops 20 V dc. What is the value of the ripple voltage?
4. What is the rms ripple voltage of a full-wave rectifier with output voltage 8 V dc?

§ 19.3 Capacitor Filter

5. A simple capacitor filter fed by a full-wave rectifier develops 14.5 V dc at 8.5% ripple factor. What is the output ripple voltage (rms)?
6. A full-wave rectified signal of 18 V peak is fed into a capacitor filter. What is the voltage regulation of the filter if the output is 17 V dc at full load?
7. A full-wave rectified voltage of 18 V peak is connected to a 400-μF filter capacitor. What are the ripple and dc voltages across the capacitor at a load of 100 mA?
8. A full-wave rectifier operating from the 60-Hz ac supply produces a 20-V peak rectified voltage. If a 200-μF capacitor is used, calculate the ripple at a load of 120 mA.
9. A full-wave rectifier (operating from a 60-Hz supply) drives a capacitor-filter circuit ($C = 100$ μF), which develops 12 V dc when connected to a 2.5-kΩ load. Calculate the output voltage ripple.
10. Calculate the size of the filter capacitor needed to obtain a filtered voltage having 15% ripple at a load of 150 mA. The full-wave rectified voltage is 24 V dc, and the supply is 60 Hz.
11. * A 500-μF capacitor provides a load current of 200 mA at 8% ripple. Calculate the peak rectified voltage obtained from the 60-Hz supply and the dc voltage across the filter capacitor.
12. Calculate the size of the filter capacitor needed to obtain a filtered voltage with 7% ripple at a load of 200 mA. The full-wave rectified voltage is 30 V dc, and the supply is 60 Hz.
13. Calculate the percent ripple for the voltage developed across a 120-μF filter capacitor when providing a load current of 80 mA. The full-wave rectifier operating from the 60-Hz supply develops a peak rectified voltage of 25 V.

§ 19.4 *RC* Filter

14. An *RC* filter stage is added after a capacitor filter to reduce the percent of ripple to 2%. Calculate the ripple voltage at the output of the *RC* filter stage providing 80 V dc.
15. * An *RC* filter stage ($R = 33$ Ω, $C = 120$ μF) is used to filter a signal of 24 V dc with 2 V rms operating from a full-wave rectifier. Calculate the percent ripple at the output of the *RC* section for a 100-mA load. Also, calculate the ripple of the filtered signal applied to the *RC* stage.
16. * A simple capacitor filter has an input of 40 V dc. If this voltage is fed through an *RC* filter section ($R = 50$ Ω, $C = 40$ μF), what is the load current for a load resistance of 500 Ω?
17. Calculate the rms ripple voltage at the output of an *RC* filter section that feeds a 1-kΩ load when the filter input is 50 V dc with 2.5-V rms ripple from a full-wave rectifier and capacitor filter. The *RC* filter section components are $R = 100$ Ω and $C = 100$ μF.
18. If the no-load output voltage for Problem 17 is 50 V, calculate the percent voltage regulation with a 1-kΩ load.

§ 19.5 Discrete Transistor Voltage Regulation

19. * Calculate the output voltage and Zener diode current in the regulator circuit of Fig. 19.36.
20. What regulated output voltage results in the circuit of Fig. 19.37?

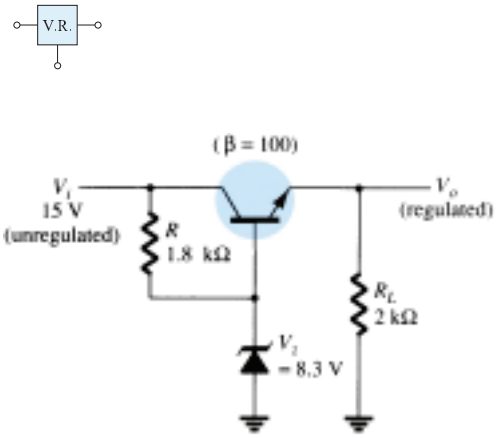


Figure 19.36 Problem 19

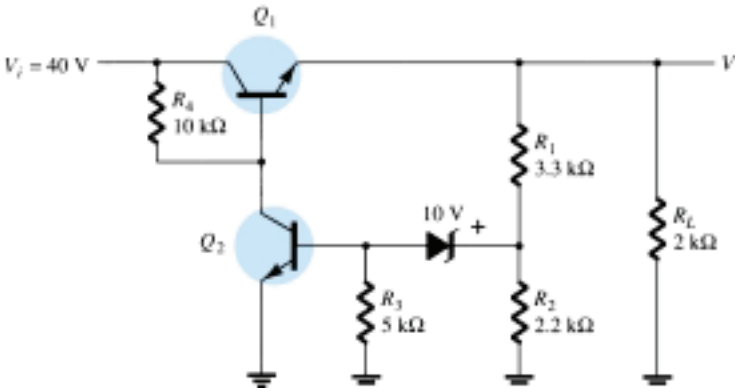


Figure 19.37 Problem 20

21. Calculate the regulated output voltage in the circuit of Fig. 19.38.

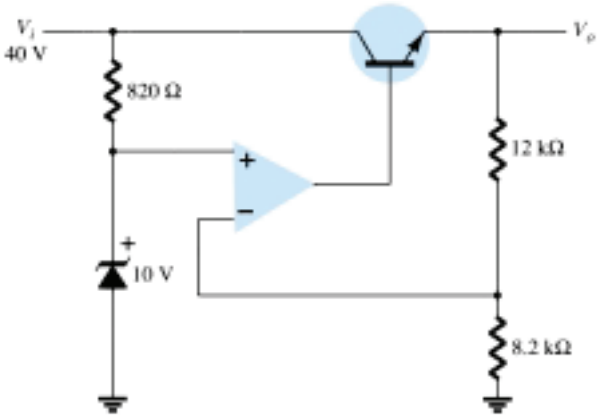


Figure 19.38 Problem 21

22. Determine the regulated voltage and circuit currents for the shunt regulator of Fig. 19.39.

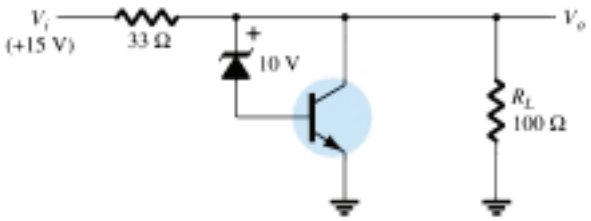


Figure 19.39 Problem 22

§ 19.6 IC Voltage Regulators

23. Draw the circuit of a voltage supply comprised of a full-wave bridge rectifier, capacitor filter, and IC regulator to provide an output of +12 V.

* **24.** Calculate the minimum input voltage of the full-wave rectifier and filter capacitor network in Fig. 19.40 when connected to a load drawing 250 mA.

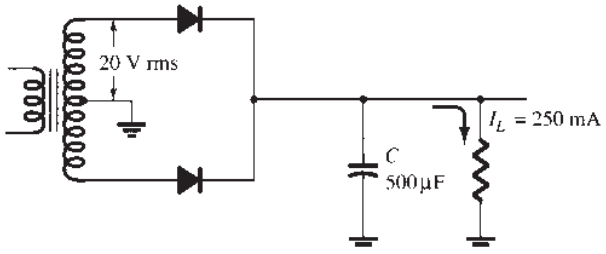


Figure 19.40 Problem 24

* **25.** Determine the maximum value of load current at which regulation is maintained for the circuit of Fig. 19.41.

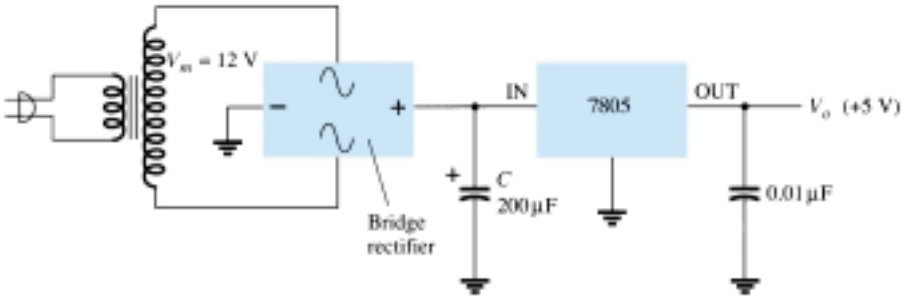


Figure 19.41 Problem 25

26. Determine the regulated voltage in the circuit of Fig. 19.30 with $R_1 = 240\ \Omega$ and $R_2 = 1.8\ \text{k}\Omega$.

27. Determine the regulated output voltage from the circuit of Fig. 19.42.

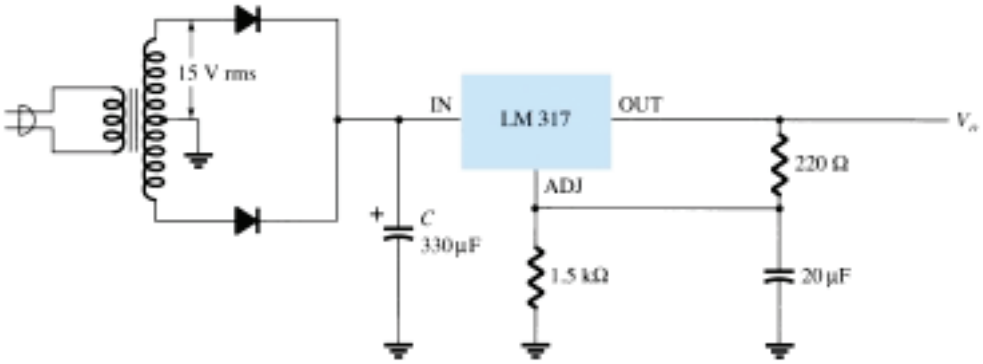


Figure 19.42 Problem 27

§ 19.7 PSpice Windows

* **28.** Modify the circuit of Fig. 19.32 to include a load resistor, R_L. Keeping the input voltage fixed at 10 V, do a sweep of the load resistor from 100 Ω to 20 kΩ, showing the output voltage using Probe.

* **29.** For the circuit of Fig. 19.34, do a sweep showing the output voltage for R_L varied from 5 kΩ to 20 kΩ.

* **30.** Run a PSpice analysis of the circuit of Fig. 19.19 for $V_Z = 4.7$ V, beta (Q_1) = beta (Q_2) = 100, and vary V_i from 5 V to 20 V.

*Please Note: Asterisks indicate more difficult problems.

CHAPTER

20 Other Two-Terminal Devices

20.1 INTRODUCTION

There are a number of two-terminal devices having a single *p-n* junction like the semiconductor or Zener diode but with different modes of operation, terminal characteristics, and areas of application. A number, including the Schottky, tunnel, varactor, photodiode, and solar cell, will be introduced in this chapter. In addition, two-terminal devices of a different construction, such as the photoconductive cell, LCD (liquid-crystal display), and thermistor, will be examined.

20.2 SCHOTTKY BARRIER (HOT-CARRIER) DIODES

In recent years, there has been increasing interest in a two-terminal device referred to as a *Schottky-barrier, surface-barrier,* or *hot-carrier* diode. Its areas of application were first limited to the very high frequency range due to its quick response time (especially important at high frequencies) and a lower noise figure (a quantity of real importance in high-frequency applications). In recent years, however, it is appearing more and more in low-voltage/high-current power supplies and ac-to-dc converters. Other areas of application of the device include radar systems, Schottky TTL logic for computers, mixers and detectors in communication equipment, instrumentation, and analog-to-digital converters.

Its construction is quite different from the conventional *p-n* junction in that a metal-semiconductor junction is created such as shown in Fig. 20.1. The semiconductor is

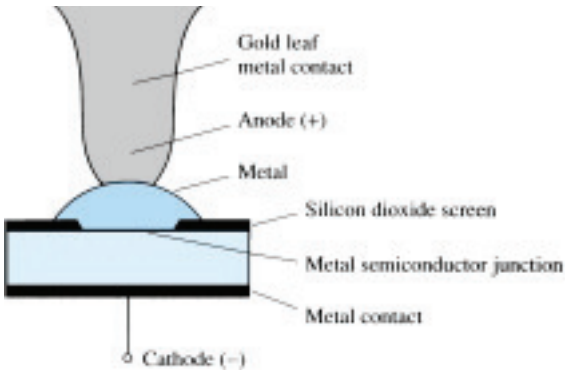


Figure 20.1 Passivated hot-carrier diode.

normally *n*-type silicon (although *p*-type silicon is sometimes used), while a host of different metals, such as molybdenum, platinum, chrome, or tungsten, are used. Different construction techniques will result in a different set of characteristics for the device, such as increased frequency range, lower forward bias, and so on. Priorities do not permit an examination of each technique here, but information will usually be provided by the manufacturer. In general, however, Schottky diode construction results in a more uniform junction region and a high level of ruggedness.

In both materials, the electron is the majority carrier. In the metal, the level of minority carriers (holes) is insignificant. When the materials are joined, the electrons in the *n*-type silicon semiconductor material immediately flow into the adjoining metal, establishing a heavy flow of majority carriers. Since the injected carriers have a very high kinetic energy level compared to the electrons of the metal, they are commonly called "hot carriers." In the conventional *p-n* junction, there was the injection of minority carriers into the adjoining region. Here the electrons are injected into a region of the same electron plurality. Schottky diodes are therefore unique in that conduction is entirely by majority carriers. The heavy flow of electrons into the metal creates a region near the junction surface depleted of carriers in the silicon material—much like the depletion region in the *p-n* junction diode. The additional carriers in the metal establish a "negative wall" in the metal at the boundary between the two materials. The net result is a "surface barrier" between the two materials, preventing any further current. That is, any electrons (negatively charged) in the silicon material face a carrier-free region and a "negative wall" at the surface of the metal.

The application of a forward bias as shown in the first quadrant of Fig. 20.2 will reduce the strength of the negative barrier through the attraction of the applied positive potential for electrons from this region. The result is a return to the heavy flow of electrons across the boundary, the magnitude of which is controlled by the level of the applied bias potential. The barrier at the junction for a Schottky diode is less than that of the *p-n* junction device in both the forward- and reverse-bias regions. The result is therefore a higher current at the same applied bias in the forward- and reverse-bias regions. This is a desirable effect in the forward-bias region but highly undesirable in the reverse-bias region.

The exponential rise in current with forward bias is described by Eq. (1.4) but with η dependent on the construction technique (1.05 for the metal whisker type of

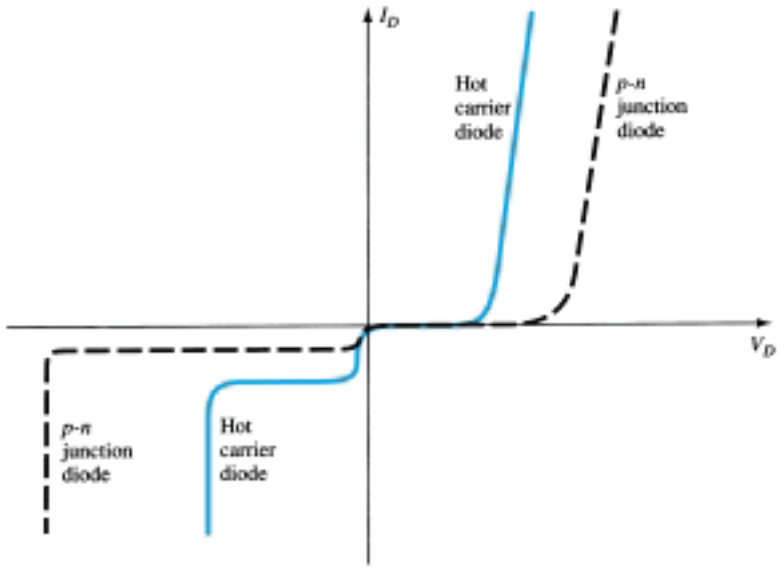


Figure 20.2 Comparison of characteristics of hot-carrier and *p-n* junction diodes.

construction, which is somewhat similar to the germanium diode). In the reverse-bias region, the current I_s is due primarily to those electrons in the metal passing into the semiconductor material. One of the areas of continuing research on the Schottky diode centers on reducing the high leakage currents that result with temperatures over 100°C. Through design, improvement units are now becoming available that have a temperature range from −65 to +150°C. At room temperature, I_s is typically in the microampere range for low-power units and milliampere range for high-power devices, although it is typically larger than that encountered using conventional *p-n* junction devices with the same current limits. In addition, the PIV of Schottky diodes is usually significantly less than that of a comparable *p-n* junction unit. Typically, for a 50-A unit, the PIV of the Schottky diode would be about 50 V as compared to 150 V for the *p-n* junction variety. Recent advances, however, have resulted in Schottky diodes with PIVs greater than 100 V at this current level. It is obvious from the characteristics of Fig. 20.2 that the Schottky diode is closer to the ideal set of characteristics than the point contact and has levels of V_T less than the typical silicon semiconductor *p-n* junction. The level of V_T for the "hot-carrier" diode is controlled to a large measure by the metal employed. There exists a required trade-off between temperature range and level of V_T. An increase in one appears to correspond to a resulting increase in the other. In addition, the lower the range of allowable current levels, the lower the value of V_T. For some low-level units, the value of V_T can be assumed to be essentially zero on an approximate basis. For the middle and high range, however, a value of 0.2 V would appear to be a good representative value.

The maximum current rating of the device is presently limited to about 75 A, although 100-A units appear to be on the horizon. One of the primary areas of application of this diode is in *switching power supplies* that operate in the frequency range of 20 kHz or more. A typical unit at 25°C may be rated at 50 A at a forward voltage of 0.6 V with a recovery time of 10 ns for use in one of these supplies. A *p-n* junction device with the same current limit of 50 A may have a forward voltage drop of 1.1 V and a recovery time of 30 to 50 ns. The difference in forward voltage may not appear significant, but consider the power dissipation difference: $P_{\text{hot carrier}} = (0.6\text{ V})(50\text{ A}) = 30\text{ W}$ compared to $P_{p\text{-}n} = (1.1\text{ V})(50\text{ A}) = 55\text{ W}$, which is a measurable difference when efficiency criteria must be met. There will, of course, be a higher dissipation in the reverse-bias region for the Schottky diode due to the higher leakage current, but the total power loss in the forward- and reverse-bias regions is still significantly improved as compared to the *p-n* junction device.

Recall from our discussion of reverse recovery time for the semiconductor diode that the injected minority carriers accounted for the high level of t_{rr} (the reverse recovery time). The absence of minority carriers at any appreciable level in the Schottky diode results in a reverse recovery time of significantly lower levels, as indicated above. This is the primary reason Schottky diodes are so effective at frequencies approaching 20 GHz, where the device must switch states at a very high rate. For higher frequencies the point-contact diode, with its very small junction area, is still employed.

The equivalent circuit for the device (with typical values) and a commonly used symbol appear in Fig. 20.3. A number of manufacturers prefer to use the standard diode symbol for the device since its function is essentially the same. The inductance L_P and capacitance C_P are package values, and r_B is the series resistance, which includes the contact and bulk resistance. The resistance r_d and capacitance C_J are values defined by equations introduced in earlier sections. For many applications, an excellent approximate equivalent circuit simply includes an ideal diode in parallel with the junction capacitance as shown in Fig. 20.4.

A number of hot-carrier rectifiers manufactured by Motorola Semiconductor Products, Inc., appear in Fig. 20.5 with their specifications and terminal identification.

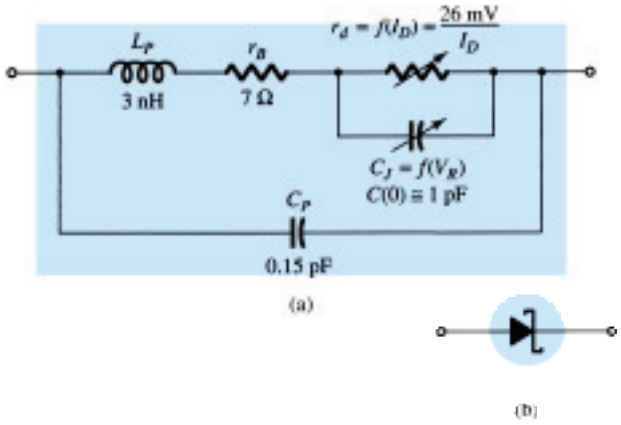


Figure 20.3 Schottky (hot-carrier) diode: (a) equivalent circuit; (b) symbol.

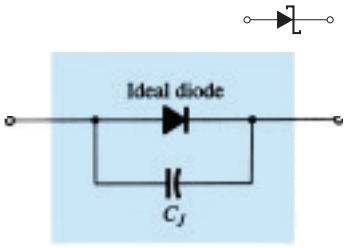
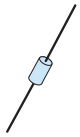
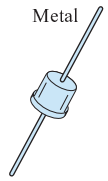


Figure 20.4 Approximate equivalent circuit for the Schottky diode.

I_o, Average rectified forward current (amperes)															
		0.5 A	1.0 A		3.0 A		3.0 A	5.0 A	15 A		25 A		40 A		
	Case	51-02 (DO-7) Glass	59-04 Plastic		267 Plastic		60 Metal		257 (DO-4) Metal				257 (DO-5) Metal		430-2 (DO-21) Metal
V_{RRM} (Volts)	Anode / Cathode:														
20		MBR020	IN5817	MBR120P	IN5820	MBR320P	MBR320M	IN5823	IN5826	MBR1520	IN5829	MBR2520	IN5832	MBR4020	MBR4020PF
30		MBR030	IN5818	MBR130P	IN5821	MBR330P	MBR330M	IN5824	IN5827	MBR1530	IN5830	MBR2530	IN5833	MBR4030	MBR4030PF
35				MBR135P		MBR335P	MBR335M			MBR1535		MBR2535		MBR4035	MBR4035PF
40			IN5819	MBR140P	IN5822	MBR340P	MBR340M	IN5825	IN5828	MBR1540	IN5831	MBR2540	IN5834	MBR4040	
I_{FSM} (Amps)		5.0	100	50	250	200	500	500	500	500	800	800	800	800	800
T_C @ Rated I_o (°C)									85	80	85	80	75	70	50
T_J Max		125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C	125°C
Max V_F @ $I_{FM} = I_o$		0.50 V	*0.60 V	0.65 V	*0.525 V	0.60 V	0.45 V@5A	*0.38 V	*0.50 V	0.55 V	*0.48 V	0.55 V	*0.59 V	0.63 V	0.63 V

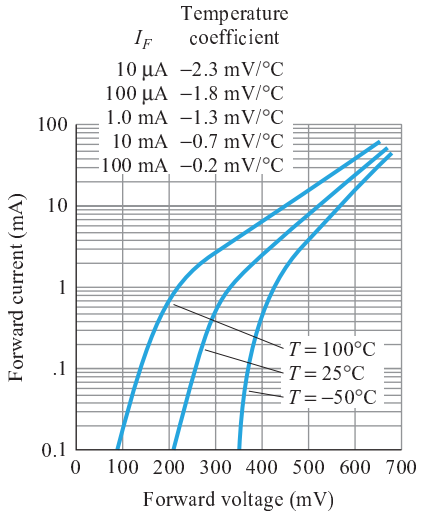
. . . Schottky barrier devices, ideal for use in low-voltage, high-frequency power supplies and as free-wheeling diodes. These units feature very low forward voltages and switching times estimated at less than 10 ns. They are offered in current ranges of 0.5 to 5.0 amperes and in voltages to 40.

V_{RRM} –respective peak reverse voltage
I_{FSM} –forward current, surge peak
I_{FM} –forward current, maximum

Figure 20.5 Motorola Schottky barrier devices. (Courtesy Motorola Semiconductor Products, Incorporated.)

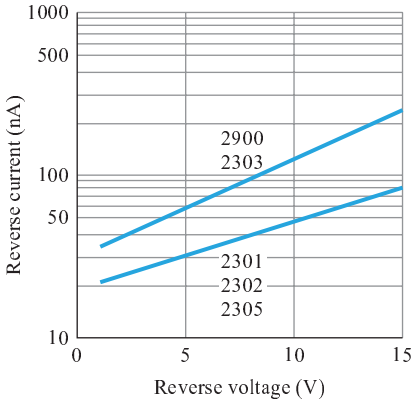
Note that the maximum forward voltage drop V_F does not exceed 0.65 V for any of the devices, while this was essentially V_T for a silicon diode.

Three sets of curves for the Hewlett-Packard 5082-2300 series of general-purpose Schottky barrier diodes are provided in Fig. 20.6. Note at $T = 100°C$ in Fig. 20.6a that V_F is only 0.1 V at a current of 0.01 mA. Note also that the reverse current has been limited to nanoamperes in Fig. 20.6b and the capacitance to 1 pF in Fig. 20.6c to ensure a high switching rate.



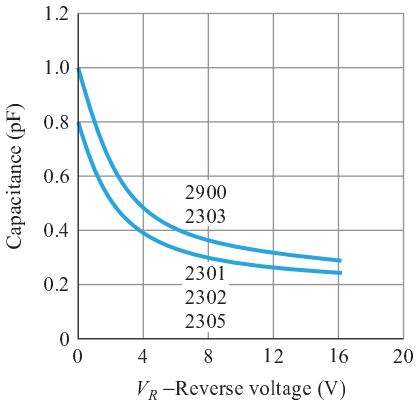
I-V Curve Showing Typical Temperature Variation for 5082-2300 Series Schottky Diodes.

(a)



5082-2300 Series Typical Reverse Current vs. Reverse Voltage at $T_A = 25°C$.

(b)



5082-2300 Series Typical Capacitance vs. Reverse Voltage at $T_A = 25°C$.

(c)

Figure 20.6 Characteristic curves for Hewlett-Packard 5082-2300 series of general-purpose Schottky barrier diodes. (Courtesy Hewlett-Packard Corporation.)

20.3 VARACTOR (VARICAP) DIODES

Varactor [also called varicap, VVC (voltage-variable capacitance), or tuning] diodes are semiconductor, voltage-dependent, variable capacitors. Their mode of operation depends on the capacitance that exists at the *p-n* junction when the element is reverse-biased. Under reverse-bias conditions, it was established that there is a region of uncovered charge on either side of the junction that together the regions make up the depletion region and define the depletion width W_d. The transition capacitance (C_T) established by the isolated uncovered charges is determined by

$$C_T = \epsilon \frac{A}{W_d} \tag{20.1}$$

where ϵ is the permittivity of the semiconductor materials, A the p-n junction area, and W_d the depletion width.

As the reverse-bias potential increases, the width of the depletion region increases, which in turn reduces the transition capacitance. The characteristics of a typical commercially available varicap diode appear in Fig. 20.7. Note the initial sharp decline in C_T with increase in reverse bias. The normal range of V_R for VVC diodes is limited to about 20 V. In terms of the applied reverse bias, the transition capacitance is given approximately by

$$C_T = \frac{K}{(V_T + V_R)^n} \tag{20.2}$$

where K = constant determined by the semiconductor material and construction technique
V_T = knee potential as defined in Section 1.6
V_R = magnitude of the applied reverse-bias potential
n = $\frac{1}{2}$ for alloy junctions and $\frac{1}{3}$ for diffused junctions

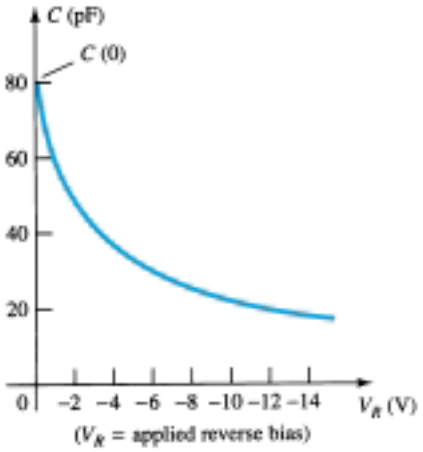


Figure 20.7 Varicap characteristics: C (pF) versus V_R.

In terms of the capacitance at the zero-bias condition $C(0)$, the capacitance as a function of V_R is given by

$$C_T(V_R) = \frac{C(0)}{(1 + |V_R/V_T|)^n} \tag{20.3}$$

The symbols most commonly used for the varicap diode and a first approximation for its equivalent circuit in the reverse-bias region are shown in Fig. 20.8. Since

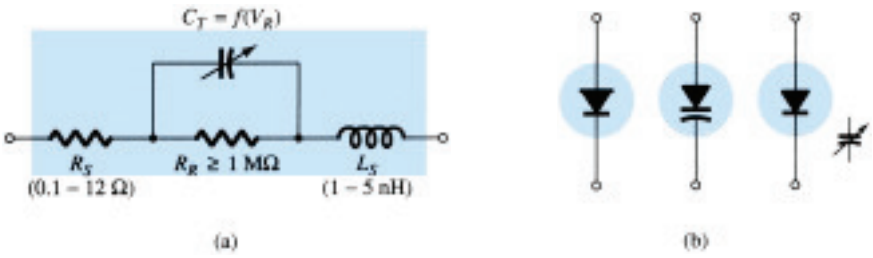


Figure 20.8 Varicap diode: (a) equivalent circuit in the reverse-bias region; (b) symbols.

we are in the reverse-bias region, the resistance in the equivalent circuit is very large in magnitude—typically 1 MΩ or larger—while R_S, the geometric resistance of the diode, is, as indicated in Fig. 20.8, very small. The magnitude of C_T will vary from about 2 to 100 pF depending on the varicap considered. To ensure that R_R is as large (for minimum leakage current) as possible, silicon is normally used in varicap diodes. The fact that the device will be employed at very high frequencies requires that we include the inductance L_S even though it is measured in nanohenries. Recall that $X_L = 2\pi fL$ and a frequency of 10 GHz with $L_S = 1$ nH will result in an $X_{LS} = 2\pi fL = (6.28)(10^{10}\text{ Hz})(10^{-9}\text{ F}) = 62.8\ \Omega$. There is obviously, therefore, a frequency limit associated with the use of each varicap diode.

Assuming the proper frequency range and a low value of R_S and X_{L_S} compared to the other series elements, then the equivalent circuit for the varicap of Fig. 20.8a can be replaced by the variable capacitor alone. The complete data sheet and its characteristic curves appear in Figs. 20.9 and 20.10, respectively. The C_3/C_{25} ratio in Fig. 20.9

BB 139

VHF/FM VARACTOR DIODE

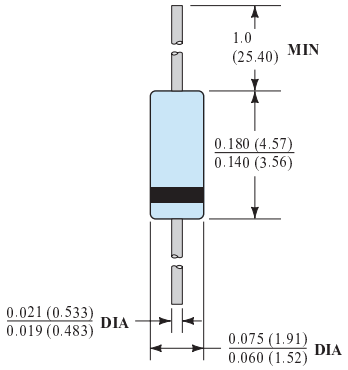
DIFFUSED SILICON PLANAR

- C_3/C_{25} . . . 5.0-6.5
- **MATCHED SETS** (Note 2)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Temperatures		
Storage Temperature Range		−55°C to +150°C
Maximum Junction Operating Temperature		+150°C
Lead Temperature		+260°C
Maximum Voltage		
WIV	Working Inverse Voltage	30 V

DC-35 OUTLINE



NOTES:
Copper clad steel leads, tin plated
Gold plated leads available
Hermetically sealed glass package
Package weight is 0.14 gram

ELECTRICAL CHARACTERISTICS (25°C Ambient Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS
BV	Breakdown Voltage	30			V	$I_R = 100\ \mu A$
I_R	Reverse Current		10 0.1	50 0.5	nA μA	$V_R = 28$ V $V_R = 28$ V, $T_A = 60°C$
C	Capacitance	 4.3	29 5.1	 6.0	pF pF	$V_R = 3.0$ V, $f = 1$ MHz $V_R = 25$ V, $f = 1$ MHz
C_3/C_{25}	Capacitance Ratio	5.0	5.7	6.5		$V_R = 3$ V/25 V, $f = 1$ MHz
Q	Figure of Merit		150			$V_R = 3.0$ V, $f = 100$ MHz
R_S	Series Resistance		0.35		Ω	$C = 10$ pF, $f = 600$ MHz
L_S	Series Inductance		2.5		nH	1.5 mm from case
f_o	Series Resonant Frequency		1.4		GHz	$V_R = 25$ V

NOTES;
1. These ratings are limiting values above which the serviceability of the diodes may be impaired.
2. The capacitance diffrence between any two diodes in one set is less than 3% over the reverse voltage range of 0.5 V to 28 V

Figure 20.9 Electrical characteristics for a VHF/FM Fairchild varactor diode. (Courtesy Fairchild Camera and Instrument Corporation.)

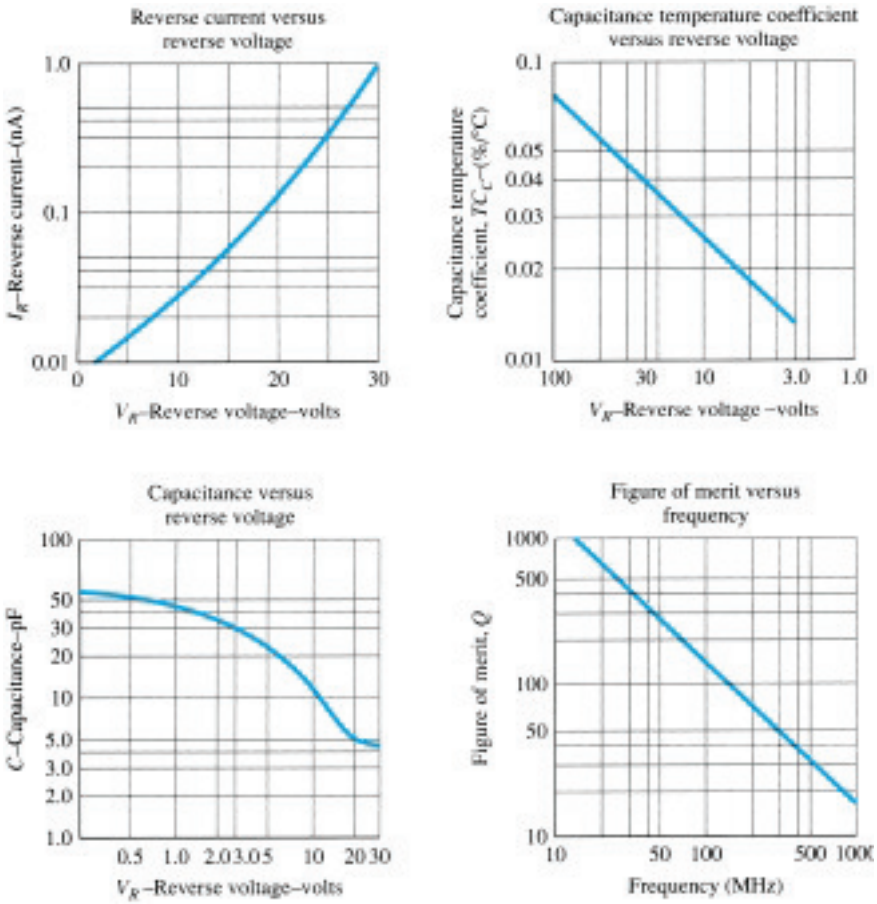


Figure 20.10 Characteristic curves for a VHF/FM Fairchild varactor diode. (Courtesy Fairchild Camera and Instrument Corporation.)

is the ratio of capacitance levels at reverse-bias potentials of 3 and 25 V. It provides a quick estimate of how much the capacitance will change with reverse-bias potential. The figure of merit is a quantity of consideration in the application of the device and is a measure of the ratio of energy stored by the capacitive device per cycle to the energy dissipated (or lost) per cycle. Since energy loss is seldom considered a positive attribute, the higher its relative value the better. The resonant frequency of the device is determined by $f_o = 1/2\pi\sqrt{LC}$ and affects the range of application of the device.

In Fig. 20.10, most quantities are self-explanatory. However, the *capacitance temperature coefficient* is defined by

$$TC_C = \frac{\Delta C}{C_0(T_1 - T_0)} \times 100\% \qquad \%/°C \qquad (20.4)$$

where ΔC is the change in capacitance due to the temperature change $T_1 - T_0$ and C_0 is the capacitance at T_0 for a particular reverse-bias potential. For example, Fig. 20.9 indicates that $C_0 = 29$ pF with $V_R = 3$ V and $T_0 = 25°C$. A change in capacitance ΔC could then be determined using Eq. (20.4) simply by substituting the new temperature T_1 and the TC_C as determined from the graph (= 0.013). At a new V_R, the value of TC_C would change accordingly. Returning to Fig. 20.9, note that the maximum frequency appearing is 600 MHz. At this frequency,

$$X_L = 2\pi fL = (6.28)(600 \times 10^6 \text{ Hz})(2.5 \times 10^{-9} \text{ F}) = 9.42\ \Omega$$

normally a quantity of sufficiently small magnitude to be ignored.

Some of the high-frequency (as defined by the small capacitance levels) areas of application include FM modulators, automatic-frequency-control devices, adjustable bandpass filters, and parametric amplifiers.

In Fig. 20.11, the varactor diode is employed in a tuning network. That is, the resonant frequency of the parallel L-C combination is determined by $f_p = 1/2\pi\sqrt{L_2C_T'}$ (high-Q system) with the level of $C_T' = C_T + C_C$ determined by the applied reverse-bias potential V_{DD}. The coupling capacitor C_C is present to provide isolation between the shorting effect of L_2 and the applied bias. The selected frequencies of the tuned network are then passed on to the high input amplifier for further amplification.

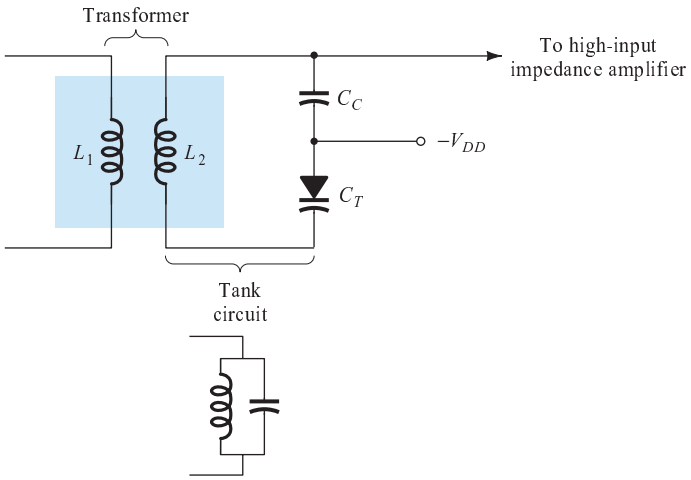


Figure 20.11 Tuning network employing a varactor diode.

20.4 POWER DIODES

There are a number of diodes designed specifically to handle the high-power and high-temperature demands of some applications. The most frequent use of power diodes occurs in the rectification process, in which ac signals (having zero average value) are converted to ones having an average or dc level. As noted in Chapter 2, when used in this capacity, diodes are normally referred to as *rectifiers*.

The majority of the power diodes are constructed using silicon because of its higher current, temperature, and PIV ratings. The higher current demands require that the junction area be larger, to ensure that there is a low forward diode resistance. If the forward resistance were too large, the I^2R losses would be excessive. The current capability of power diodes can be increased by placing two or more in parallel, and the PIV rating can be increased by stacking the diodes in series.

Various types of power diodes and their current rating have been provided in Fig. 20.12a. The high temperatures resulting from the heavy current require, in many cases, that heat sinks be used to draw the heat away from the element. A few of the various types of heat sinks available are shown in Fig. 20.12b. If heat sinks are not employed, stud diodes are designed to be attached directly to the chassis, which in turn will act as the heat sink.

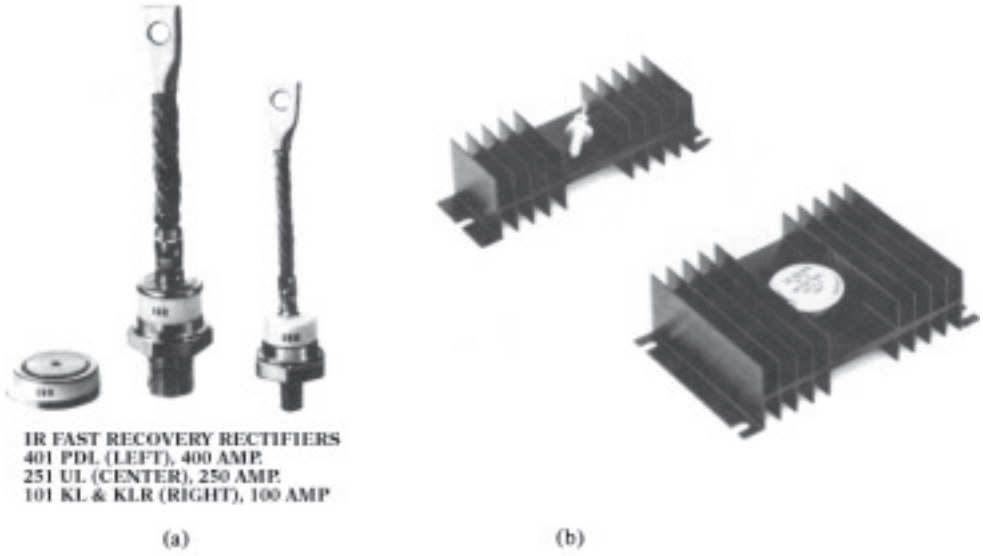


Figure 20.12 Power diodes and heat sinks. (Courtesy International Rectifier Corporation.)

20.5 TUNNEL DIODES

The tunnel diode was first introduced by Leo Esaki in 1958. Its characteristics, shown in Fig. 20.13, are different from any diode discussed thus far in that it has a negative-resistance region. In this region, an increase in terminal voltage results in a reduction in diode current.

The tunnel diode is fabricated by doping the semiconductor materials that will form the *p-n* junction at a level one hundred to several thousand times that of a typical semiconductor diode. This will result in a greatly reduced depletion region, of the order of magnitude of 10^{-6} cm, or typically about $\frac{1}{100}$ the width of this region for a typical semiconductor diode. It is this thin depletion region that many carriers can "tunnel" through, rather than attempt to surmount, at low forward-bias potentials that accounts for the peak in the curve of Fig. 20.13. For comparison purposes, a typical

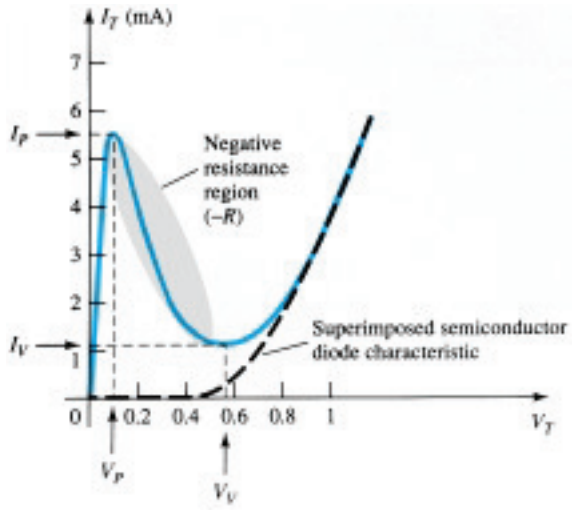


Figure 20.13 Tunnel diode characteristics.

semiconductor diode characteristic has been superimposed on the tunnel-diode characteristic of Fig. 20.13.

This reduced depletion region results in carriers "punching through" at velocities that far exceed those available with conventional diodes. The tunnel diode can therefore be used in high-speed applications such as in computers, where switching times in the order of nanoseconds or picoseconds are desirable.

You will recall from Section 1.14 that an increase in the doping level will drop the Zener potential. Note the effect of a very high doping level on this region in Fig. 20.13. The semiconductor materials most frequently used in the manufacture of tunnel diodes are germanium and gallium arsenide. The ratio I_P/I_V is very important for computer applications. For germanium, it is typically 10:1, while for gallium arsenide, it is closer to 20:1.

The peak current, I_P, of a tunnel diode can vary from a few microamperes to several hundred amperes. The peak voltage, however, is limited to about 600 mV. For this reason, a simple VOM with an internal dc battery potential of 1.5 V can severely damage a tunnel diode if applied improperly.

The tunnel diode equivalent circuit in the negative-resistance region is provided in Fig. 20.14, with the symbols most frequently employed for tunnel diodes. The values for each parameter are for the 1N2939 tunnel diode whose specifications appear in Table 20.1. The inductor L_S is due mainly to the terminal leads. The resistor R_S is due to the leads, ohmic contact at the lead–semiconductor junction, and the semiconductor materials themselves. The capacitance C is the junction diffusion capacitance, and the R is the negative resistance of the region. The negative resistance finds application in oscillators to be described later.

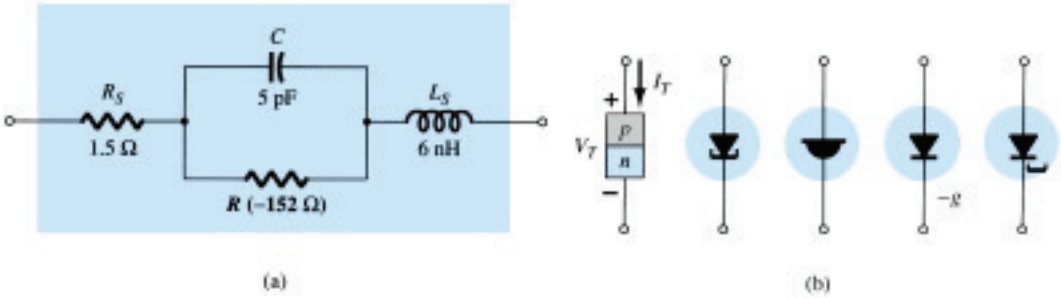


Figure 20.14 Tunnel diode: (a) equivalent circuit; (b) symbols.

TABLE 20.1 Specifications: Ge 1N2939

	Minimum	*Typical*	*Maximum*	
Absolute maximum ratings (25°C)				
Forward current (−55 to +100°C)		5 mA		
Reverse current (−55 to +100°C)		10 mA		
Electrical characteristics (25°C)($\frac{1}{8}$-in. leads)				
I_P	0.9	1.0	1.1	mA
I_V		0.1	0.14	mA
V_P	50	60	65	mV
V_V		350		mV
Reverse voltage (I_R = 1.0 mA)			30	mV
Forward peak point current voltage, V_{fp}	450	500	600	mV
I_P/I_V		10		
$-R$		−152		Ω
C		5	15	pF
L_S		6		nH
R_S		1.5	4.0	Ω

Note the lead length of $\frac{1}{8}$ in. included in the specifications. An increase in this length will cause L_S to increase. In fact, it was given for this device that L_S will vary 1 to 12 nH, depending on lead length. At high frequencies ($X_{L_S} = 2\pi f L_S$), this factor can take its toll.

The fact that $V_{fp} = 500$ mV (typ.) and I_{forward} (max.) = 5 mA indicates that tunnel diodes are low-power devices [$P_D = (0.5\text{ V})(5\text{ mA}) = 2.5$ mW], which is also excellent for computer applications. A rendering of the device appears in Fig. 20.15.

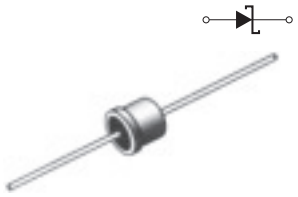


Figure 20.15 A Ge IN2939 tunnel diode. (Courtesy Powerex, Inc.)

Although the use of tunnel diodes in present-day high-frequency systems has been dramatically stalled by manufacturing techniques that suggest alternatives to the tunnel diode, its simplicity, linearity, low power drain, and reliability ensure its continued life and application. The basic construction of an advance design tunnel diode appears in Fig. 20.16 with a photograph of the actual junction.

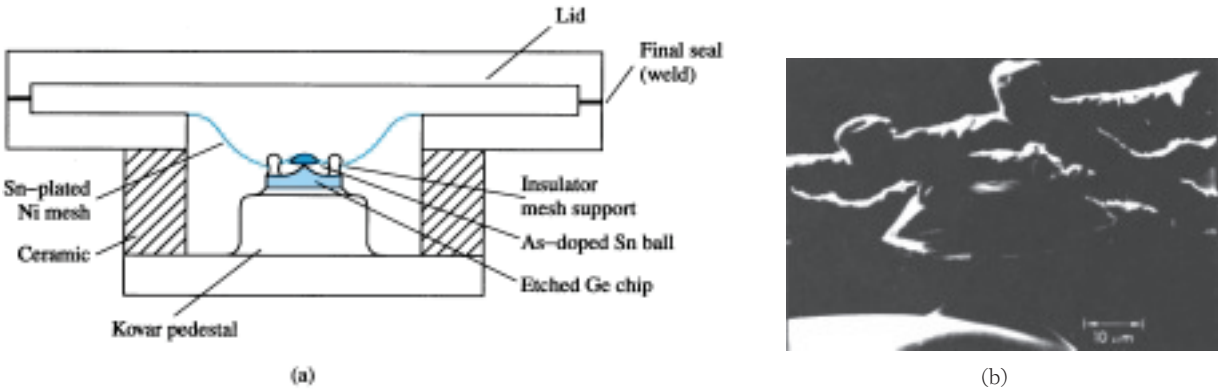


Figure 20.16 Tunnel diode: (a) construction; (b) photograph. (Courtesy *COM SAT Technical Review*, P. F. Varadi and T. D. Kirkendall.)

In Fig. 20.17, the chosen supply voltage and load resistance have defined a load line that intersects the tunnel diode characteristics at three points. Keep in mind that the load line is determined solely by the network and the characteristics by the device. The intersections at *a* and *b* are referred to as *stable* operating points, due to the positive resistance characteristic. That is, at either of these operating points, a slight disturbance in the network will not set the network into oscillations or result in a significant change in the location of the *Q*-point. For instance, if the defined operating point is at *b*, a slight increase in supply voltage *E* will move the operating point up the curve since the voltage across the diode will increase. Once the disturbance has

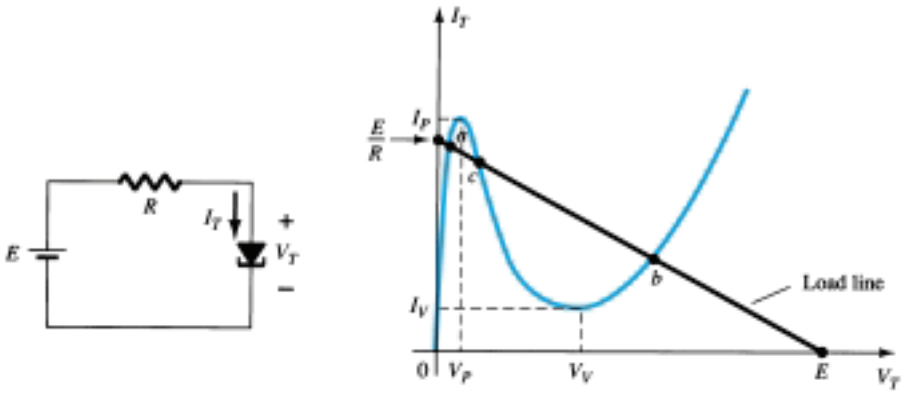


Figure 20.17 Tunnel diode and resulting load line.

passed, the voltage across the diode and the associated diode current will return to the levels defined by the Q-point at b. The operating point defined by c is an *unstable* one because a slight change in the voltage across or current through the diode will result in the Q-point moving to either a or b. For instance, the slightest increase in E will cause the voltage across the tunnel diode to increase above its level at c. In this region, however, an increase in V_T will cause a decrease in I_T and a further increase in V_T. This increased level in V_T will result in a continuing decrease in I_T, and so on. The result is an increase in V_T and a change in I_T until the stable operating point at b is established. A slight drop in supply voltage would result in a transition to stability at point a. In other words, point c can be defined as the operating point using the load-line technique, but once the system is energized, it will eventually stabilize at location a or b.

The availability of a negative resistance region can be put to good use in the design of oscillators, switching networks, pulse generators, and amplifiers.

In Fig. 20.18a, a *negative-resistance oscillator* was constructed using a tunnel diode. The choice of network elements is designed to establish a load line such as shown in Fig. 20.18b. Note that the only intersection with the characteristics is in the unstable negative-resistance region—a stable operating point is not defined. When the power is turned on, the terminal voltage of the supply will build up from 0 V to a final value of E volts. Initially, the current I_T will increase from 0 mA to I_P, resulting in a storage of energy in the inductor in the form of a magnetic field. However, once I_P is reached, the diode characteristics suggest that the current I_T must now decrease with increase in voltage across the diode. This is a contradiction to the fact that

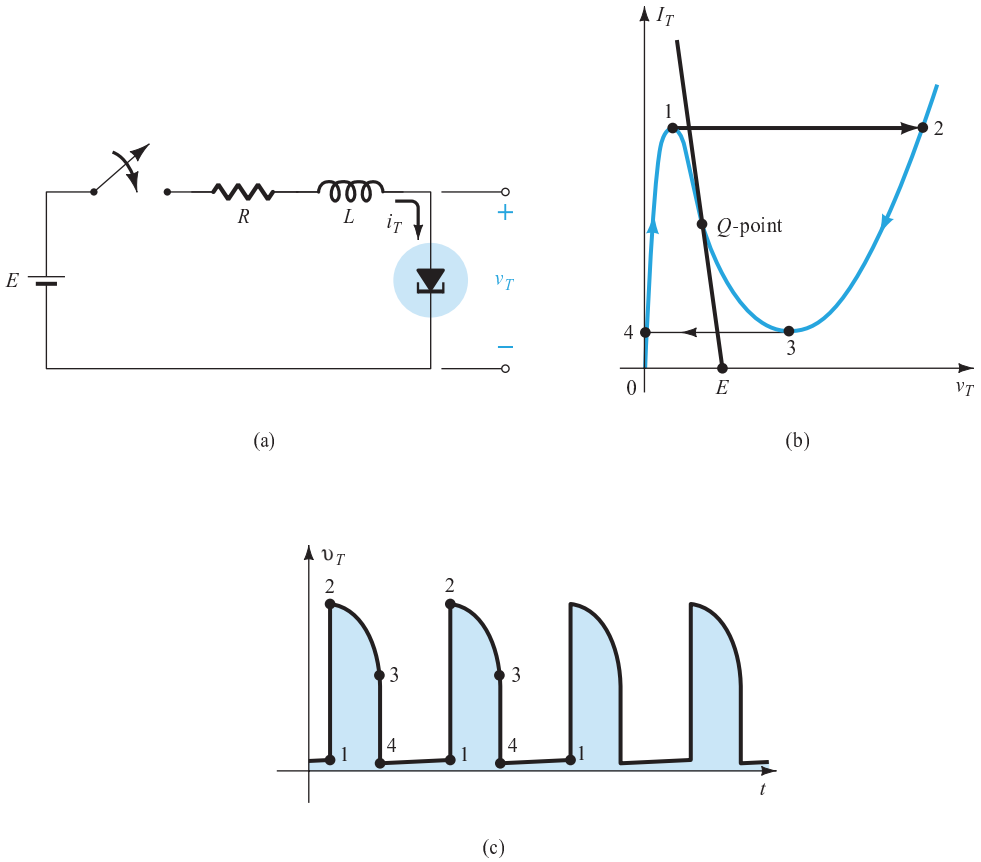


Figure 20.18 Negative-resistance oscillator.

$$E = I_T R + I_T(-R_T)$$

and

$$E = \underbrace{I_T}_{\text{less}}\underbrace{(R - R_T)}_{\text{less}}$$

If both elements of the equation above were to decrease, it would be impossible for the supply voltage to reach its set value. Therefore, for the current I_T to continue rising, the point of operation must shift from point 1 to point 2. However, at point 2, the voltage V_T has jumped to a value greater than the applied voltage (point 2 is to the right of any point on the network load line). To satisfy Kirchhoff's voltage law, the polarity of the transient voltage across the coil must reverse and the current begin to decrease as shown from 2 to 3 on the characteristics. When V_T drops to V_V, the characteristics suggest that the current I_T will begin to increase again. This is unacceptable since V_T is still more than the applied voltage and the coil is discharging through the series circuit. The point of operation must shift to point 4 to permit a continuation of the decrease in I_T. However, once at point 4, the potential levels are such that the tunnel current can again increase from 0 mA to I_P as shown on the characteristics. The process will repeat itself again and again, never settling in on the operating point defined for the unstable region. The resulting voltage across the tunnel diode appears in Fig. 20.18c and will continue as long as the dc supply is energized. The result is an oscillatory output established by a fixed supply and a device with a negative-resistance characteristic. The waveform of Fig. 20.18c has extensive application in timing and computer logic circuitry.

A tunnel diode can also be used to generate a sinusoidal voltage using simply a dc supply and a few passive elements. In Fig. 20.19a, the closing of the switch will result in a sinusoidal voltage that will decrease in amplitude with time. Depending on the elements employed, the time period can be from one almost instantaneous to one measurable in minutes using typical parameter values. This *damping* of the oscillatory output with time is due to the dissipative characteristics of the resistive elements. By placing a tunnel diode in series with the tank circuit as shown in Fig. 20.19c, the negative resistance of the tunnel diode will offset the resistive characteristics of the tank circuit, resulting in the *undamped* response appearing in the same figure. The

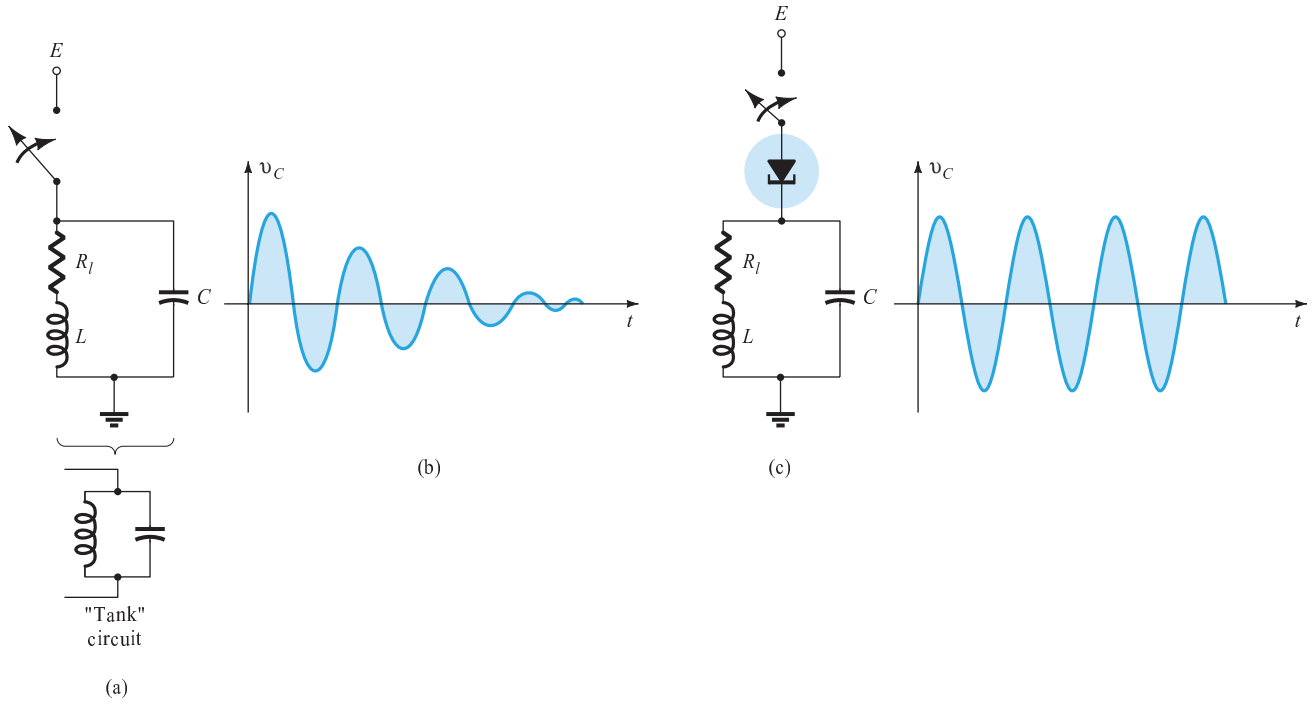


Figure 20.19 Sinusoidal oscillator.

design must continue to result in a load line that will intersect the characteristics only in the negative-resistance region. In another light, the sinusoidal generator of Fig. 20.19 is simply an extension of the pulse oscillator of Fig. 20.18, with the addition of the capacitor to permit an exchange of energy between the inductor and the capacitor during the various phases of the cycle depicted in Fig. 20.18b.

20.6 PHOTODIODES

The interest in light-sensitive devices has been increasing at an almost exponential rate in recent years. The resulting field of *optoelectronics* will be receiving a great deal of research interest as efforts are made to improve efficiency levels. Through the advertising media, the layperson has become quite aware that light sources offer a unique source of energy. This energy, transmitted as discrete packages called *photons,* has a level directly related to the frequency of the traveling light wave as determined by the following equation:

$$W = \hbar f \quad \text{joules} \tag{20.5}$$

where $\hbar$ is called Planck's constant and is equal to 6.624×10^{-34} joule-second. It clearly states that since $\hbar$ is a constant, the energy associated with incident light waves is directly related to the frequency of the traveling wave.

The frequency is, in turn, directly related to the wavelength (distance between successive peaks) of the traveling wave by the following equation:

$$\lambda = \frac{v}{f} \tag{20.6}$$

where λ = wavelength, meters
v = velocity of light, 3×10^8 m/s
f = frequency of the traveling wave, hertz

The wavelength is usually measured in angstrom units (Å) or micrometers (μm), where

$$1 \text{ Å} = 10^{-10} \text{ m} \qquad \text{and} \qquad 1 \ \mu\text{m} = 10^{-6} \text{ m}$$

The wavelength is important because it will determine the material to be used in the optoelectronic device. The relative spectral response for Ge, Si, and selenium is provided in Fig. 20.20. The visible-light spectrum has also been included with an indication of the wavelength associated with the various colors.

The number of free electrons generated in each material is proportional to the *intensity* of the incident light. Light intensity is a measure of the amount of *luminous flux* falling in a particular surface area. Luminous flux is normally measured in *lumens* (lm) or watts. The two units are related by

$$1 \text{ lm} = 1.496 \times 10^{-10} \text{ W}$$

The light intensity is normally measured in lm/ft^2, footcandles (fc), or W/m^2, where

$$1 \text{ lm/ft}^2 = 1 \text{ fc} = 1.609 \times 10^{-9} \text{ W/m}^2$$

The photodiode is a semiconductor p-n junction device whose region of operation is limited to the reverse-bias region. The basic biasing arrangement, construction, and symbol for the device appear in Fig. 20.21.

Recall from Chapter 1 that the reverse saturation current is normally limited to a few microamperes. It is due solely to the thermally generated minority carriers in the

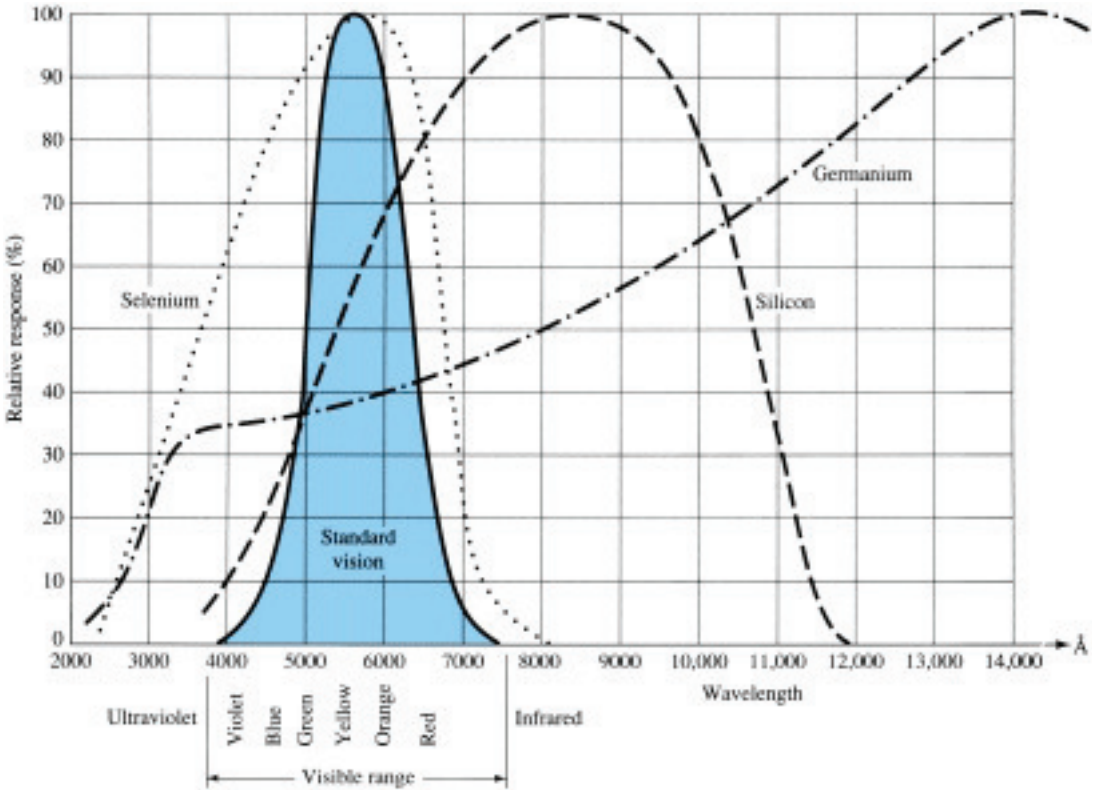


Figure 20.20 Relative spectral response for Si, Ge, and selenium as compared to the human eye.

n- and *p*-type materials. The application of light to the junction will result in a transfer of energy from the incident traveling light waves (in the form of photons) to the atomic structure, resulting in an increased number of minority carriers and an increased level of reverse current. This is clearly shown in Fig. 20.22 for different intensity levels. The *dark* current is that current that will exist with no applied illumination. Note that the current will only return to zero with a positive applied bias equal to V_T. In addition, Fig. 20.21 demonstrates the use of a lens to concentrate the light on the junction region. Commercially available photodiodes appear in Fig. 20.23.

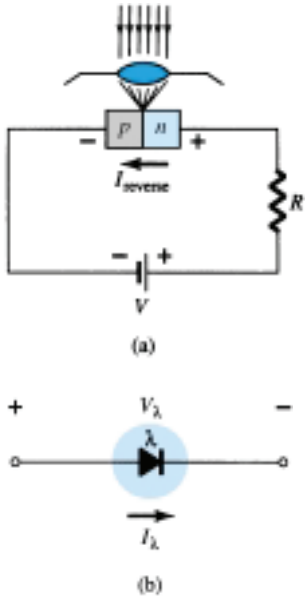


Figure 20.21 Photodiode: (a) basic biasing arrangement and construction; (b) symbol.

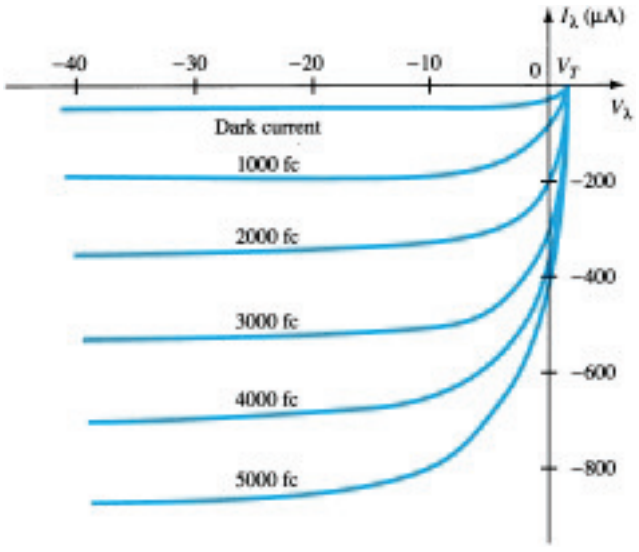


Figure 20.22 Photodiode characteristics.

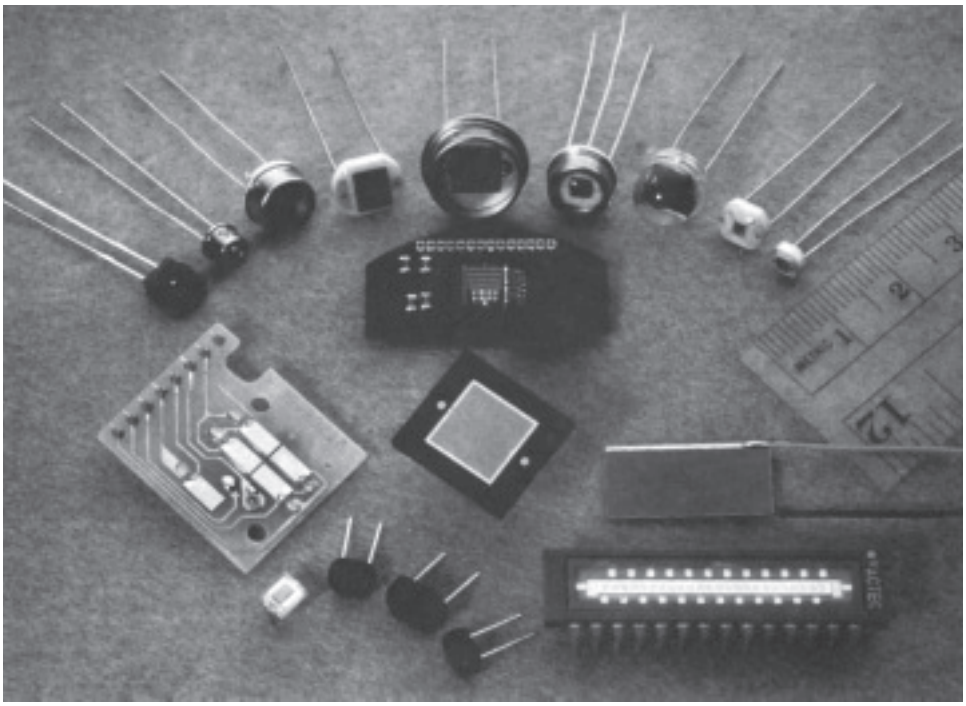


Figure 20.23 Photodiodes (Courtesy EG&G VACTEC, Inc.)

The almost equal spacing between the curves for the same increment in luminous flux reveals that the reverse current and luminous flux are almost linearly related. In other words, an increase in light intensity will result in a similar increase in reverse current. A plot of the two to show this linear relationship appears in Fig. 20.24 for a fixed voltage V_λ of 20 V. On the relative basis, we can assume that the reverse current is essentially zero in the absence of incident light. Since the rise and fall times (change-of-state parameters) are very small for this device (in the nanosecond range), the device can be used for high-speed counting or switching applications. Returning to Fig. 20.20, we note that Ge encompasses a wider spectrum of wavelengths than Si. This would make it suitable for incident light in the infrared region as provided by lasers and IR (infrared) light sources, to be described shortly. Of course, Ge has a higher dark current than silicon, but it also has a higher level of reverse current. The level of current generated by the incident light on a photodiode is not such that it could be used as a direct control, but it can be amplified for this purpose.

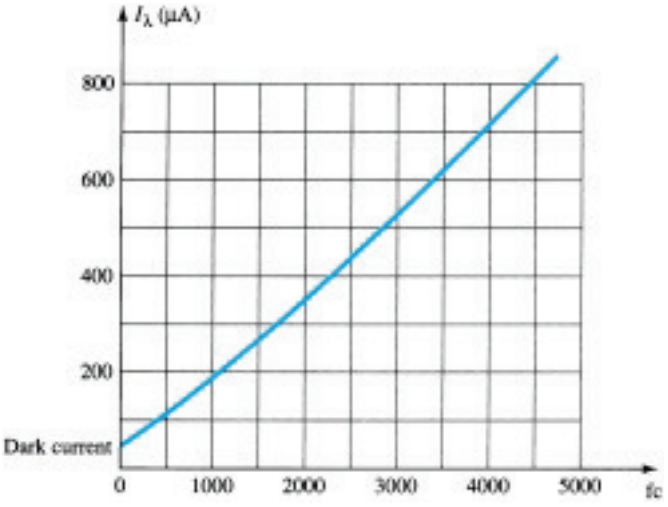


Figure 20.24 $I_\lambda(\mu A)$ versus fc (at $V_\lambda = 20$ V) for the photodiode of Fig. 20.22.

In Fig. 20.25, the photodiode is employed in an alarm system. The reverse current I_λ will continue to flow as long as the light beam is not broken. If interrupted, I_λ drops to the dark current level and sounds the alarm. In Fig. 20.26, a photodiode is used to count items on a conveyor belt. As each item passes the light beam is broken, I_λ drops to the dark current level and the counter is increased by one.

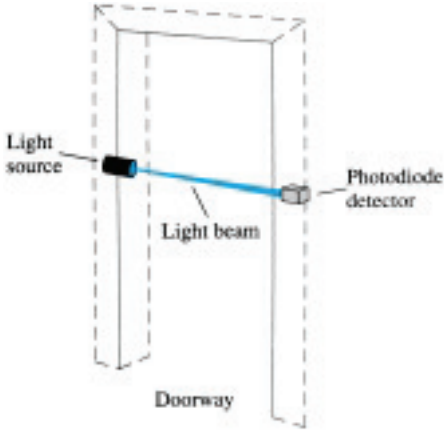


Figure 20.25 Using a photodiode in an alarm system.

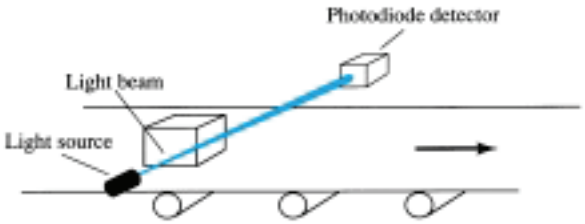
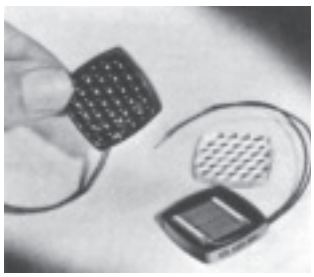


Figure 20.26 Using a photodiode in a counter operation.

20.7 PHOTOCONDUCTIVE CELLS

The photoconductive cell is a two-terminal semiconductor device whose terminal resistance will vary (linearly) with the intensity of the incident light. For obvious reasons, it is frequently called a *photoresistive device.* A typical photoconductive cell and the most widely used graphical symbol for the device appear in Fig. 20.27.



(a)

(b)

Figure 20.27 Photoconductive cell: (a) appearance; (b) symbol. [(a) Courtesy International Rectifier Corporation.]

The photoconductive materials most frequently used include cadmium sulfide (CdS) and cadmium selenide (CdSe). The peak spectral response of CdS occurs at approximately 5100 Å and for CdSe at 6150 Å (note Fig. 20.20). The response time of CdS units is about 100 ms, and 10 ms for CdSe cells. The photoconductive cell does not have a junction like the photodiode. A thin layer of the material connected between terminals is simply exposed to the incident light energy.

As the illumination on the device increases in intensity, the energy state of a larger number of electrons in the structure will also increase because of the increased availability of the photon packages of energy. The result is an increasing number of relatively "free" electrons in the structure and a decrease in the terminal resistance. The sensitivity curve for a typical photoconductive device appears in Fig. 20.28. Note the linearity (when plotted using a log-log scale) of the resulting curve and the large change in resistance (100 kΩ $\longrightarrow$ 100 Ω) for the indicated change in illumination.

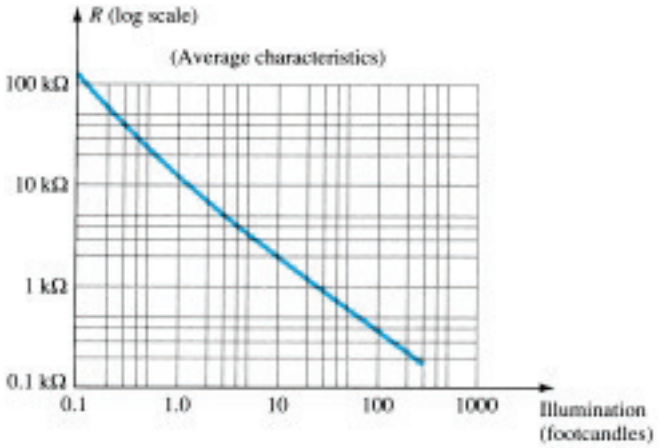


Figure 20.28 Photoconductive cell-terminal characteristics (GE type B425).

One rather simple, but interesting, application of the device appears in Fig. 20.29. The purpose of the system is to maintain V_o at a fixed level even though V_i may fluctuate from its rated value. As indicated in the figure, the photoconductive cell, bulb, and resistor all form part of this voltage-regulator system. If V_i should drop in magnitude for any number of reasons, the brightness of the bulb would also decrease. The decrease in illumination would result in an increase in the resistance (R_λ) of the photoconductive cell to maintain V_o at its rate level as determined by the voltage-divider rule, that is,

$$V_o = \frac{R_\lambda V_i}{R_\lambda + R_1} \tag{20.7}$$

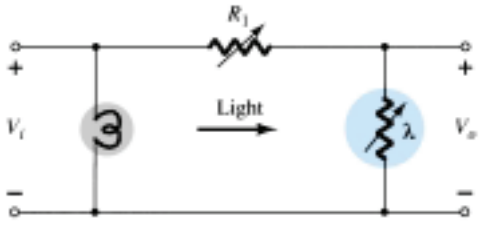
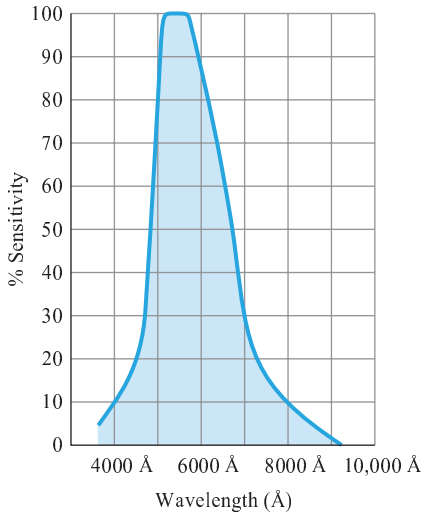


Figure 20.29 Voltage regulator employing a photoconductive cell.

In an effort to demonstrate the wealth of material available on each device from manufacturers, consider the CdS (cadmium sulfide) photoconductive cell described in Fig. 20.30. Note again the concern with temperature and response time.



Variation of Conductance With Temperature and Light

Footcandles	*0.01*	*0.1*	*1.0*	*10*	*100*
Temperature			*% Conductance*		
−25°C	103	104	104	102	106
0	98	102	102	100	103
25°C	100	100	100	100	100
50°C	98	102	103	104	99
75°C	90	106	108	109	104

Response Time Versus Light

Footcandles	*0.01*	*0.1*	*1.0*	*10*	*100*
Rise (seconds)	0.5	0.095	0.022	0.005	0.002
Decay (seconds)	0.125	0.021	0.005	0.002	0.001

Figure 20.30 Characteristics of a Clairex CdS photoconductive cell. (Courtesy Clairex Electronics.)

20.8 IR EMITTERS

Infrared-emitting diodes are solid-state gallium arsenide devices that emit a beam of radiant flux when forward-biased. The basic construction of the device is shown in Fig. 20.31. When the junction is forward-biased, electrons from the *n*-region will recombine with excess holes of the *p*-material in a specially designed recombination region sandwiched between the *p*- and *n*-type materials. During this recombination process, energy is radiated away from the device in the form of photons. The generated photons will either be reabsorbed in the structure or leave the surface of the device as radiant energy, as shown in Fig. 20.31.

The radiant flux in mW versus the dc forward current for a typical device appears in Fig. 20.32. Note the almost linear relationship between the two. An interesting pattern for such devices is provided in Fig. 20.33. Note the very narrow pattern for de-

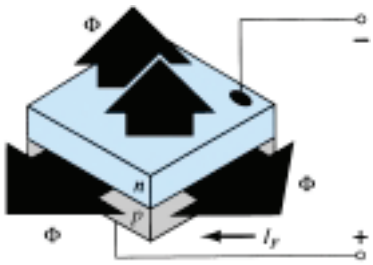


Figure 20.31 General structure of a semiconductor IR-emitting diode. (Courtesy RCA Solid State Division.)

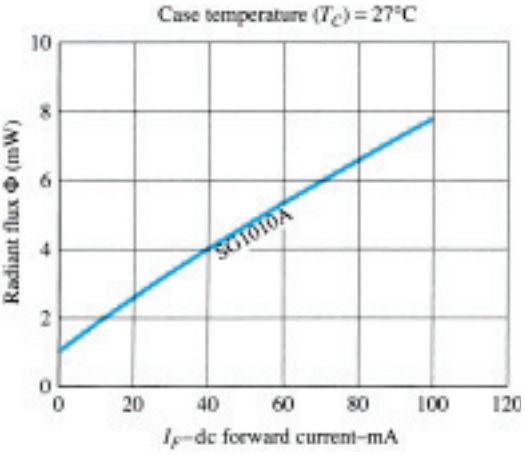


Figure 20.32 Typical radiant flux versus dc forward current for an IR-emitting diode. (Courtesy RCA Solid State Division.)

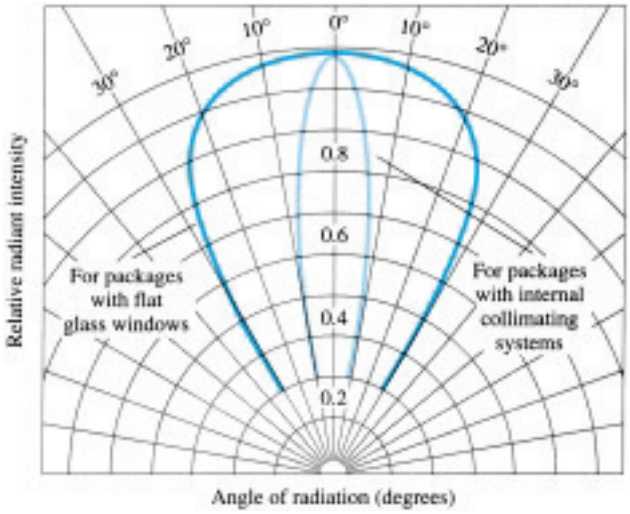
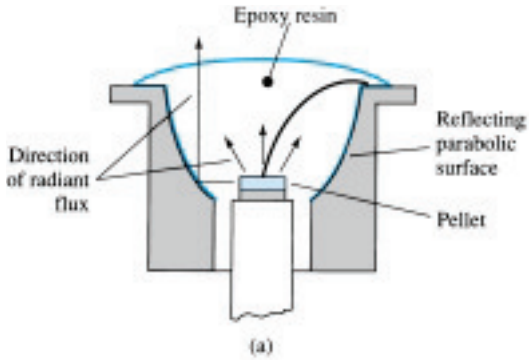


Figure 20.33 Typical radiant intensity patterns of RCA IR-emitting diodes. (Courtesy RCA Solid State Division.)

vices with an internal collimating system. One such device appears in Fig. 20.34, with its internal construction and graphical symbol. A few areas of application for such devices include card and paper-tape readers, shaft encoders, data-transmission systems, and intrusion alarms.



Approx. 2X actual size
(b)

Figure 20.34 RCA IR-emitting diode: (a) construction; (b) photo; (c) symbol. (Courtesy RCA Solid State Division.)

20.9 LIQUID-CRYSTAL DISPLAYS

The liquid-crystal display (LCD) has the distinct advantage of having a lower power requirement than the LED. It is typically in the order of microwatts for the display, as compared to the same order of milliwatts for LEDs. It does, however, require an external or internal light source and is limited to a temperature range of about 0° to 60°C. Lifetime is an area of concern because LCDs can chemically degrade. The types receiving the major interest today are the field-effect and dynamic-scattering units. Each will be covered in some detail in this section.

A liquid crystal is a material (normally organic for LCDs) that will flow like a liquid but whose molecular structure has some properties normally associated with solids. For the light-scattering units, the greatest interest is in the *nematic liquid crystal,* having the crystal structure shown in Fig. 20.35. The individual molecules have a rodlike appearance as shown in the figure. The indium oxide conducting surface is transparent, and under the condition shown in the figure, the incident light will simply pass through and the liquid-crystal structure will appear clear. If a voltage (for commercial units the threshold level is usually between 6 and 20 V) is applied across the conducting surfaces, as shown in Fig. 20.36, the molecular arrangement is disturbed, with the result that regions will be established with different indices of refraction. The incident light is therefore reflected in different directions at the interface between regions of different indices of refraction (referred to as *dynamic scattering*—first studied by RCA in 1968) with the result that the scattered light has a frosted-glass appearance. Note in Fig. 20.36, however, that the frosted look occurs

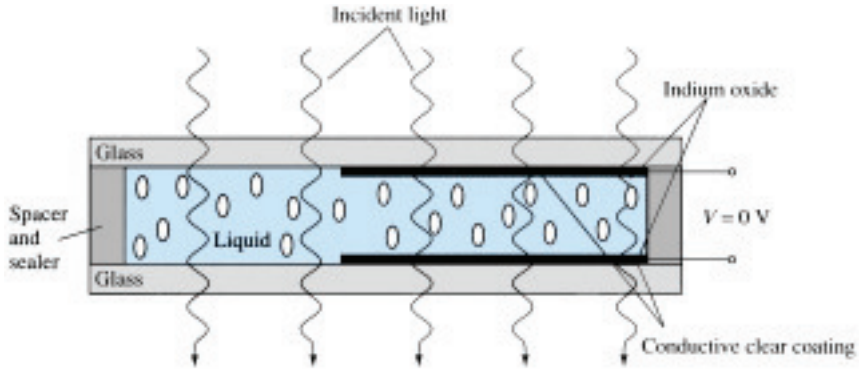


Figure 20.35 Nematic liquid crystal with no applied bias.

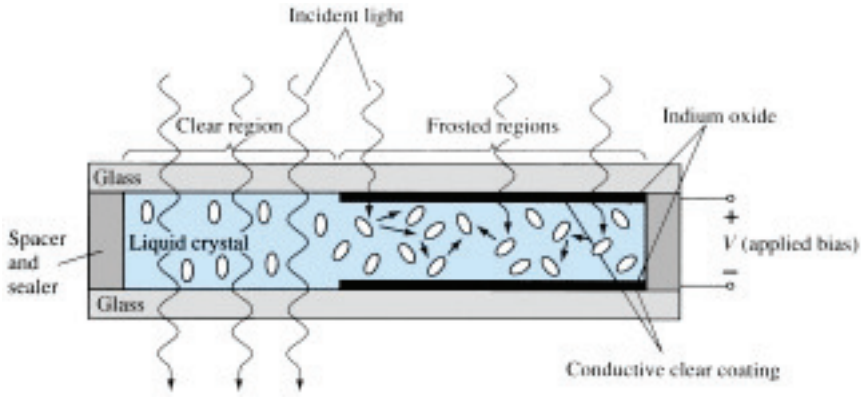


Figure 20.36 Nematic liquid crystal with applied bias.

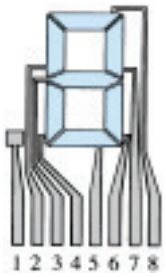


Figure 20.37 LCD eight-segment digit display.

only where the conducting surfaces are opposite each other and the remaining areas remain translucent.

A digit on an LCD display may have the segment appearance shown in Fig. 20.37. The black area is actually a clear conducting surface connected to the terminals below for external control. Two similar masks are placed on opposite sides of a sealed thick layer of liquid-crystal material. If the number 2 were required, the terminals 8, 7, 3, 4, and 5 would be energized, and only those regions would be frosted while the other areas would remain clear.

As indicated earlier, the LCD does not generate its own light but depends on an external or internal source. Under dark conditions, it would be necessary for the unit to have its own internal light source either behind or to the side of the LCD. During the day, or in lighted areas, a reflector can be put behind the LCD to reflect the light back through the display for maximum intensity. For optimum operation, current watch manufacturers are using a combination of the transmissive (own light source) and reflective modes called *transflective*.

The *field-effect* or *twisted nematic* LCD has the same segment appearance and thin layer of encapsulated liquid crystal, but its mode of operation is very different. Similar to the dynamic-scattering LCD, the field-effect LCD can be operated in the reflective or transmissive mode with an internal source. The transmissive display appears in Fig. 20.38. The internal light source is on the right, and the viewer is on the left. This figure is most noticeably different from Fig. 20.35 in that there is an addition of a *light polarizer*. Only the vertical component of the entering light on the right can pass through the vertical-light polarizer on the right. In the field-effect LCD, either the clear conducting surface to the right is chemically etched or an organic film is applied to orient the molecules in the liquid crystal in the vertical plane, parallel to the cell wall. Note the rods to the far right in the liquid crystal. The opposite conducting surface is also treated to ensure that the molecules are 90° out of phase in the direction shown (horizontal) but still parallel to the cell wall. In between the two walls of the liquid crystal there is a general drift from one polarization to the other, as shown in the figure. The left-hand light polarizer is also such that it permits the passage of only the vertically polarized incident light. If there is no applied voltage to the conducting surfaces, the vertically polarized light enters the liquid-crystal region and follows the 90° bending of the molecular structure. Its horizontal polarization at the left-hand vertical light polarizer does not allow it to pass through, and the viewer sees a uniformly dark pattern across the entire display. When a threshold voltage is applied (for commercial units from 2 to 8 V), the rodlike molecules align themselves with the field (perpendicular to the wall) and the light passes directly through without the 90° shift. The vertically incident light can then press directly through the second vertically polarized screen, and a light area is seen by the viewer. Through proper excita-

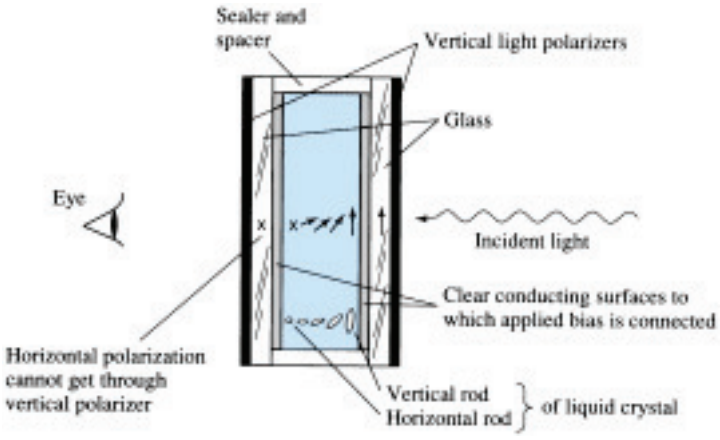


Figure 20.38 Transmissive field-effect LCD with no applied bias.

tion of the segments of each digit, the pattern will appear as shown in Fig. 20.39. The reflective-type field-effect LCD is shown in Fig. 20.40. In this case, the horizontally polarized light at the far left encounters a horizontally polarized filter and passes through to the reflector, where it is reflected back into the liquid crystal, bent back to the other vertical polarization, and returned to the observer. If there is no applied voltage, there is a uniformly lit display. The application of a voltage results in a vertically incident light encountering a horizontally polarized filter at the left, which it will not be able to pass through and will be reflected. A dark area results on the crystal, and the pattern as shown in Fig. 20.41 appears.

Figure 20.39 Reflective-type LCD. (Courtesy RCA Solid State Division.)

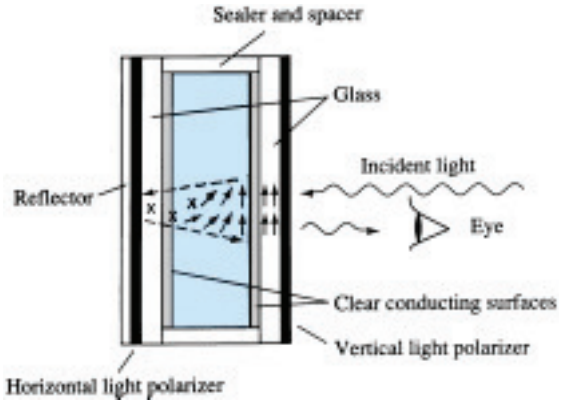


Figure 20.40 Reflective field-effect LCD with no applied bias.

Figure 20.41 Transmissive-type LCD. (Courtesy RCA Solid State Division.)

Field-effect LCDs are normally used when a source of energy is a prime factor (e.g., in watches, portable instrumentation, etc.) since they absorb considerably less power than the light-scattering types—the microwatt range compared to the low-milliwatt range. The cost is typically higher for field-effect units, and their height is limited to about 2 in. while light-scattering units are available up to 8 in. in height.

A further consideration in displays is turn-on and turn-off time. LCDs are characteristically much slower then LEDs. LCDs typically have response times in the range 100 to 300 ms, while LEDs are available with response times below 100 ns. However, there are numerous applications, such as in a watch, where the difference between 100 ns and 100 ms ($\frac{1}{10}$ of a second) is of little consequence. For such applications, the lower power demand of LCDs is a very attractive characteristic. The lifetime of LCD units is steadily increasing beyond the 10,000+ hours limit. Since the color generated by LCD units is dependent on the source of illumination, there is a greater range of color choice.

20.10 SOLAR CELLS

In recent years, there has been increasing interest in the solar cell as an alternative source of energy. When we consider that the power density received from the sun at sea level is about 100 mW/cm^2 (1 kW/m^2), it is certainly an energy source that requires further research and development to maximize the conversion efficiency from solar to electrical energy.

The basic construction of a silicon *p-n* junction solar cell appears in Fig. 20.42. As shown in the top view, every effort is made to ensure that the surface area perpendicular to the sun is a maximum. Also, note that the metallic conductor connected to the *p*-type material and the thickness of the *p*-type material are such that they ensure that a maximum number of photons of light energy will reach the junction. A photon of light energy in this region may collide with a valence electron and impart to it sufficient energy to leave the parent atom. The result is a generation of free electrons and holes. This phenomenon will occur on each side of the junction. In the

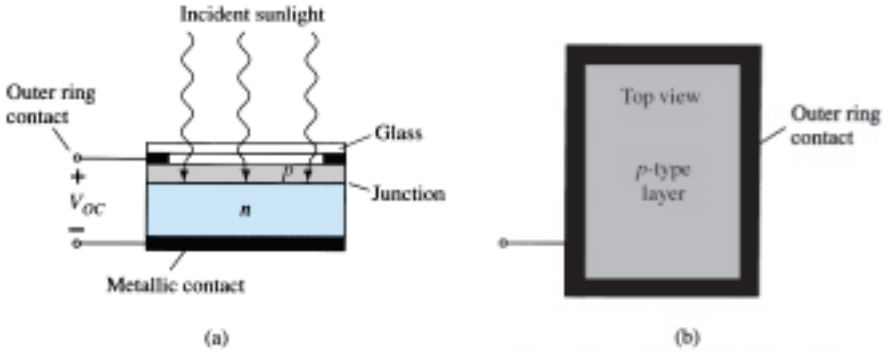


Figure 20.42 Solar cell: (a) cross section; (b) top view.

p-type material, the newly generated electrons are minority carriers and will move rather freely across the junction as explained for the basic *p-n* junction with no applied bias. A similar discussion is true for the holes generated in the *n*-type material. The result is an increase in the minority-carrier flow, which is opposite in direction to the conventional forward current of a *p-n* junction. This increase in reverse current is shown in Fig. 20.43. Since $V = 0$ anywhere on the vertical axis and represents a short-circuit condition, the current at this intersection is called the *short-circuit current* and is represented by the notation I_{SC}. Under open-circuit conditions ($i_d = 0$), the *photovoltaic* voltage V_{OC} will result. This is a logarithmic function of the illumination, as shown in Fig. 20.44. V_{OC} is the terminal voltage of a battery under no-load (open-circuit) conditions. Note, however, in the same figure that the short-circuit current is a linear function of the illumination. That is, it will double for the same increase in illumination (f_{C_1} and $2f_{C_1}$ in Fig. 20.44) while the change in V_{OC} is less for this region. The major increase in V_{OC} occurs for lower-level increases in illumination. Eventually, a further increase in illumination will have very little effect on V_{OC}, although I_{SC} will increase, causing the power capabilities to increase.

Selenium and silicon are the most widely used materials for solar cells, although gallium arsenide, indium arsenide, and cadmium sulfide, among others, are also used.

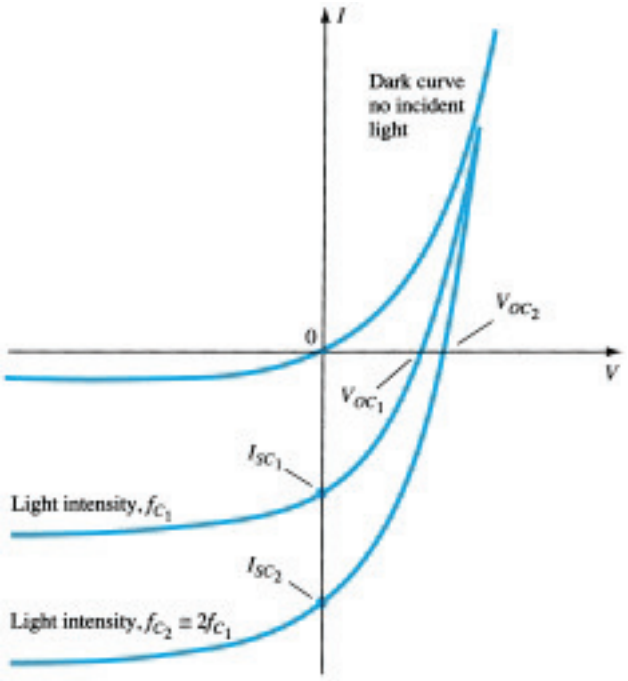


Figure 20.43 Short-circuit current and open-circuit voltage versus light intensity for a solar cell.

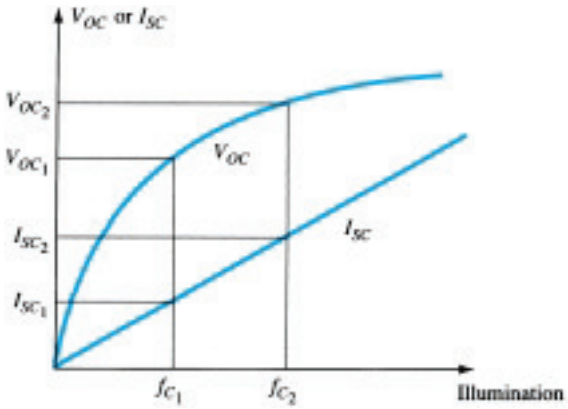


Figure 20.44 V_{OC} and I_{SC} versus illumination for a solar cell.

The wavelength of the incident light will affect the response of the *p-n* junction to the incident photons. Note in Fig. 20.45 how closely the selenium cell response curve matches that of the eye. This fact has widespread application in photographic equipment such as exposure meters and automatic exposure diaphragms. Silicon also overlaps the visible spectrum but has its peak at the 0.8 μm (8000 Å) wavelength, which is in the infrared region. In general, silicon has a higher conversion efficiency, greater stability, and is less subject to fatigue. Both materials have excellent temperature characteristics. That is, they can withstand extreme high or low temperatures without a significant drop-off in efficiency. Typical solar cells, with their electrical characteristics, appear in Fig. 20.46.

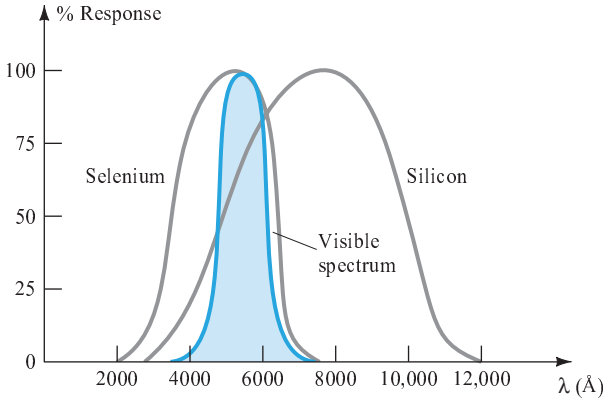


Figure 20.45 Spectral response of Se, Si, and the naked eye.

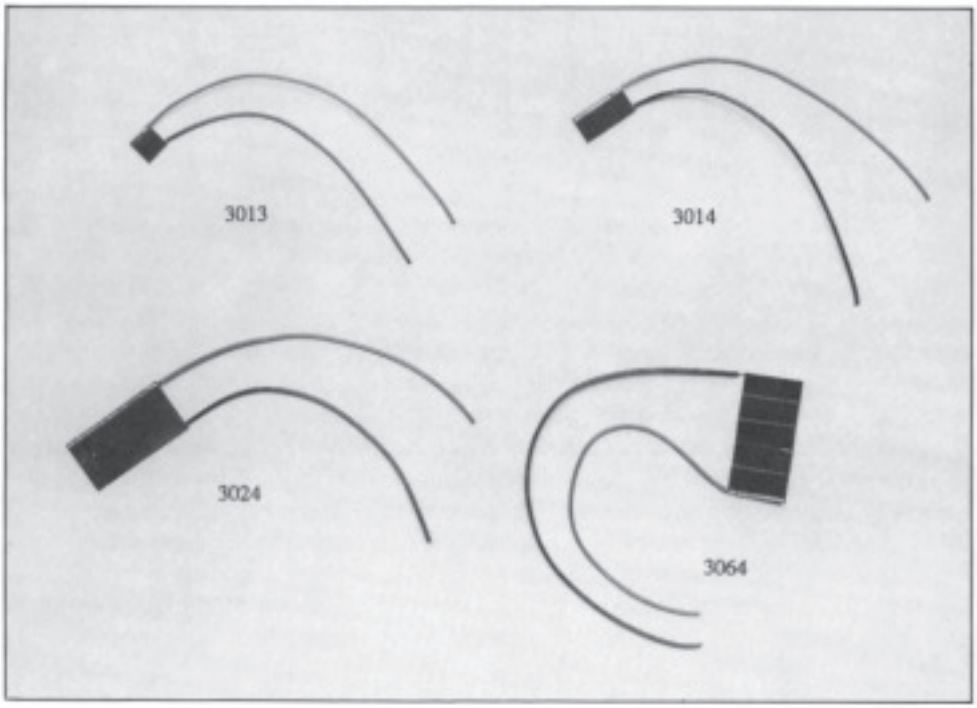


Figure 20.46 Typical solar cells and their electrical characteristics. (Courtesy EG&G VACTEC, Inc.)

Electrical Characteristics

Part No.	Active Area	Test Voltage	Minimum current Test voltage
3013	0.032 in² (0.21 cm²)	0.4 V	4.2 mA
3014	0.065 in² (0.42 cm²)	0.4 V	8.4 mA
3024	0.29 in² (1.87 cm²)	0.4 V	38 mA
3064	0.325 in² (2.1 cm²)	2 V	8.4 mA

A very recent innovation in the use of solar cells appears in Fig. 20.47. The series arrangement of solar cells permits a voltage beyond that of a single element. The performance of a typical four-cell array appears in the same figure. At a current of approximately 2.6 mA, the output voltage is about 1.6 V, resulting in an output power of 4.16 mW. The Schottky barrier diode is included to prevent battery current drain through the power converter. That is, the resistance of the Schottky diode is so high to charge flowing down through (+ to −) the power converter that it will appear as an open circuit to the rechargeable battery and not draw current from it.

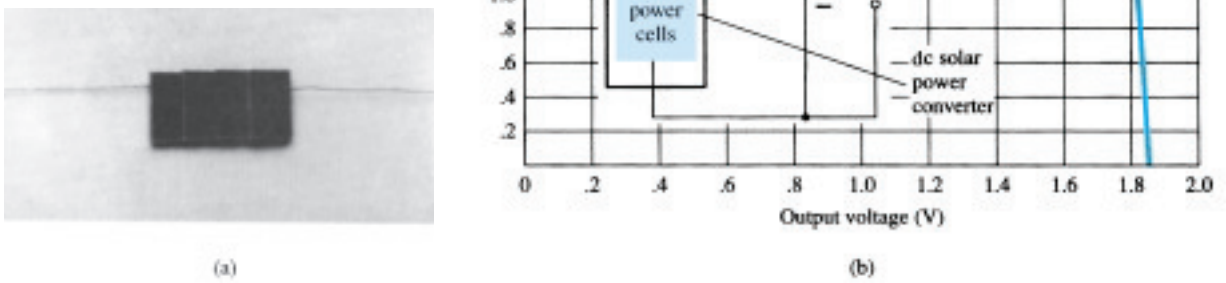


Figure 20.47 International Rectifier four-cell array: (a) appearance; (b) characteristics. (Courtesy International Rectifier Corporation.)

It might be of interest to note that the Lockheed Missiles and Space Company is working on a grant from the National Aeronautics and Space Administration to develop a massive solar-array wing for the space shuttle. The wing will measure 13.5 ft by 105 ft when extended and will contain 41 panels, each carrying 3060 silicon solar cells. The wing can generate a total of 12.5 kW of electrical power.

The efficiency of operation of a solar cell is determined by the electrical power output divided by the power provided by the light source. That is,

$$\eta = \frac{P_{o(\text{electrical})}}{P_{i(\text{light energy})}} \times 100\% = \frac{P_{\max(\text{device})}}{(\text{area in cm}^2)(100\ \text{mW/cm}^2)} \times 100\% \qquad (20.8)$$

Typical levels of efficiency range from 10% to 40%—a level that should improve measurably if the present interest continues. A typical set of output characteristics for silicon solar cells of 10% efficiency with an active area of 1 cm^2 appears in Fig. 20.48. Note the optimum power locus and the almost linear increase in output current with luminous flux for a fixed voltage.

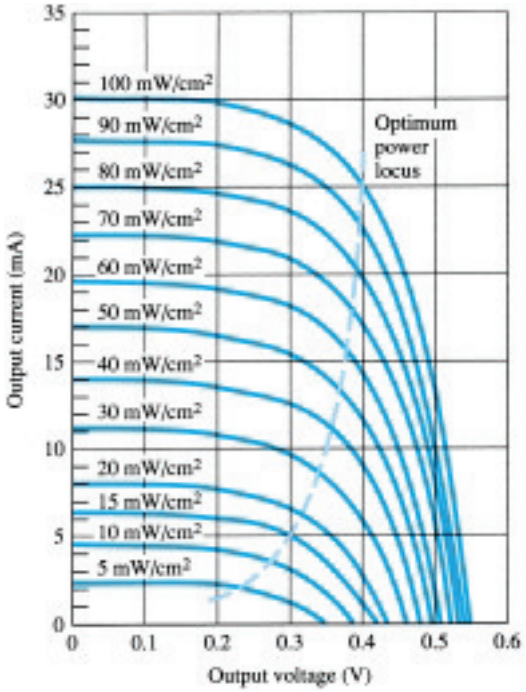


Figure 20.48 Typical output characteristics for silicon solar cells of 10% efficiency having an active area of 1 cm^2. Cell temperature is 30°C.

20.11 THERMISTORS

The thermistor is, as the name implies, a temperature-sensitive resistor; that is, its terminal resistance is related to its body temperature. It is not a junction device and is constructed of Ge, Si, or a mixture of oxides of cobalt, nickel, strontium, or manganese. The compound employed will determine whether the device has a positive or negative temperature coefficient.

The characteristics of a representative thermistor with a negative temperature coefficient are provided in Fig. 20.49, with the commonly used symbol for the device. Note in particular that at room temperature (20°C) the resistance of the thermistor is approximately 5000 Ω, while at 100°C (212°F) the resistance has decreased to 100 Ω. A temperature span of 80°C has therefore resulted in a 50:1 change in resis-

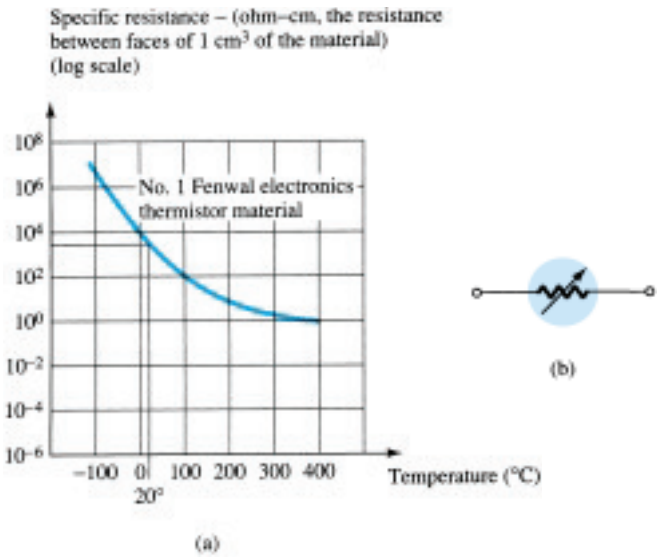


Figure 20.49 Thermistor: (a) typical set of characteristics; (b) symbol.

tance. It is typically 3% to 5% per degree change in temperature. There are fundamentally two ways to change the temperature of the device: internally and externally. A simple change in current through the device will result in an internal change in temperature. A small applied voltage will result in a current too small to raise the body temperature above that of the surroundings. In this region, as shown in Fig. 20.50, the thermistor will act like a resistor and have a positive temperature coefficient. However, as the current increases, the temperature will rise to the point where the negative temperature coefficient will appear as shown in Fig. 20.50. The fact that the rate of internal flow can have such an effect on the resistance of the device introduces a wide vista of applications in control, measuring techniques, and so on. An external change would require changing the temperature of the surrounding medium or immersing the device in a hot or cold solution.

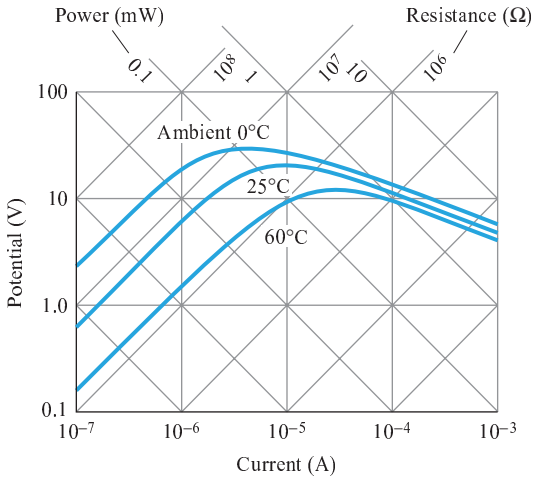


Figure 20.50 Steady-state voltage–current characteristics of Fenwal Electronics BK65VI Thermistor. (Courtesy Fenwal Electronics, Incorporated.)

A photograph of a number of commercially available thermistors is provided in Fig. 20.51. A simple temperature-indicating circuit appears in Fig. 20.52. Any increase in the temperature of the surrounding medium will result in a decrease in the resistance of the thermistor and an increase in the current I_T. An increase in I_T will

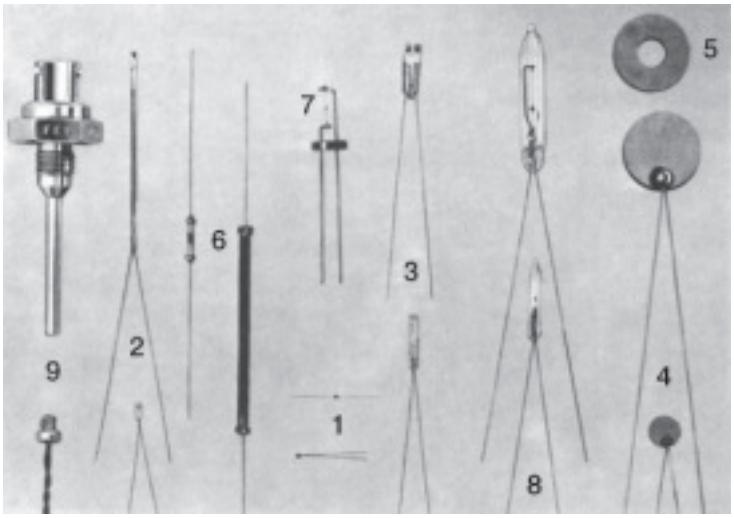


Figure 20.51 Various types of thermistors: (1) beads; (2) glass probes; (3) iso-curve interchangeable probes and beads; (4) disks; (5) washers; (6) rods; (7) specially mounted beads; (8) vacuum and gas-filled probes; (9) special probe assemblies. (Courtesy Fenwal Electronics, Incorporated.)

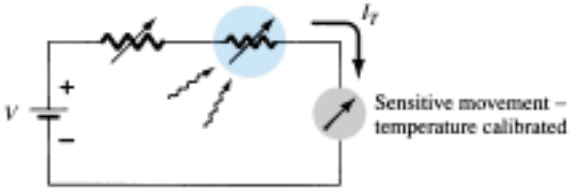


Figure 20.52 Temperature-indicating circuit.

produce an increased movement deflection, which when properly calibrated will accurately indicate the higher temperature. The variable resistance was added for calibration purposes.

PROBLEMS

§ 20.2 Schottky Barrier (Hot-Carrier) Diodes

1. (a) Describe in your own words how the construction of the hot-carrier diode is significantly different from the conventional semiconductor diode.
(b) In addition, describe its mode of operation.

2. (a) Consult Fig. 20.2. How would you compare the dynamic resistances of the diodes in the forward-bias regions?
(b) How do the levels of I_s and V_Z compare?

3. Referring to Fig. 20.5, how does the maximum surge current I_{FSM} relate to the average rectified forward current? Is it typically greater than 20:1? Why is it possible to have such high levels of current? What noticeable difference is there in construction as the current rating increases?

4. Referring to Fig. 20.6a, at what temperature is the forward voltage drop 300 mV at a current of 1 mA? Which current levels have the highest levels of temperature coefficients? Assume a linear progression between temperature levels.

* **5.** For the curve of Fig. 20.6b denoted 2900/2303, determine the percent change in I_R for a change in reverse voltage from 5 to 10 V. At what reverse voltage would you expect to reach a reverse current of 1 μA? Note the log scale for I_R .

* **6.** Determine the percent change in capacitance between 0 and 2 V for the 2900/2303 curve of Fig. 20.6c. How does this compare to the change between 8 and 10 V?

§ 20.3 Varactor (Varicap) Diodes

7. (a) Determine the transition capacitance of a diffused junction varicap diode at a reverse potential of 4.2 V if $C(0) = 80$ pF and $V_T = 0.7$ V.
(b) From the information of part (a), determine the constant K in Eq. (20.2).

8. (a) For a varicap diode having the characteristics of Fig. 20.7, determine the difference in capacitance between reverse-bias potentials of -3 and -12 V.
(b) Determine the incremental rate of change ($\Delta C/\Delta V_r$) at $V = -8$ V. How does this value compare with the incremental change determined at -2 V?

* **9.** (a) The resonant frequency of a series RLC network is determined by $f_0 = 1/(2\pi\sqrt{LC})$. Using the value of f_0 and L_S provided in Fig. 20.9, determine the value of C.
(b) How does the value calculated in part (a) compare with that determined by the curve in Fig. 20.10 at $V_R = 25$ V?

10. Referring to Fig. 20.10, determine the ratio of capacitance at $V_R = 3$ V to $V_R = 25$ V and compare to the value of C_3/C_{25} given in Fig. 20.9 (maximum = 6.5).

11. Determine T_1 for a varactor diode if $C_0 = 22$ pF, $TC_C = 0.02\%/°C$, and $\Delta C = 0.11$ pF due to an increase in temperature above $T_0 = 25°C$.

12. What region of V_R would appear to have the greatest change in capacitance per change in reverse voltage for the BB139 varactor diode of Figs. 20.9 and 20.10? Be aware that the scales are nonlinear.

* **13.** If $Q = X_L/R = 2\pi fL/R$, determine the figure of merit (Q) at 600 MHz using the fact that $R_S = 0.35\ \Omega$ and $L_S = 2.5$ nH. Comment on the change in Q with frequency and the support or nonsupport of the curve in Fig. 20.10.

§ 20.4 Power Diodes

14. Consult a manufacturer's data book and compare the general characteristics of a high-power device (>10 A) to a low-power unit (<100 mA). Is there a significant change in the data and characteristics provided? Why?

§ 20.5 Tunnel Diodes

15. What are the essential differences between a semiconductor junction diode and a tunnel diode?

***16.** Note in the equivalent circuit of Fig. 20.14 that the capacitor appears in parallel with the negative resistance. Determine the reactance of the capacitor at 1 MHz and 100 MHz if $C = 5$ pF, and determine the total impedance of the parallel combination (with $R = -152\ \Omega$) at each frequency. Is the magnitude of the inductive reactance anything to be overly concerned about at either of these frequencies if $L_S = 6$ nH?

***17.** Why do you believe the maximum reverse current rating for the tunnel diode can be greater than the forward current rating? (*Hint:* Note the characteristics and consider the power rating.)

18. Determine the negative resistance for the tunnel diode of Fig. 20.13 between $V_T = 0.1$ V and $V_T = 0.3$ V.

19. Determine the stable operating points for the network of Fig. 20.17 if $E = 2$ V, $R = 0.39$ kΩ, and the tunnel diode of Fig. 20.13 is employed. Use typical values from Table 20.1.

***20.** For $E = 0.5$ V and $R = 51\ \Omega$, sketch v_T for the network of Figure 20.18 and the tunnel diode of Fig. 20.13.

21. Determine the frequency of oscillation for the network of Fig. 20.19 if $L = 5$ mH, $R_l = 10\ \Omega$, and $C = 1\ \mu$F.

§ 20.6 Photodiodes

22. Determine the energy associated with the photons of green light if the wavelength is 5000 Å. Give your answer in joules and electron volts.

23. (a) Referring to Fig. 20.20, what would appear to be the frequencies associated with the upper and lower limits of the visible spectrum?
(b) What is the wavelength in microns associated with the peak relative response of silicon?
(c) If we define the bandwidth of the spectral response of each material to occur at 70% of its peak level, what is the bandwidth of silicon?

24. Referring to Fig. 20.22, determine I_λ if $V_\lambda = 30$ V and the light intensity is 4×10^{-9} W/m^2.

25. (a) Which material of Fig. 20.20 would appear to provide the best response to yellow, red, green, and infrared (less than 11,000 Å) light sources?
(b) At a frequency of 0.5×10^{15} Hz, which color has the maximum spectral response?

***26.** Determine the voltage drop across the resistor of Fig. 20.21 if the incident flux is 3000 fc, $V_\lambda = 25$ V, and $R = 100$ kΩ. Use the characteristics of Fig. 20.22.

§ 20.7 Photoconductive Cells

***27.** What is the approximate rate of change of resistance with illumination for a photoconductive cell with the characteristics of Fig. 20.28 for the ranges (a) 0.1 → 1 kΩ, (b) 1 → 10 kΩ, and (c) 10 → kΩ? (Note that this is a log scale.) Which region has the greatest rate of change in resistance with illumination?

28. What is the "dark current" of a photodiode?

29. If the illumination on the photoconductive diode in Fig. 20.29 is 10 fc, determine the magnitude of V_i to establish 6 V across the cell if R_1 is equal to 5 kΩ. Use the characteristics of Fig. 20.28.

***30.** Using the data provided in Fig. 20.30, sketch a curve of percent conductance versus temperature for 0.01, 1.0, and 100 fc. Are there any noticeable effects?

***31.** (a) Sketch a curve of rise time versus illumination using the data from Fig. 20.30.
(b) Repeat part (a) for the decay time.
(c) Discuss any noticeable effects of illumination in parts (a) and (b).

32. Which colors is the CdS unit of Fig. 20.30 most sensitive to?

§ 20.8 IR Emitters

33. (a) Determine the radiant flux at a dc forward current of 70 mA for the device of Fig. 20.32.
(b) Determine the radiant flux in lumens at a dc forward current of 45 mA.

***34.** (a) Through the use of Fig. 20.33, determine the relative radiant intensity at an angle of 25° for a package with a flat glass window.
(b) Plot a curve of relative radiant intensity versus degrees for the flat package.

***35.** If 60 mA of dc forward current is applied to an SG1010A IR emitter, what will be the incident radiant flux in lumens 5° off the center if the package has an internal collimating system? Refer to Figs. 20.32 and 20.33.

§ 20.9 Liquid-Crystal Displays

36. Referring to Fig. 20.37, which terminals must be energized to display number 7?

37. In your own words, describe the basic operation of an LCD.

38. Discuss the relative differences in mode of operation between an LED and an LCD display.

39. What are the relative advantages and disadvantages of an LCD display as compared to an LED display?

§ 20.10 Solar Cells

40. A 1-cm by 2-cm solar cell has a conversion efficiency of 9%. Determine the maximum power rating of the device.

***41.** If the power rating of a solar cell is determined on a very rough scale by the product $V_{OC}\, I_{SC}$, is the greatest rate of increase obtained at lower or higher levels of illumination? Explain your reasoning.

42. (a) Referring to Fig. 20.48, what power density is required to establish a current of 24 mA at an output voltage of 0.25 V?
(b) Why is 100 mW/cm^2 the maximum power density in Fig. 20.48?
(c) Determine the output current if the power is 40 mW/cm^2 and the output voltage is 0.3 V.

***43.** (a) Sketch a curve of output current versus power density at an output voltage of 0.15 V using the characteristics of Fig. 20.48.
(b) Sketch a curve of output voltage versus power density at a current of 19 mA.
(c) Is either of the curves from parts (a) and (b) linear within the limits of the maximum power limitation?

§ 20.11 Thermistors

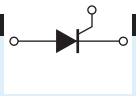
***44.** For the thermistor of Fig. 20.49, determine the dynamic rate of change in specific resistance with temperature at $T = 20°C$. How does this compare to the value determined at $T = 300°C$? From the results, determine whether the greatest change in resistance per unit change in temperature occurs at lower or higher levels of temperature. Note the vertical log scale.

45. Using the information provided in Fig. 20.49, determine the total resistance of a 2-cm length of the material having a perpendicular surface area of 1 cm^2 at a temperature of 0°C. Note the vertical log scale.

46. (a) Referring to Fig. 20.50, determine the current at which a 25°C sample of the material changes from a positive to negative temperature coefficient. (Figure 20.50 is a log scale.)
(b) Determine the power and resistance levels of the device (Fig. 20.50) at the peak of the 0°C curve.
(c) At a temperature of 25°C, determine the power rating if the resistance level is 1 MΩ.

47. In Fig. 20.52, $V = 0.2$ V and $R_{\text{variable}} = 10\ \Omega$. If the current through the sensitive movement is 2 mA and the voltage drop across the movement is 0 V, what is the resistance of the thermistor?

*Please Note: Asterisks indicate more difficult problems.



CHAPTER

21 *pnpn* and Other Devices

21.1 INTRODUCTION

In this chapter, a number of important devices not discussed in detail in earlier chapters are introduced. The two-layer semiconductor diode has led to three-, four-, and even five-layer devices. A family of four-layer *pnpn* devices will first be considered: SCR (silicon-controlled rectifier), SCS (silicon-controlled switch), GTO (gate turn-off switch), LASCR (light-activated SCR), followed by an increasingly important device—the UJT (unijunction transistor). Those four-layer devices with a control mechanism are commonly referred to as *thyristors,* although the term is most frequently applied to the SCR (silicon-controlled rectifier). The chapter closes with an introduction to the phototransistor, opto-isolators, and the PUT (programmable unijunction transistor).

pnpn DEVICES

21.2 SILICON-CONTROLLED RECTIFIER

Within the family of *pnpn* devices, the silicon-controlled rectifier (SCR) is unquestionably of the greatest interest today. It was first introduced in 1956 by Bell Telephone Laboratories. A few of the more common areas of application for SCRs include relay controls, time-delay circuits, regulated power suppliers, static switches, motor controls, choppers, inverters, cycloconverters, battery chargers, protective circuits, heater controls, and phase controls.

In recent years, SCRs have been designed to *control* powers as high as 10 MW with individual ratings as high as 2000 A at 1800 V. Its frequency range of application has also been extended to about 50 kHz, permitting some high-frequency applications such as induction heating and ultrasonic cleaning.

21.3 BASIC SILICON-CONTROLLED RECTIFIER OPERATION

As the terminology indicates, the SCR is a rectifier constructed of silicon material with a third terminal for control purposes. Silicon was chosen because of its high temperature and power capabilities. The basic operation of the SCR is different from the fundamental two-layer semiconductor diode in that a third terminal, called a *gate,* de-

termines when the rectifier switches from the open-circuit to short-circuit state. It is not enough to simply forward-bias the anode-to-cathode region of the device. In the conduction region, the dynamic resistance of the SCR is typically 0.01 to 0.1 Ω. The reverse resistance is typically 100 kΩ or more.

The graphic symbol for the SCR is shown in Fig. 21.1 with the corresponding connections to the four-layer semiconductor structure. As indicated in Fig. 21.1a, if forward conduction is to be established, the anode must be positive with respect to the cathode. This is not, however, a sufficient criterion for turning the device on. A pulse of sufficient magnitude must also be applied to the gate to establish a turn-on gate current, represented symbolically by I_{GT}.

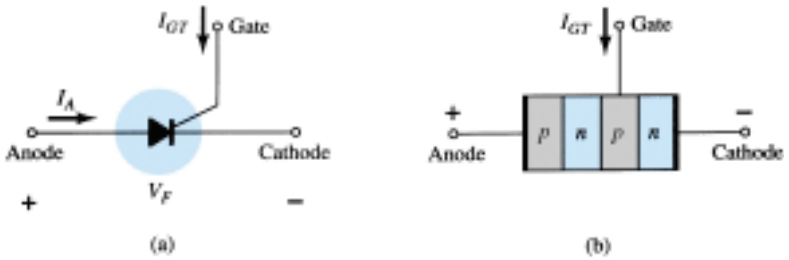


Figure 21.1 (a) SCR symbol; (b) basic construction.

A more detailed examination of the basic operation of an SCR is best effected by splitting the four-layer *pnpn* structure of Fig. 21.1b into two three-layer transistor structures as shown in Fig. 21.2a and then considering the resultant circuit of Fig. 21.2b.

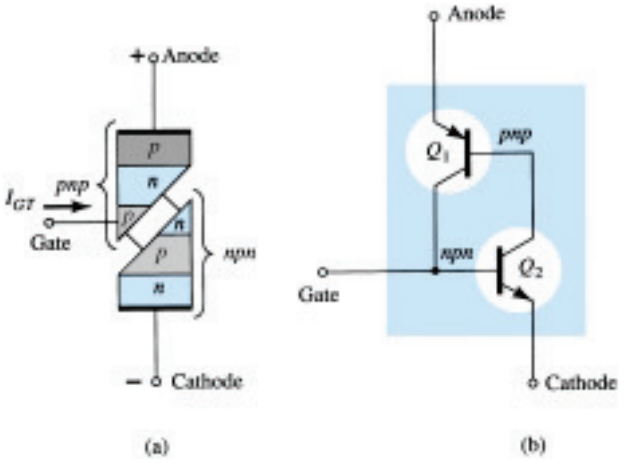


Figure 21.2 SCR two-transistor equivalent circuit.

Note that one transistor for Fig. 21.2 is an *npn* device while the other is a *pnp* transistor. For discussion purposes, the signal shown in Fig. 21.3a will be applied to the gate of the circuit of Fig. 21.2b. During the interval $0 \rightarrow t_1, V_{\text{gate}} = 0$ V, the circuit of Fig. 21.2b will appear as shown in Fig. 21.3b ($V_{\text{gate}} = 0$ V is equivalent to the gate terminal being grounded as shown in the figure). For $V_{BE_2} = V_{\text{gate}} = 0$ V, the base current $I_{B_2} = 0$ and I_{C_2} will be approximately I_{CO}. The base current of Q_1, $I_{B_1} = I_{C_2} = I_{CO}$, is too small to turn Q_1 on. Both transistors are therefore in the "off" state, resulting in a high impedance between the collector and emitter of each transistor and the open-circuit representation for the controlled rectifier as shown in Fig. 21.3c.

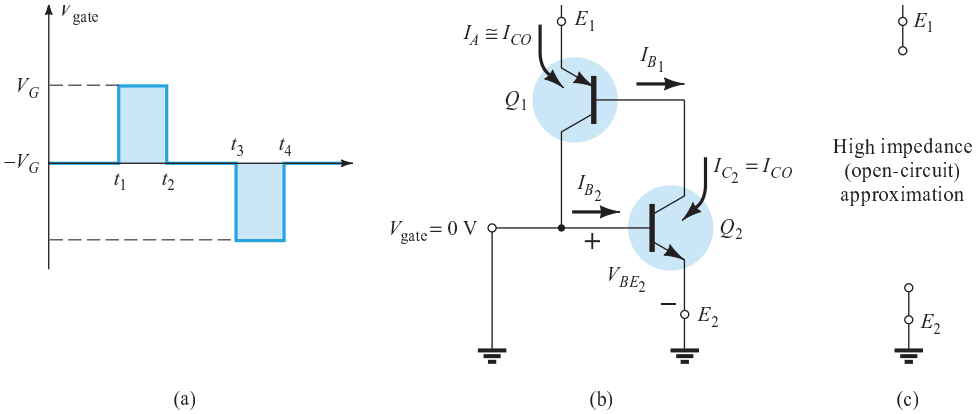


Figure 21.3 "Off" state of the SCR.

At $t = t_1$, a pulse of V_G volts will appear at the SCR gate. The circuit conditions established with this input are shown in Fig. 21.4a. The potential V_G was chosen sufficiently large to turn Q_2 on ($V_{BE_2} = V_G$). The collector current of Q_2 will then rise to a value sufficiently large to turn Q_1 on ($I_{B_1} = I_{C_2}$). As Q_1 turns on, I_{C_1} will increase, resulting in a corresponding increase in I_{B_2}. The increase in base current for Q_2 will result in a further increase in I_{C_2}. The net result is a regenerative increase in the collector current of each transistor. The resulting anode-to-cathode resistance ($R_{SCR} = V/I_A$) is then small because I_A is large, resulting in the short-circuit representation for the SCR as indicated in Fig. 21.4b. The regenerative action described above results in SCRs having typical turn-on times of 0.1 to 1 μs. However, high-power devices in the range 100 to 400 A may have 10- to 25-μs turn-on times.

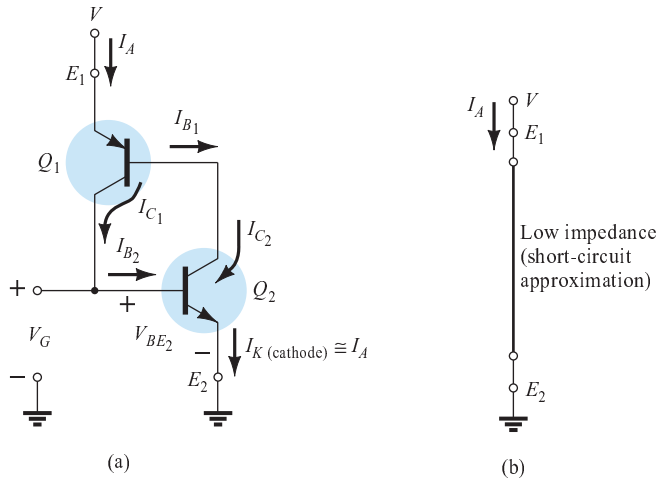


Figure 21.4 "On" state of the SCR.

In addition to gate triggering, SCRs can also be turned on by significantly raising the temperature of the device or raising the anode-to-cathode voltage to the breakover value shown on the characteristics of Fig. 21.7.

The next question of concern is: How long is the turn-off time and how is turn-off accomplished? An SCR *cannot* be turned off by simply removing the gate signal, and only a special few can be turned off by applying a negative pulse to the gate terminal as shown in Fig. 21.3a at $t = t_3$.

The two general methods for turning off an SCR are categorized as the anode current interruption and the forced-commutation technique.

The two possibilities for current interruption are shown in Fig. 21.5. In Fig. 21.5a, I_A is zero when the switch is opened (series interruption), while in Fig. 21.5b, the same condition is established when the switch is closed (shunt interruption).

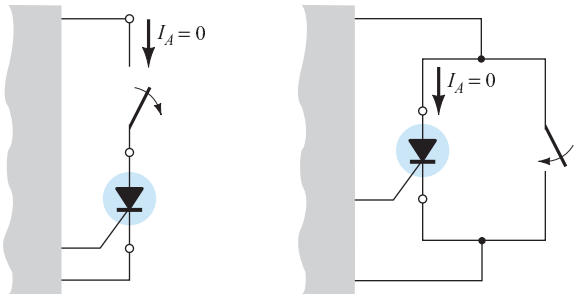


Figure 21.5 Anode current interruption.

Forced commutation is the "forcing" of current through the SCR in the direction opposite to forward conduction. There are a wide variety of circuits for performing this function, a number of which can be found in the manuals of major manufacturers in this area. One of the more basic types is shown in Fig. 21.6. As indicated in the figure, the turn-off circuit consists of an *npn* transistor, a dc battery V_B, and a pulse generator. During SCR conduction, the transistor is in the "off" state, that is, $I_B = 0$ and the collector-to-emitter impedance is very high (for all practical purposes an open circuit). This high impedance will isolate the turn-off circuitry from affecting the operation of the SCR. For turn-off conditions, a positive pulse is applied to the base of the transistor, turning it heavily on, resulting in a very low impedance from collector to emitter (short-circuit representation). The battery potential will then appear directly across the SCR as shown in Fig. 21.6b, forcing current through it in the reverse direction for turn-off. Turn-off times of SCRs are typically 5 to 30 μs.

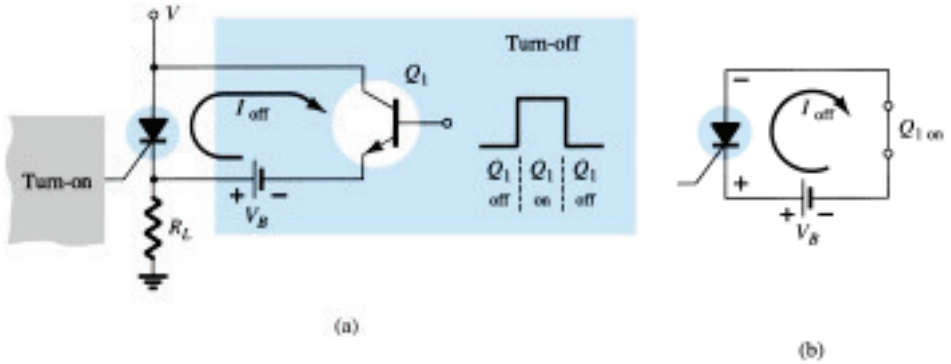
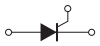


Figure 21.6 Forced-commutation technique.

21.4 SCR CHARACTERISTICS AND RATINGS

The characteristics of an SCR are provided in Fig. 21.7 for various values of gate current. The currents and voltages of usual interest are indicated on the characteristic. A brief description of each follows.



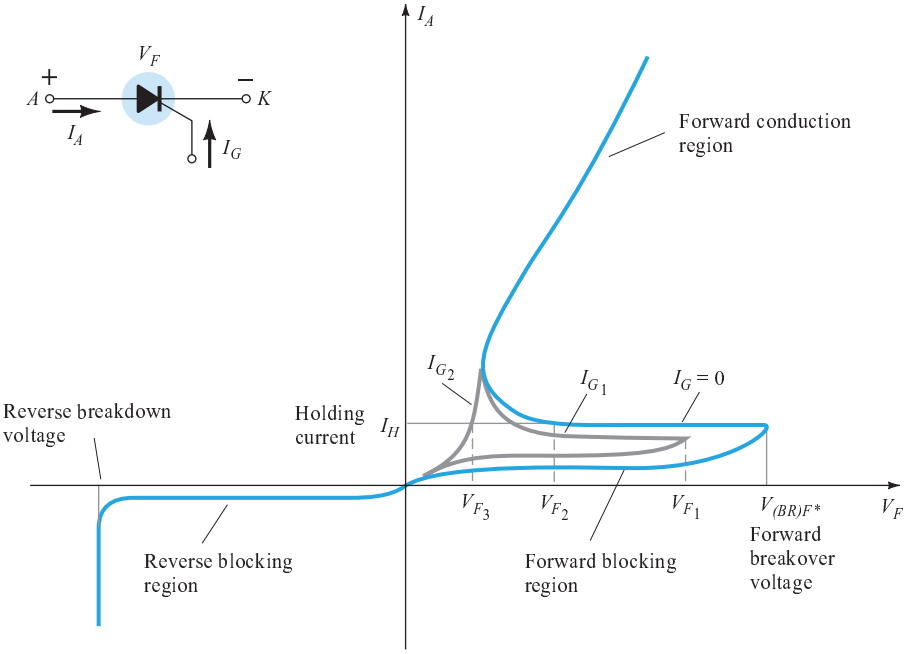


Figure 21.7 SCR characteristics.

1. *Forward breakover voltage* $V_{(BR)F*}$ is that voltage above which the SCR enters the conduction region. The asterisk (*) is a letter to be added that is dependent on the condition of the gate terminal as follows:

   O = open circuit from G to K

   S = short circuit from G to K

   R = resistor from G to K

   V = fixed bias (voltage) from G to K

2. *Holding current* (I_H) is that value of current below which the SCR switches from the conduction state to the forward blocking region under stated conditions.
3. *Forward and reverse blocking regions* are the regions corresponding to the open-circuit condition for the controlled rectifier which *block* the flow of charge (current) from anode to cathode.
4. *Reverse breakdown voltage* is equivalent to the Zener or avalanche region of the fundamental two-layer semiconductor diode.

It should be immediately obvious that the SCR characteristics of Fig. 21.7 are very similar to those of the basic two-layer semiconductor diode except for the horizontal offshoot before entering the conduction region. It is this horizontal jutting region that gives the gate control over the response of the SCR. For the characteristic having the solid blue line in Fig. 21.7 ($I_G = 0$), V_F must reach the largest required breakover voltage ($V_{(BR)F*}$) before the "collapsing" effect will result and the SCR can enter the conduction region corresponding to the *on* state. If the gate current is increased to I_{G_1}, as shown in the same figure by applying a bias voltage to the gate terminal, the value of V_F required for the conduction (V_{F_1}) is considerably less. Note also that I_H drops with increase in I_G. If increased to I_{G_2}, the SCR will fire at very low values of voltage (V_{F_3}) and the characteristics begin to approach those of the basic *p-n* junction diode. Looking at the characteristics in a completely different sense, for a particular V_F voltage, say V_{F_2} (Fig. 21.7), if the gate current is increased from $I_G = 0$ to I_{G1} or more, the SCR will fire.

The gate characteristics are provided in Fig. 21.8. The characteristics of Fig. 21.8b are an expanded version of the shaded region of Fig. 21.8a. In Fig. 21.8a, the three gate ratings of greatest interest, P_{GFM}, I_{GFM}, and V_{GFM} are indicated. Each is included on the characteristics in the same manner employed for the transistor. Except for portions of the shaded region, any combination of gate current and voltage that falls within this region will fire any SCR in the series of components for which these characteristics are provided. Temperature will determine which sections of the shaded region must be avoided. At $-65°C$ the minimum current that will trigger the series of SCRs is 100 mA, while at $+150°C$ only 20 mA are required. The effect of temperature on the minimum gate voltage is usually not indicated on curves of this type since gate potentials of 3 V or more are usually obtained easily. As indicated on Fig. 21.8b, a minimum of 3 V is indicated for all units for the temperature range of interest.

Other parameters usually included on the specification sheet of an SCR are the turn-on time (t_{on}), turn-off time (t_{off}), junction temperature (T_J), and case temperature (T_C), all of which should by now be, to some extent, self-explanatory.

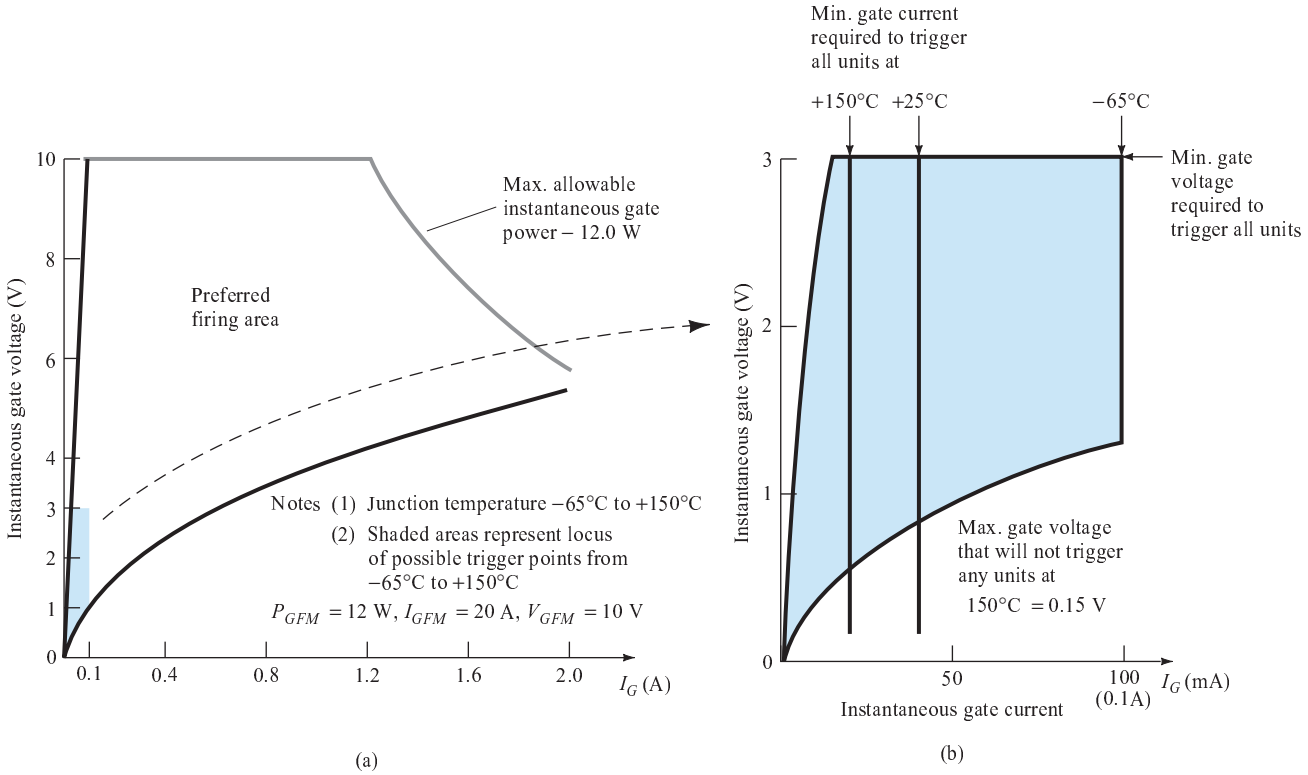


Figure 21.8 SCR gate characteristics (GE series C38).

21.5 SCR CONSTRUCTION AND TERMINAL IDENTIFICATION

The basic construction of the four-layer pellet of an SCR is shown in Fig. 21.9a. The complete construction of a thermal fatigue-free, high-current SCR is shown in Fig. 21.9b. Note the position of the gate, cathode, and anode terminals. The pedestal acts as a heat sink by transferring the heat developed to the chassis on which the SCR is mounted. The case construction and terminal identification of SCRs will vary with the application. Other case-construction techniques and the terminal identification of each are indicated in Fig. 21.10.

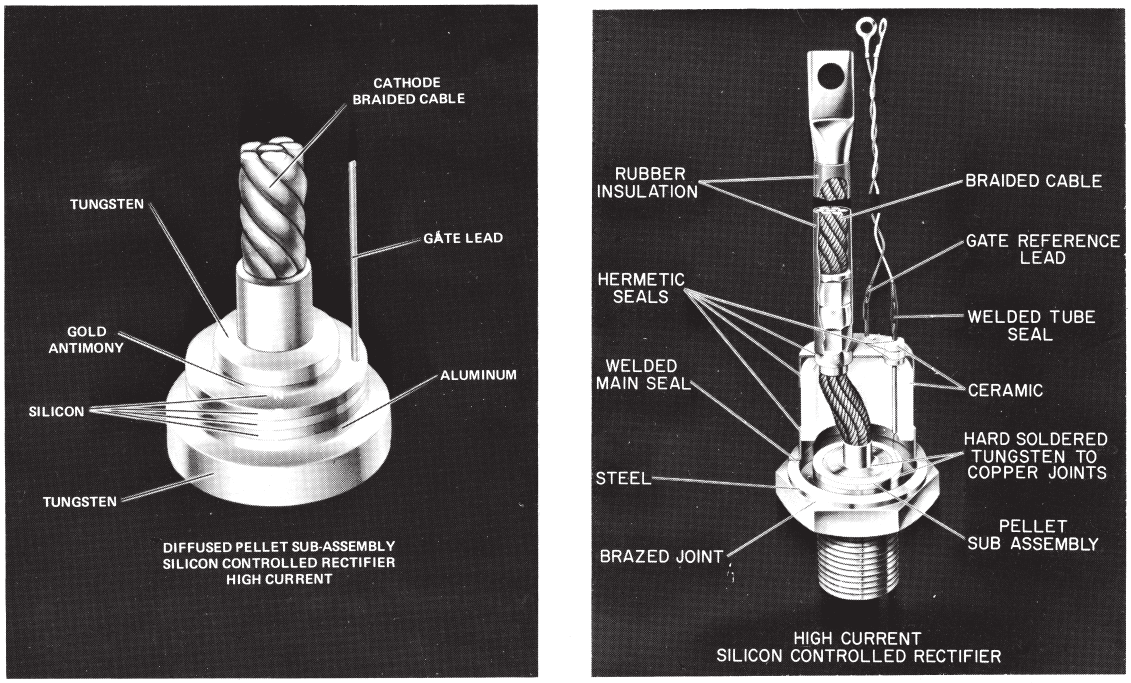


Figure 21.9 (a) Alloy-diffused SCR pellet; (b) thermal fatigue-free SCR construction. (Courtesy General Electric Company.)

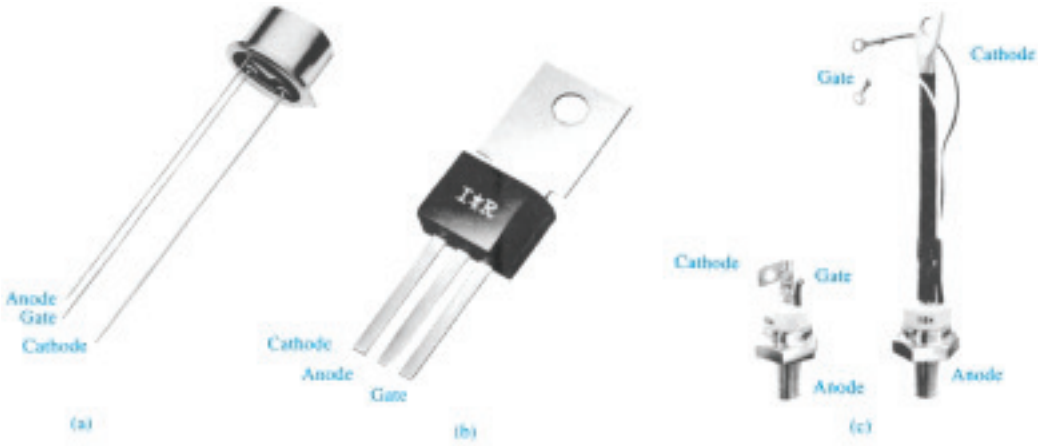


Figure 21.10 SCR case construction and terminal identification. [(a) Courtesy General Electric Company; (b) and (c) courtesy International Rectifier Corporation.]

21.6 SCR APPLICATIONS

A few of the possible applications for the SCR are listed in the introduction to the SCR (Section 21.2). In this section, we consider five: a static switch, phase-control system, battery charger, temperature controller, and single-source emergency-lighting system.

A half-wave *series static switch* is shown in Fig. 21.11a. If the switch is closed as shown in Fig. 21.11b, a gate current will flow during the positive portion of the input signal, turning the SCR on. Resistor R_1 limits the magnitude of the gate cur-

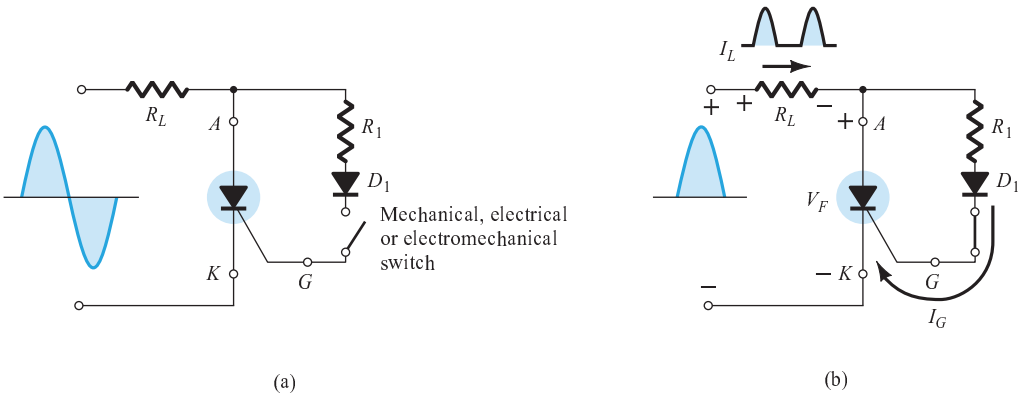


Figure 21.11 Half-wave series static switch.

rent. When the SCR turns on, the anode-to cathode voltage (V_F) will drop to the conduction value, resulting in a greatly reduced gate current and very little loss in the gate circuitry. For the negative region of the input signal, the SCR will turn off since the anode is negative with respect to the cathode. The diode D_1 is included to prevent a reversal in gate current.

The waveforms for the resulting load current and voltage are shown in Fig. 21.11b. The result is a half-wave-rectified signal through the load. If less than 180° conduction is desired, the switch can be closed at any phase displacement during the positive portion of the input signal. The switch can be electronic, electromagnetic, or mechanical, depending on the application.

A circuit capable of establishing a conduction angle between 90° and 180° is shown in Fig. 21.12a. The circuit is similar to that of Fig. 21.11a except for the addition of a variable resistor and the elimination of the switch. The combination of the resistors R and R_1 will limit the gate current during the positive portion of the input signal. If R_1 is set to its maximum value, the gate current may never reach turn-on magnitude. As R_1 is decreased from the maximum, the gate current will increase from the same input voltage. In this way, the required turn-on gate current can be established in any point between 0° and 90° as shown in Fig. 21.12b. If R_1 is low, the SCR will fire almost immediately, resulting in the same action as that obtained from the circuit of Fig. 21.11a (180° conduction). However, as indicated above, if R_1 is increased, a larger input voltage (positive) will be required to fire the SCR. As shown in Fig. 21.12b, the control cannot be extended past a 90° phase displacement since the input is at its maximum at this point. If it fails to fire at this and lesser values of input voltage on the positive slope of the input, the same response must be expected from the negatively sloped portion of the signal waveform. The operation here is normally referred to in technical terms as *half-wave variable-resistance phase control.* It is an effective method of controlling the rms current and therefore power to the load.

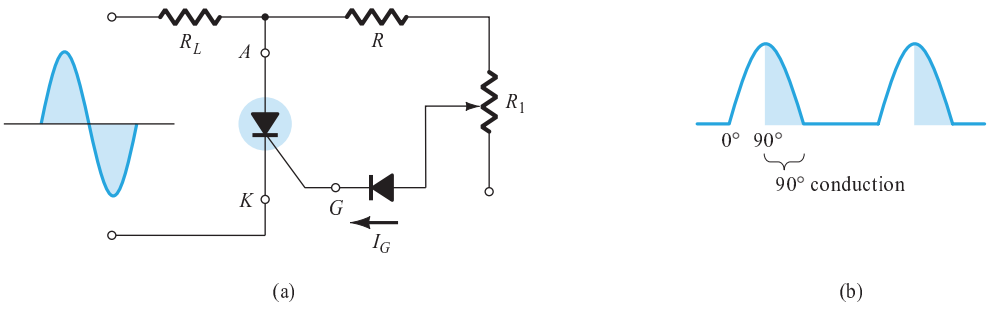


Figure 21.12 Half-wave variable-resistance phase control.

A third popular application of the SCR is in a *battery-charging regulator*. The fundamental components of the circuit are shown in Fig. 21.13. You will note that the control circuit has been blocked off for discussion purposes.

As indicated in the figure, D_1 and D_2 establish a full-wave-rectified signal across SCR_1 and the 12-V battery to be charged. At low battery voltages, SCR_2 is in the "off" state for reasons to be explained shortly. With SCR_2 open, the SCR_1 controlling circuit is exactly the same as the series static switch control discussed earlier in this section. When the full-wave-rectified input is sufficiently large to produce the required turn-on gate current (controlled by R_1), SCR_1 will turn on and charging of the battery will commence. At the start of charging, the low battery voltage will result in a low voltage V_R as determined by the simple voltage-divider circuit. Voltage V_R is in turn too small to cause 11.0-V Zener conduction. In the off state, the Zener is effectively an open circuit, maintaining SCR_2 in the "off" state since the gate current is zero. The capacitor C_1 is included to prevent any voltage transients in the circuit from accidentally turning on SCR_2. Recall from your fundamental study of circuit analysis that the voltage cannot change instantaneously across a capacitor. In this way, C_1 prevents transient effects from affecting the SCR.

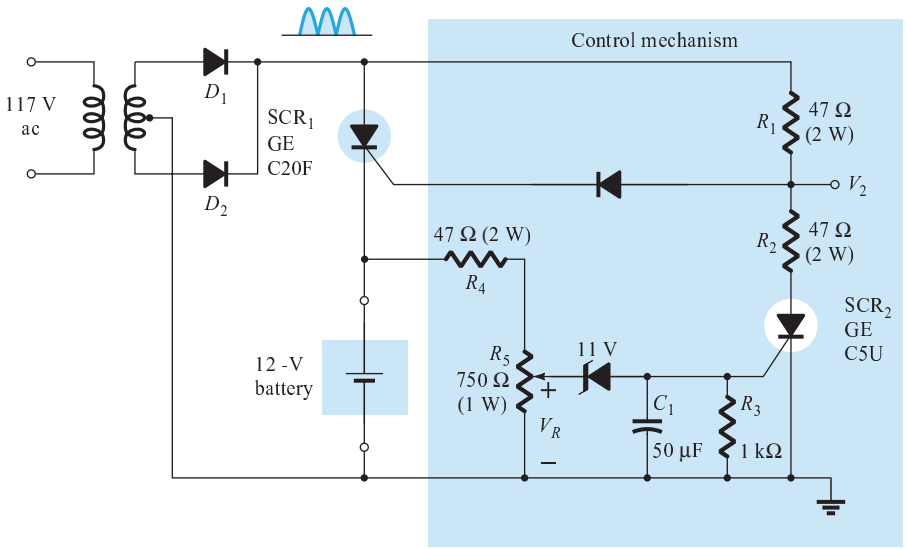


Figure 21.13 Battery-charging regulator.

As charging continues, the battery voltage rises to a point where V_R is sufficiently high to both turn on the 11.0-V Zener and fire SCR_2. Once SCR_2 has fired, the short-circuit representation for SCR_2 will result in a voltage-divider circuit determined by R_1 and R_2 that will maintain V_2 at a level too small to turn SCR_1 on. When this occurs, the battery is fully charged and the open-circuit state of SCR_1 will cut off the charging current. Thus the regulator recharges the battery whenever the voltage drops and prevents overcharging when fully charged.

The schematic diagram of a 100-W heater control using an SCR appears in Fig. 21.14. It is designed such that the 100-W heater will turn on and off as determined by thermostats. Mercury-in-glass thermostats are very sensitive to temperature change. In fact, they can sense changes as small as 0.1°C. It is limited in application, however, in that it can handle only very low levels of current—below 1 mA. In this application, the SCR serves as a current amplifier in a load-switching element. It is not

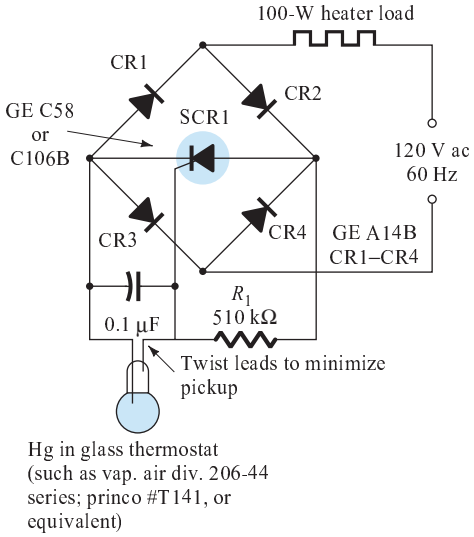


Figure 21.14 Temperature controller. (Courtesy General Electric Semiconductor Products Division.)

an amplifier in the sense that it magnifies the current level of the thermostat. Rather it is a device whose higher current level is controlled by the behavior of the thermostat.

It should be clear that the bridge network is connected to the ac supply through the 100-W heater. This will result in a full-wave-rectified voltage across the SCR. When the thermostat is open, the voltage across the capacitor will charge to a gate-firing potential through each pulse of the rectified signal. The charging time constant is determined by the RC product. This will trigger the SCR during each half-cycle of the input signal, permitting a flow of charge (current) to the heater. As the temperature rises, the conductive thermostat will short-circuit the capacitor, eliminating the possibility of the capacitor charging to the firing potential and triggering the SCR. The 510-kΩ resistor will then contribute to maintaining a very low current (less than 250 μA) through the thermostat.

The last application for the SCR to be described is shown in Fig. 21.15. It is a single-source emergency-lighting system that will maintain the charge on a 6-V battery to ensure its availability and also provide dc energy to a bulb if there is a power shortage. A full-wave-rectified signal will appear across the 6-V lamp due to diodes D_2 and D_1. The capacitor C_1 will charge to a voltage slightly less than a difference between the peak value of the full-wave-rectified signal and the dc voltage across R_2 established by the 6-V battery. In any event, the cathode of SCR_1 is higher than the

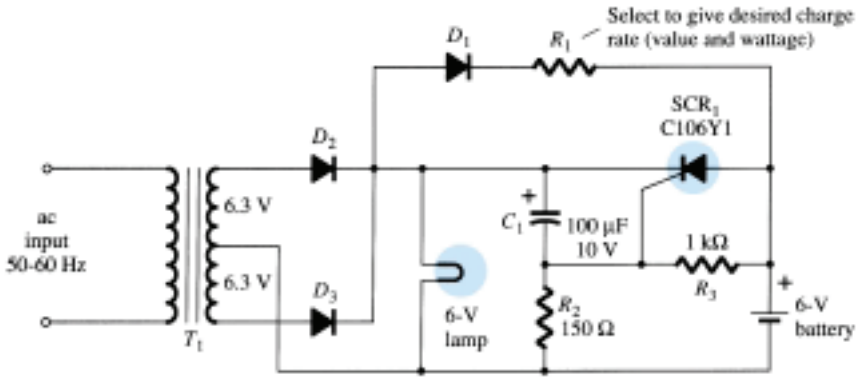


Figure 21.15 Single-source emergency-lighting system. (Courtesy General Electric Semiconductor Products Division.)

anode and the gate-to-cathode voltage is negative, ensuring that the SCR is nonconducting. The battery is being charged through R_1 and D_1 at a rate determined by R_1. Charging will only take place when the anode of D_1 is more positive than its cathode. The dc level of the full-wave-rectified signal will ensure that the bulb is lit when the power is on. If the power should fail, the capacitor C_1 will discharge through D_1, R_1, and R_3 until the cathode of SCR_1 is less positive than the anode. At the same time, the junction of R_2 and R_3 will become positive and establish sufficient gate-to-cathode voltage to trigger the SCR. Once fired, the 6-V battery would discharge through the SCR_1 and energize the lamp and maintain its illumination. Once power is restored, the capacitor C_1 will recharge and re-establish the nonconducting state of SCR_1 as described above.

21.7 SILICON-CONTROLLED SWITCH

The silicon-controlled switch (SCS), like the silicon-controlled rectifier, is a four-layer *pnpn* device. All four semiconductor layers of the SCS are available due to the addition of an anode gate, as shown in Fig. 21.16a. The graphic symbol and transistor equivalent circuit are shown in the same figure. The characteristics of the device are essentially the same as those for the SCR. The effect of an anode gate current is very similar to that demonstrated by the gate current in Fig. 21.7. The higher the anode gate current, the lower the required anode-to-cathode voltage to turn the device on.

The anode gate connection can be used to turn the device either on or off. To turn on the device, a negative pulse must be applied to the anode gate terminal, while a positive pulse is required to turn off the device. The need for the type of pulse indicated above can be demonstrated using the circuit of Fig. 21.16c. A negative pulse at the anode gate will forward-bias the base-to-emitter junction of Q_1, turning it on. The resulting heavy collector current I_{C_1} will turn on Q_2, resulting in a regenerative action and the on state for the SCS device. A positive pulse at the anode gate will reverse-bias the base-to-emitter junction of Q_1, turning it off, resulting in the open-circuit "off" state of the device. In general, the triggering (turn-on) anode gate current is larger in magnitude than the required cathode gate current. For one representative SCS device, the triggering anode gate current is 1.5 mA while the required cathode gate current is 1 μA. The required turn-on gate current at either terminal is affected by many factors. A few include the operating temperature, anode-to-cathode voltage, load placement, and type of cathode, gate-to-cathode or anode gate-to-anode connection (short-circuit, open-circuit, bias, load, etc.). Tables, graphs, and curves are normally available for each device to provide the type of information indicated above.

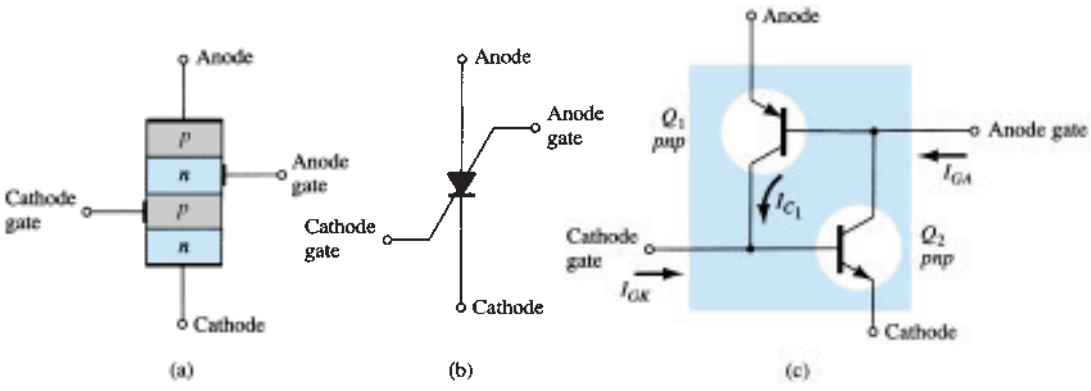


Figure 21.16 Silicon-controlled switch (SCS): (a) basic construction; (b) graphic symbol; (c) equivalent transistor circuit.

Three of the more fundamental types of turn-off circuits for the SCS are shown in Fig. 21.17. When a pulse is applied to the circuit of Fig. 21.17a, the transistor conducts heavily, resulting in a low-impedance (≅ short-circuit) characteristic between collector and emitter. This low-impedance branch diverts anode current away from the SCS, dropping it below the holding value and consequently turning it off. Similarly, the positive pulse at the anode gate of Fig. 21.17b will turn the SCS off by the mechanism described earlier in this section. The circuit of Fig. 21.17c can be turned either off *or* on by a pulse of the proper magnitude at the cathode gate. The turn-off characteristic is possible only if the correct value of R_A is employed. It will control the amount of regenerative feedback, the magnitude of which is critical for this type of operation. Note the variety of positions in which the load resistor R_L can be placed. There are a number of other possibilities that can be found in any comprehensive semiconductor handbook or manual.

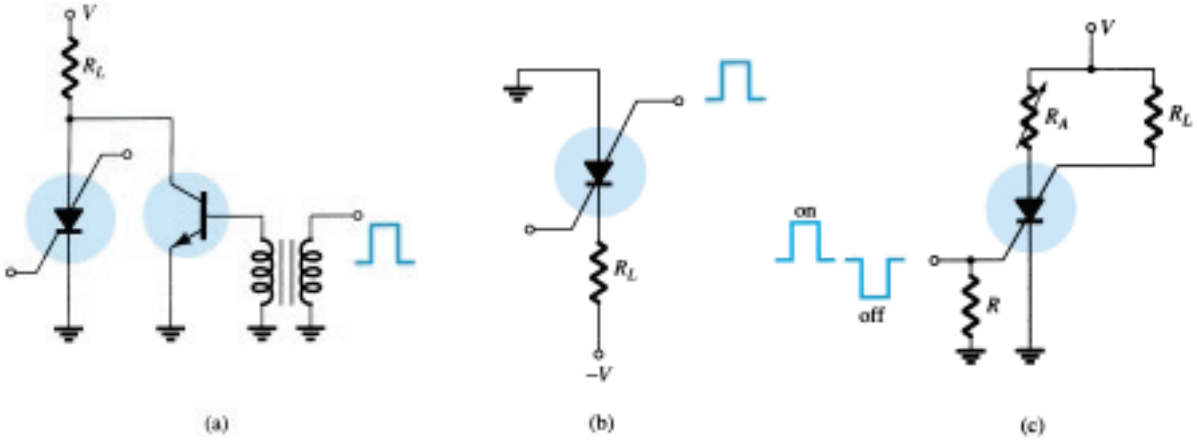


Figure 21.17 SCS turn-off techniques.

An advantage of the SCS over a corresponding SCR is the reduced turn-off time, typically within the range 1 to 10 μs for the SCS and 5 to 30 μs for the SCR. Some of the remaining advantages of the SCS over an SCR include increased control and triggering sensitivity and a more predictable firing situation. At present, however, the SCS is limited to low power, current, and voltage ratings. Typical maximum anode currents range from 100 to 300 mA with dissipation (power) ratings of 100 to 500 mW.

A few of the more common areas of application include a wide variety of computer circuits (counters, registers, and timing circuits), pulse generators, voltage sensors, and oscillators. One simple application for an SCS as a voltage-sensing device is shown in Fig. 21.18. It is an alarm system with n inputs from various stations. Any single input will turn that particular SCS on, resulting in an energized alarm relay and light in the anode gate circuit to indicate the location of the input (disturbance).

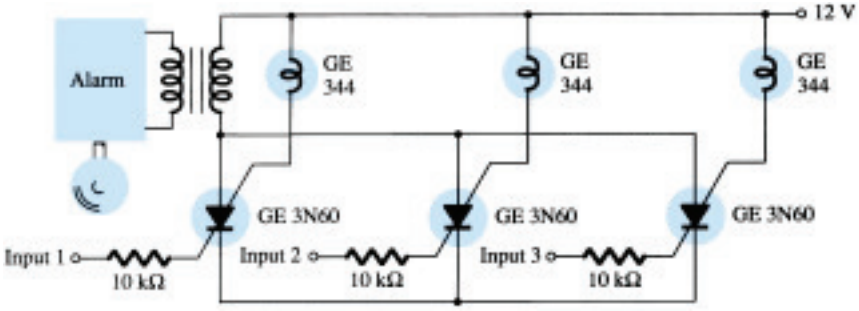


Figure 21.18 SCS alarm circuit.

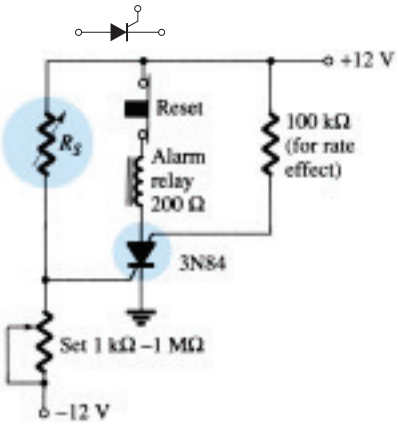


Figure 21.19 Alarm circuit. (Courtesy General Electric Semiconductor Products Division.)

One additional application of the SCS is in the alarm circuit of Fig. 21.19. R_S represents a temperature-, light-, or radiation-sensitive resistor, that is, an element whose resistance will decrease with the application of any of the three energy sources listed above. The cathode gate potential is determined by the divider relationship established by R_S and the variable resistor. Note that the gate potential is at approximately 0 V if R_S equals the value set by the variable resistor since both resistors will have 12 V across them. However, if R_S decreases, the potential of the junction will increase until the SCS is forward-biased, causing the SCS to turn on and energize the alarm relay.

The 100-kΩ resistor is included to reduce the possibility of accidental triggering of the device through a phenomenon known as *rate effect*. It is caused by the stray capacitance levels between gates. A high-frequency transient can establish sufficient base current to turn the SCS on accidentally. The device is reset by pressing the reset button, which in turn opens the conduction path of the SCS and reduces the anode current to zero.

Sensitivity to temperature-, light-, or radiation-sensitive resistors whose resistance increases due to the application of any of the three energy sources described above can be accommodated by simply interchanging the location of R_S and the variable resistor. The terminal identification of an SCS is shown in Fig. 21.20 with a packaged SCS.

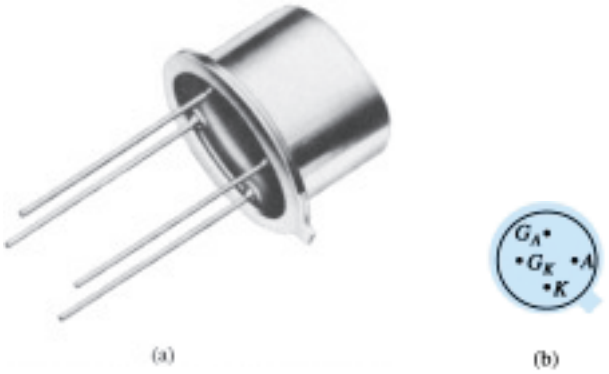


Figure 21.20 Silicon-controlled switch (SCS): (a) device; (b) terminal identification. (Courtesy General Electric Company.)

21.8 GATE TURN-OFF SWITCH

The gate turn-off switch (GTO) is the third *pnpn* device to be introduced in this chapter. Like the SCR, however, it has only three external terminals, as indicated in Fig. 21.21a. Its graphical symbol is also shown in Fig. 21.21b. Although the graphical symbol is different from either the SCR or the SCS, the transistor equivalent is exactly the same and the characteristics are similar.

The most obvious advantage of the GTO over the SCR or SCS is the fact that it can be turned on *or* off by applying the proper pulse to the cathode gate (without the

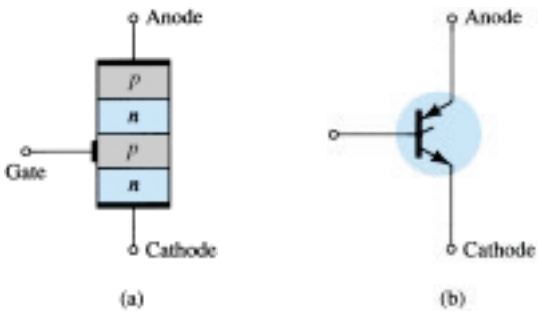


Figure 21.21 Gate turn-off switch (GTO): (a) basic construction; (b) symbol.

anode gate and associated circuitry required for the SCS). A consequence of this turn-off capability is an increase in the magnitude of the required gate current for triggering. For an SCR and GTO of similar maximum rms current ratings, the gate-triggering current of a particular SCR is 30 μA while the triggering current of the GTO is 20 mA. The turn-off current of a GTO is slightly larger than the required triggering current. The maximum rms current and dissipation ratings of GTOs manufactured today are limited to about 3 A and 20 W, respectively.

A second very important characteristic of the GTO is improved switching characteristics. The turn-on time is similar to the SCR (typically 1 μs), but the turn-off time of about the *same* duration (1 μs) is much smaller than the typical turn-off time of an SCR (5 to 30 μs). The fact that the turn-off time is similar to the turn-on time rather than considerably larger permits the use of this device in high-speed applications.

A typical GTO and its terminal identification are shown in Fig. 21.22. The GTO gate input characteristics and turn-off circuits can be found in a comprehensive manual or specification sheet. The majority of the SCR turn-off circuits can also be used for GTOs.

Some of the areas of application for the GTO include counters, pulse generators, multivibrators, and voltage regulators. Figure 21.23 is an illustration of a simple sawtooth generator employing a GTO and a Zener diode.

Figure 21.22 Typical GTO and its terminal identification. (Courtesy General Electric Company.)

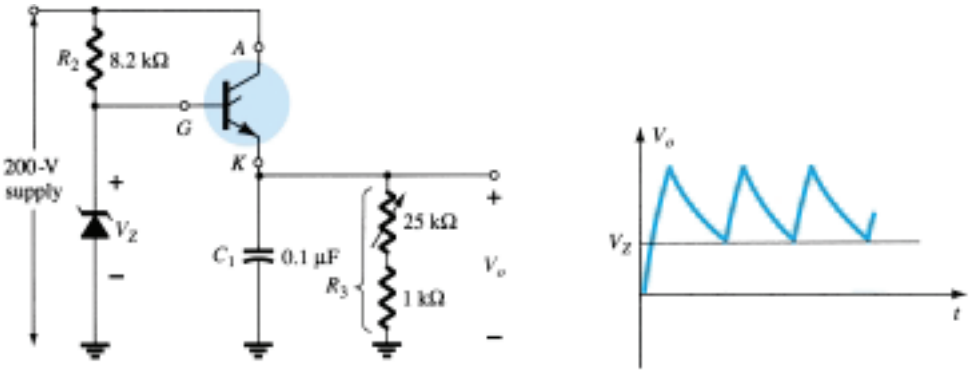


Figure 21.23 GTO sawtooth generator.

When the supply is energized, the GTO will turn on, resulting in the short-circuit equivalent from anode to cathode. The capacitor C_1 will then begin to charge toward the supply voltage as shown in Fig. 21.23. As the voltage across the capacitor C_1 charges above the Zener potential, a reversal in gate-to-cathode voltage will result, establishing a reversal in gate current. Eventually, the negative gate current will be large enough to turn the GTO off. Once the GTO turns off, resulting in the open-circuit representation, the capacitor C_1 will discharge through the resistor R_3. The discharge time will be determined by the circuit time constant $\tau = R_3C_1$. The proper choice of R_3 and C_1 will result in the sawtooth waveform of Fig. 21.23. Once the output potential V_o drops below V_Z, the GTO will turn on and the process will repeat.

21.9 LIGHT-ACTIVATED SCR

The next in the series of *pnpn* devices is the light-activated SCR (LASCR). As indicated by the terminology, it is an SCR whose state is controlled by the light falling upon a silicon semiconductor layer of the device. The basic construction of an LASCR is shown in Fig. 21.24a. As indicated in Fig. 21.24a, a gate lead is also provided to permit triggering the device using typical SCR methods. Note also in the figure that

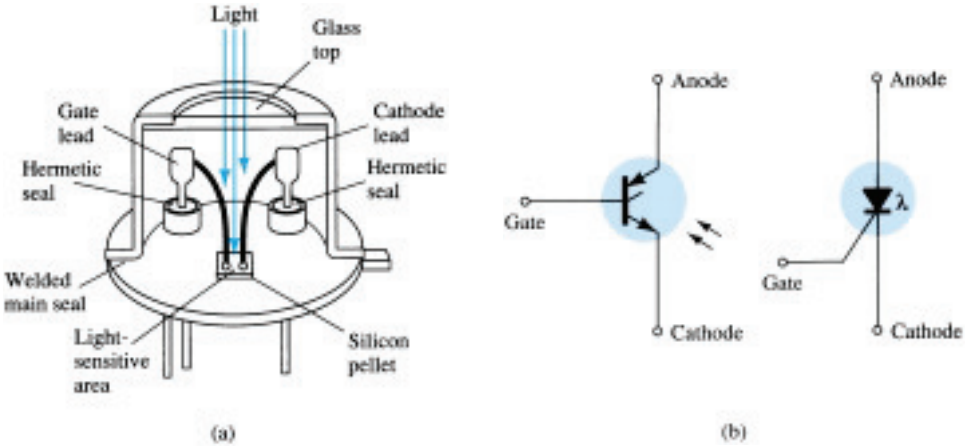


Figure 21.24 Light-activated SCR (LASCR): (a) basic construction; (b) symbols.

the mounting surface for the silicon pellet is the anode connection for the device. The graphical symbols most commonly employed for the LASCR are provided in Fig. 21.24b. The terminal identification and a typical LASCR appear in Fig. 21.25a.

Some of the areas of application for the LASCR include optical light controls, relays, phase control, motor control, and a variety of computer applications. The

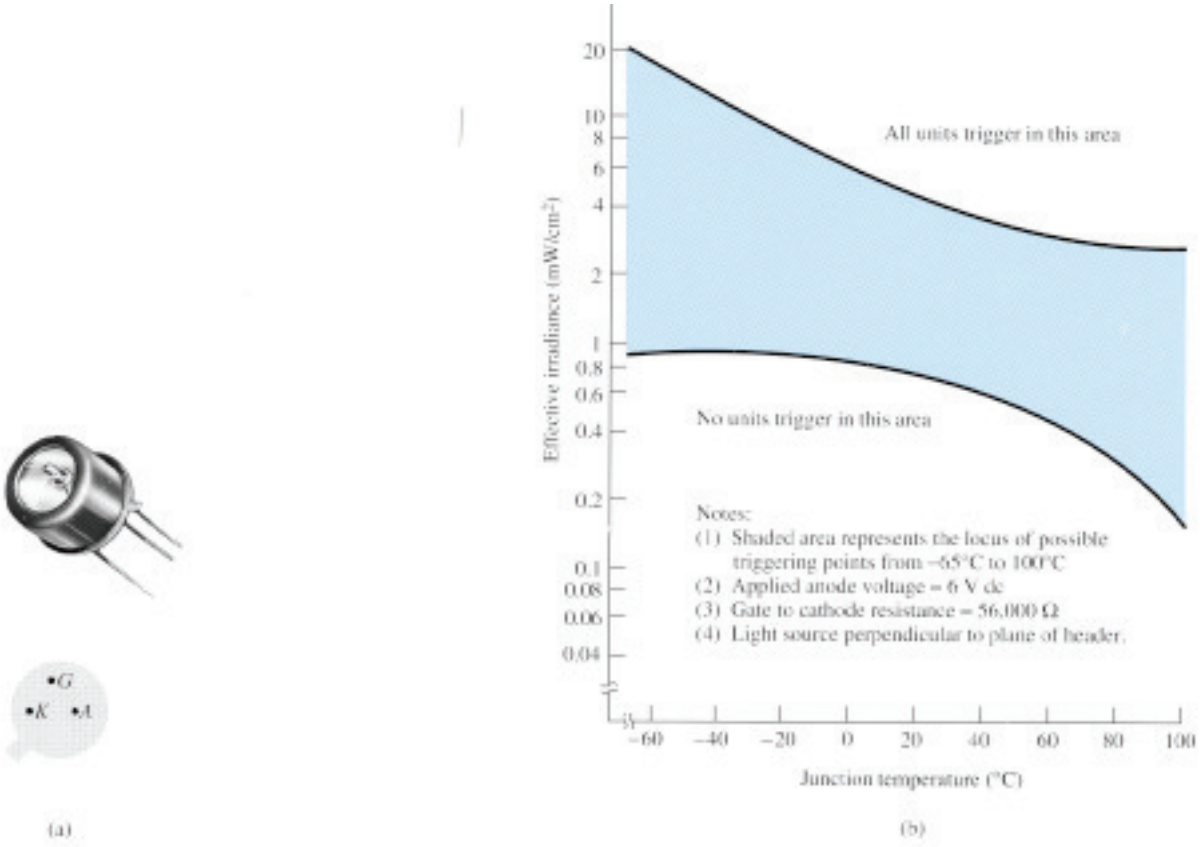


Figure 21.25 LASCR: (a) appearance and terminal identification; (b) light-triggering characteristics. (Courtesy General Electric Company.)

maximum current (rms) and power (gate) ratings for LASCRs commercially available today are about 3 A and 0.1 W. The characteristics (light triggering) of a representative LASCR are provided in Fig. 21.25b. Note in this figure that an increase in junction temperature results in a reduction in light energy required to activate the device.

One interesting application of an LASCR is in the AND and OR circuits of Fig. 21.26. Only when light falls on $LASCR_1$ *and* $LASCR_2$ will the short-circuit representation for each be applicable and the supply voltage appear across the load. For the OR circuit, light energy applied to $LASCR_1$ *or* $LASCR_2$ will result in the supply voltage appearing across the load.

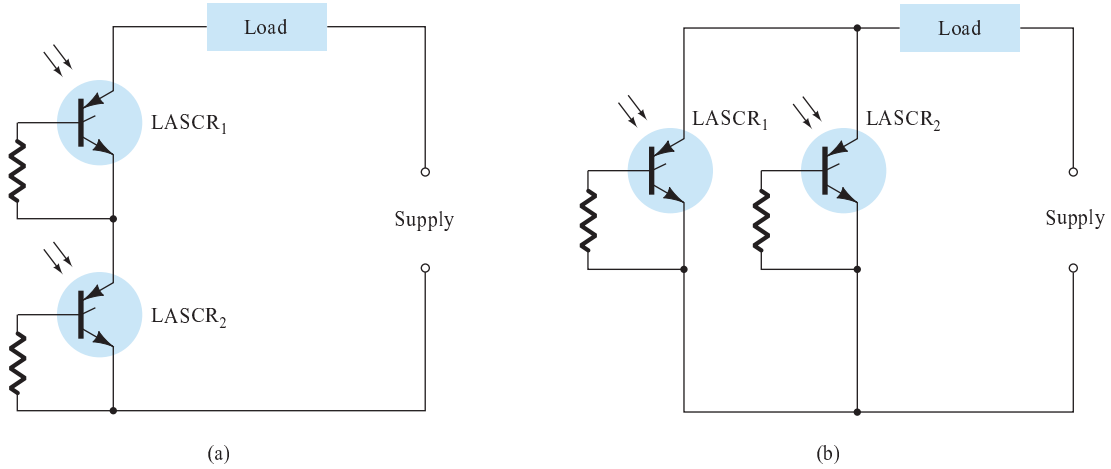


Figure 21.26 LASCR optoelectronic logic circuitry: (a) AND gate: input to $LASCR_1$ *and* $LASCR_2$ required for energization of the load; (b) OR gate: input to either $LASCR_1$ *or* $LASCR_2$ will energize the load.

The LASCR is most sensitive to light when the gate terminal is open. Its sensitivity can be reduced and controlled somewhat by the insertion of a gate resistor, as shown in Fig. 21.26.

A second application of the LASCR appears in Fig. 21.27. It is the semiconductor analog of an electromechanical relay. Note that it offers complete isolation between the input and switching element. The energizing current can be passed through a light-emitting diode or a lamp, as shown in the figure. The incident light will cause the LASCR to turn on and permit a flow of charge (current) through the load as established by the dc supply. The LASCR can be turned off using the reset switch S_1. This system offers the additional advantages over an electromechanical switch of long life, microsecond response, small size, and the elimination of contact bounce.

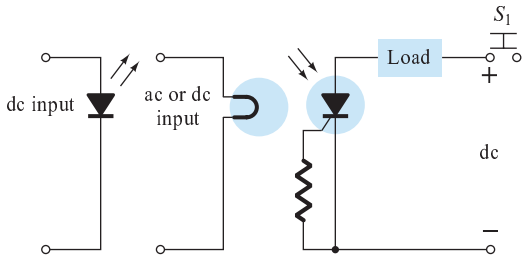


Figure 21.27 Latching relay. (Courtesy Powerex, Inc.)

21.10 SHOCKLEY DIODE

The Shockley diode is a four-layer *pnpn* diode with only two external terminals, as shown in Fig. 21.28a with its graphical symbol. The characteristics (Fig. 21.28b) of the device are exactly the same as those encountered for the SCR with $I_G = 0$. As indicated by the characteristics, the device is in the off state (open-circuit representation) until the breakover voltage is reached, at which time avalanche conditions develop and the device turns on (short-circuit representation).

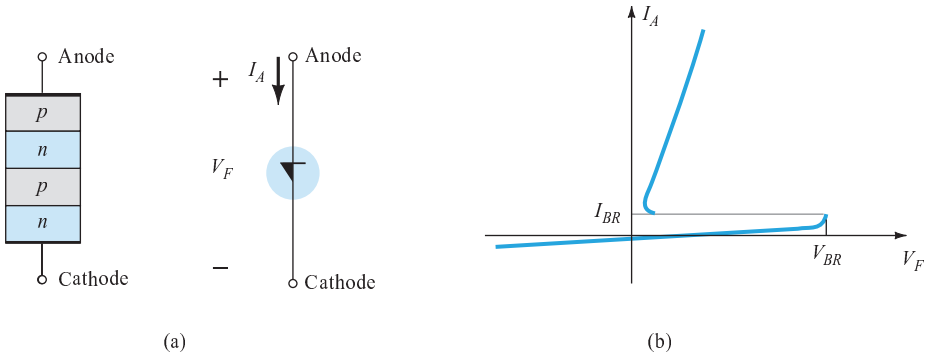


Figure 21.28 Shockley diode: (a) basic construction and symbol; (b) characteristics.

One common application of the Shockley diode is shown in Fig. 21.29, where it is employed as a trigger switch for an SCR. When the circuit is energized, the voltage across the capacitor will begin to change toward the supply voltage. Eventually, the voltage across the capacitor will be sufficiently high to first turn on the Shockley diode and then the SCR.

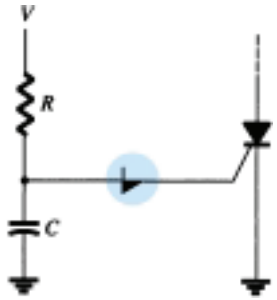


Figure 21.29 Shockley diode application—trigger switch for an SCR.

21.11 DIAC

The diac is basically a two-terminal parallel-inverse combination of semiconductor layers that permits triggering in either direction. The characteristics of the device, presented in Fig. 21.30a, clearly demonstrate that there is a breakover voltage in either

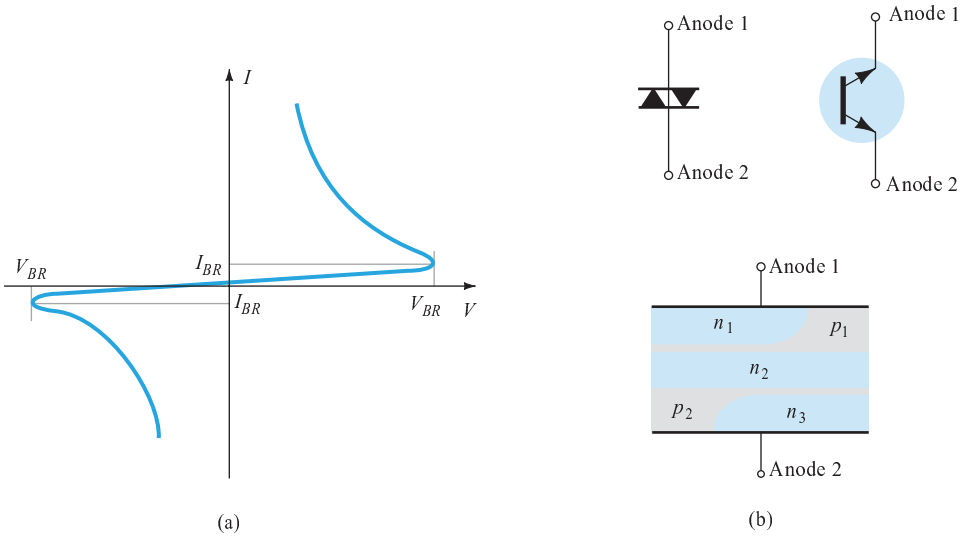


Figure 21.30 Diac: (a) characteristics; (b) symbols and basic construction. (Courtesy General Electric Company.)

direction. This possibility of an *on* condition in either direction can be used to its fullest advantage in ac applications.

The basic arrangement of the semiconductor layers of the diac is shown in Fig. 21.30b, along with its graphical symbol. Note that neither terminal is referred to as the cathode. Instead, there is an anode 1 (or electrode 1) and an anode 2 (or electrode 2). When anode 1 is positive with respect to anode 2, the semiconductor layers of particular interest are $p_1n_2p_2$ and n_3. For anode 2 positive with respect to anode 1, the applicable layers are $p_2n_2p_1$ and n_1.

For the unit appearing in Fig. 21.30, the breakdown voltages are very close in magnitude but may vary from a minimum of 28 V to a maximum of 42 V. They are related by the following equation provided in the specification sheet:

$$V_{BR_1} = V_{BR_2} \pm 0.1V_{BR_2} \tag{21.1}$$

The current levels (I_{BR_1} and I_{BR_2}) are also very close in magnitude for each device. For the unit of Fig. 21.30, both current levels are about 200 μA = 0.2 mA.

The use of the diac in a proximity detector appears in Fig. 21.31. Note the use of an SCR in series with the load and the programmable unijunction transistor (to be described in Section 21.13) connected directly to the sensing electrode.

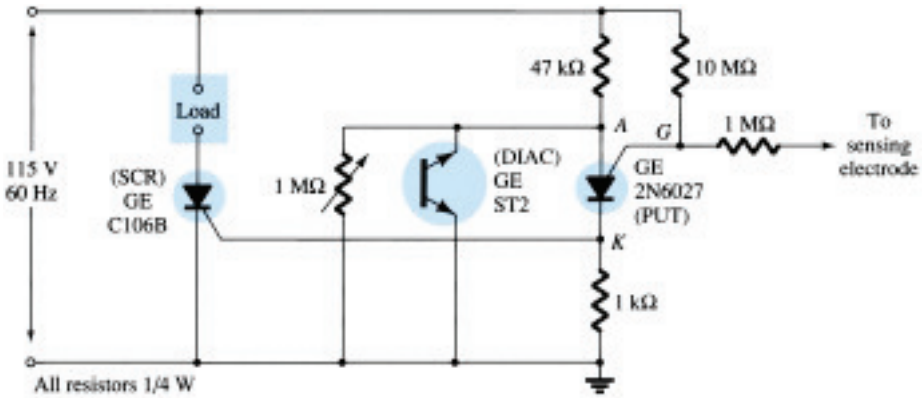


Figure 21.31 Proximity detector or touch switch. (Courtesy Powerex, Inc.)

As the human body approaches the sensing electrode, the capacitance between the electrode and ground will increase. The programmable UJT (PUT) is a device that will fire (enter the short-circuit state) when the anode voltage (V_A) is at least 0.7 V (for silicon) greater than the gate voltage (V_G). Before the programmable device turns on, the system is essentially as shown in Fig. 21.32. As the input voltage rises, the

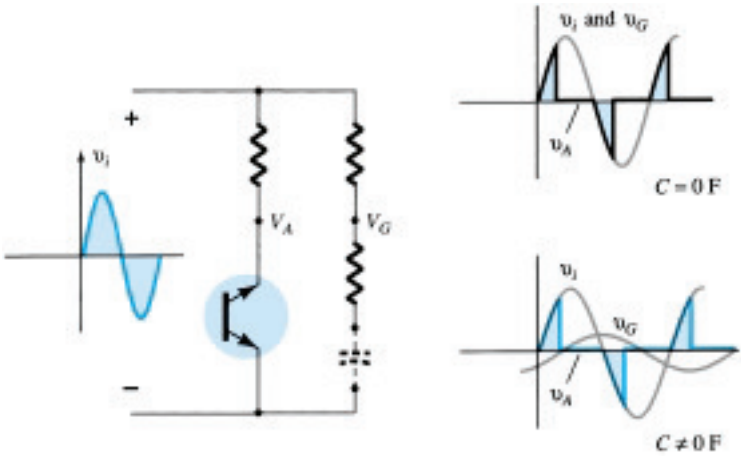


Figure 21.32 Effect of capacitive element on the behavior of the network of Fig. 21.31.

diac voltage V_G will follow as shown in the figure until the firing potential is reached. It will then turn on and the diac voltage will drop substantially, as shown. Note that the diac is in essentially an open-circuit state until it fires. Before the capacitive element is introduced, the voltage V_G will be the same as the input. As indicated in the figure, since both V_A and V_G follow the input, V_A can never be greater than V_G by 0.7 V and turn on the device. However, as the capacitive element is introduced, the voltage V_G will begin to lag the input voltage by an increasing angle, as indicated in the figure. There is therefore a point established where V_A can exceed V_G by 0.7 V and cause the programmable device to fire. A heavy current is established through the PUT at this point, raising the voltage V_K and turning on the SCR. A heavy SCR current will then exist through the load, reacting to the presence of the approaching person.

A second application of the diac appears in the next section (Fig. 21.34) as we consider an important power-control device: the triac.

21.12 TRIAC

The triac is fundamentally a diac with a gate terminal for controlling the turn-on conditions of the bilateral device in either direction. In other words, for either direction the gate current can control the action of the device in a manner very similar to that demonstrated for an SCR. The characteristics, however, of the triac in the first and third quadrants are somewhat different from those of the diac, as shown in Fig. 21.33c. Note the holding current in each direction not present in the characteristics of the diac.

The graphical symbol for the device and the distribution of the semiconductor layers are provided in Fig. 21.33 with photographs of the device. For each possible direction of conduction, there is a combination of semiconductor layers whose state will be controlled by the signal applied to the gate terminal.

One fundamental application of the triac is presented in Fig. 21.34. In this capacity, it is controlling the ac power to the load by switching on and off during the positive and negative regions of input sinusoidal signal. The action of this circuit during the positive portion of the input signal is very similar to that encountered for the Shockley diode in Fig. 21.29. The advantage of this configuration is that during the negative portion of the input signal, the same type of response will result since both the diac and triac can fire in the reverse direction. The resulting waveform for the current through the load is provided in Fig. 21.34. By varying the resistor R, the conduction angle can be controlled. There are units available today that can handle in excess of 10-kW loads.

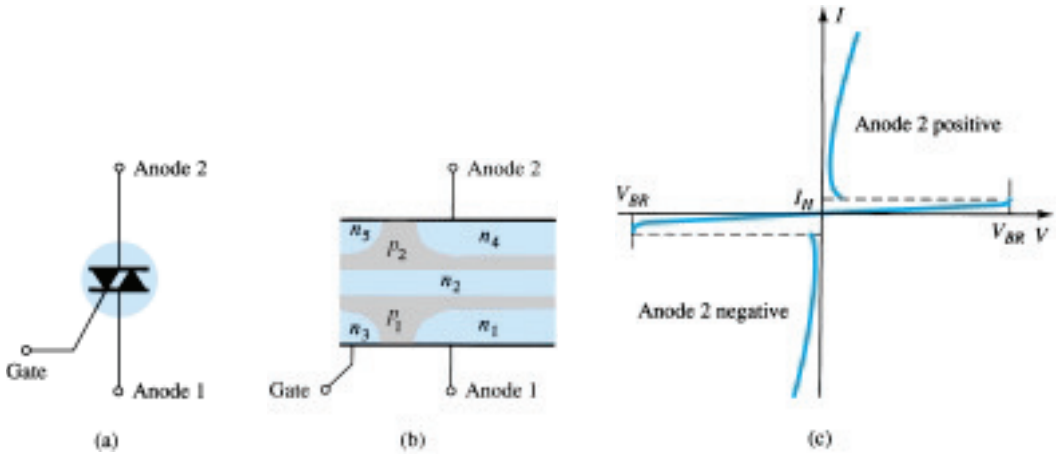


Figure 21.33 Triac: (a) symbol; (b) basic construction; (c) characteristics; (d) photographs.

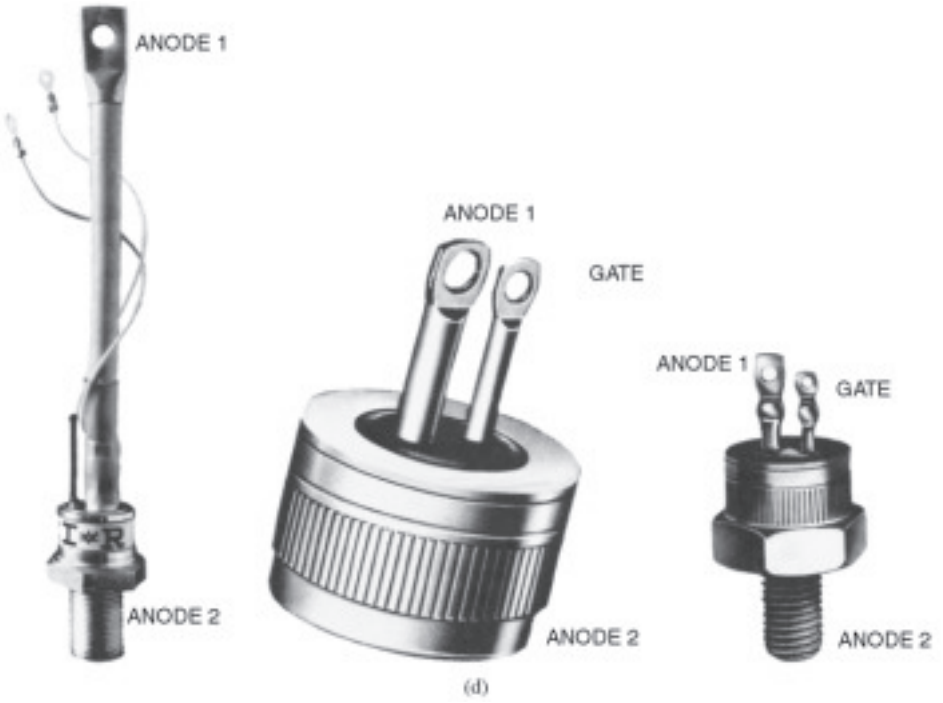


Figure 21.33 Continued

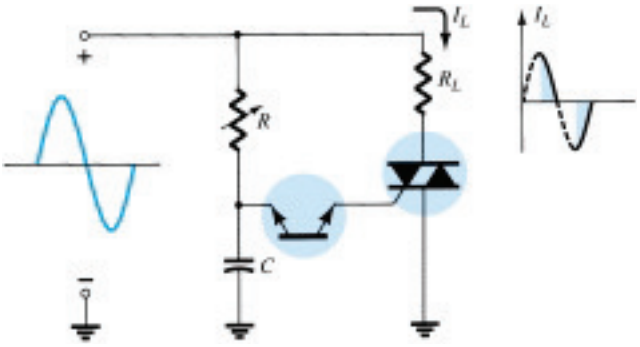
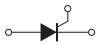


Figure 21.34 Triac application: phase (power) control.

OTHER DEVICES

21.13 UNIJUNCTION TRANSISTOR

Recent interest in the unijunction transistor (UJT) has, like that for the SCR, been increasing at an exponential rate. Although first introduced in 1948, the device did not become commercially available until 1952. The low cost per unit combined with the excellent characteristics of the device have warranted its use in a wide variety of applications. A few include oscillators, trigger circuits, sawtooth generators, phase control, timing circuits, bistable networks, and voltage- or current-regulated supplies. The fact that this device is, in general, a low-power-absorbing device under normal operating conditions is a tremendous aid in the continual effort to design relatively efficient systems.



The UJT is a three-terminal device having the basic construction of Fig. 21.35. A slab of lightly doped (increased resistance characteristic) *n*-type silicon material has two base contacts attached to both ends of one surface and an aluminum rod alloyed to the opposite surface. The *p*-*n* junction of the device is formed at the boundary of the aluminum rod and the *n*-type silicon slab. The single *p*-*n* junction accounts for the terminology *unijunction*. It was originally called a duo (double) base diode due to the presence of two base contacts. Note in Fig. 21.35 that the aluminum rod is alloyed to the silicon slab at a point closer to the base 2 contact than the base 1 contact and that the base 2 terminal is made positive with respect to the base 1 terminal by V_{BB} volts. The effect of each will become evident in the paragraphs to follow.

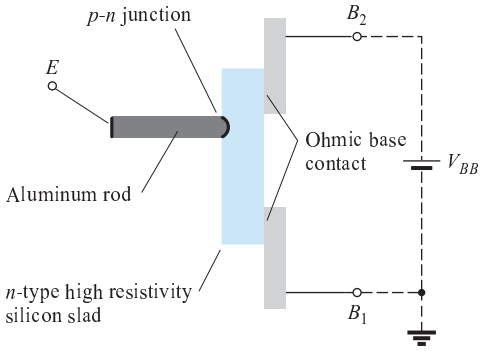


Figure 21.35 Unijunction transistor (UJT): basic construction.

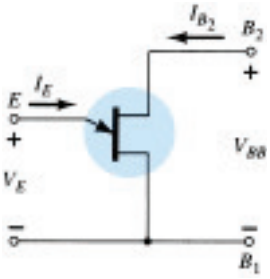


Figure 21.36 Symbol and basic biasing arrangement for the unijunction transistor.

The symbol for the unijunction transistor is provided in Fig. 21.36. Note that the emitter leg is drawn at an angle to the vertical line representing the slab of *n*-type material. The arrowhead is pointing in the direction of conventional current (hole) flow when the device is in the forward-biased, active, or conducting state.

The circuit equivalent of the UJT is shown in Fig. 21.37. Note the relative simplicity of this equivalent circuit: two resistors (one fixed, one variable) and a single diode. The resistance R_{B_1} is shown as a variable resistor since its magnitude will vary with the current I_E. In fact, for a representative unijunction transistor, R_{B_1} may vary from 5 kΩ down to 50 Ω for a corresponding change of I_E from 0 to 50 μA. The interbase resistance R_{BB} is the resistance of the device between terminals B_1 and B_2 when $I_E = 0$. In equation form,

$$R_{BB} = (R_{B_1} + R_{B_2})|_{I_E} = 0 \tag{21.2}$$

(R_{BB} is typically within the range of 4 to 10 kΩ.) The position of the aluminum rod of Fig. 21.35 will determine the relative values of R_{B_1} and R_{B_2} with $I_E = 0$. The magnitude of $V_{R_{B_1}}$ (with $I_E = 0$) is determined by the voltage-divider rule in the following manner:

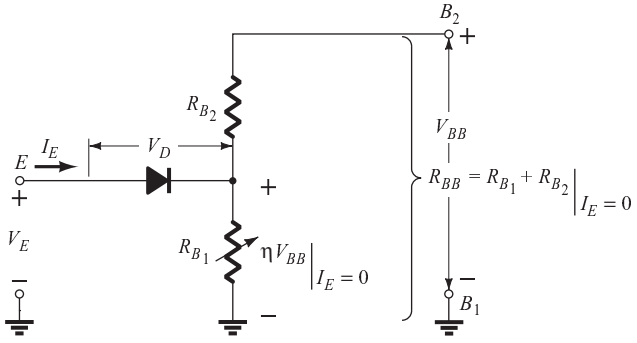


Figure 21.37 UJT equivalent circuit.

$$V_{R_{B_1}} = \frac{R_{B_1} V_{BB}}{R_{B_1} + R_{B_2}} = \eta V_{BB}\Big|_{I_E=0} \tag{21.3}$$

The Greek letter η (eta) is called the *intrinsic stand-off* ratio of the device and is defined by

$$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}\Big|_{I_E=0} = \frac{R_{B_1}}{R_{BB}} \tag{21.4}$$

For applied emitter potentials (V_E) greater than $V_{R_{B_1}} (= \eta V_{BB})$ by the forward voltage drop of the diode V_D (0.35 $\rightarrow$ 0.70 V), the diode will fire. Assume the short-circuit representation (on an ideal basis), and I_E will begin to flow through R_{B_1}. In equation form, the emitter firing potential is given by

$$V_P = \eta V_{BB} + V_D \tag{21.5}$$

The characteristics of a representative unijunction transistor are shown for V_{BB} = 10 V in Fig. 21.38. Note that for emitter potentials to the left of the peak point, the magnitude of I_E is never greater than I_{EO} (measured in microamperes). The current I_{EO} corresponds very closely with the reverse leakage current I_{CO} of the conventional bipolar transistor. This region, as indicated in the figure, is called the cutoff region. Once conduction is established at $V_E = V_P$, the emitter potential V_E will drop with increase in I_E. This corresponds exactly with the decreasing resistance R_{B_1} for increasing current I_E, as discussed earlier. This device, therefore, has a *negative resistance* region that is stable enough to be used with a great deal of reliability in the areas of application listed earlier. Eventually, the valley point will be reached, and any further increase in I_E will place the device in the saturation region. In this region, the characteristics approach that of the semiconductor diode in the equivalent circuit of Fig. 21.37.

The decrease in resistance in the active region is due to the holes injected into the *n*-type slab from the aluminum *p*-type rod when conduction is established. The increased hole content in the *n*-type material will result in an increase in the number of free electrons in the slab, producing an increase in conductivity (G) and a corresponding

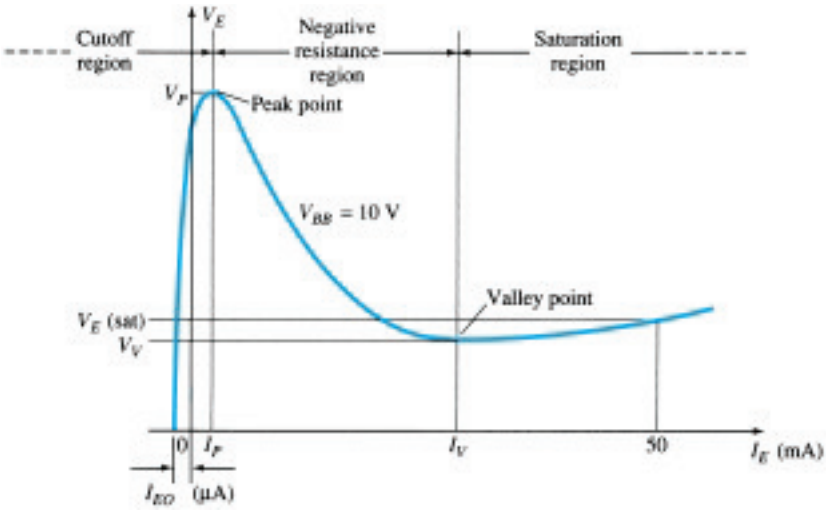


Figure 21.38 UJT static emitter-characteristic curve.

drop in resistance ($R \downarrow = 1/G \uparrow$). Three other important parameters for the unijunction transistor are I_P, V_V, and I_V. Each is indicated on Fig. 21.38. They are all self-explanatory.

The emitter characteristics as they normally appear are provided in Fig. 21.39. Note that I_{EO} (μA) is not in evidence since the horizontal scale is in milliamperes. The intersection of each curve with the vertical axis is the corresponding value of V_P. For fixed values of η and V_D, the magnitude of V_P will vary as V_{BB}, that is,

$$V_P \uparrow = \eta V_{BB} \uparrow + V_D$$

(fixed)

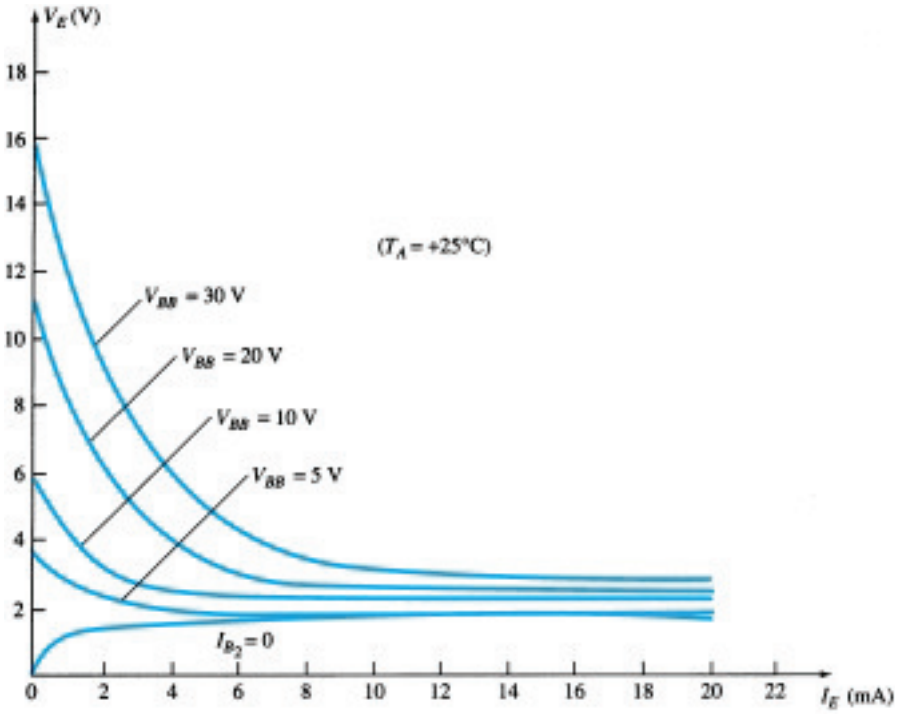


Figure 21.39 Typical static emitter-characteristic curves for a UJT.

A typical set of specifications for the UJT is provided in Fig. 21.40b. The discussion of the last few paragraphs should make each quantity readily recognizable. The terminal identification is provided in the same figure with a photograph of a representative UJT. Note that the base terminals are opposite each other while the emitter terminal is between the two. In addition, the base terminal to be tied to the higher potential is closer to the extension on the lip of the casing.

One rather common application of the UJT is in the triggering of other devices such as the SCR. The basic elements of such a triggering circuit are shown in Fig. 21.41. The resistor R_1 must be chosen to ensure that the load line determined by R_1 passes through the device characteristics in the negative resistance region, that is, to the right of the peak point but to the left of the valley point as shown in Fig. 21.42. If the load line fails to pass to the right of the peak point, the device cannot turn on. An equation for R_1 that will ensure a turn-on condition can be established if we consider the peak point at which $I_{R_1} = I_P$ and $V_E = V_P$. (The equality $I_{R_1} = I_P$ is valid since the charging current of the capacitor, at this instant, is zero. That is, the capacitor is at this particular instant changing from a charging to a discharging state.) Then

Absolute maximum ratings (25°C):

Power dissipation	300 mW
RMS emitter current	50 mA
Peak emitter current	2 A
Emitter reverse voltage	30 V
Interbase voltage	35 V
Operating temperature range	−65°C to +125°C
Storage temperature range	−65°C to +150°C

Electrical characteristics (25°C):

		Min.	Typ.	Max.
Intrinsic standoff ratio		0.56	0.65	
(V_{BB} = 10 V)	η	0.56	0.65	0.75
Interbase resistance (kΩ)				
(V_{BB} = 3 V, I_E = 0)	R_{BB}	4.7	7	9.1
Emitter saturation voltage				
(V_{BB} = 10 V, I_E = 50 mA)	$V_{E(sat)}$		2	
Emitter reverse current				
(V_{BB} = 3 V, I_{B1} = 0)	I_{EO}		0.05	12
Peak point emitter current	I_P (μA)		0.04	5
(V_{BB} = 25 V)				
Valley point current				
(V_{BB} = 20 V)	I_V (mA)	4	6	

(a) (b) (c)

Figure 21.40 UJT: (a) appearance; (b) specification sheet; (c) terminal identification. (Courtesy General Electric Company.)

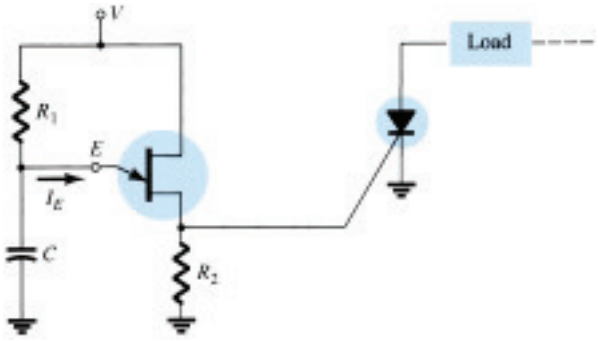


Figure 21.41 UJT triggering of an SCR.

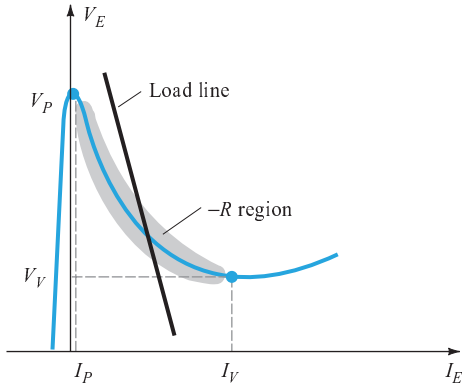


Figure 21.42 Load line for a triggering application.

$V - I_{R_1}R_1 = V_E$ and $R_1 = (V - V_E)/I_{R_1} = (V - V_P)/I_P$ at the peak point. To ensure firing,

$$R_1 < \frac{V - V_P}{I_P} \tag{21.6}$$

At the valley point $I_E = I_V$ and $V_E = V_V$, so that

$$V - I_{R_1}R_1 = V_E$$

becomes

$$V - I_V R_1 = V_V$$

and

$$R_1 = \frac{V - V_V}{I_V}$$

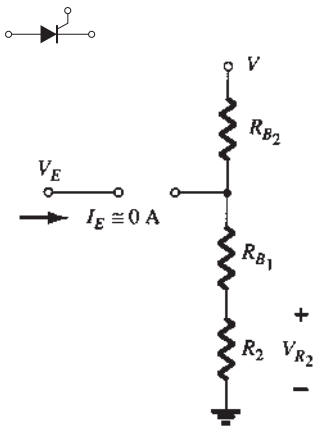


Figure 21.43 Triggering network when $I_E \cong 0$ A.

or to ensure turning off,

$$R_1 > \frac{V - V_V}{I_V} \tag{21.7}$$

The range of R_1 is therefore limited by

$$\frac{V - V_V}{I_V} < R_1 < \frac{V - V_P}{I_P} \tag{21.8}$$

The resistance R_2 must be chosen small enough to ensure that the SCR is not turned on by the voltage V_{R_2} of Fig. 21.43 when $I_E \cong 0$ A. The voltage V_{R_2} is then given by:

$$V_{R_2} \cong \left.\frac{R_2 V}{R_2 + R_{BB}}\right|_{IE \cong 0 \text{ A}} \tag{21.9}$$

The capacitor C will determine, as we shall see, the time interval between triggering pulses and the time span of each pulse.

At the instant the dc supply voltage V is applied, the voltage $v_E = v_C$ will charge toward V volts from V_V as shown in Fig. 21.44 with a time constant $\tau = R_1 C$.

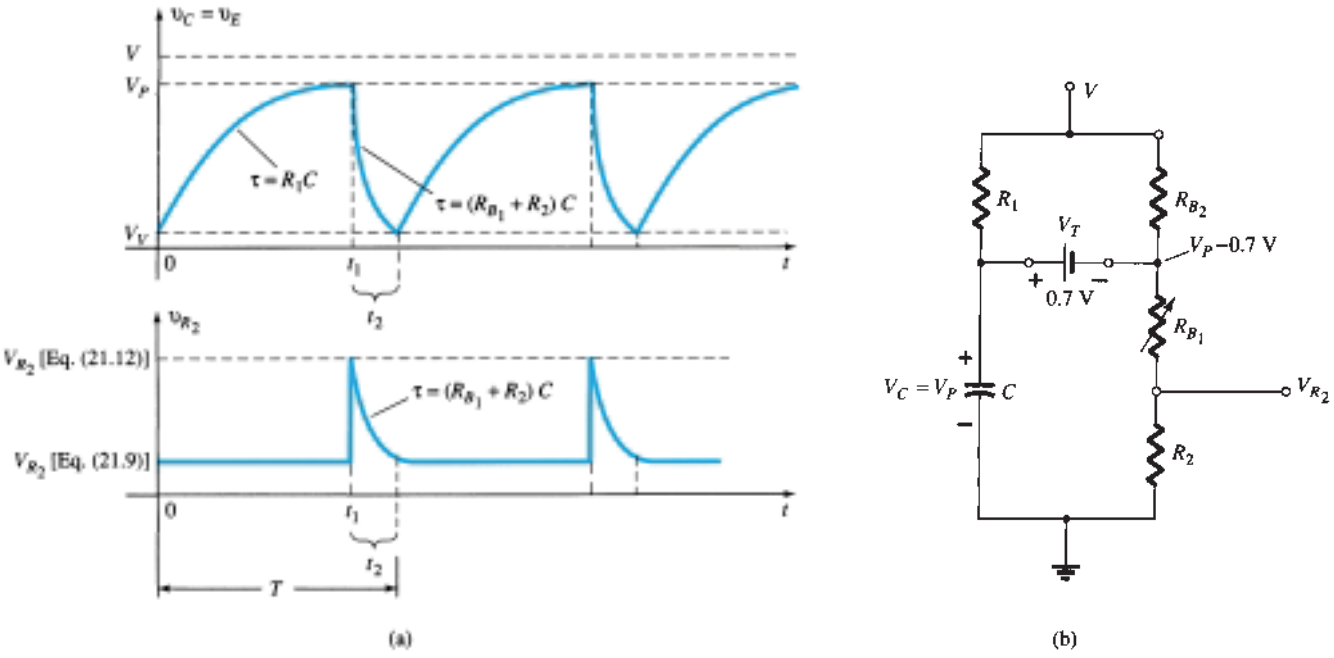


Figure 21.44 (a) Charging and discharging phases for trigger network of Fig. 21.41; (b) equivalent network when UJT turns on.

The general equation for the charging period is

$$v_C = V_V + (V - V_V)(1 - e^{-t/R_1 C}) \tag{21.10}$$

As noted in Fig. 21.44, the voltage across R_2 is determined by Eq. (21.9) during this charging period. When $v_C = v_E = V_P$, the UJT will enter the conduction state and the capacitor will discharge through R_{B_1} and R_2 at a rate determined by the time constant $\tau = (R_{B_1} + R_2)C$.

The discharge equation for the voltage $v_C = v_E$ is the following:

$$v_C \cong V_P e^{-t/(R_{B_1} + R_2)C} \tag{21.11}$$

Equation (21.11) is complicated somewhat by the fact that R_{B_1} will decrease with increasing emitter current and the other elements of the network, such as R_1 and V, will affect the discharge rate and final level. However, the equivalent network appears as shown in Fig. 21.44 and the magnitudes of R_1 and R_{B_2} are typically such that a Thévenin network for the network surrounding the capacitor C will be only slightly affected by these two resistors. Even though V is a reasonably high voltage, the voltage-divider contribution to the Thévenin voltage can be ignored on an approximate basis.

Using the reduced equivalent of Fig. 21.45 for the discharge phase will result in the following approximation for the peak value of V_{R_2}:

$$V_{R_2} \cong \frac{R_2(V_P - 0.7)}{R_2 + R_{B_1}} \tag{21.12}$$

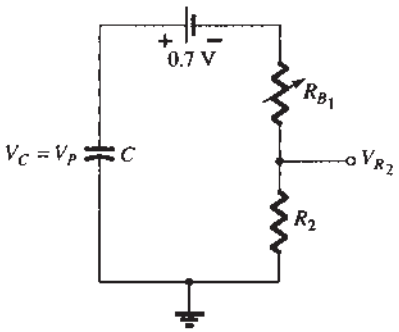


Figure 21.45 Reduced equivalent network when UJT turns on.

The period t_1 of Fig. 21.44 can be determined in the following manner:

$$\begin{aligned} v_C\,(\text{charging}) &= V_V + (V - V_V)(1 - e^{-t/R_1C}) \\ &= V_V + V - V_V - (V - V_V)e^{-t/R_1C} \\ &= V - (V - V_V)e^{-t/R_1C} \end{aligned}$$

when $v_C = V_P$, $t = t_1$, and $V_P = V - (V - V_V)e^{-t_1/R_1C}$, or

$$\frac{V_P - V}{V - V_V} = -e^{-t_1/R_1C}$$

and

$$e^{-t_1/R_1C} = \frac{V - V_P}{V - V_V}$$

Using logs, we have

$$\log_e e^{-t_1/R_1C} = \log_e \frac{V - V_P}{V - V_V}$$

and

$$\frac{-t_1}{R_1C} = \log_e \frac{V - V_P}{V - V_V}$$

with

$$t_1 = R_1C \log_e \frac{V - V_V}{V - V_P} \tag{21.13}$$

For the discharge period the time between t_1 and t_2 can be determined from Eq. (21.11) as follows:

$$v_C\,(\text{discharging}) = V_P\, e^{-t/(R_{B_1}+R_2)C}$$

Establishing t_1 as $t = 0$ gives us

$$v_C = V_V \text{ at } t = t_2$$

and

$$V_V = V_P e^{-t_2/(R_{B_1} + R_2)C}$$

or

$$e^{-t_2/(R_{B_1} + R_2)C} = \frac{V_V}{V_P}$$

Using logs yields

$$\frac{-t_2}{(R_{B_1} + R_2)C} = \log_e \frac{V_V}{V_P}$$

and

$$\boxed{t_2 = (R_{B_1} + R_2)C \log_e \frac{V_P}{V_V}} \tag{21.14}$$

The period of time to complete one cycle is defined by T in Fig. 21.44. That is,

$$\boxed{T = t_1 + t_2} \tag{21.15}$$

If the SCR were dropped from the configuration, the network would behave as a *relaxation oscillator,* generating the waveform of Fig. 21.44. The frequency of oscillation is determined by

$$\boxed{f_{\text{osc}} = \frac{1}{T}} \tag{21.16}$$

In many systems, $t_1 \gg t_2$ and

$$T \cong t_1 = R_1 C \log_e \frac{V - V_V}{V - V_P}$$

Since $V \gg V_V$ in many instances,

$$T \cong t_1 = R_1 C \log_e \frac{V}{V - V_P}$$

$$= R_1 C \log_e \frac{1}{1 - V_P/V}$$

but $\eta = V_P/V$ if we ignore the effects of V_D in Eq. (21.5) and

$$T \cong R_1 C \log_e \frac{1}{1 - \eta}$$

or

$$\boxed{f \cong \frac{1}{R_1 C \log_e [1/(1 - \eta)]}} \tag{21.17}$$

EXAMPLE 21.2

Given the relaxation oscillator of Fig. 21.46:

(a) Determine R_{B_1} and R_{B_2} at $I_E = 0$ A.

(b) Calculate V_P, the voltage necessary to turn on the UJT.

(c) Determine whether R_1 is within the permissible range of values as determined by Eq. (21.8) to ensure firing of the UJT.

(d) Determine the frequency of oscillation if $R_{B_1} = 100\ \Omega$ during the discharge phase.

(e) Sketch the waveform of v_C for a full cycle.

(f) Sketch the waveform of v_{R_2} for a full cycle.

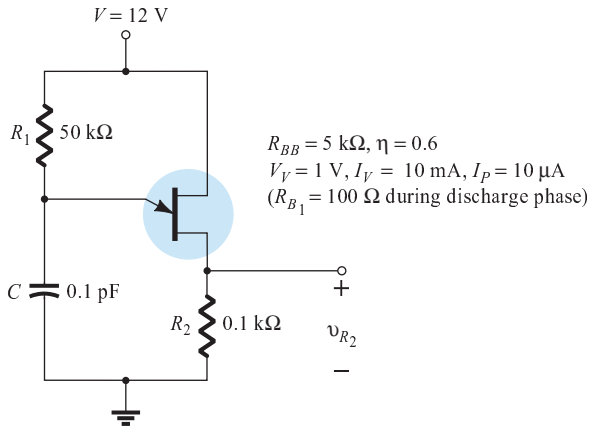


Figure 21.46 Example 21.1

Solution

(a) $\eta = \dfrac{R_{B_1}}{R_{B_1} + R_{B_2}}$

$$0.6 = \frac{R_{B_1}}{R_{BB}}$$

$$R_{B_1} = 0.6R_{BB} = 0.6(5\ \text{k}\Omega) = \mathbf{3\ k\Omega}$$

$$R_{B_2} = R_{BB} - R_{B_1} = 5\ \text{k}\Omega - 3\ \text{k}\Omega = \mathbf{2\ k\Omega}$$

(b) At the point where $v_C = V_P$, if we continue with $I_E = 0$ A, the network of Fig. 21.47 will result, where

$$V_P = 0.7\ \text{V} + \underbrace{\frac{(R_{B_1} + R_2)12\ \text{V}}{R_{B_1} + R_{B_2}}}_{R_{BB}} + R_2$$

$$= 0.7\ \text{V} + \frac{(3\ \text{k}\Omega + 0.1\ \text{k}\Omega)12\ \text{V}}{5\ \text{k}\Omega + 0.1\ \text{k}\Omega} = 0.7\ \text{V} + 7.294\ \text{V}$$

$$\cong \mathbf{8\ V}$$

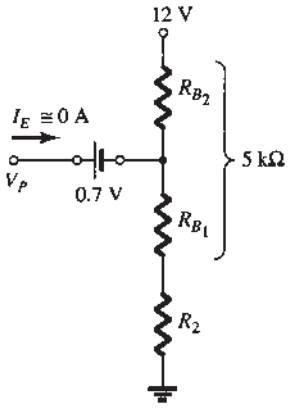


Figure 21.47 Network to determine V_P, the voltage required to turn on the UJT.

(c) $$\frac{V - V_V}{I_V} < R_1 < \frac{V - V_P}{I_P}$$

$$\frac{12\ \text{V} - 1\ \text{V}}{10\ \text{mA}} < R_1 < \frac{12\ \text{V} - 8\ \text{V}}{10\ \mu\text{A}}$$

$$1.1\ \text{k}\Omega < R_1 < 400\ \text{k}\Omega$$

The resistance $R_1 = 50\ \text{k}\Omega$ falls within this range.

(d) $$t_1 = R_1 C \log_e \frac{V - V_V}{V - V_P}$$

$$= (50\ \text{k}\Omega)(0.1\ \text{pF}) \log_e \frac{12\ \text{V} - 1\ \text{V}}{12\ \text{V} - 8\ \text{V}}$$

$$= 5 \times 10^{-3} \log_e \frac{11}{4} = 5 \times 10^{-3}(1.01)$$

$$= 5.05\ \text{ms}$$

$$t_2 = (R_{B_1} + R_2)C \log_e \frac{V_P}{V_V}$$
$$= (0.1\ \text{k}\Omega + 0.1\ \text{k}\Omega)(0.1\ \text{pF}) \log_e \frac{8}{1}$$
$$= (0.02 \times 10^{-6})(2.08)$$
$$= 41.6\ \mu\text{s}$$

and
$$T = t_1 + t_2 = 5.05\ \text{ms} + 0.0416\ \text{ms}$$
$$= 5.092\ \text{ms}$$

with
$$f_{\text{osc}} = \frac{1}{T} = \frac{1}{5.092\ \text{ms}} \cong \mathbf{196\ Hz}$$

Using Eq. (21.17) gives us
$$f \cong \frac{1}{R_1 C \log_e [1/(1 - \eta)]}$$
$$= \frac{1}{5 \times 10^{-3} \log_e 2.5}$$
$$= \mathbf{218\ Hz}$$

(e) See Fig. 21.48.

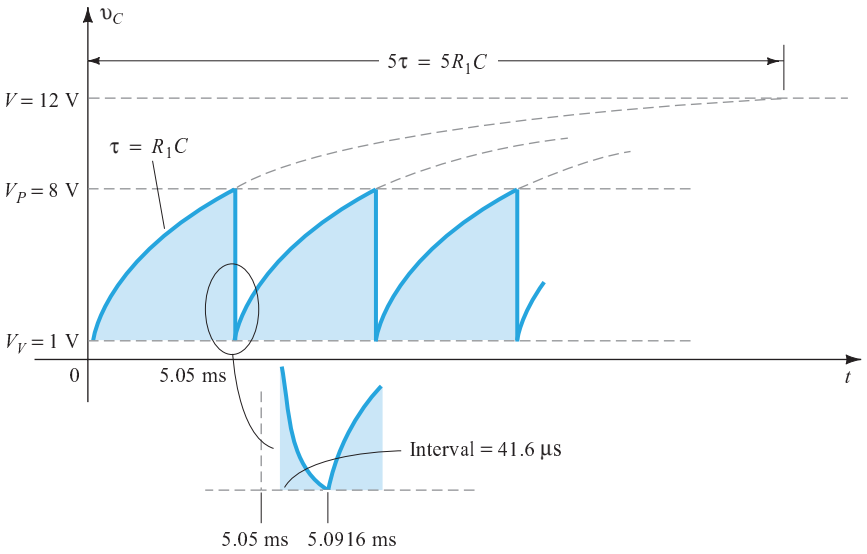


Figure 21.48 The voltage v_C for the relaxation oscillator of Fig. 21.46.

(f) During the charging phase, (Eq. 21.9)
$$V_{R_2} = \frac{R_2 V}{R_2 + R_{BB}} = \frac{0.1\ \text{k}\Omega(12\ \text{V})}{0.1\ \text{k}\Omega + 5\ \text{k}\Omega} = \mathbf{0.235\ V}$$

When $v_C = V_P$ (Eq. 21.12)
$$V_{R_2} \cong \frac{R_2(V_P - 0.7\ \text{V})}{R_2 + R_{B_1}} = \frac{0.1\ \text{k}\Omega(8\ \text{V} - 0.7\ \text{V})}{0.1\ \text{k}\Omega + 0.1\ \text{k}\Omega}$$
$$= \mathbf{3.65\ V}$$

The plot of v_{R_2} appears in Fig. 21.49.

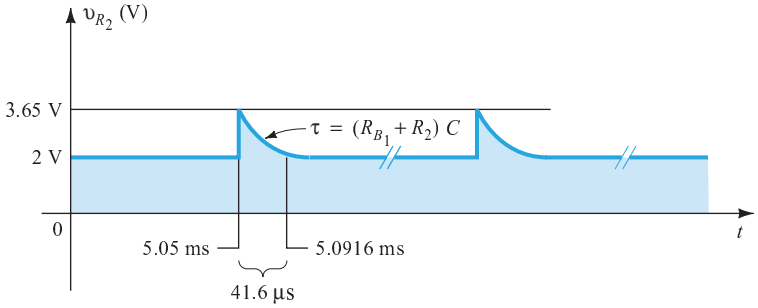


Figure 21.49 The voltage v_{R_2} for the relaxation oscillator of Fig. 21.46.

21.14 PHOTOTRANSISTORS

The fundamental behavior of photoelectric devices was introduced earlier with the description of the photodiode. This discussion will now be extended to include the phototransistor, which has a photosensitive collector–base *p-n* junction. The current induced by photoelectric effects is the base current of the transistor. If we assign the notation I_λ for the photoinduced base current, the resulting collector current, on an approximate basis, is

$$I_C \cong h_{fe}\, I_\lambda \tag{21.18}$$

A representative set of characteristics for a phototransistor is provided in Fig. 21.50 with the symbolic representation of the device. Note the similarities between these curves and those of a typical bipolar transistor. As expected, an increase in light intensity corresponds with an increase in collector current. To develop a greater degree of familiarity with the light-intensity unit of measurement, milliwatts per square centimeter, a curve of base current versus flux density appears in Fig. 21.51a. Note the exponential increase in base current with increasing flux density. In the same figure, a sketch of the phototransistor is provided with the terminal identification and the angular alignment.

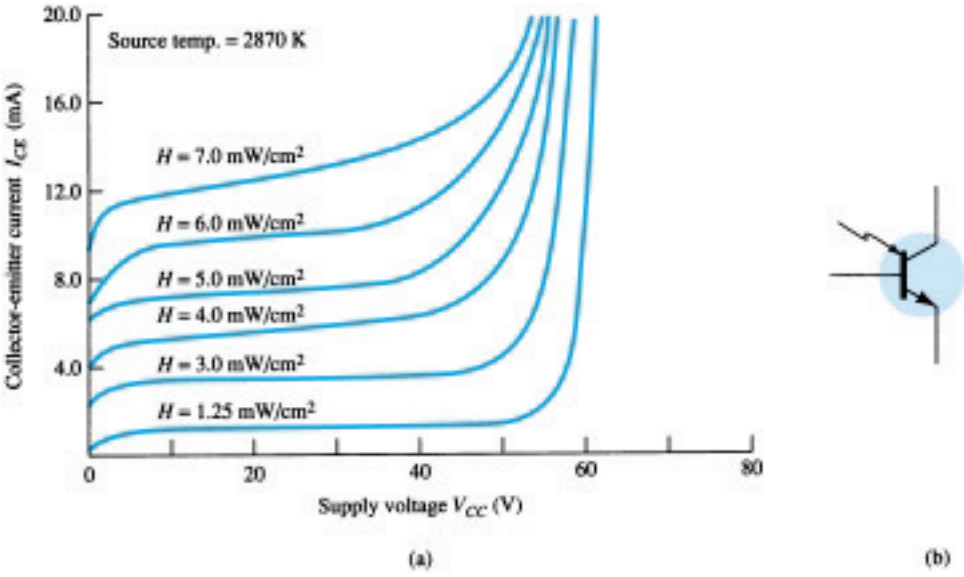


Figure 21.50 Phototransistor: (a) collector characteristics (MRD300); (b) symbol. (Courtesy Motorola, Inc.)

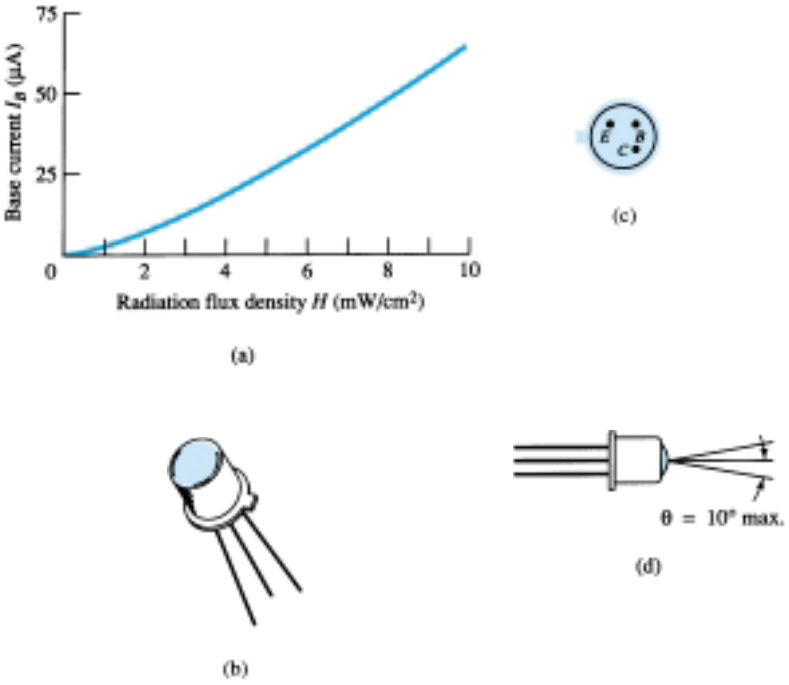


Figure 21.51 Phototransistor: (a) base current versus flux density; (b) device; (c) terminal identification; (d) angular alignment. (Courtesy Motorola, Inc.)

Some of the areas of application for the phototransistor include punch-card readers, computer logic circuitry, lighting control (highways, etc.), level indication, relays, and counting systems.

A high-isolation AND gate is shown in Fig. 21.52 using three phototransistors and three LEDs (light-emitting diodes). The LEDs are semiconductor devices that emit light at an intensity determined by the forward current through the device. With the aid of discussions in Chapter 1, the circuit behavior should be relatively easy to understand. The terminology *high isolation* simply refers to the lack of an electrical connection between the input and output circuits.

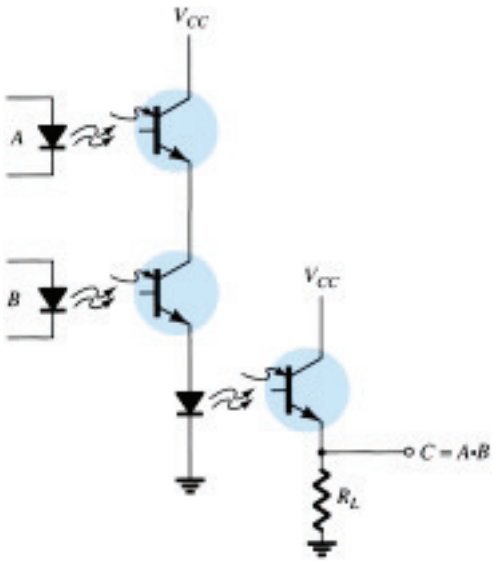


Figure 21.52 High-isolation AND gate employing phototransistors and light-emitting diodes (LEDs).

21.15 OPTO-ISOLATORS

The *opto-isolator* is a device that incorporates many of the characteristics described in the preceding section. It is simply a package that contains both an infrared LED and a photodetector such as a silicon diode, transistor Darlington pair, or SCR. The wavelength response of each device is tailored to be as identical as possible to permit the highest measure of coupling possible. In Fig. 21.53, two possible chip configurations are provided, with a photograph of each. There is a transparent insulating cap between each set of elements embedded in the structure (not visible) to permit the passage of light. They are designed with response times so small that they can be used to transmit data in the megahertz range.

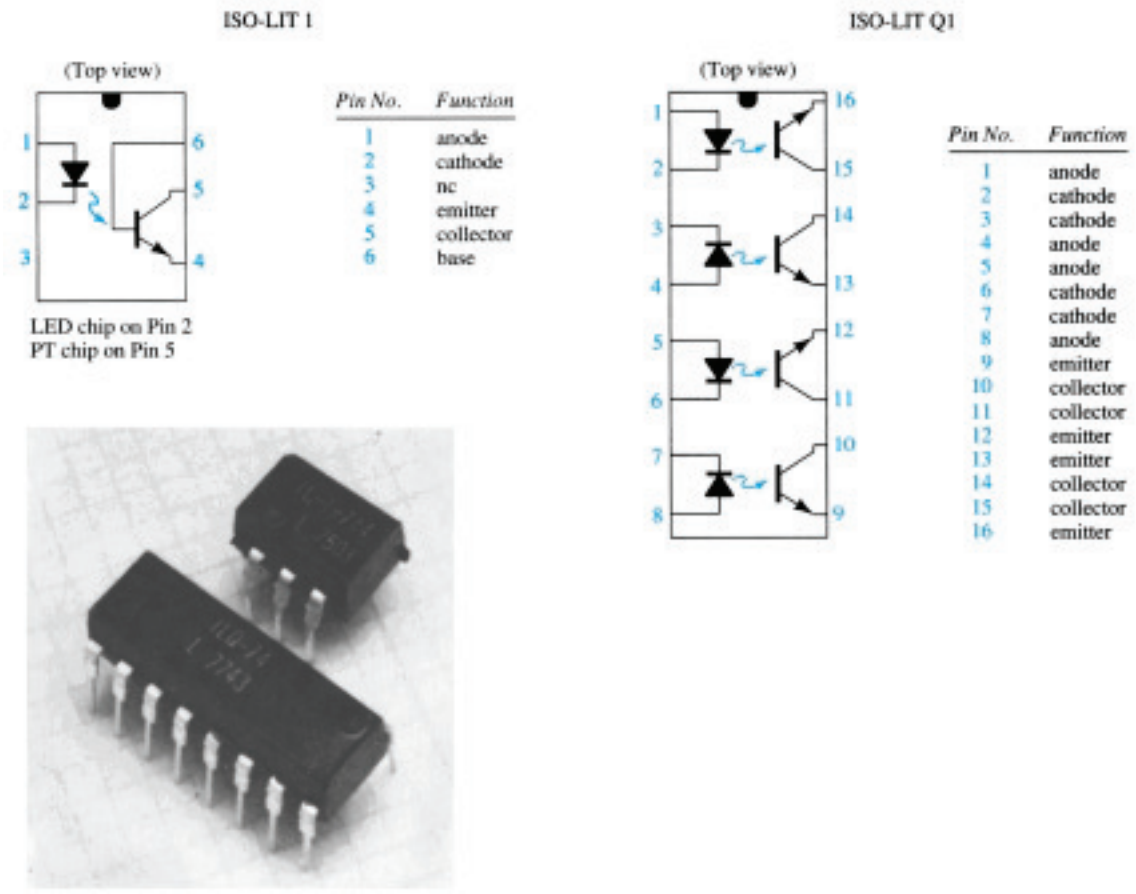
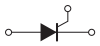


Figure 21.53 Two Litronix opto-isolators. (Courtesy Siemens Components, Inc.)

The maximum ratings and electrical characteristics for the IL-1 model are provided in Fig. 21.54. Note that I_{CEO} is measured in nanoamperes and that the power dissipation of the LED and transistor are about the same.

The typical optoelectronic characteristic curves for each channel are provided in Figs. 21.55 through 21.59. Note the very pronounced effect of temperature on the output current at low temperatures but the fairly level response at or above room temperature (25°C). As mentioned earlier, the level of I_{CEO} is improving steadily with improved design and construction techniques (the lower the better). In Fig. 21.55, we do not reach 1 μA until the temperature rises above 75°C. The transfer characteristics of Fig. 21.56 compare the input LED current (which establishes the luminous



(a) Maximum Ratings

Gallium arsenide LED (each channel) IL-1	
Power dissipation @ 25°C	200 mW
Derate linearly from 25°C	2.6 mW/°C
Continuous forward current	150 mA
Detector silicon phototransistor (each channel) IL-1	
Power dissipation @ 25°C	200 mW
Derate linearly from 25°C	2.6 mW/°C
Collector-emitter breakdown voltage	30 V
Emitter-collector breakdown voltage	7 V
Collector-base breakdown voltage	70 V
Package IL-1	
Total package dissipation at 25°C ambient (LED plus detector)	250 mW
Derate linearly from 25°C	3.3 mW/°C
Storage temperature	−55°C to +150°C
Operating temperature	−55°C to +100°C

(b) Electrical Characteristics per Channel (at 25°C Ambient)

Parameter	*Min.*	*Typ.*	*Max.*	*Unit*	*Test Conditions*
Gallium arsenide LED					
Forward voltage		1.3	1.5	V	$I_F = 60$ mA
Reverse current		0.1	10	µA	$V_R = 3.0$ V
Capacitance		100		pF	$V_R = 0$ V
Phototransistor detector					
BV_{CEO}	30			V	$I_C = 1$ mA
I_{CEO}		5.0	50	nA	$V_{CE} = 10$ V, $I_F = 0$ A
Collector-emitter capacitance		2.0		pF	$V_{CE} = 0$ V
BV_{ECO}	7			V	$I_E = 100$ µA
Coupled characteristics					
dc current transfer ratio	0.2	0.35			$I_F = 10$ mA, $V_{CE} = 10$ V
Capacitance, input to output		0.5		pF	
Breakdown voltage	2500			V	DC
Resistance, input to output		100		GΩ	
V_{sat}			0.5	V	$I_C = 1.6$ mA, $I_F = 16$ mA
Propagation delay					
$t_{D\,on}$		6.0		µs	$R_L = 2.4$ kΩ, $V_{CE} = 5$ V
$t_{D\,off}$		25		µs	$I_F = 16$ mA

Figure 21.54 Litronix IL-1 opto-isolator.

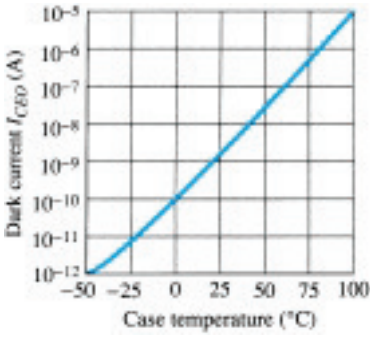


Figure 21.55 Dark current (I_{CEO}) versus temperature.

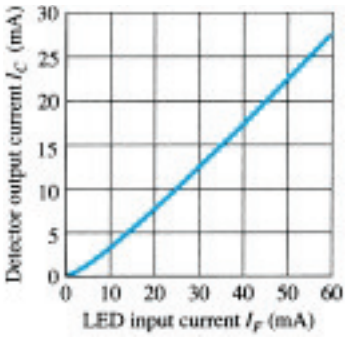


Figure 21.56 Transfer characteristics.

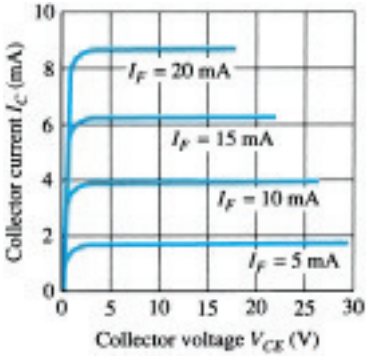


Figure 21.57 Detector output characteristics.

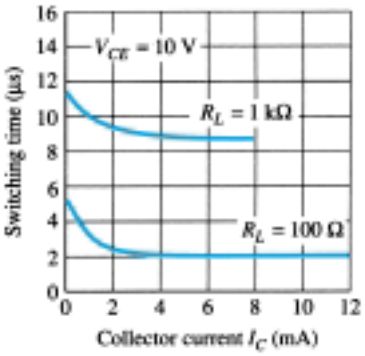


Figure 21.58 Switching time versus collector current.

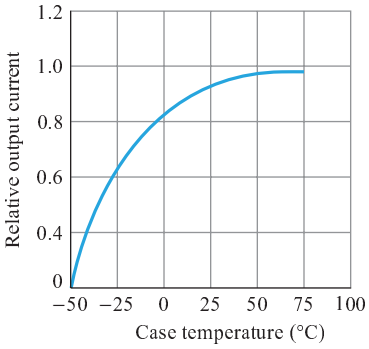


Figure 21.59 Relative output versus temperature.

flux) to the resulting collector current of the output transistor (whose base current is determined by the incident flux). In fact, Fig. 21.57 demonstrates that the V_{CE} voltage affects the resulting collector current only very slightly. It is interesting to note in Fig. 21.58 that the switching time of an opto-isolator decreases with increased current, while for many devices it is exactly the reverse. Consider that it is only 2 μs for a collector current of 6 mA and a load R_L of 100 Ω. The relative output versus temperature appears in Fig. 21.59.

The schematic representation for a transistor coupler appears in Fig. 21.53. The schematic representations for a photodiode, photo-Darlington, and photo-SCR opto-isolator appear in Fig. 21.60.

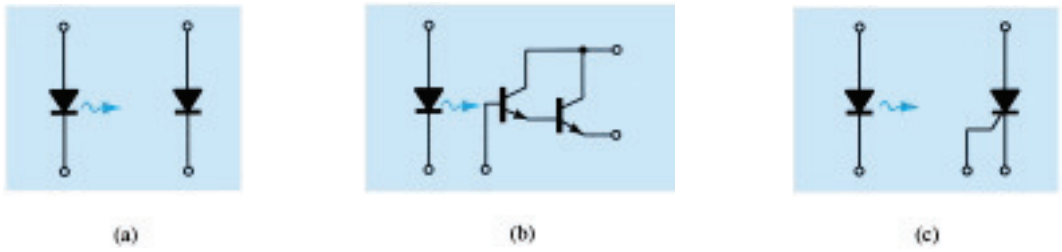


Figure 21.60 Opto-isolators: (a) photodiode; (b) photo-Darlington; (c) photo-SCR.

21.16 PROGRAMMABLE UNIJUNCTION TRANSISTOR

Although there is a similarity in name, the actual construction and mode of operation of the programmable unijunction transistor (PUT) is quite different from the unijunction transistor. The fact that the *I*—*V* characteristics and applications of each are similar prompted the choice of labels.

As indicated in Fig. 21.61, the PUT is a four-layer *pnpn* device with a gate connected directly to the sandwiched *n*-type layer. The symbol for the device and the basic biasing arrangement appears in Fig. 21.62. As the symbol suggests, it is essentially an SCR with a control mechanism that permits a duplication of the characteristics of the typical SCR. The term *programmable* is applied because R_{BB}, η, and V_P as defined for the UJT can be controlled through the resistors R_{B_1}, R_{B_2}, and the supply voltage V_{BB}. Note in Fig. 21.62 that through an application of the voltage-divider rule, when $I_G = 0$:

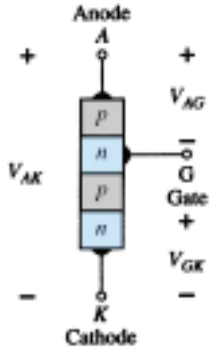


Figure 21.61 Programmable UJT (PUT).

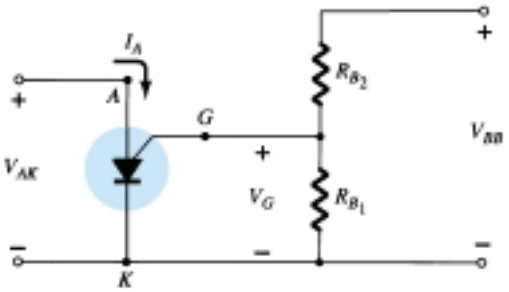


Figure 21.62 Basic biasing arrangement for the PUT.

$$V_G = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} V_{BB} = \eta V_{BB} \tag{21.19}$$

where $$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}$$

as defined for the UJT.

The characteristics of the device appear in Fig. 21.63. As noted on the diagram, the "off" state (I low, V between 0 and V_P) and the"on" state ($I \geq I_V$, $V \geq V_V$) are separated by the unstable region as occurred for the UJT. That is, the device cannot stay in the unstable state—it will simply shift to either the "off" or "on" stable states.

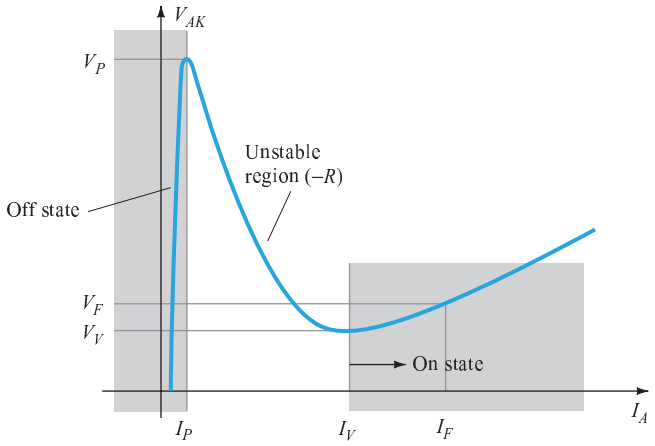


Figure 21.63 PUT characteristics.

The firing potential (V_P) or voltage necessary to "fire" the device is given by

$$V_P = \eta V_{BB} + V_D \tag{21.20}$$

as defined for the UJT. However, V_P represents the voltage drop V_{AK} in Fig. 21.61 (the forward voltage drop across the conducting diode). For silicon, V_D is typically 0.7 V. Therefore,

$$V_{AK} = V_{AG} + V_{GK}$$
$$V_P = V_D + V_G$$

and $$V_P = \eta V_{BB} + 0.7 \text{ V} \quad \text{silicon} \tag{21.21}$$

We noted above, however, that $V_G = \eta V_{BB}$ with the result that

$$\boxed{V_P = V_G + 0.7}_{\text{silicon}} \tag{21.22}$$

Recall that for the UJT both R_{B_1} and R_{B_2} represent the bulk resistance and ohmic base contacts of the device—both inaccessible. In the development above, we note that R_{B_1} and R_{B_2} are external to the device, permitting an adjustment of η and hence V_G above. In other words, the PUT provides a measure of control on the level of V_P required to turn on the device.

Although the characteristics of the PUT and UJT are similar, the peak and valley currents of the PUT are typically lower than those of a similarly rated UJT. In addition, the minimum operating voltage is also less for a PUT.

If we take a Thévenin equivalent of the network to the right of the gate terminal in Fig. 21.62, the network of Fig. 21.64 will result. The resulting resistance R_S is important because it is often included in specification sheets since it affects the level of I_V.

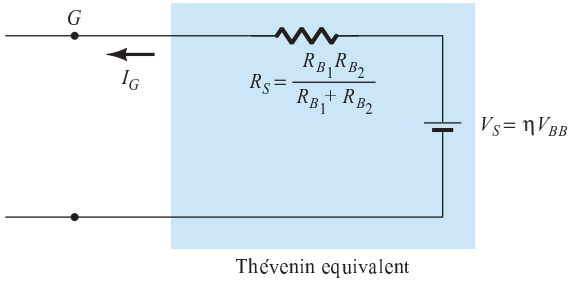


Figure 21.64 Thévenin equivalent for the network to the right of the gate terminal in Fig. 21.62.

The basic operation of the device can be reviewed through reference to Fig. 21.63. A device in the "off" state will not change state until the voltage V_P as defined by V_G and V_D is reached. The level of current until I_P is reached is very low, resulting in an open-circuit equivalent since $R = V$ (high)/I (low) will result in a high resistance level. When V_P is reached, the device will switch through the unstable region to the "on" state, where the voltage is lower but the current higher, resulting in a terminal resistance $R = V$ (low)/I(high), which is quite small, representing short-circuit equivalent on an approximate basis. The device has therefore switched from essentially an open-circuit to a short-circuit state at a point determined by the choice of R_{B_1}, R_{B_2}, and V_{BB}. Once the device is in the "on" state, the removal of V_G will not turn the device off. The level of voltage V_{AK} must be dropped sufficiently to reduce the current below a holding level.

EXAMPLE 21.2

Determine R_{B_1} and V_{BB} for a silicon PUT if it is determined that $\eta = 0.8$, $V_P = 10.3$ V, and $R_{B_2} = 5$ kΩ.

Solution

$$\text{Eq. (21.4): } \eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}} = 0.8$$

$$R_{B_1} = 0.8(R_{B_1} + R_{B_2})$$

$$0.2R_{B_1} = 0.8R_{B_2}$$

$$R_{B_1} = 4R_{B_2}$$

$$R_{B_1} = 4(5\ \text{k}\Omega) = \mathbf{20\ k\Omega}$$

Eq. (21.20): $V_P = \eta V_{BB} + V_D$

$$10.3 \text{ V} = (0.8)(V_{BB}) + 0.7 \text{ V}$$

$$9.6 \text{ V} = 0.8V_{BB}$$

$$V_{BB} = \mathbf{12 \text{ V}}$$

One popular application of the PUT is in the relaxation oscillator of Fig. 21.65. The instant the supply is connected, the capacitor will begin to charge toward V_{BB} volts since there is no anode current at this point. The charging curve appears in Fig. 21.66. The period T required to reach the firing potential V_P is given approximately by

$$T \cong RC\log_e \frac{V_{BB}}{V_{BB} - V_P} \tag{21.23}$$

or when $V_P \cong \eta V_{BB}$

$$T \cong RC\log_e \left(1 + \frac{R_{B_1}}{R_{B_2}}\right) \tag{21.24}$$

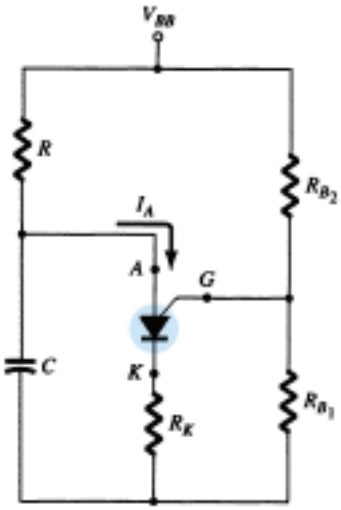


Figure 21.65 PUT relaxation oscillator.

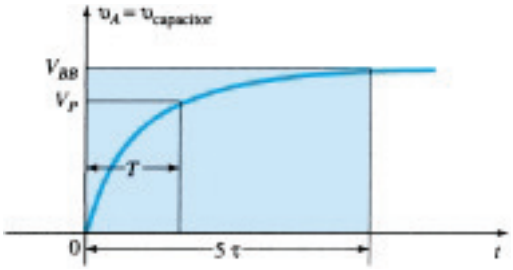


Figure 21.66 Charging wave for the capacitor C of Fig. 21.65.

The instant the voltage across the capacitor equals V_P, the device will fire and a current $I_A = I_P$ will be established through the PUT. If R is too large, the current I_P cannot be established and the device will not fire. At the point of transition,

$$I_P R = V_{BB} - V_P$$

and

$$R_{\max} = \frac{V_{BB} - V_P}{I_P} \tag{21.25}$$

The subscript is included to indicate that any R greater than $R_{\max}$ will result in a current less than I_P. The level of R must also be such to ensure it is less than I_V if oscillations are to occur. In other words, we want the device to enter the unstable region and then return to the "off" state. From reasoning similar to that above:

$$R_{\min} = \frac{V_{BB} - V_V}{I_V} \tag{21.26}$$

The discussion above requires that R be limited to the following for an oscillatory system:

$$R_{\min} < R < R_{\max}$$

The waveforms of v_A, v_G, and v_K appear in Fig. 21.67. Note that T determines the maximum voltage v_A can charge to. Once the device fires, the capacitor will rapidly discharge through the PUT and R_K, producing the drop shown. Of course, v_K will peak at the same time due to the brief but heavy current. The voltage v_G will rapidly drop down from V_G to a level just greater than 0 V. When the capacitor voltage drops to a low level, the PUT will once again turn off and the charging cycle will be repeated. The effect on V_G and V_K is shown in Fig. 21.67.

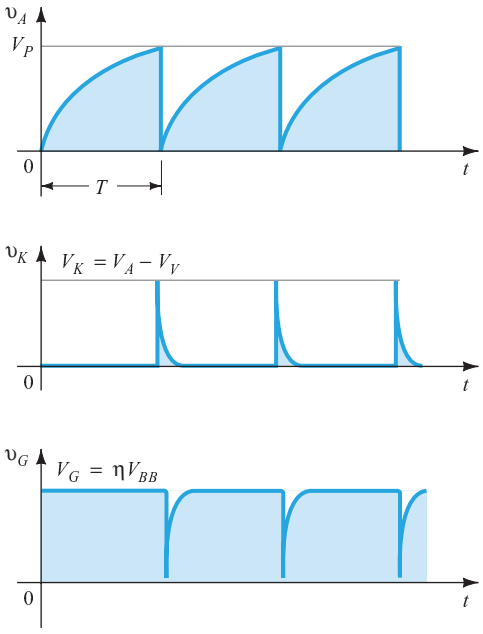


Figure 21.67 Waveforms for PUT oscillator of Fig. 21.65.

EXAMPLE 21.3

If $V_{BB} = 12$ V, $R = 20$ kΩ, $C = 1$ μF, $R_K = 100$ Ω, $R_{B_1} = 10$ kΩ, $R_{B_2} = 5$ kΩ, $I_P = 100$ μA, $V_V = 1$ V, and $I_V = 5.5$ mA, determine:

(a) V_P.
(b) $R_{\max}$ and $R_{\min}$.
(c) T and frequency of oscillation.
(d) The waveforms of v_A, v_G, and v_K.

Solution

(a) Eq. 21.20: $V_P = \eta V_{BB} + V_D$

$$= \frac{R_{B_1}}{R_{B_1} + R_{B_2}} V_{BB} + 0.7 \text{ V}$$

$$= \frac{10 \text{ k}\Omega}{10 \text{ k}\Omega + 5 \text{ k}\Omega} (12 \text{ V}) + 0.7 \text{ V}$$

$$= (0.67)(12 \text{ V}) + 0.7 \text{ V} = \mathbf{8.7 \text{ V}}$$

(b) From Eq. (21.25): $R_{\max} = \dfrac{V_{BB} - V_P}{I_P}$

$$= \frac{12 \text{ V} - 8.7 \text{ V}}{100 \text{ } \mu\text{A}} = \mathbf{33 \text{ k}\Omega}$$

From Eq. (21.26): $R_{\min} = \dfrac{V_{BB} - V_V}{I_V}$

$$= \frac{12\text{ V} - 1\text{ V}}{5.5\text{ mA}} = \mathbf{2\ k\Omega}$$

R: $2\text{ k}\Omega < 20\text{ k}\Omega < 33\text{ k}\Omega$

(c) Eq. (21.23): $T = RC\log_e \dfrac{V_{BB}}{V_{BB} - V_P}$

$$= (20\text{ k}\Omega)(1\ \mu\text{F})\log_e \frac{12\text{ V}}{12\text{ V} - 8.7\text{ V}}$$

$$= 20 \times 10^{-3}\log_e (3.64)$$

$$= 20 \times 10^{-3}(1.29)$$

$$= \mathbf{25.8\ ms}$$

$$f = \frac{1}{T} = \frac{1}{25.8\text{ ms}} = \mathbf{38.8\ Hz}$$

(d) As indicated in Fig. 21.68.

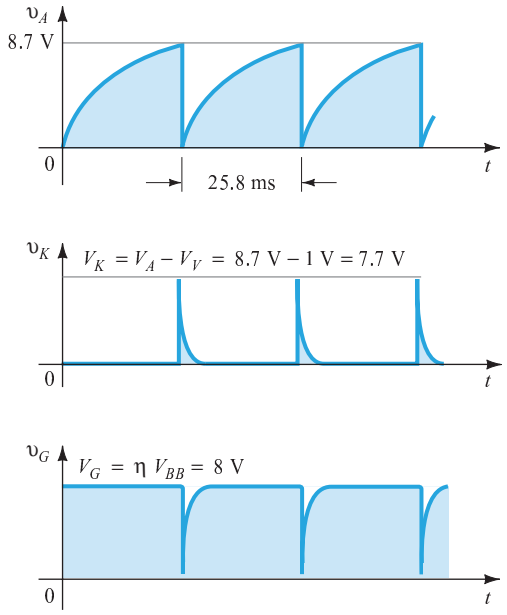


Figure 21.68 Waveforms for the oscillator of Example 21.3.

PROBLEMS

§ 21.3 Basic Silicon-Controlled Rectifier Operation

1. Describe in your own words the basic behavior of the SCR using the two-transistor equivalent circuit.

2. Describe two techniques for turning an SCR off.

3. Consult a manufacturer's manual or specification sheet and obtain a turn-off network. If possible, describe the turn-off action of the design.

§ 21.4 SCR Characteristics and Ratings

* **4.** (a) At high levels of gate current, the characteristics of an SCR approach those of what two-terminal device?

(b) At a fixed anode-to-cathode voltage less than $V_{(BR)F^*}$, what is the effect on the firing of the SCR as the gate current is reduced from its maximum value to the zero level?
(c) At a fixed gate current greater than $I_G = 0$, what is the effect on the firing of the SCR as the gate voltage is reduced from $V_{(BR)F^*}$?
(d) For increasing levels of I_G, what is the effect on the holding current?

5. (a) Using Fig. 21.8, will a gate current of 50 mA fire the device at room temperature (25°C)?
(b) Repeat part (a) for a gate current of 10 mA.
(c) Will a gate voltage of 2.6 V trigger the device at room temperature?
(d) Is $V_G = 6$ V, $I_G = 800$ mA a good choice for firing conditions? Would $V_G = 4$ V, $I_G = 1.6$ A be preferred? Explain.

§ 21.6 SCR Applications

6. In Fig. 21.11b, why is there very little loss in potential across the SCR during conduction?

7. Fully explain why reduced values of R_1 in Fig. 21.12 will result in an increased angle of conduction.

* **8.** Refer to the charging network of Fig. 21.13.
(a) Determine the dc level of the full-wave rectified signal if a 1:1 transformer were employed.
(b) If the battery in its uncharged state is sitting at 11 V, what is the anode-to-cathode voltage drop across SCR_1?
(c) What is the maximum possible value of V_R ($V_{GK} \cong 0.7$ V)?
(d) At the maximum value of part (c), what is the gate potential of SCR_2?
(e) Once SCR_2 has entered the short-circuit state, what is the level of V_2?

§ 21.7 Silicon-Controlled Switch

9. Fully describe in your own words the behavior of the networks of Fig. 21.17.

§ 21.8 Gate Turn-Off Switch

10. (a) In Fig. 21.23, if $V_Z = 50$ V, determine the maximum possible value the capacitor C_1 can charge to ($V_{GK} \cong 0.7$ V).
(b) Determine the approximate discharge time (5τ) for $R_3 = 20$ kΩ.
(c) Determine the internal resistance of the GTO if the rise time is one-half the decay period determined in part (b).

§ 21.9 Light-Activated SCR

11. (a) Using Fig. 21.25b, determine the minimum irradiance required to fire the device at room temperature (25°C).
(b) What percent reduction in irradiance is allowable if the junction temperature is increased from 0°C (32°F) to 100°C (212°F)?

§ 21.10 Shockley Diode

12. For the network of Fig. 21.29, if $V_{BR} = 6$ V, $V = 40$ V, $R = 10$ kΩ, $C = 0.2$ μF, and V_{GK} (firing potential) = 3 V, determine the time period between energizing the network and the turning on of the SCR.

§ 21.11 Diac

13. Using whatever reference you require, find an application of a diac and explain the network behavior.

14. If V_{BR_2} is 6.4 V, determine the range for V_{BR_1} using Eq. (21.1).

§ 21.12 Triac

15. Repeat Problem 13 for the triac.

§ 21.13 Unijunction Transistor

16. For the network of Fig. 21.41, in which $V = 40$ V, $\eta = 0.6$, $V_V = 1$ V, $I_V = 8$ mA, and $I_P = 10\ \mu$A, determine the range of R_1 for the triggering network.

17. For a unijunction transistor with $V_{BB} = 20$ V, $\eta = 0.65$, $R_{B_1} = 2$ kΩ ($I_E = 0$), and $V_D = 0.7$ V, determine:
(a) R_{B_2}.
(b) R_{BB}.
(c) $V_{R_{B_1}}$.
(d) V_P.

* **18.** Given the relaxation oscillator of Fig. 21.69:
(a) Find R_{B_1} and R_{B_2} at $I_E = 0$ A.
(b) Determine V_P, the voltage necessary to turn on the UJT.
(c) Determine whether R_1 is within the permissible range of values defined by Eq. (21.8).
(d) Determine the frequency of oscillation if $R_{B_1} = 200\ \Omega$ during the discharge phase.
(e) Sketch the waveform of v_C for two full cycles.
(f) Sketch the waveform of v_{R_2} for two full cycles.
(g) Determine the frequency using Eq. (21.17) and compare to the value determined in part (d). Account for any major differences.

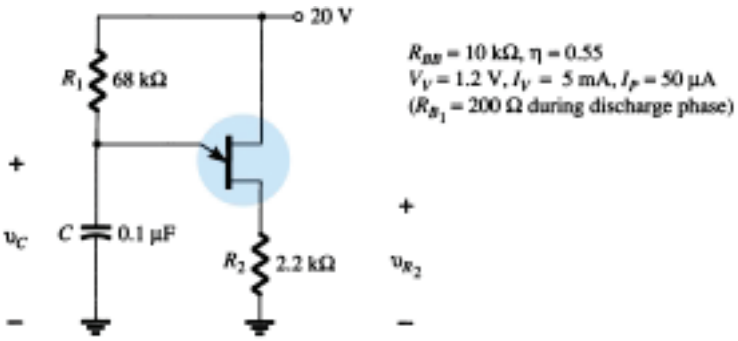


Figure 21.69 Problem 18

§ 21.14 Phototransistors

19. For a phototransistor having the characteristics of Fig. 21.51, determine the photoinduced base current for a radiant flux density of 5 mW/cm^2. If $h_{fe} = 40$, find I_C.

* **20.** Design a high-isolation OR-gate employing phototransistors and LEDs.

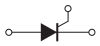
§ 21.15 Opto-Isolators

21. (a) Determine an average derating factor from the curve of Fig. 21.59 for the region defined by temperatures between −25°C and +50°C.
(b) Is it fair to say that for temperatures greater than room temperature (up to 100°C), the output current is somewhat unaffected by temperature?

22. (a) Determine from Fig. 21.55 the average change in I_{CEO} per degree change in temperature for the range 25 to 50°C.
(b) Can the results of part (a) be used to determine the level of I_{CEO} at 35°C? Test your theory.

23. Determine from Fig. 21.56 the ratio of LED output current to detector input current for an output current of 20 mA. Would you consider the device to be relatively efficient in its purpose?

* **24.** (a) Sketch the maximum-power curve of $P_D = 200$ mW on the graph of Fig. 21.57. List any noteworthy conclusions.
(b) Determine β_{dc} (defined by I_C/I_F) for the system at $V_{CE} = 15$ V, $I_F = 10$ mA.
(c) Compare the results of part (b) with those obtained from Fig. 21.56 at $I_F = 10$ mA. Do they compare? Should they? Why?



* **25.** (a) Referring to Fig. 21.58, determine the collector current above which the switching time does not change appreciably for $R_L = 1\ \text{k}\Omega$ and $R_L = 100\ \Omega$.
(b) At $I_C = 6$ mA, how does the ratio of switching times for $R_L = 1\ \text{k}\Omega$ and $R_L = 100\ \Omega$ compare to the ratio of resistance levels?

§ 21.16 Programmable Unijunction Transistor

26. Determine η and V_G for a PUT with $V_{BB} = 20$ V and $R_{B_1} = 3R_{B_2}$.

27. Using the data provided in Example 21.3, determine the impedance of the PUT at the firing and valley points. Are the approximate open- and short-circuit states verified?

28. Can Eq. (21.24) be derived exactly as shown from Eq. (21.23)? If not, what element is missing in Eq. (21.24)?

* **29.** (a) Will the network of Example 21.3 oscillate if V_{BB} is changed to 10 V? What minimum value of V_{BB} is required (V_V a constant)?
(b) Referring to the same example, what value of R would place the network in the stable "on" state and remove the oscillatory response of the system?
(c) What value of R would make the network a 2-ms time-delay network? That is, provide a pulse v_K 2 ms after the supply is turned on and then stay in the "on" state.

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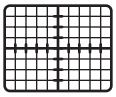
*Please Note: Asterisks indicate more difficult problems.



CHAPTER

22 Oscilloscope and Other Measuring Instruments

22.1 INTRODUCTION

One of the basic functions of electronic circuits is the generation and manipulation of electronic waveshapes. These electronic signals may represent audio information, computer data, television signals, timing signals (as used in radar), and so on. The common meters used in electronic measurement are the multimeter—analog or digital, to enable measuring dc or ac voltages, currents, or impedances. Most meters provide ac measurements that are correct for nondistorted sinusoidal signals only. The oscilloscope, on the other hand, displays the exact waveform, and the viewer can decide what to make of the various readings observed.

The cathode ray oscilloscope (CRO) provides a visual presentation of any waveform applied to the input terminals. A cathode ray tube (CRT), much like a television tube, provides the visual display showing the form of the signal applied as a waveform on the front screen. An electron beam is deflected as it sweeps across the tube face, leaving a display of the signal applied to input terminals.

While multimeters provide numeric information about an applied signal, the oscilloscope allows the actual form of the waveform to be displayed. A wide range of oscilloscopes is available, some suited to measure signals below a specified frequency, others to provide measuring signals of the shortest time span. A CRO may be built to operate from a few hertz up to hundreds of megahertz; CROs may also be used to measure time spans from fractions of a nanosecond (10^{-9}) to many seconds.

22.2 CATHODE RAY TUBE — THEORY AND CONSTRUCTION

The CRT is the "heart" of the CRO, providing visual display of an input signal's waveform. A CRT contains four basic parts:

1. An electron gun to produce a stream of electrons.
2. Focusing and accelerating elements to produce a well-defined beam of electrons.
3. Horizontal and vertical deflecting plates to control the path of the electron beam.
4. An evacuated glass envelope with a phosphorescent screen, which glows visibly when struck by the electron beam.

Figure 22.1 shows the basic construction of a CRT. We will first consider the device's basic operation. A cathode (K) containing an oxide coating is heated indirectly

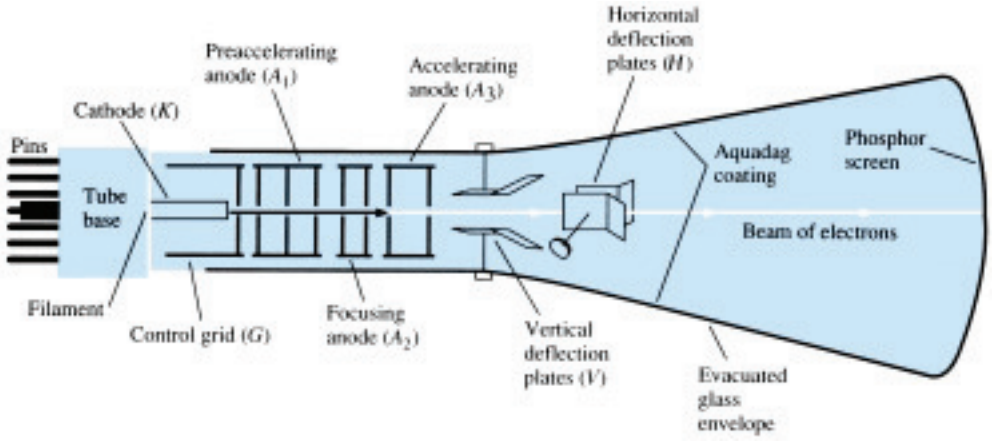


Figure 22.1 Cathode ray tube: basic construction.

by a filament, resulting in the release of electrons from the cathode surface. A control grid (G) provides for control of the number of electrons passing farther into the tube. A voltage on the control grid determines how many of the electrons freed by heating are allowed to continue moving toward the face of the tube. After the electrons pass the control grid, they are focused into a tight beam and accelerated to a higher velocity by the focusing and accelerating anodes. The parts discussed so far comprise the electron gun of the CRT.

The high-velocity, well-defined electron beam then passes through two sets of deflection plates. The first set of plates is oriented to deflect the electron beam vertically, up or down. The direction of the vertical deflection is determined by the voltage polarity applied to the deflecting plates. The amount of deflection is set by the magnitude of the applied voltage. The beam is also deflected horizontally (left or right) by a voltage applied to the horizontal deflecting plates. The deflected beam is then further accelerated by very high voltages applied to the tube, with the beam finally striking a phosphorescent material on the inside face of the tube. This phosphor glows when struck by the energetic electrons—the visible glow seen at the front of the tube by the person using the scope.

The CRT is a self-contained unit with leads brought out through a base to pins. Various types of CRTs are manufactured in a variety of sizes, with different phosphor materials and deflection electrode placement. We can now consider how the CRT is used in an oscilloscope.

22.3 CATHODE RAY OSCILLOSCOPE OPERATION

For operation as an oscilloscope, the electron beam is deflected horizontally by a sweep voltage and vertically by the voltage to be measured. While the electron beam is moved across the face of the CRT by the horizontal sweep signal, the input signal deflects the beam vertically, resulting in a display of the input signal waveform. One sweep of the beam across the face of the tube, followed by a "blank" period during which the beam is turned off while being returned to the starting point across the tube face, constitutes one sweep of the beam.

A steady display is obtained when the beam repeatedly sweeps across the tube with exactly the same image each sweep. This requires a synchronization, starting the sweep at the same point in a repetitive waveform cycle. If the signal is properly synchronized, the display will be stationary. In the absence of sync, the picture will appear to drift or move horizontally across the screen.

Basic Parts of a CRO

The basic parts of a CRO are shown in Fig. 22.2. We will first consider the CRO's operation for this simplified block diagram. To obtain a noticeable beam deflection from a centimeter to a few centimeters, the usual voltage applied to the deflection plates must be on the order of tens to hundreds of volts. Since the signals measured using a CRO are typically only a few volts, or even a few millivolts, amplifier circuits are needed to increase the input signal to the voltage levels required to operate the tube. There are amplifier sections for both the vertical and the horizontal deflection of the beam. To adjust the level of a signal, each input goes through an attenuator circuit, which can adjust the amplitude of the display.

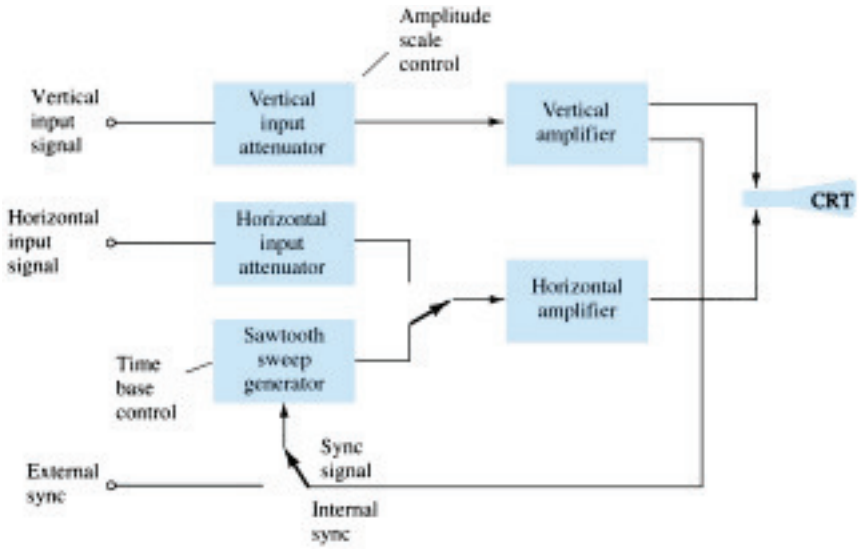


Figure 22.2 Cathode ray oscilloscope: general block diagram.

22.4 VOLTAGE SWEEP OPERATION

When the vertical input is 0 V, the electron beam may be positioned at the vertical center of the screen. If 0 V is also applied to the horizontal input, the beam is then at the center of the CRT face and remains a stationary dot. The vertical and horizontal positioning controls allow moving the dot anywhere on the tube face. Any dc voltage applied to an input will result in shifting the dot. Figure 22.3 shows a CRT face with a centered dot and with a dot moved by a positive horizontal voltage (to the right) and a negative vertical input voltage (down from center).

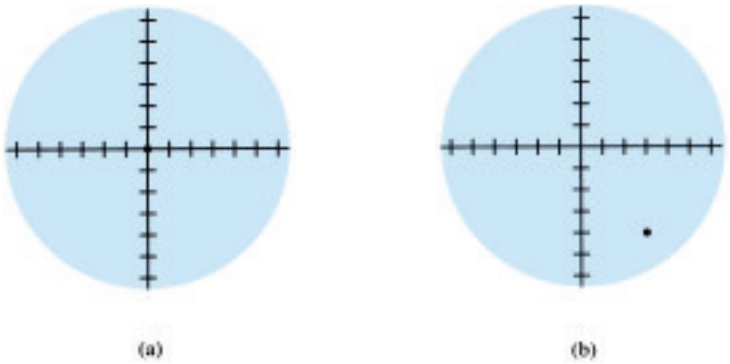


Figure 22.3 Dot on CRT screen due to stationary electron beam: (a) centered dot due to stationary electron beam; (b) off-center stationary dot.

Horizontal Sweep Signal

To view a signal on the CRT face, it is necessary to deflect the beam across the CRT with a horizontal sweep signal so that any variation of the vertical signal can be observed. Figure 22.4 shows the resulting straight-line display for a positive voltage applied to the vertical input using a linear (sawtooth) sweep signal applied to the horizontal channel. With the electron beam held at a constant vertical distance, the horizontal voltage, going from negative to zero to positive voltage, causes the beam to move from the left side of the tube, to the center, to the right side. The resulting display is a straight line above the vertical center with the dc voltage properly displayed as a straight line.

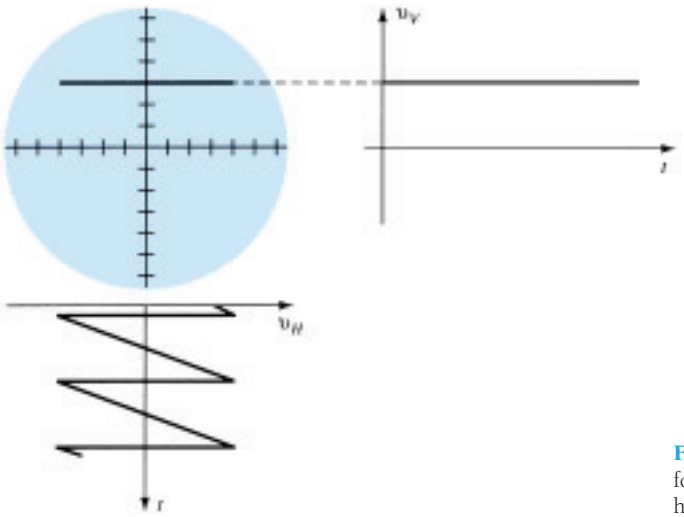


Figure 22.4 Scope display for dc vertical signal and linear horizontal sweep signal.

The sweep voltage is shown to be a continuous waveform, not just a single sweep. This is necessary if a long-term display is to be seen. A single sweep across the tube face would quickly fade out. By repeating the sweep, the display is generated over and over, and if enough sweeps are generated per second, the display appears present continuously. If the sweep rate is slowed down (as set by the time-scale controls of the scope), the actual travel of the beam across the tube face can be observed.

Applying only a sinusoidal signal to the vertical inputs (no horizontal sweep) results in a vertical straight line as shown in Fig. 22.5. If the sweep speed (frequency

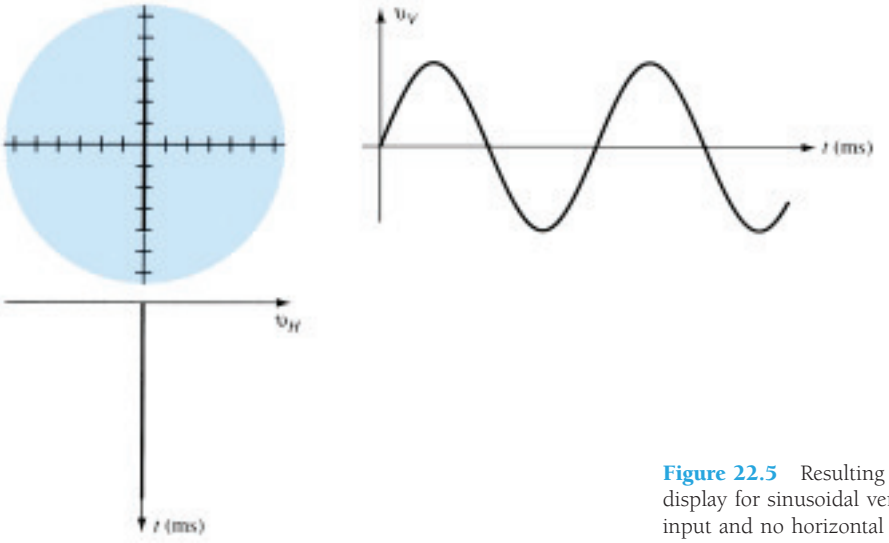


Figure 22.5 Resulting scope display for sinusoidal vertical input and no horizontal input.

of the sinusoidal signal) is reduced, it is possible to see the electron beam moving up and down along a straight-line path.

Use of Linear Sawtooth Sweep to Display Vertical Input

To view a sinusoidal signal, it is necessary to use a sweep signal on the horizontal channel so that the signal applied to the vertical channel can be seen on the tube face. Figure 22.6 shows the resulting CRO display from a horizontal linear sweep and a sinusoidal input to the vertical channel. For one cycle of the input signal to appear as shown in Fig. 22.6a, it is necessary that the signal and linear sweep frequencies be synchronized. If there is any difference, the display will appear to move (not be synchronized) unless the sweep frequency is some multiple of the sinusoidal frequency. Lowering the sweep frequency allows more cycles of the sinusoidal signal to be displayed, whereas increasing the sweep frequency results in less of the sinusoidal vertical input to be displayed, thereby appearing as a magnification of a part of the input signal.

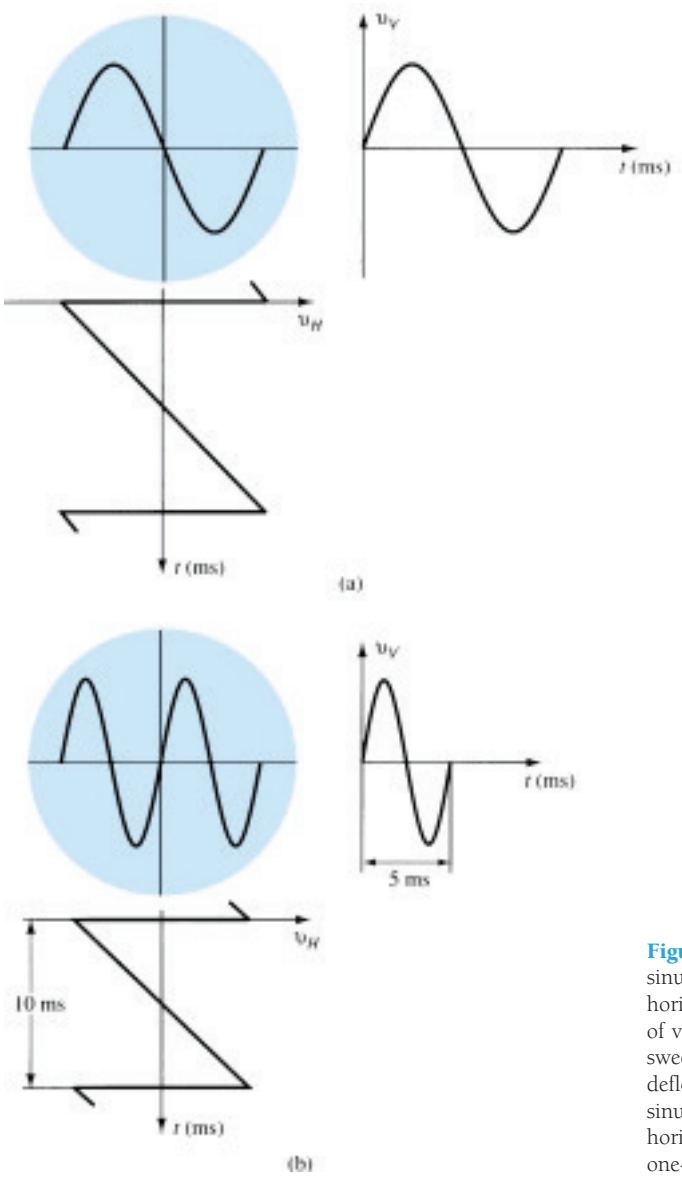


Figure 22.6 Display of sinusoidal vertical input and horizontal sweep input: (a) display of vertical input signal using linear sweep signal for horizontal deflection; (b) scope display for a sinusoidal vertical input and a horizontal sweep speed equal to one-half that of the vertical signal.

EXAMPLE 22.1

Determine how many cycles of a 2-kHz sinusoidal signal are viewed if the sweep frequency is:
(a) 2 kHz.
(b) 4 kHz.
(c) 1 kHz.

Solution

(a) When the two signals have the same frequency, a full cycle will be seen.
(b) When the sweep frequency is increased to 4 kHz, a half-cycle will be seen.
(c) When the sweep frequency is reduced to 1 kHz, two cycles will be seen.

Figure 22.7 shows a pulse-type waveform applied as vertical input with a horizontal sweep, resulting in a scope display of the pulse signal. The numbering at each waveform permits following the display for variation of input and sweep voltage during one cycle.

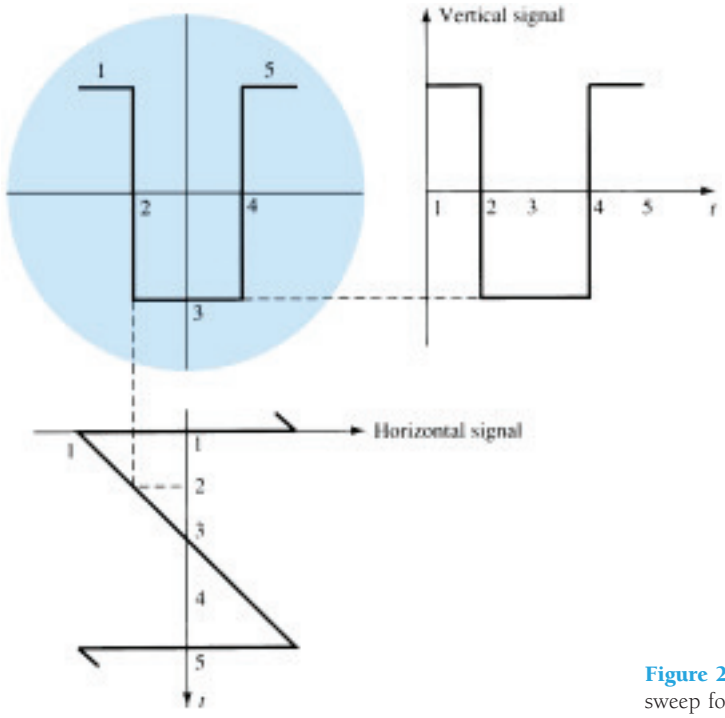


Figure 22.7 Use of the linear sweep for a pulse-type waveform.

22.5 SYNCHRONIZATION AND TRIGGERING

A CRO display can be adjusted by setting the sweep speed (frequency) to display either one cycle, a number of cycles, or part of a cycle. This is a very valuable feature of the CRO. Figure 22.8 shows the display resulting for a few cycles of the sweep signal. Each time the horizontal sawtooth sweep voltage goes through a linear sweep cycle (from maximum negative to zero to maximum positive), the electron beam is caused to move horizontally across the tube face, from left to center to right. The sawtooth voltage then drops quickly back to the negative starting voltage, with the beam back to the left side. During the time the sweep voltage goes quickly

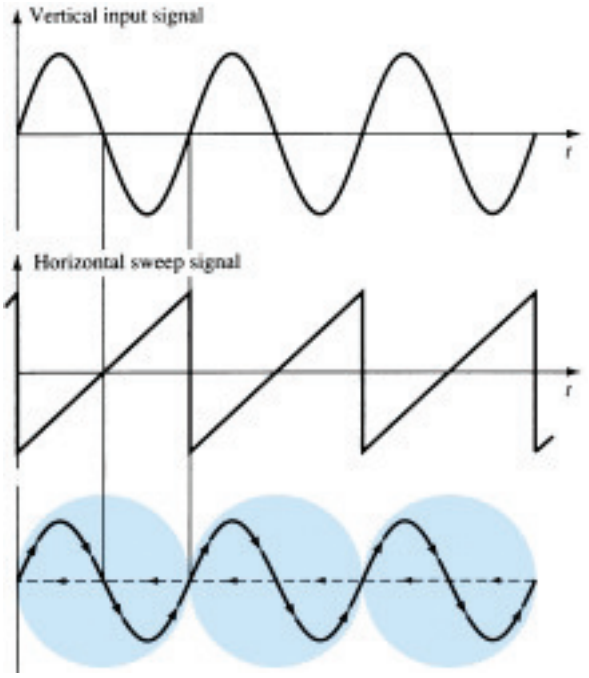


Figure 22.8 Steady scope display—input and sweep signals synchronized.

negative (retrace), the beam is blanked (the grid voltage prevents the electrons from hitting the tube face).

To see a steady display each time the beam is swept across the face of the tube, it is necessary to start the sweep at the same point in the input signal cycle. In Fig. 22.9, the sweep frequency is too low and the CRO display will have an apparent "drift" to the left. Figure 22.10 shows the result of setting the sweep frequency too high, with an apparent drift to the right.

It should be obvious that adjusting the sweep frequency to exactly the same as the signal frequency to obtain a steady sweep is impractical. A more practical proce-

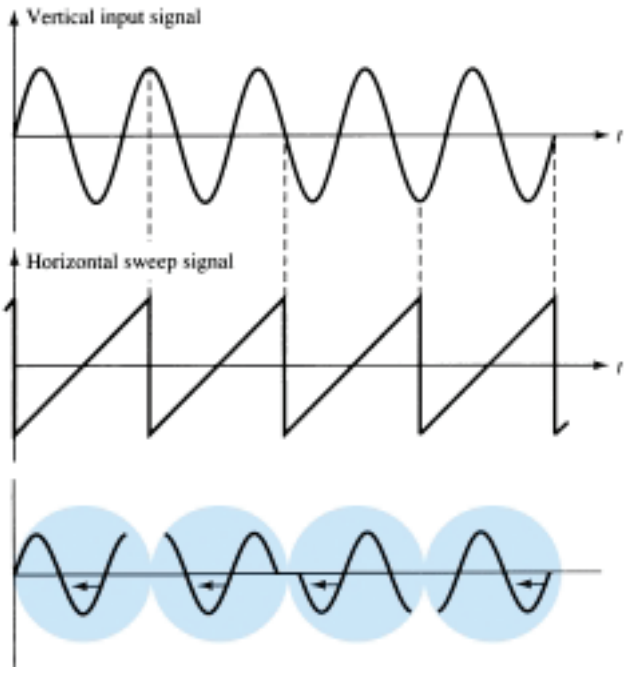


Figure 22.9 Sweep frequency too *low*—apparent drift to left.

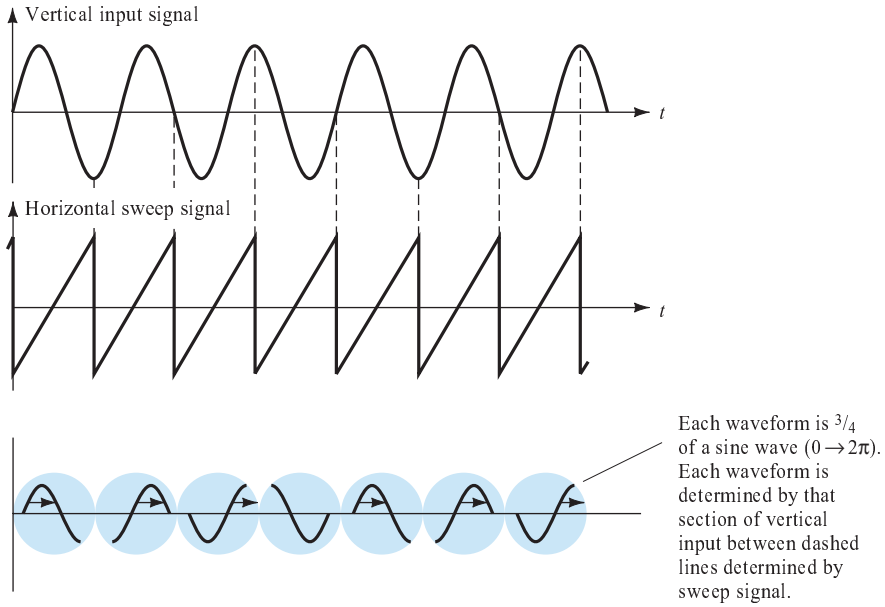


Figure 22.10 Sweep frequency too *high*—apparent drift to right.

dure is to wait until the signal reaches the same point in a cycle to start the trace. This triggering has a number of features, as described next.

Triggering

The usual method of synchronizing uses a portion of the input signal to trigger a sweep generator so that the sweep signal is locked or synchronized to the input signal. Using a portion of the same signal to be viewed to provide the synchronizing signal assures synchronization. Figure 22.11 shows a block diagram of how a trigger signal is derived in a single-channel display. The trigger signal source is obtained from the line frequency (60 Hz) for viewing signals related to the line voltage, from an external signal (one other than that to be viewed), or more likely, from a signal derived

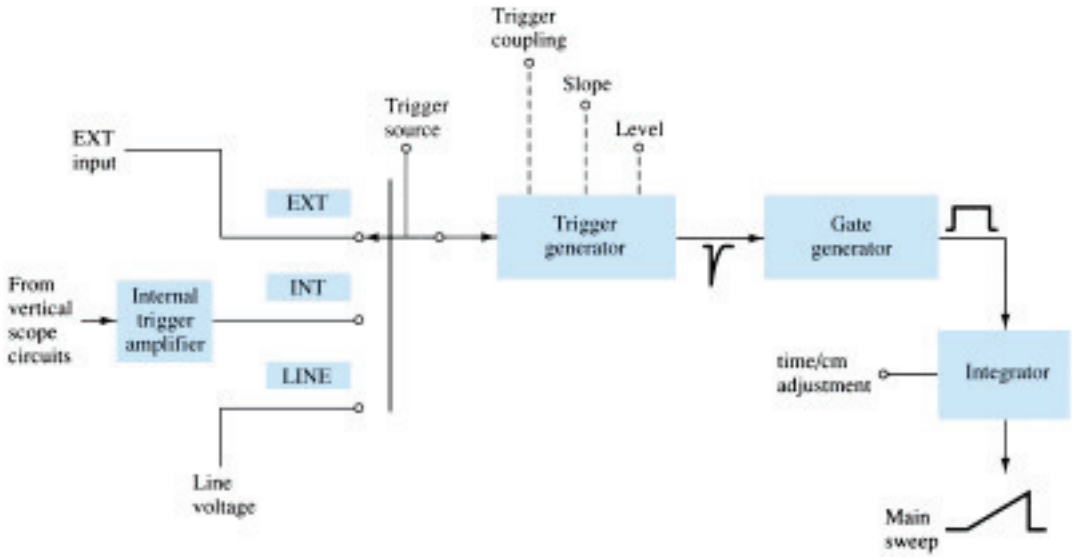


Figure 22.11 Block diagram showing trigger operation of scope.

from that applied as vertical input. The selector switch on the scope being set to INTERNAL will provide a part of the input signal to the trigger generator circuit. The output of the trigger generator is a trigger signal that is used to start the main sweep of the scope, which lasts a time set by the time/cm adjustment. Figure 22.12 shows triggering being started at various points in a signal cycle.

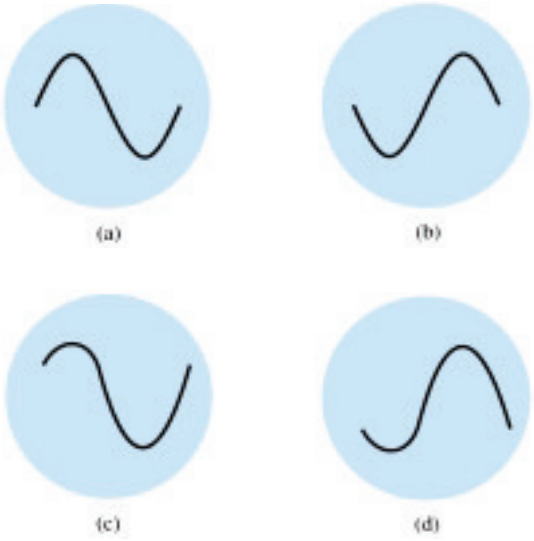


Figure 22.12 Triggering at various points of signal level (*Note:* sine starts at same point in cycle each sweep and is therefore synchronized): (a) positive-going zero level; (b) negative-going zero level; (c) positive-voltage trigger level; (d) negative-voltage trigger level.

The trigger sweep operation can also be seen by looking at some of the resulting waveforms. From a given input signal, a trigger waveform is obtained to provide for a sweep signal. As seen in Fig. 22.13, the sweep is started at a time in the input signal cycle and lasts a period set by the sweep length controls. Then the scope waits until the input reaches an identical point in its cycle before starting another sweep operation. The length of the sweep determines how many cycles will be viewed, while the triggering assures that synchronization takes place.

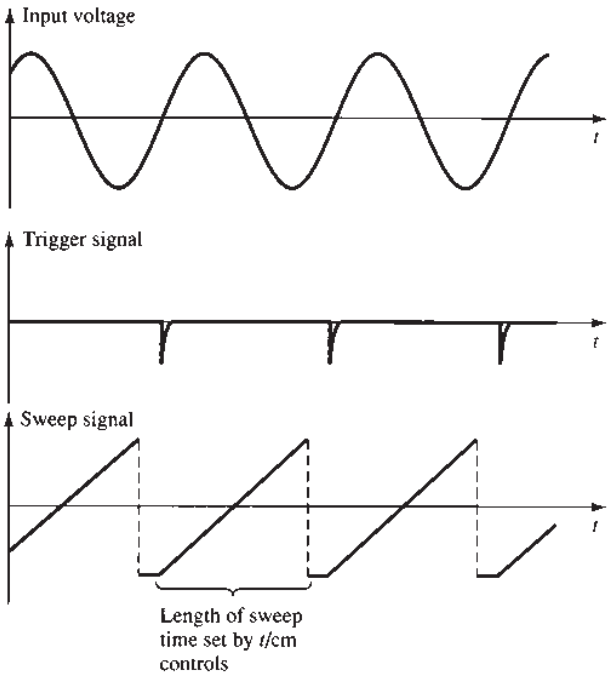


Figure 22.13 Triggered sweep.

22.6 MULTITRACE OPERATION

Most modern oscilloscopes provide for viewing two or more traces on the scope face at the same time. This allows comparing amplitude, special waveform features, and other important waveform characteristics. A multiple trace can be obtained using more than one electron gun, with the separate beams creating separate displays. More often, however, a single electron beam is used to create the multiple images.

Two methods of developing two traces are CHOPPED and ALTERNATE. With two input signals applied, an electronic switch first connects one input, then the other, to the deflection circuitry. In the ALTERNATE mode of operation, the beam is swept across the tube face displaying however many cycles of one input signal are to be displayed. Then the input switches (alternates) to the second input and displays the same number of cycles of the second signal. Figure 22.14a shows the operation with alternate display. In the CHOPPED mode of operation (Fig. 22.14b), the beam repeatedly switches between the two input signals during one sweep of the beam. As long as the signal is of relatively low frequency, the action of switching is not visible and two separate displays are seen.

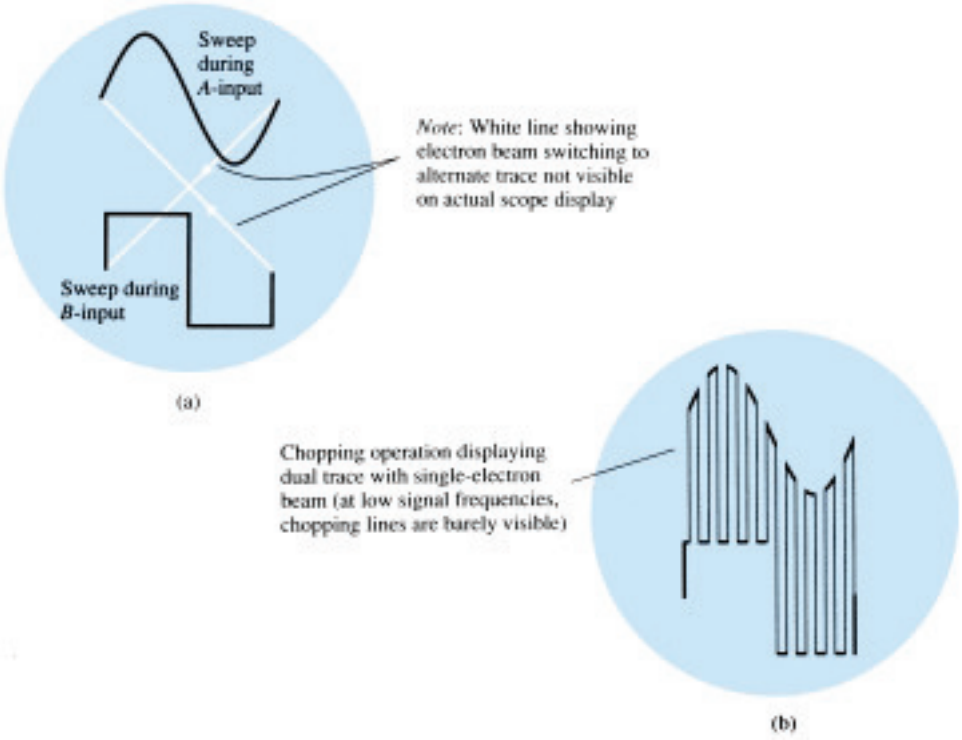


Figure 22.14 Alternate and chopped mode displays for dual-trace operation: (a) alternate mode for dual-trace using single electron beam; (b) chopped mode for dual-trace using single electron beam.

22.7 MEASUREMENT USING CALIBRATED CRO SCALES

The oscilloscope tube face has a calibrated scale to use in making amplitude or time measurements. Figure 22.15 shows a typical calibrated scale. The boxes are divided into centimeters (cm), 4 cm on each side of center. Each centimeter (box) is further divided into 0.2-cm intervals.

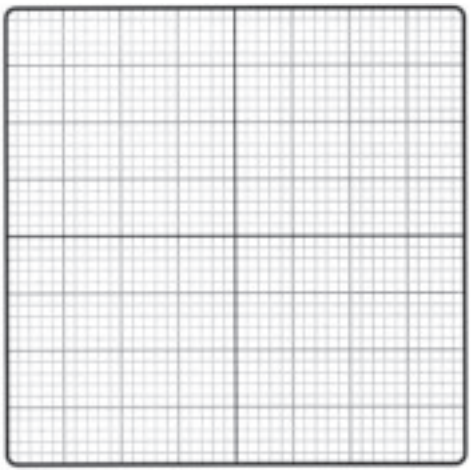


Figure 22.15 Calibrated scope face.

Amplitude Measurements

The vertical scale is calibrated in either volts per centimeter (V/cm) or millivolts per centimeter (mV/cm). Using the scale setting of the scope and the signal measured off the face of the scope, one typically can measure peak-to-peak or peak voltages for an ac signal.

EXAMPLE 22.2

Calculate the peak-to-peak amplitude of the sinusoidal signal in Fig. 22.16 if the scope scale is set to 5 mV/cm.

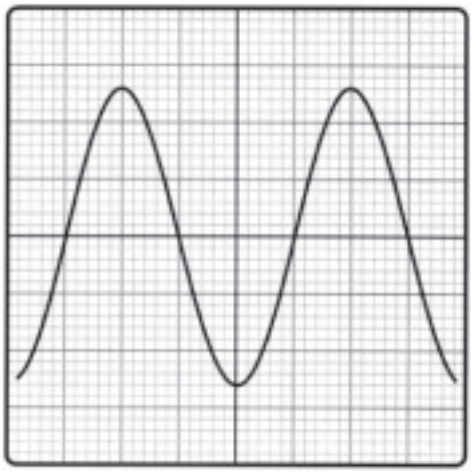


Figure 22.16 Waveform for Example 22.2.

Solution

The peak-to-peak amplitude is

$$2 \times 2.6 \text{ cm} \times 5 \text{ mV/cm} = \mathbf{26\ mV}$$

Note that a scope provides easy measurement of peak-to-peak values, whereas a multimeter typically provides measurement of rms (for a sinusoidal waveform).

Calculate the amplitude of the pulse signal in Fig. 22.17 (scope setting 100 mV/cm). *EXAMPLE 22.3*

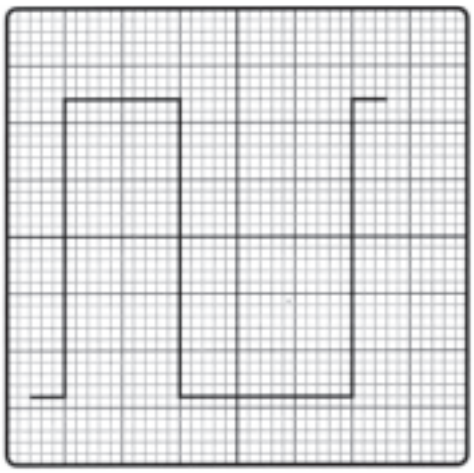


Figure 22.17 Waveform for Example 22.3.

Solution

The peak-to-peak amplitude is

$$(2.8 \text{ cm} + 2.4 \text{ cm}) \times 100 \text{ mV/cm} = \mathbf{520\ mV} = \mathbf{0.52\ V}$$

Time Measurements

PERIOD

The horizontal scale of the scope can be used to measure time, in seconds (s), milliseconds (ms), microseconds (μs), or nanoseconds (ns). The interval of a pulse from start to end is the period of the pulse. When the signal is repetitive, the period is one cycle of the waveform.

Calculate the period of the waveform shown in Fig. 22.18 (scope setting at 20 μs/cm). *EXAMPLE 22.4*

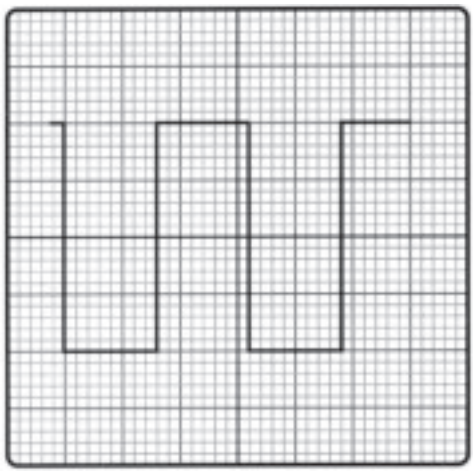


Figure 22.18 Waveform for Example 22.4.

Solution

For the waveform of Fig. 22.18,

$$\text{period} = T = 3.2 \text{ cm} \times 20 \ \mu\text{s/cm} = \mathbf{64\ \mu s}$$

FREQUENCY

The measurement of a repetitive waveform's period can be used to calculate the signal's frequency. Since frequency is the reciprocal of the period,

$$f = \frac{1}{T} \tag{22.1}$$

EXAMPLE 22.5 Determine the frequency of the waveform shown in Fig. 22.18 (scope setting at 5 μs/cm).

Solution

From the waveform

$$\text{period} = T = 3.2 \text{ cm} \times 5 \ \mu\text{s/cm} = 16 \ \mu\text{s}$$

$$f = \frac{1}{T} = \frac{1}{16 \ \mu\text{s}}$$

$$= \mathbf{62.5\ kHz}$$

PULSE WIDTH

The time interval that a waveform is high (or low) is the pulse width of the signal. When the waveform edges go up and down instantly, the width is measured from start (leading edge) to end (trailing edge) (see Fig. 22.19a). For a waveform with edges that rise or fall over some time, the pulse width is measured between the 50% points as shown in Fig. 22.19b.

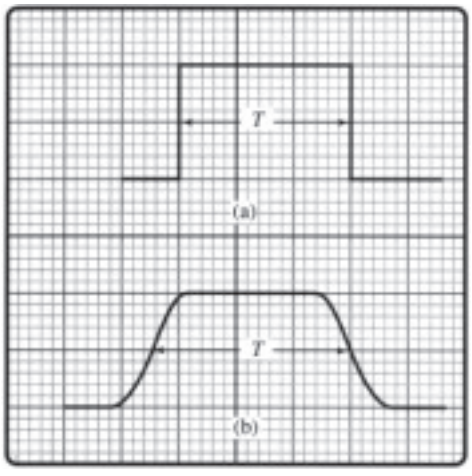


Figure 22.19 Pulse-width measurement.

Determine the pulse width of the waveform in Fig. 22.20. *EXAMPLE 22.6*

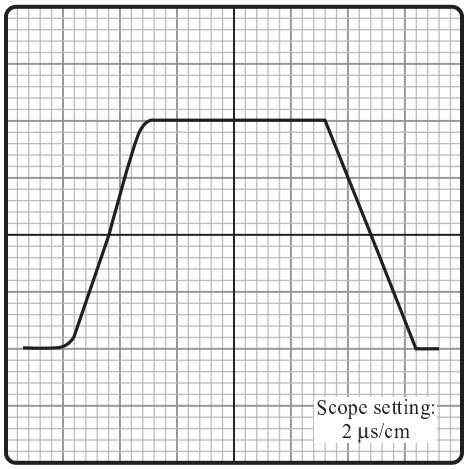


Figure 22.20 Waveform for Example 22.6.

Solution

For a reading of 4.6 cm at the midpoint of the waveform, the pulse width is

$$T_{PW} = 4.6 \text{ cm} \times 2 \ \mu\text{s/cm} = \mathbf{9.2\ \mu s}$$

PULSE DELAY

The time interval between pulses is called the pulse delay. For waveforms, as shown in Fig. 22.21, the pulse delay is measured between the midpoint (50% point) at the start of each pulse.

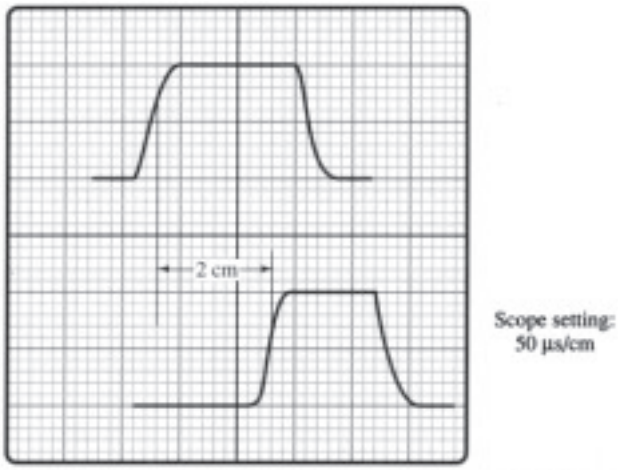


Figure 22.21 Waveform for Example 22.7.

Determine the pulse delay for the waveforms of Fig. 22.21. *EXAMPLE 22.7*

Solution

From the waveforms in Fig. 22.21,

$$\text{pulse delay} = T_{PD} = 2 \text{ cm} \times 50 \ \mu\text{s/cm} = \mathbf{100\ \mu s}$$

22.8 SPECIAL CRO FEATURES

The CRO has become more sophisticated and specialized in use. The range of amplitude measurements, the scales of time measurements, the number of traces displayed, the methods of providing sweep triggering, and the types of measurements are different depending on the area of specialized scope usage.

Delayed Sweep

A useful CRO feature uses two time bases to provide selection of a small part of the signal for viewing. One time base selects the overall signal viewed on the scope, while a second permits selecting a small part of the viewed signal to be displayed in an expanded mode. The main time base is referred to as the A time base, while the second time base, referred to as B, displays the signal after a selected delay time.

Figure 22.22 provides a block diagram showing the operation of the two time bases. With front-panel controls set to operate from the A sweep, a main sweep signal is set to view a number of cycles of the input signal. The controls then allow setting the B sweep using a variable setting dial, with the B sweep usually an intensified interval that can be moved over the face of the displayed sweep. When the desired portion of the displayed sweep is set, the controls are moved to display the delayed part of the signal, which is seen at the second time base setting as a magnified display. Figure 22.23 shows a pulse-type signal first viewed using the A sweep and then the selected portion on a magnified sweep setting.

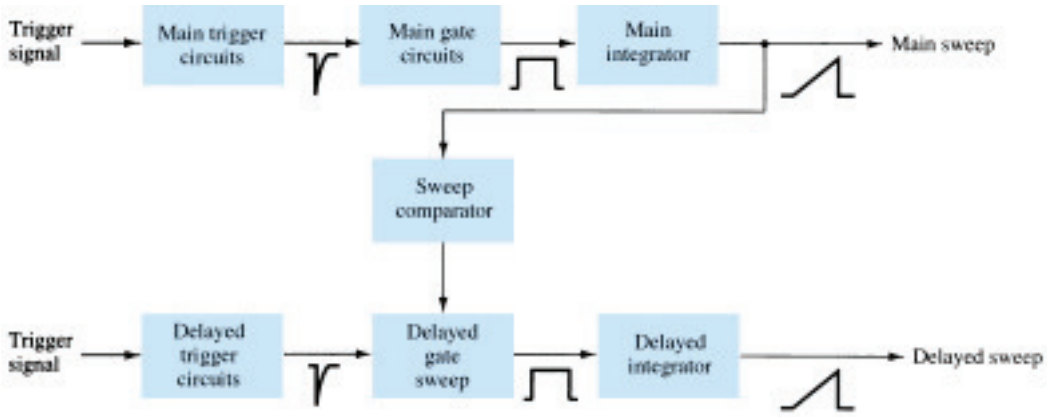


Figure 22.22 Operation of delayed sweep—block diagram.

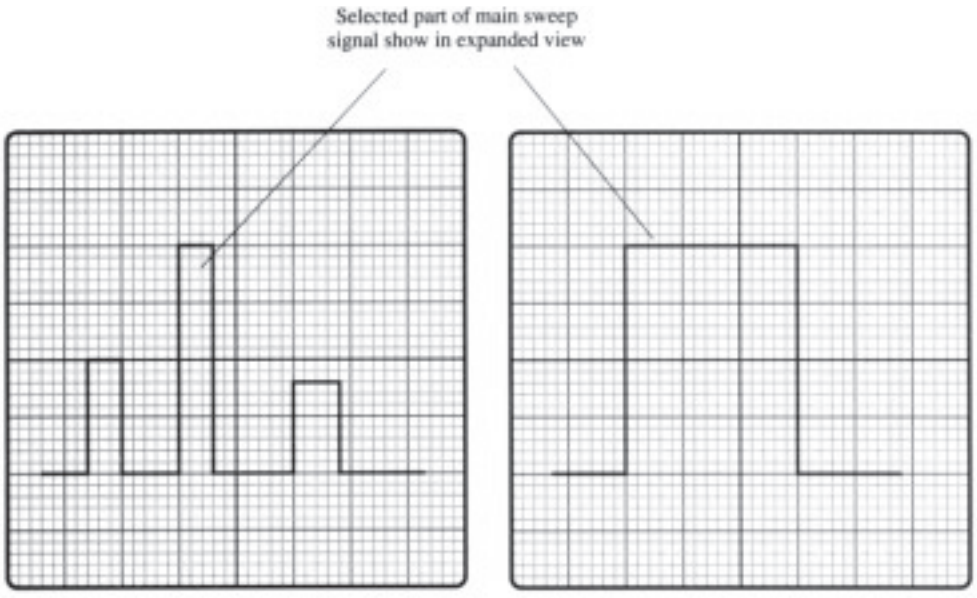


Figure 22.23 Main and delayed sweeps.

22.9 SIGNAL GENERATORS

A signal generator provides an ac signal of adjustable amplitude and varying frequency to use when operating an amplifier or other linear circuit. The frequency can typically be adjusted from a few hertz to a few megahertz. The signal amplitude can be adjusted from millivolts to a few volts of amplitude. While the signal is typically a sinusoidal waveform, pulse waveforms or even triangular waveforms are often available.

Waveform Generator IC(8038)

A precision waveform generator is provided by the 8038 IC unit shown in Fig. 22.24. The single 14-pin IC is capable of producing highly accurate sinusoidal, square, or triangular waveforms to use in operating or testing other equipment. Consideration of the IC's operation will help understand how any commercially available signal generator operates. This particular IC can provide output frequency that may be adjusted from less than 1 Hz up to about 300 kHz. The range of commercial units can be considerably higher. As indicated in Fig. 22.24, the IC provides three types of output waveform, and all at the same frequency, the frequency being selected by the user.

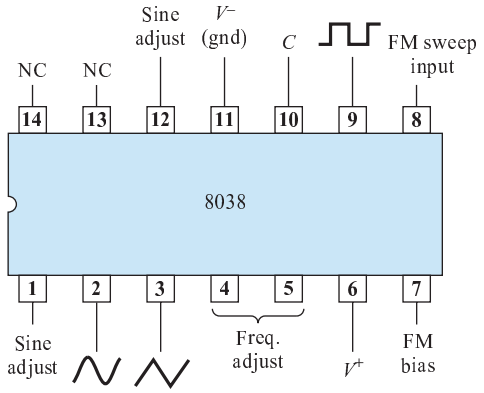


Figure 22.24 8038 waveform generator IC.

Figure 22.25 shows the connection of the IC when used to provide an adjustable frequency output. The frequency of the unit would then be

$$f = \frac{0.15}{RC} \tag{22.2}$$

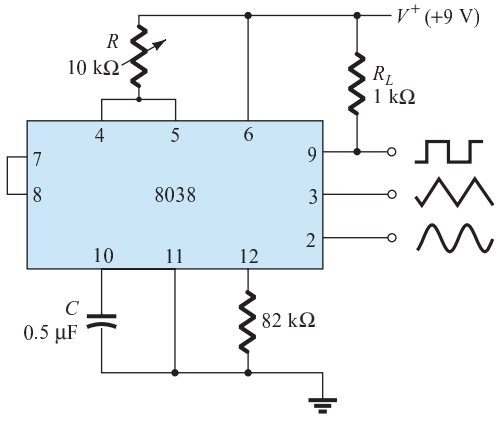


Figure 22.25 Connection of 8038 as variable frequency generator.

EXAMPLE 22.8

Referring to Fig. 22.25, determine the lowest and highest frequencies obtained when varying the 10-kΩ potentiometer from its minimum to its maximum setting.

Solution

Using Eq. (22.2), for a potentiometer set at 0, $R = 10\ \Omega$:

$$f = \frac{0.15}{(10\ \Omega)(0.5\ \mu\text{F})} = \mathbf{30\ kHz}$$

For a potentiometer set to its maximum,

$$f = \frac{0.15}{(10\ \text{k}\Omega)(0.5\ \mu\text{F})} = \mathbf{30\ Hz}$$

ADJUSTABLE OUTPUT AMPLITUDE

The connection of Fig. 22.26 shows how to provide adjustment of the sinusoidal waveform amplitude with the sinusoidal output provided through a buffered driver. The 310 op-amp is a unity-gain buffer providing the sinusoidal output from a low-impedance output. [The 310 has a voltage gain near unity (1), with an output impedance of about 1 Ω.] The output frequency is adjustable over a range from about 30 Hz to 30 kHz, with an amplitude adjustable up to about 9 V peak.

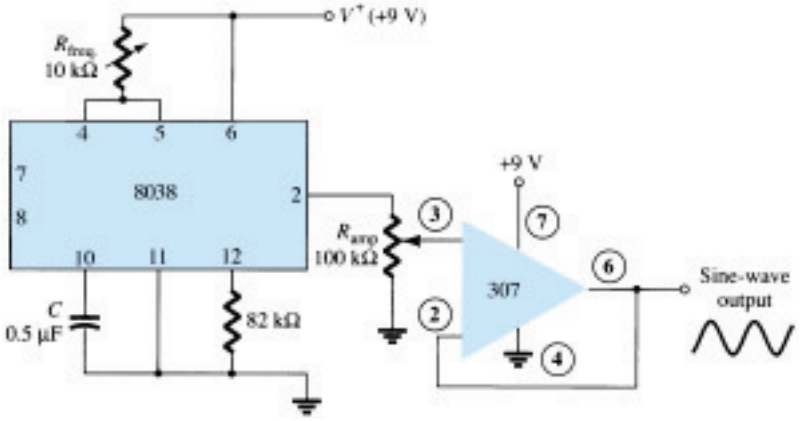


Figure 22.26 Sinusoidal waveform generator with adjustable frequency and amplitude.

5-V (TTL) PULSE GENERATOR

A circuit providing a 5-V pulse waveform for use with TTL digital circuits is shown in Fig. 22.27. The 8038 IC provides a rectangular or pulse waveform at a fixed output between 0 and +5 V. The frequency of the output can be varied from about 30 Hz to 30 kHz when adjusting the value of the 10-kΩ potentiometer. A commercial signal generator would probably include switched capacitors to provide frequency over a range of values. As long as the supply uses an IC regulator to provide the +5-V supply voltage, the output will be a well-defined value, as is typically used in TTL circuits. The 310 unity follower provides the output from a low-impedance source, making it possible to connect the output to a number of loads without affecting the amplitude or frequency of the signal waveform.

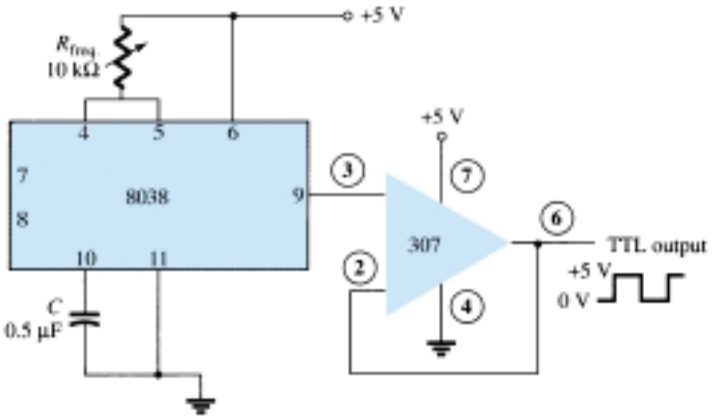


Figure 22.27 TTL signal waveform generator.

Preface

As we approached the 30th anniversary of the text it became increasingly clear that this Seventh Edition should continue to include the major revision work that went into the Sixth Edition. The growing use of computer software, packaged IC units, and the expanded range of coverage necessary in the basic courses which contributed to the refinement of the last edition have continued to be driving factors affecting the content of the new edition as well. Over the years, we have learned that improved readability can be attained through the general appearance of the text, so we have become committed to the format you will find in the Seventh Edition to make the text material appear "friendlier" to a broad range of students. As in the past, we continue to be committed to the strong pedagogical sense of the text, accuracy, and a broad range of ancillary materials that support the educational process.

PEDAGOGY

Without question, one of the most important improvements retained from the Sixth Edition is the manner in which the content lends itself to the typical course syllabus. The resequencing of concept presentation which affected the last edition has been retained in this new edition. Our teaching experience with this presentation has reinforced our belief that the material now has an improved pedagogy to support the instructor's lecture and help students build the foundation necessary for their future studies. The number of examples, which were substantially increased in the previous edition, have been retained. Isolated boldfaced ("bullet") statements identify important statements and conclusions. The format has been designed to establish a friendly appearance to the student and ensure that the artwork is as close to the reference as possible. An additional color is employed in a manner that helps define important characteristics or isolate specific quantities in a network or on a characteristic. Icons, developed for each chapter of the text, facilitate referencing a particular area of the text as quickly as possible. Problems, which have been developed for each section of the text, progress from the simple to the more complex. In addition, an asterisk identifies the more difficult exercises. The title of each section is also reproduced in the problem section to clearly identify the exercises of interest for a particular topic of study.

SYSTEMS APPROACH

On numerous visits to other schools, technical institutes, and meetings of various societies it was noted that a more "systems approach" should be developed to support a student's need to become adept in the application of packaged systems. Chapters 8, 9, and 10 are specifically organized to develop the foundation of systems analysis to the degree possible at this introductory level. Although it may be easier to consider the effects of R_s and R_L with each configuration when first introduced, the effects of R_s and R_L also provide an opportunity to apply some of the fundamental concepts of system analysis. The later chapters on op-amps and IC units further develop the concepts introduced in these early chapters.

ACCURACY

There is no question that a primary goal of any publication is that it be as free of errors as possible. Certainly, the intent is not to challenge the instructor or student with planned inconsistencies. In fact, there is nothing more distressing to an author than to hear of errors in a text. We believe this text will enjoy the highest level of accuracy obtainable for a publication of this kind.

TRANSISTOR MODELING

BJT transistor modeling is an area that is approached in various ways. Some institutions employ the r_e model exclusively, while others lean toward the hybrid approach or a combination of these two. The Seventh Edition will emphasize the r_e model with sufficient coverage of the hybrid model to permit comparison between models and the application of both. An entire chapter (Chapter 7) has been devoted to the introduction of the models to ensure a clear, correct understanding of each and the relationships that exist between the two.

PSpice

The last few years have seen a continuing growth of the computer content in introductory courses. Not only is the use of word-processing appearing in the first semester, but spreadsheets and the use of a software analysis package such as PSpice are also being introduced in numerous educational institutions.

PSpice was chosen as the package to appear throughout this text because it is most frequently employed. Other possible packages include Micro-Cap III and Breadboard. The coverage of PSpice provides sufficient content to permit drawing the schematic for the majority of networks analyzed in this text. No prior knowledge of computer software packages is presumed. PSpice permits entering the circuit schematic, which can then be analyzed with output results provided as text files or as **probe** graphic displays.

ELECTRONICS WORKBENCH

The EWB CD-ROM included with this text also contains a fully functional EWB demo that will operate circuits from throughout the text. In addition, the CD-ROM contains a tutorial that instructs students how to operate EWB and how to simulate circuits. The CD-ROM also includes a locked version of Electronics Workbench® Stu-

dent Version 5.0 that can be unlocked by calling Interactive Image Technologies. Instructions for unlocking the software are included on the CD-ROM.

TROUBLESHOOTING

Troubleshooting is undoubtedly one of the most difficult abilities to introduce, develop, and demonstrate in a text mode. It is an art that can be introduced using a variety of techniques, but experience and exposure are obviously the key elements in developing the necessary skills. The content is essentially a review of situations that frequently occur in the laboratory environment. Some general hints as to how to isolate a problem area are introduced along with a list of typical causes. This is not to suggest that the student will become proficient in the debugging of networks introduced in this text, but at the very least the reader will have some understanding of what is involved with the troubleshooting process.

ANCILLARIES

The range of ancillary material is comprehensive. In addition to a Laboratory Manual with an associated Solutions Manual (with typical data), there is an Instructor's Manual with more than 150 Transparency Masters, a Test Item File, PowerPoint Transparencies, and a Prentice Hall Custom Test (Windows). The Instructor's Manual with Transparency Masters and the Solutions Manual have been carefully prepared and reviewed to ensure the highest level of accuracy. In fact, a majority of the solutions were tested using PSpice.

USE OF TEXT

In general the text is divided into two main components: the dc analysis and the ac or frequency response. For some schools the dc section is sufficient for a one-semester sequence, while for others the entire text may be covered in one semester by choosing specific topics. In any event the text is one that "builds" from the early chapters. Superfluous material is relegated to the later chapters to avoid excessive content on a particular subject early in the development stage. For each device the text covers a majority of the important configurations and applications. By choosing specific examples and applications the instructor can reduce the content of a course without losing the progressive building characteristics of the text. Then again, if an instructor feels that a specific area is particularly important, the detail is provided for a more extensive review.

ROBERT BOYLESTAD

LOUIS NASHELSKY

Glossary

acceptor atom Atom with three valence electrons added to a semiconductor to reduce the number of electrons in it, thus creating holes in the semiconductor's valence band.

active region Area on a device characteristic where the ratio between applied voltage and resulting current is constant. That is, the device is not operating in regions such as saturation, cutoff, or ohmic.

amplification Process of changing the amplitude of a signal with minimum alteration in its shape.

amplifier Assembly that produces an output quantity such as voltage or current in linear proportion to an applied input quantity. The output quantity is not necessarily larger than the input quantity.

analog-to-digital converter (ADC) Circuit that converts an analog signal to a digital signal whose binary value represents the amplitude of the original analog signal.

anode Positive terminal of a bipolar device.

astable multivibrator Oscillator circuit that produces a rectangular wave output.

bandwidth Range of frequencies for which the gain is at least 0.707 of midband gain.

bias line Graphical technique in circuit analysis which describes the bias circuit, external to a device, on the device transfer characteristic curve.

bias(ing) Fixed dc voltage applied to a circuit that is intended to set a device's operation at a particular point on its characteristic curve.

bipolar Type of device whose functioning involves both majority and minority charge carriers.

bipolar junction transistor. *See* BJT

BJT Bipolar junction transistor is a 3-layer device containing both types of semiconductor material (either in *p*-*n*-*p* or *n*-*p*-*n* form). It typically has three terminals.

Bode plot Graph of gain or phase shift versus frequency for a circuit.

body resistance Inherent resistance of the block(s) of material composing an electronic device—one aspect of how a practical device deviates from ideal.

bridge Network of four components arranged in a square with identical opposite pairs of elements. The input is attached across one diagonal, and the output across the other.

candela Unit of light intensity in SI.

cascade amplifier Amplifier with two or more stages in which the output of one stage serves as the input to the next.

cascode amplifier High frequency amplifier made up of a common-emitter amplifier with a common-base amplifier in its collector network.

cathode Negative terminal of a bipolar device.

characteristics Set of graphs that display any operating feature of an electronic device, such as collector current vs. collector-emitter voltage for a set of different base currents.

chip Common name for an integrated circuit. Many chips are cut from a single wafer of silicon that has been doped and etched to form many elements and components.

clamping Process of shifting an input ac signal to a different zero point.

clipper Circuit that cuts off some portion of an input signal.

clipping Failure of a circuit to respond to signals above a certain amplitude, causing distortion of the output signal.

CMOS Complimentary MOS: digital integrated circuitry in which both *n*- and *p*-channel MOSFETs are used.

common Path for current returning to the power supply from a circuit.

common base (emitter, etc.) Configuration in which the base (emitter, etc.) the terminal of a three-terminal device is common to both the input and output loops of the circuit.

common-mode rejection Ratio of the differential gain of an op-amp to its common-mode gain.

comparator Op-amp circuit that compares two input voltages and provides a DC output that indicates which input is greater.

conduction angle Portion of a half wave, expressed in degrees, during which a silicon-controlled rectifier is conducting.

constant-current source Circuit that provides constant current to a changing load.

contact resistance Resistance at the contacts with the material of an electronic device—one aspect of how a practical device deviates from ideal.

conversion efficiency For an amplifier, the ratio of output ac power to input dc power.

corner frequency Frequency at which the gain of an amplifier has dropped to 0.707 of midband value.

crystal oscillator An oscillator with a piezoelectric crystal in its feedback network to maintain a stable frequency of oscillations.

current mirror Circuit consisting of two matching transistors with the collector of one connected to the bases of both, thus producing the same collector current in each transistor.

current-limiting circuit Protection circuitry that prevents the output current from exceeding a maximum value under an overload or short-circuit condition.

cut-off State of a semiconductor device in which the current is a minimum.

cut-off frequency *See* corner frequency

Darlington pair connection Two bipolar junction transistors with their collectors connected together and the emitter of one connected to the base of the other.

demodulation Process of extracting a signal that has been impressed on a carrier wave.

depletion Application of an electric field that repels majority carriers in a volume of semiconductor material.

depletion region Region near the junction of a semiconducting device that has few free carriers because electrons and holes have combined.

detection *See* Demodulation

die Another term for chip.

differential amplifier Amplifier in which the output voltage is proportional to the difference between the voltages applied to its two input terminals.

digital-to-analog converter (DAC) Circuit that converts a digital signal to an analog signal whose amplitude is proportional to the binary value of the digital signal.

diode Two-terminal device that conducts unidirectionally.

discrete component Package containing only a single electrical or electronic component.

donor atom Atom with five valence electrons added to a semiconductor to increase the number of electrons in it.

donor level Energy level of the valence band in a semiconductor with doping, which reduces the energy gap between the valence band and the conduction band.

doping Process of adding small quantities of particular impurities to an intrinsically pure semiconductor in order to alter its conducting properties.

dropout voltage Minimum value by which the input voltage of a voltage regulator must exceed the output voltage for regulation to occur.

efficacy Measure of the ability of a device to produce a desired effect.

electroluminescence Emission of light by a device when electrical energy is supplied.

electron volt Energy required to move a charge of one electron through a potential difference of 1 V; equals 1.602×10^{-19}J.

enhancement Application of an electric field that attracts majority carriers to a volume of semiconductor material.

equivalent circuit Combination of elements intended to mimic the characteristics of an electronic device with mathematical aspects that are simpler than those of the actual device. *See also* model

extrinsic material Semiconducting material that has had its conducting properties altered by doping; *n*-type material contains extra electrons; *p*-type material contains extra holes.

feedback Application of a portion of an amplifier's output to its input. It is used to improve amplifier performance or to cause oscillation.

feedback pair Two bipolar junction transistors with the collector of the *npn* connected the emitter of the *pnp* and the collector of the *pnp* connected the base of the *npn*.

FET Field-effect transistor

filter Part of a power supply that converts the rectified sine wave from the rectifier into a dc voltage with ripple.

foldback limiting Protection circuitry that causes the output current to decrease to a low value under an overload or short-circuit condition.

follower Voltage amplifier whose output "follows" the input, and so has a gain of approximately one.

forward-bias Voltage applied to a *p*-*n* junction (positive to *p*, negative to *n*) that diminishes the depletion region and increases the flow of majority carriers.

Fourier analysis Mathematical technique for describing a complex waveform as the sum of the harmonics of a fundamental.

free Of electrons, those that are only loosely bound to an atom or ion—they are able to migrate readily through a material under the application of small electric fields.

frequency modulation Process of varying the frequency of a signal such that the instantaneous value of the frequency is proportional to the amplitude of a control voltage or signal.

frequency-shift keying Form of frequency modulation in which the value of a digital signal sets the frequency at one of two values.

full-wave rectification Converting ac to dc using both halves of each ac input cycle.

fundamental Lowest frequency component of a waveform.

gain Amplification factor of an amplifier, the ratio of output to input.

gain margin Value in decibels of the amplitude of the βA factor of a feedback amplifier at the frequency for which the phase shift of βA is 180°.

gain-bandwidth product Transistor parameter that indicates the maximum possible product of gain and bandwidth.

gradient Regular change in a quantity along a given line or dimension; a the rate of change of such quantity.

half-power frequency *See* corner frequency

half-wave rectification Converting ac to dc using only half the input of each full ac cycle.

harmonic A sine wave that is an integral multiple of a fundamental frequency. *See also* fundamental

hole Vacancy in a normally filled site in a valence shell or band, created by doping with an acceptor atom. A hole is mobile and conducts as if it were a positive charge.

hybrid Involving the combination of unlike quantities or materials, as for example, voltage and current.

hybrid IC Integrated circuit that is composed of monolithic components and either thin-film or thick-film components.

IC component Package containing more than one electrical or electronic component in a single package.

ideal device Device that performs its function perfectly; e.g., an ideal transducer converts without loss all the energy applied to it.

ideal diode Diode that conducts perfectly in one direction and not at all in the opposite direction (zero resistance in one direction and infinite resistance in the opposite direction).

integrated circuit (IC) Collection of solid-state devices combined with other circuit elements printed on a single chip.

interface circuit Circuit that links input and output signals of different types of logic families with each other or with analog signals.

intrinsic carriers Charges constituting a current that are able to move simply because of the nature of the material and its temperature. *see also* extrinsic

ionization Process by which an electron is removed from an atom by the application of some form of energy.

ionization potential Electrical potential that is just sufficient to remove an electron from a shell of its atom.

JFET Junction field-effect transistor

junction The area of contact between volumes of *n*- and *p*-type extrinsic material.

lattice Regular spacing in three-dimensions of atoms in a crystal.

leakage current Minority carrier current in a reverse-biased junction in the absence of injected minority carriers.

light-emitting diode Diode that will emit light when forward biased.

linear circuit Circuit in which one quantity changes in direct proportion to another quantity.

load line Graphical technique in circuit analysis which describes the output circuit, external to a device, on the device output characteristic.

load-line analysis Method of describing the operation of an electronic device using the intersection of a line representing the load on the device and a graph line of the device's characteristics. The intersection is called the *Q*-point.

load regulation Measure of the change in load voltage as load current changes from no-load to full-load value.

majority carriers Charge carriers made abundant in the doping process of extrinsic material—electrons in *n*-type material or holes in *p*-type material.

mesa transistor Transistor produced by etching away a part of the area above the collector region to form a plateau on which the base and emitter regions are then formed.

minority carriers Charge carriers that are deficient in extrinsic material—holes in *n*-type material or electrons in *p*-type material.

model Representation of a system (either concrete or abstract) intended to assist in understanding the system, either by simplifying or emphasizing particular features of the system. Consider the differences among "model airplane," "atomic model," and "fashion model." *See also* equivalent circuit

modulation Process of combining a signal with a carrier wave (which is usually at a much higher frequency).

monolithic IC Circuit in which all components are formed as *pn* junctions on or within a semiconductor substrate.

monostable multivibrator Circuit with one stable output state that, when triggered, switches to an unstable state for a fixed period of time and then returns to the stable state.

MOSFET Metal-oxide-semiconductor field-effect transistor.

negative feedback Circuitry in which a feedback signal is 180° out of phase with the input signal.

no-bias Circuit that contains no fixed applied voltage.

Nyquist diagram Plot of the βA factor of a feedback amplifier as a vector on the complex plane for frequencies from zero to infinity.

offset potential Potential difference at which a diode or transistor begins to conduct at significant currents. It is also called the firing potential or threshold potential, and is symbolized as V_T.

op-amp Operational amplifier, a high-gain amplifier with an output that corresponds to the difference between two input signals.

oscillator Electronic circuit that produces a periodic output waveform with no voltage other than dc applied.

parallel resonance Condition occurring in a parallel RLC network at the frequency where the reactance of the inductor equals the reactance of the capacitor.

peak inverse voltage *See* PIV

phase margin 180° minus the phase shift at the frequency at which the gain is 0 dB.

phase-locked loop Circuit in which the phase of the output signal is compared to the phase of the input signal and adjustments made such that the output signal will lock onto and track the input signal.

phase-shift oscillator Oscillator with a feedback network consisting of three RC high-pass networks connected in series that produce 180° phase shift.

piecewise linear equivalent circuit Equivalent circuit with elements chosen to approximate the device's characteristic with straight-line segments.

piezoelectric effect Property of a crystal that produces a voltage across opposite faces due to mechanical stress and vice versa.

PIV Peak inverse voltage, the maximum reverse-bias potential that can be applied to a diode before entering the Zener region; also called PRV.

planar transistor Transistor produced by forming the base and emitter regions within the collector region rather than above it.

port A pair of terminals.

power supply Circuit that converts a sinusoidal voltage into a dc voltage.

***Q*-point** Point on a device's characteristic from which it operates. Set by the dc components in the circuit, the *quiescent* point sets the zero for ac variations. It is the intersection of the load line with a characteristic curve.

quiescent point *See Q*-point

rectification Process of converting ac to dc.

reverse-bias Voltage applied to a *p*-*n* junction (negative to *p*, positive to *n*) that enlarges the depletion region and increases the flow of minority carriers.

ripple Ratio of the ripple voltage to the dc voltage expressed as a percentage.

ripple voltage Small variations in the amplitude of the voltage at the output of the filter in a power supply.

saturation (1) Condition in a semiconductor in which no further increase in current results, no matter how much additional voltage is applied. (2) In a BJT, the state in which the voltage from collector to emitter is a minimum, typically 100 mV. (3) In an FET, the state in which an increase in the voltage from drain to source does not result in a significant increase in non-zero drain current.

semiconductor Any material that possesses a resistivity much higher than good conductors and much lower than good insulators.

series regulator Voltage regulator in which the control element is in series with the output voltage.

series resonance Condition occurring in a series RLC network at the frequency where the reactance of the inductor equals the reactance of the capacitor.

shunt voltage regulator Voltage regulator in which the control element is in parallel with the output voltage.

signal Electrical waveform that contains information, varying according to (for example) an audio or video input.

single-crystal Any material composed only of the repetitive structure of one kind of unit crystal.

small signal AC operation of an electronic device in a small enough vicinity around the q-point that the slope of the device transfer characteristic in that vicinity can be considered constant.

source regulation Measure of the change in load voltage as source voltage changes.

strobe Control signal whose value determines whether a circuit is enabled or disabled.

switching regulator Regulator in which regulation is maintained by switching the power control devices between on and off states.

temperature coefficient Number that expresses the rate of change of a quantity with temperature as, for example, the temperature coefficient of resistance.

tetravalent atom Atom containing four electrons in its (outer) valence shell.

thick-film IC Integrated circuit with passive elements deposited on a substrate using screening and firing processes and active elements added on the surface as discrete components.

thin-film IC Integrated circuit with passive elements deposited on a substrate using a sputtering or vacuum process and active elements added on the surface as discrete components.

threshold voltage Voltage level for a diode or transistor that results in a significant increase in drain current. *See also* offset potential

tilt Measure of the loss in amplitude of a pulse from the leading edge to the trailing edge of the pulse.

transconductance factor For an FET, the ratio of the change in drain current to the change in gate voltage that induced it; symbol, g_m; unit, siemen.

transfer characteristic Graph that displays the relationship between the input and output quantities of a device.

transistor Semiconductor device useful for amplifying or switching electrical signals.

tuned oscillator Oscillator in which component values in an LC network determine the frequency of oscillations.

two-port network Generalized model of a linear circuit that has two input and two output terminals.

unipolar Device whose functioning involves only majority charge carriers.

valence Outer shell of an atom containing the electrons that determine the element's chemical characteristics.

voltage-controlled oscillator (VCO) Oscillator whose output frequency varies with a modulating input voltage.

wafer Thin slice of semiconductor crystal on which many IC circuits (chips) are formed.

Wien bridge oscillator Oscillator with a feedback network consisting of a series RC network and a parallel RC network in a bridge circuit.

yield rate Percentage of the chips obtained from a single wafer that meet specifications.

Zener potential The reverse-bias voltage at which a diode will experience a sharp increase in reverse current.

Zener region Portion of the current-voltage characteristic of a diode which shows a sharp increase in reverse current at the Zener potential.